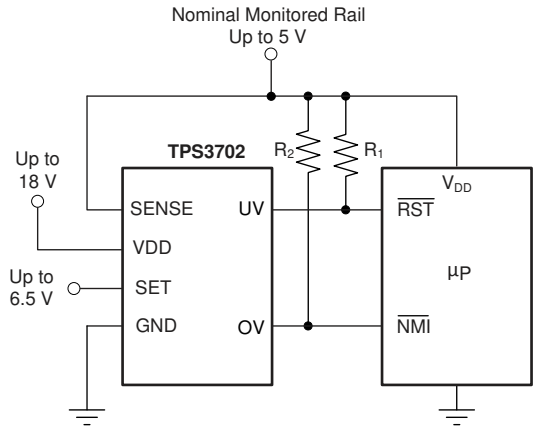
TPS3702-Q1 汽车类 高 精度过压和欠压监测

1 特性

- 符合 AEC-Q100 标准：
  - 器件温度等级 1：–40°C 至 125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 输入电压范围：2V 至 18V
- 高阈值精度：
  - 0.25%（典型值）
  - 0.9%（–40°C 至 125°C）
- 已针对 1V 和 5V 之间的标称电源轨优化的固定窗口阈值
- 用于过压和欠压检测的开漏输出
- 内部毛刺抑制功能
- 可使用 SET 引脚调整阈值
- 低静态电流：7µA（典型值）
- 内部阈值迟滞：0.55%，1.0%
- SOT-6 封装

2 应用

- 汽车安全应用
- 信息娱乐系统
- FPGA 和 ASIC 应用
- 基于 DSP 的系统
- 前置摄像头
- 后视摄像头
- 汽车雷达系统



典型应用电路

3 说明

TPS3702-Q1 是一款集成型过压和欠压窗口电压检测器，采用小型 SOT-6 封装。这款高精度电压检测器非常适合由低压电源轨供电且电源容限较窄的系统。该器件提供有 0.55% 和 1.0% 两个低阈值迟滞选项，可防止在受监视电源电压处于其标称工作范围内时出现错误的复位信号。并且内置毛刺抑制功能和噪声滤波器，进一步消除了错误信号所导致的错误复位。

TPS3702-Q1 无需使用任何外部电阻即可设置过压和欠压复位阈值，因此进一步提高了总体精度、减小了解决方案尺寸并降低了解决方案的成本。每款器件的两种可用阈值电压可使用 SET 引脚进行选择。独立的 SENSE 输入引脚和 VDD 引脚可满足安全关键型和高可靠性系统对于冗余的需求。该器件还为 OV 和 UV 引脚提供了独立复位输出；可采用开漏配置将 UV 和 OV 引脚连接在一起。

此器件的低静态电流规格为 7µA（典型值）。TPS3702-Q1 符合 AEC-Q100 1 级标准，适用于汽车应用。

器件信息

器件型号	封装 (1)	封装尺寸（标称值）(2)
TPS3702-Q1	SOT (6)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

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4 Pin Configuration and Functions

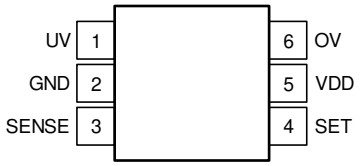


图 4-1. DDC Package
SOT-6
Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	UV	O	Active-low, open-drain undervoltage output. This pin goes low when the SENSE voltage falls below the internally set undervoltage threshold (V_{IT-}). See the timing diagram in 图 5-1 for more details. Connect this pin to a pull-up resistor terminated to the desired pull-up voltage.
2	GND	—	Ground
3	SENSE	I	Input for the monitored supply voltage rail. When the SENSE voltage goes below the undervoltage threshold, the UV pin is driven low. When the SENSE voltage goes above the overvoltage threshold, the OV pin is driven low.
4	SET	I	Use this pin to configure the threshold voltages. Refer to 表 8-1 for the desired configuration.
5	VDD	I	Supply voltage input pin. To power the device, connect a voltage supply (within the range of 2V and 18V) to VDD. Good analog design practice is to place a 0.1 µF ceramic capacitor close to this pin.
6	OV	O	Active-low, open-drain overvoltage output. This pin goes low when the SENSE voltage rises above the internally set overvoltage threshold (V_{IT+}). See the timing diagram in 图 5-1 for more details. Connect this pin to a pull-up resistor terminated to the desired pull-up voltage.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{DD}	–0.3	20	V
	V_{UV}, V_{OV}	–0.3	20	V
	V_{SENSE}, V_{SET}	–0.3	7	V
Current	I_{UV}, I_{OV}		±40	mA
Continuous total power dissipation		See the 节 5.4		
Operating junction temperature, T_J (2)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	2		18	V
V_{SENSE}	Input pin voltage	0		6.5	V
V_{SET}	SET pin voltage	0		6.5	V
V_{UV}, V_{OV}	Output pin voltage	0		18	V
I_{UV}, I_{OV}	Output pin current	0.3		10	mA
R_{PU}	Pull-up resistor	2.2		10,000	kΩ

5.4 Thermal Information

THERMAL METRIC(1)		TPS3702-Q1 DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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5.5 Electrical Characteristics

At 2V ≤ V_{DD} ≤ 18V, 1V ≤ V_{SENSE} ≤ 5V, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		2		18	V
$V_{IT+(OV)}$	Positive-going threshold accuracy	V_{SET} ≤ $V_{IL(SET)}$, V_{SET} ≥ $V_{IH(SET)}$	–0.9%	±0.25%	0.9%	
$V_{IT-(UV)}$	Negative-going threshold accuracy	V_{SET} ≤ $V_{IL(SET)}$, V_{SET} ≥ $V_{IH(SET)}$	–0.9%	±0.25%	0.9%	
V_{HYS}	Hysteresis voltage(2)	TPS3702x**X**x	0.3%	0.55%	0.8%	
$V_{(POR)}$	Power-on reset voltage(1)	$V_{OL(max)}$ = 0.25V, I_{OUT} = 15µA			0.8	V
I_{DD}	Supply current	V_{DD} = 2V		6.0	10	µA
		V_{DD} ≥ 5V		7.0	12	
I_{SENSE}	Input current, SENSE pin	V_{SENSE} = 5V		1	1.5	µA
I_{SET}	Internal pull-up current, SET pin	V_{DD} = 18V, SET pin = GND		600		nA
V_{OL}	Low-level output voltage	V_{DD} = 1.3V, I_{OUT} = 0.4mA			250	mV
		V_{DD} = 2V, I_{OUT} = 3mA			250	
		V_{DD} = 5V, I_{OUT} = 5mA			250	
$V_{IL(set)}$	Low-level SET pin input voltage				250	mV
$V_{IH(set)}$	High-level SET pin input voltage		750			mV
$I_{D(leak)}$	Open-drain output leakage current	V_{PU} = V_{DD}			300	nA
$I_{LKG(od)}$		V_{DD} = 2V, V_{PU} = 18V			300	
UVLO	Undervoltage lockout(3)	V_{DD} falling	1.3		1.7	V

(1) The outputs are undetermined below $V_{(POR)}$.
(2) Hysteresis is 0.55% of the nominal trip point.
(3) When V_{DD} falls below UVLO, UV is driven low and OV goes to high impedance.

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5.6 Timing Requirements

At V_{DD} = 2V, 2.5% input overdrive(4) with R_{PU} = 10kΩ, V_{OH} = 0.9 × V_{DD}, and V_{OL} = 400mV, unless otherwise noted. R_{PU} refers to the pull-up resistor at the UV and OV pins.

		MIN	NOM	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay(1)		19		µs
$t_{pd(LH)}$	Low-to-high propagation delay(1)		35		µs
t_R	Output rise time(2)		2.2		µs
t_F	Output fall time(2)		0.22		µs
t_{SD}	Startup delay(3)		300		µs

(1) High-to-low and low-to-high refers to the transition at the SENSE pin
(2) Output transitions from 10% to 90% for rise times and 90% to 10% for fall times.
(3) During the power-on sequence, V_{DD} must be at or above 2V for at least t_{SD} before the output is in the correct state.
(4) Overdrive = | ($V_{(VDD)}$ / V_{IT} – 1) × 100% |.

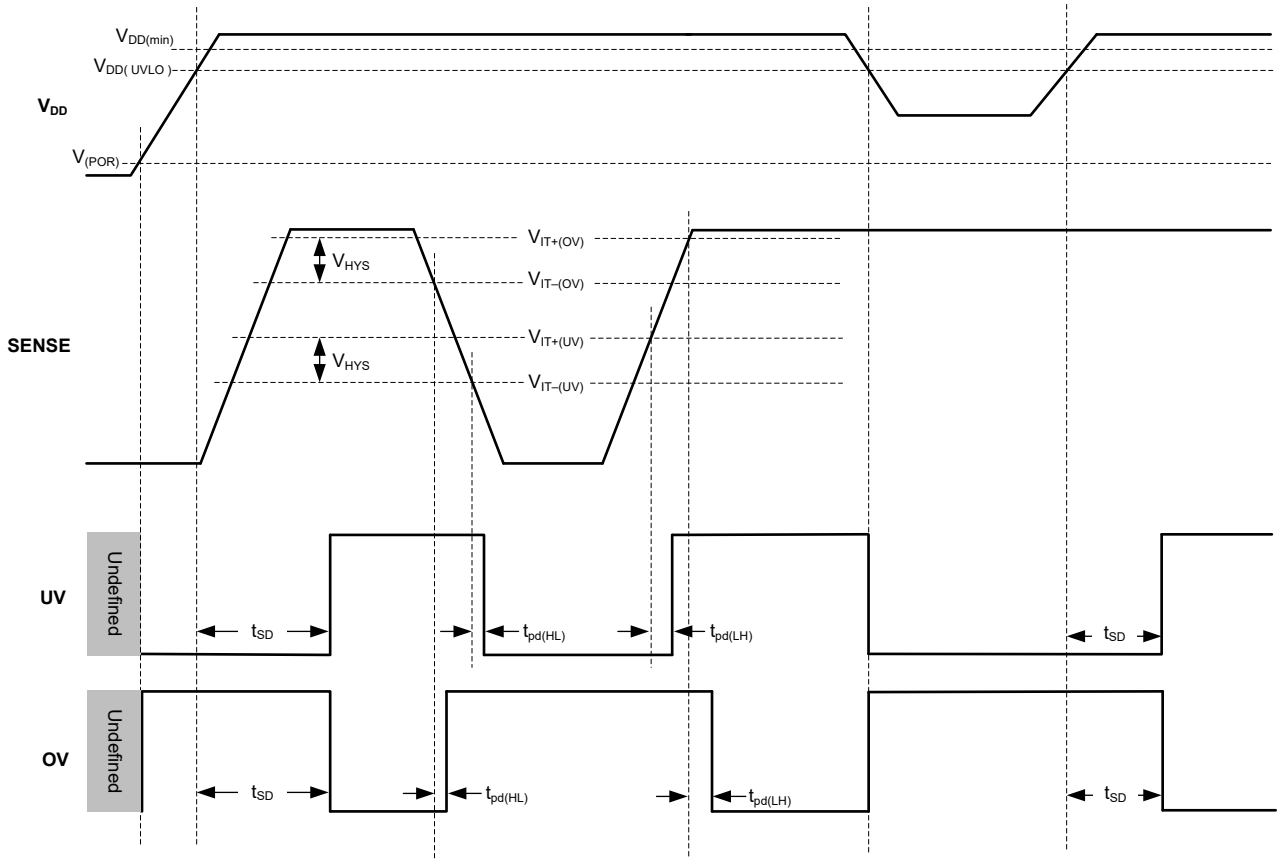
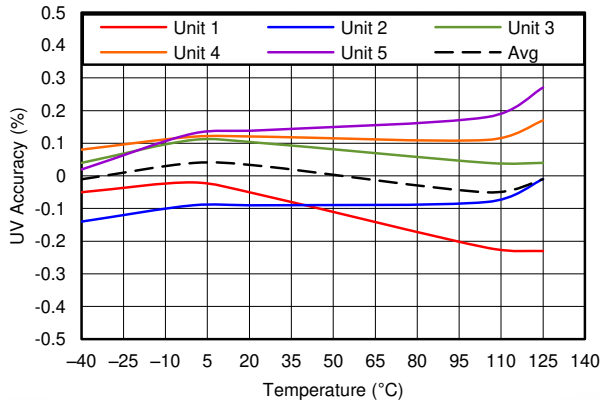


图 5-1. Timing Diagram

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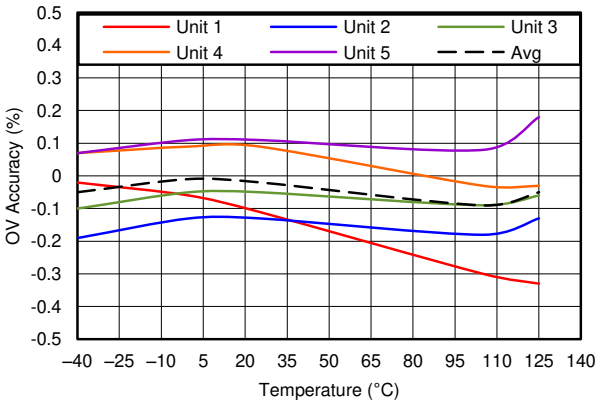
5.7 Typical Characteristics

At T_J = 25°C, V_{DD} = 3V, and R_{PU} = 10kΩ, unless otherwise noted.



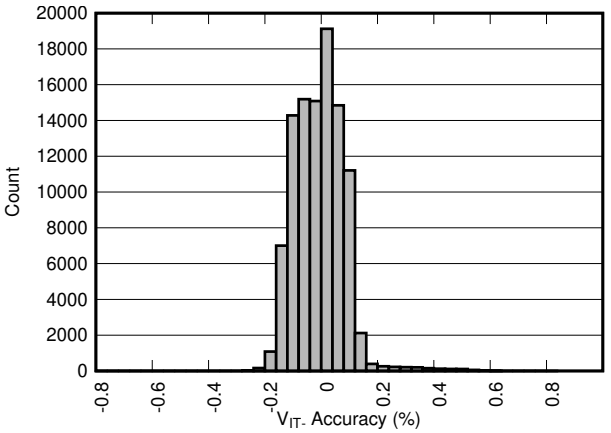
Performance is across V_{DD} with SET high or low

图 5-2. Undervoltage Accuracy vs Temperature



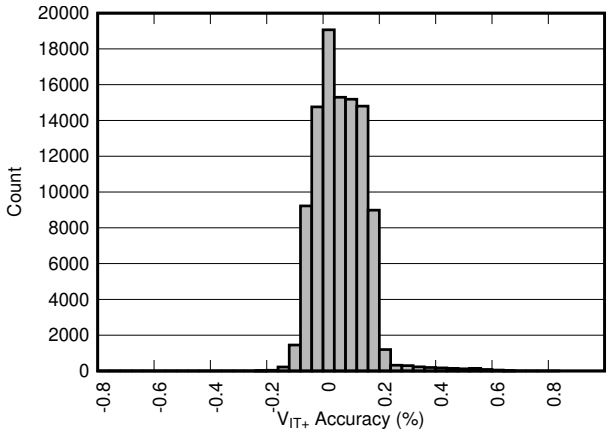
Performance is across V_{DD} with SET high or low

图 5-3. Overvoltage Accuracy vs Temperature



Performance is across V_{DD} with SET high or low

图 5-4. Undervoltage Accuracy Distribution



Performance is across V_{DD} with SET high or low

图 5-5. Overvoltage Accuracy Distribution

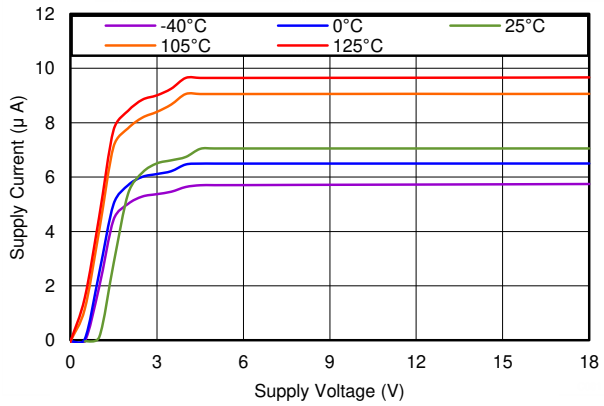


图 5-6. Supply Current vs Supply Voltage

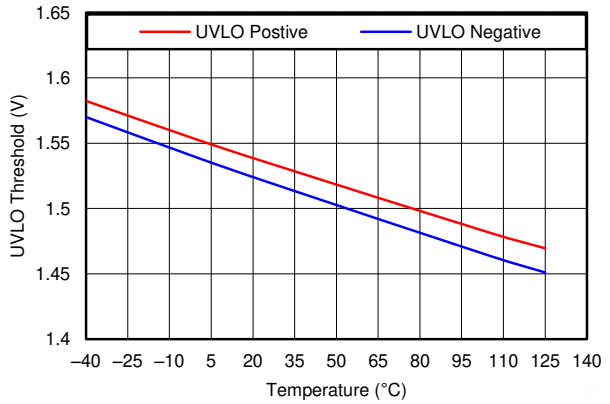
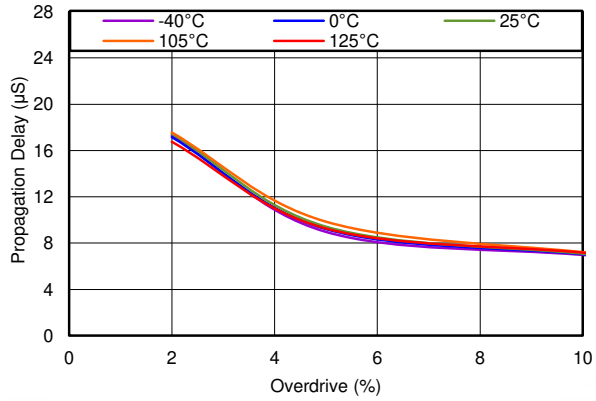


图 5-7. Undervoltage Lockout Threshold vs Temperature

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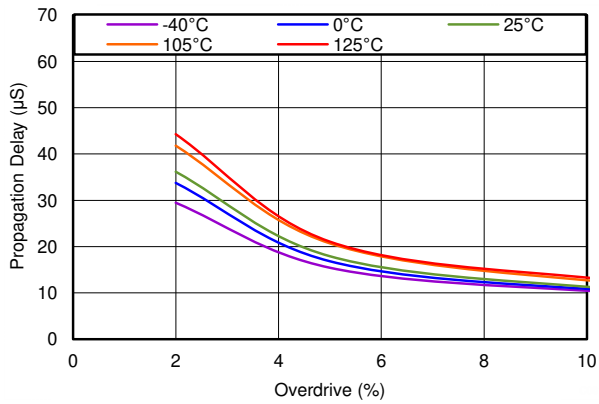
5.7 Typical Characteristics (continued)

At T_J = 25°C, V_{DD} = 3V, and R_{PU} = 10kΩ, unless otherwise noted.



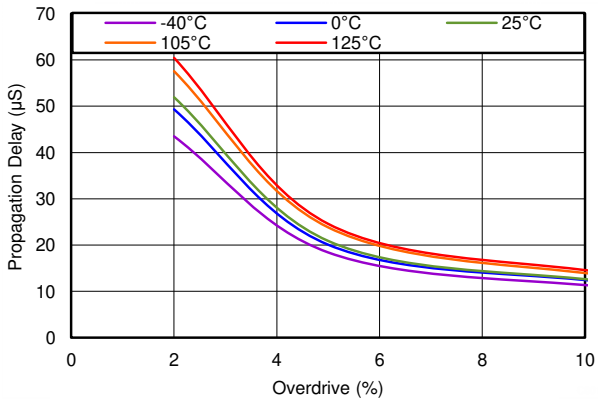
SENSE transitions from high to low

图 5-8. Undervoltage Propagation Delay vs Overdrive



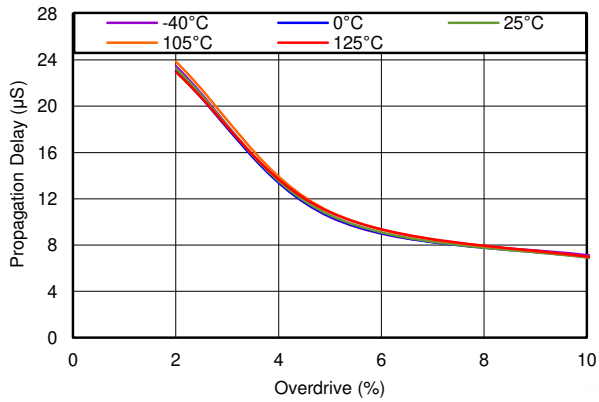
SENSE transitions from low to high

图 5-9. Overvoltage Propagation Delay vs Overdrive



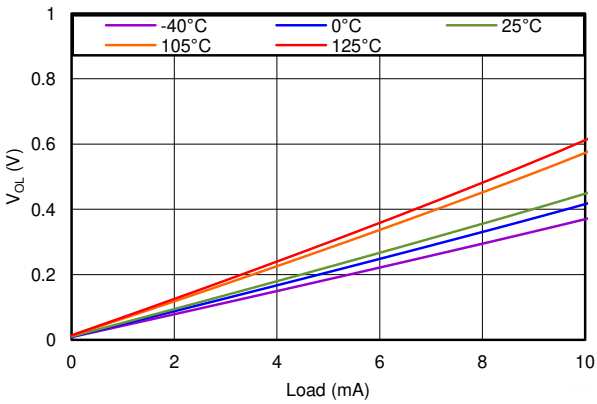
SENSE transitions from low to high

图 5-10. Undervoltage Propagation Delay vs Overdrive



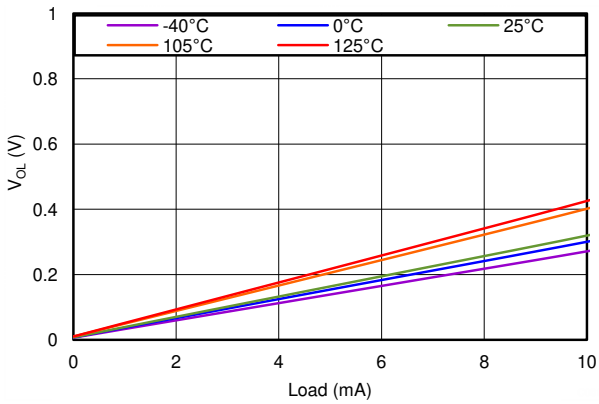
SENSE transitions from high to low

图 5-11. Overvoltage Propagation Delay vs Overdrive



V_{DD} = 1.8V

图 5-12. Low-Level Output Voltage vs Output Current



V_{DD} = 18V

图 5-13. Low-Level Output Voltage vs Output Current

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5.7 Typical Characteristics (continued)

At T_J = 25°C, V_{DD} = 3V, and R_{PU} = 10kΩ, unless otherwise noted.

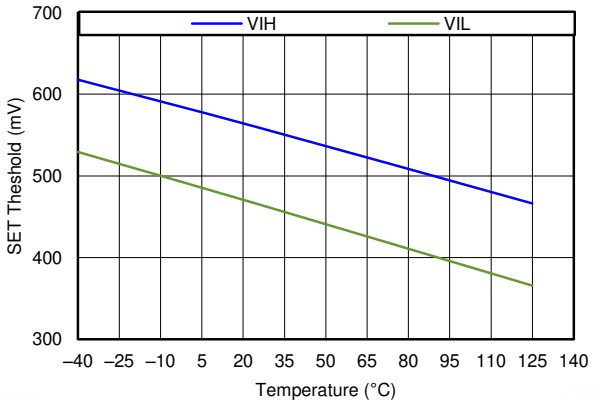


图 5-14. SET Threshold vs Temperature

6 Detailed Description

6.1 Overview

The TPS3702-Q1 family of devices combines two comparators and a precision reference for overvoltage and undervoltage detection. The TPS3702-Q1 features a wide supply voltage range (2V to 18V) and highly accurate window threshold voltages (0.9% over temperature). The TPS3702-Q1 is designed for systems that require an active low signal if the voltage from the monitored power supply exits the accuracy band. The outputs can be pulled up to 18V and can sink up to 10mA.

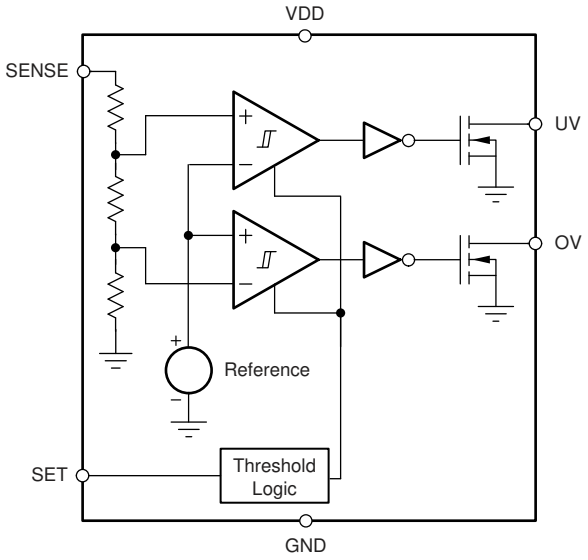
Unlike many other window voltage detectors, the TPS3702-Q1 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors.

The TPS3702-Q1 is designed to assert active low output signals when the monitored voltage is outside the window band. The relationship between the monitored voltage and the states of the outputs is shown in 表 6-1.

表 6-1. Truth Table

CONDITION	OUTPUT	STATUS
SENSE < $V_{IT-(UV)}$	UV low	UV is asserted
SENSE > $V_{IT-(UV)}$ + V_{HYS}	UV high	UV is high impedance
SENSE > $V_{IT+(OV)}$	OV low	OV is asserted
SENSE < $V_{IT+(OV)}$ – V_{HYS}	OV high	OV is high impedance

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Input (SENSE)

The TPS3702-Q1 combines two comparators with a precision reference voltage and a trimmed resistor divider. Only a single external input is monitored by the two comparators because the resistor divider is internal to the device. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides some noise immunity and maintains stable operation.

The SENSE input can vary from ground to 6.5V (7.0V, absolute maximum), regardless of the device supply voltage used. Although not required in most cases, for noisy applications good analog design practice is to place a 1nF to 10nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal.

For the undervoltage detector, the undervoltage output is driven to logic low when the SENSE voltage drops below the undervoltage falling threshold, $V_{IT-(UV)}$. When the voltage exceeds the undervoltage rising threshold, $V_{IT+(UV)}$ (which is $V_{IT-(UV)}$ + V_{HYS}), the undervoltage output goes to a high-impedance state; see 图 5-1.

For the overvoltage detector, the overvoltage output is driven to logic low when the voltage at SENSE exceeds the overvoltage rising threshold, $V_{IT+(OV)}$. When the voltage drops below the overvoltage falling threshold, $V_{IT-(OV)}$ (which is $V_{IT+(OV)}$ – V_{HYS}), the overvoltage output goes to a high-impedance state; see 图 5-1. Together, these two comparators form a window voltage detector function as described in the *节 7.1.1* section. Also see the *节 8.1.2* section.

6.3.2 Outputs (UV, OV)

In a typical TPS3702-Q1 application, the outputs are connected to a reset or enable input of a processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the outputs are connected to the enable input of a voltage regulator [such as a dc-dc converter or low-dropout regulator (LDO)].

The TPS3702-Q1 provides two open-drain outputs (UV and OV) and uses pull-up resistors to hold these lines high when the output goes to a high-impedance state. Connect the pull-up resistors to the proper voltage rails to enable the outputs to be connected to other devices at the correct interface voltage levels. The TPS3702-Q1 outputs can be pulled up to 18V, independent of the device supply voltage. To make sure of proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL}, output capacitive loading, and output leakage current ($I_{D(leak)}$). These values are specified in the *节 5.5* table. Use wired-OR logic to merge the undervoltage and overvoltage signals into one logic signal that goes low if either outputs are asserted because of a fault condition.

表 6-1 describes how the outputs are either asserted low or high impedance. See 图 5-1 for a timing diagram that describes the relationship between the threshold voltages and the respective output.

6.3.3 User-Configurable Accuracy Band (SET)

The TPS3702-Q1 has a remarkable feature allowing each device to be set for one of two accuracy bands, 表 8-1 describes the available accuracy bands with nominal thresholds ranging from ±2% to ±10% of the monitored rail nominal voltage. Forcing the voltage on the SET pin above the high-level SET pin input voltage, $V_{IH(SET)}$, sets the thresholds for the tighter window whereas forcing the voltage on the SET pin below the low-level SET pin input voltage, $V_{IL(SET)}$, sets the thresholds for the wider window.

Using the TPS3702Cxxx-Q1 as an example, when $V_{SET} \geq V_{IH(SET)}$ the nominal thresholds are set to ±4% (see 图 6-1). Thus, when the positive-going and negative-going threshold accuracy is accounted for, the device outputs an active low signal for voltage excursions outside a ±4.9% band (worst case), which is calculated by taking the nominal threshold percentage for that given part number and adding that value to the threshold accuracy found in the *节 5* section. Similarly, when $V_{SET} \leq V_{IL(SET)}$, the nominal thresholds are set to ±9% and the device outputs an active low signal for voltage excursions outside the ±9.9% band (worst case).

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The ability for the user to change the accuracy band allows a system to programmatically change the accuracy band during certain conditions. One example is during system start up when the monitored voltage can be slightly outside the typical accuracy specifications but a reset signal is not desired. In this case, V_{SET} can be set below $V_{IL(SET)}$ to detect voltage excursions outside the 10% band and, after the system is fully started up, V_{SET} can be pulled higher than $V_{IH(SET)}$, thus tightening the band to ±5%.

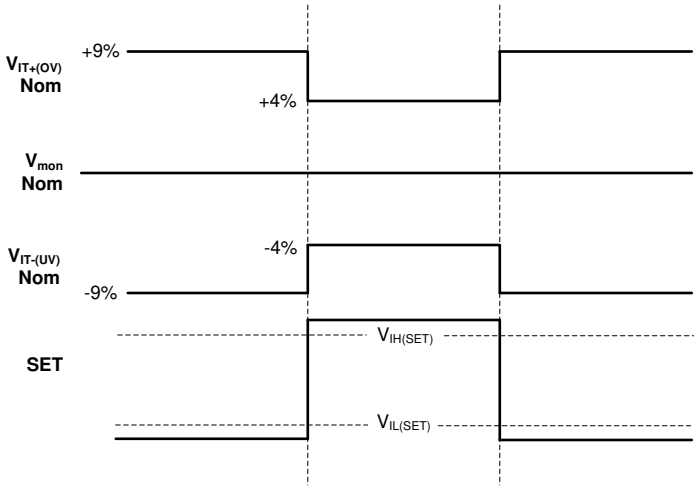


图 6-1. TPS3702Cxxx User-Configurable Accuracy Bands

Another benefit of allowing the user to change the accuracy band is the reduction in qualification costs. Users who have multiple rail monitoring needs (such as some rails that must be within ±5% of the nominal voltage and other rails that must be within ±10% of the same nominal voltage) benefit by only having to spend the time and money qualifying one device instead of two.

6.4 Device Functional Modes

6.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on VDD is greater than UVLO for approximately 300µs (t_{SD}), the undervoltage and overvoltage signals correspond to the voltage on the SENSE pin; see 表 6-1.

6.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} <$ UVLO)

When the voltage on VDD is less than the device UVLO voltage but greater than the power-on reset voltage ($V_{(POR)}$), the undervoltage output is asserted and the overvoltage output is high impedance, regardless of the voltage on SENSE.

6.4.3 Power-On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), both outputs are undefined and are not to be relied upon for proper device function.

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7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TPS3702-Q1 is a precision window voltage detector that can be used in several different configurations. The supply voltage (V_{DD}), the monitored voltage, and the output pull-up voltage can be independent voltages or connected in many configurations. 图 7-1 shows how the outputs operate with respect to the voltage on the SENSE pin.

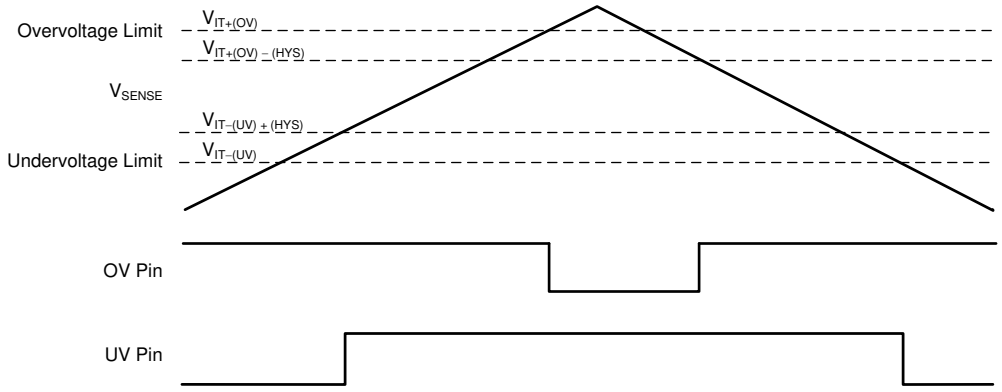


图 7-1. Window Voltage Detector Operation

The following sections show the connection configurations and the voltage limitations for each configuration.

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7.1.1 Window Voltage Detector Considerations

The inverting and non-inverting configurations of the comparators form a window voltage detector circuit by using the internal resistor divider. The internal resistor divider allows for set voltage thresholds that already account for the tolerances of the resistors in the resistor divider. The UV and OV pins signal undervoltage and overvoltage conditions, respectively, on the SENSE pin, as shown in 图 7-2.

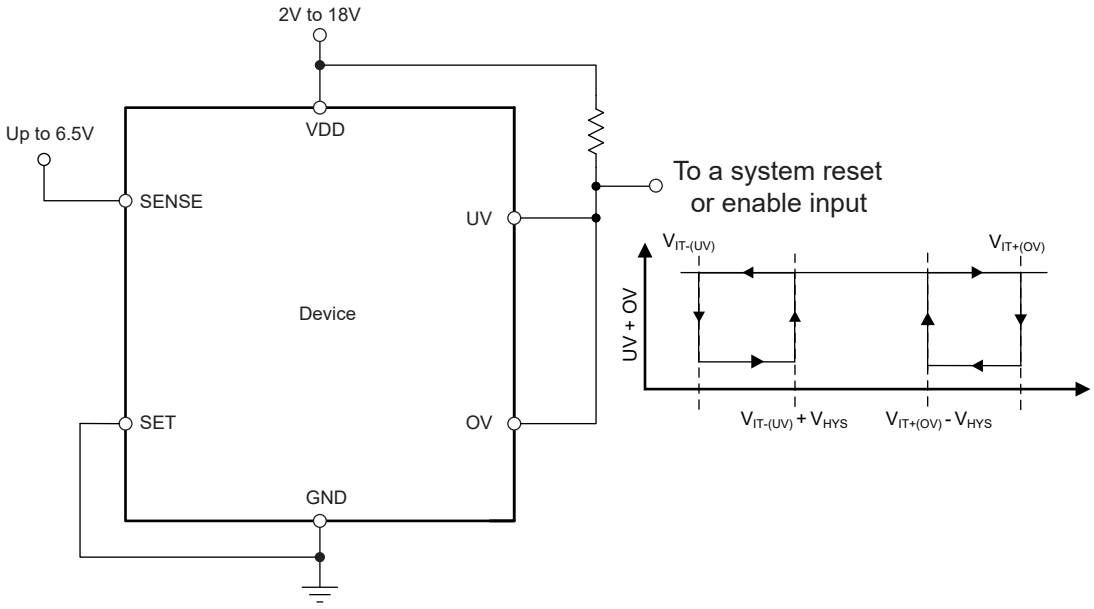


图 7-2. Window Voltage Detector Schematic

The TPS3702-Q1 flags the overvoltage or undervoltage conditions with the most accuracy to make sure of proper system operation. The highest accuracy threshold voltages are $V_{IT-(UV)}$ and $V_{IT+(OV)}$, and correspond with the falling SENSE undervoltage flag and the rising SENSE overvoltage flag, respectively. These thresholds represent the accuracy when the monitored voltage changes from being within the desired window (when both the undervoltage and overvoltage outputs are high) to when the monitored voltage goes outside the desired window, indicating a fault condition. If the monitored voltage is outside of the valid window (V_{SENSE} is less than the undervoltage limit, $V_{IT-(UV)}$, or greater than overvoltage limit, $V_{IT+(OV)}$), then the SENSE threshold voltages to enter into the valid window are $V_{IT+(UV)} = V_{IT-(UV)} + V_{HYS}$ or $V_{IT-(OV)} = V_{IT+(OV)} - V_{HYS}$.

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7.1.2 Input and Output Configurations

图 7-3 to 图 7-5 illustrate examples of the various input and output configurations.

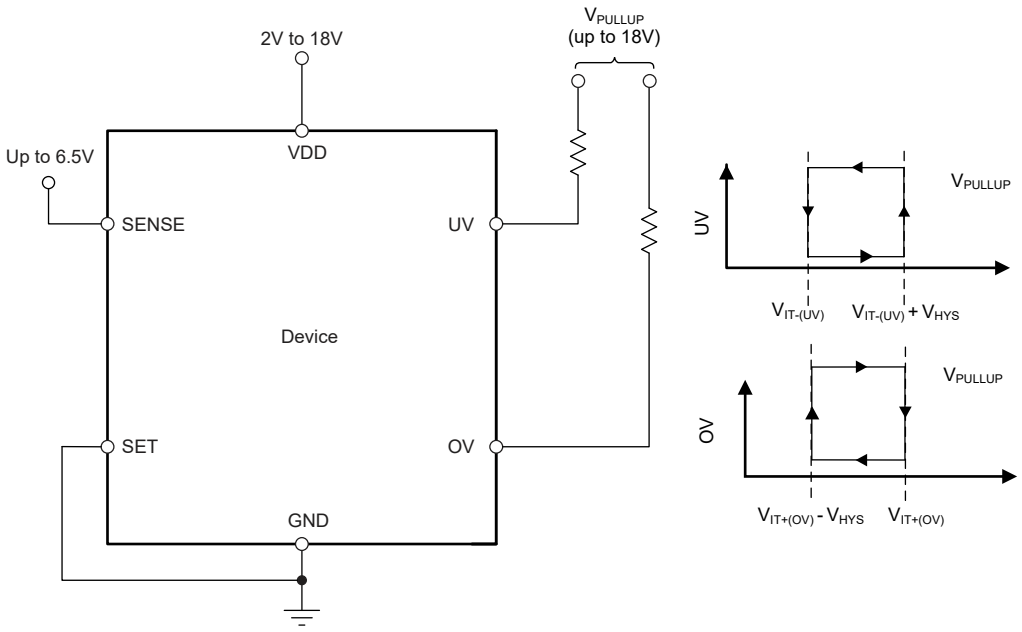


图 7-3. Interfacing to Voltages Other Than V_{DD}

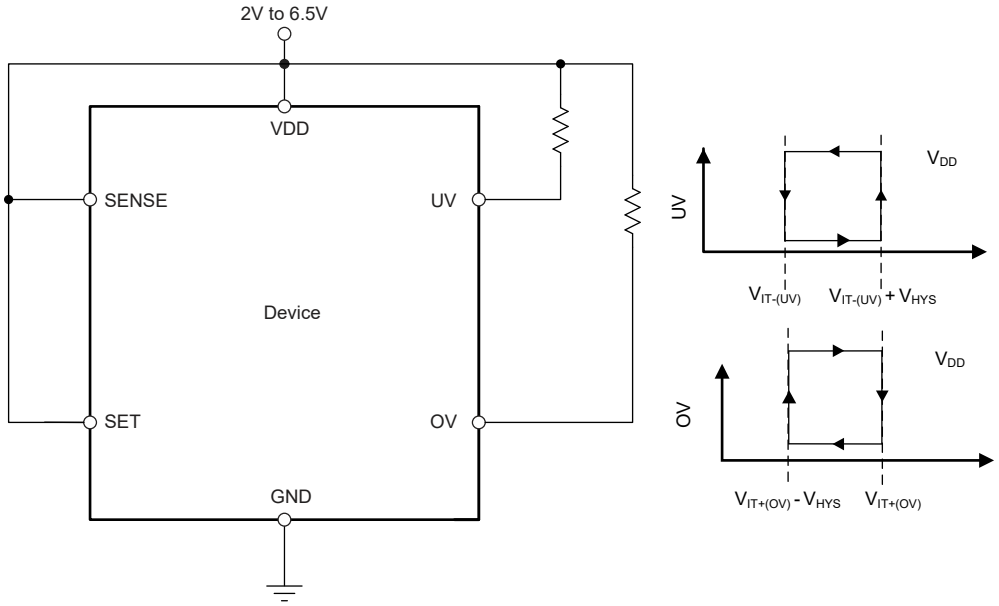


图 7-4. Monitoring the Same Voltage as V_{DD} with Wired-OR Logic

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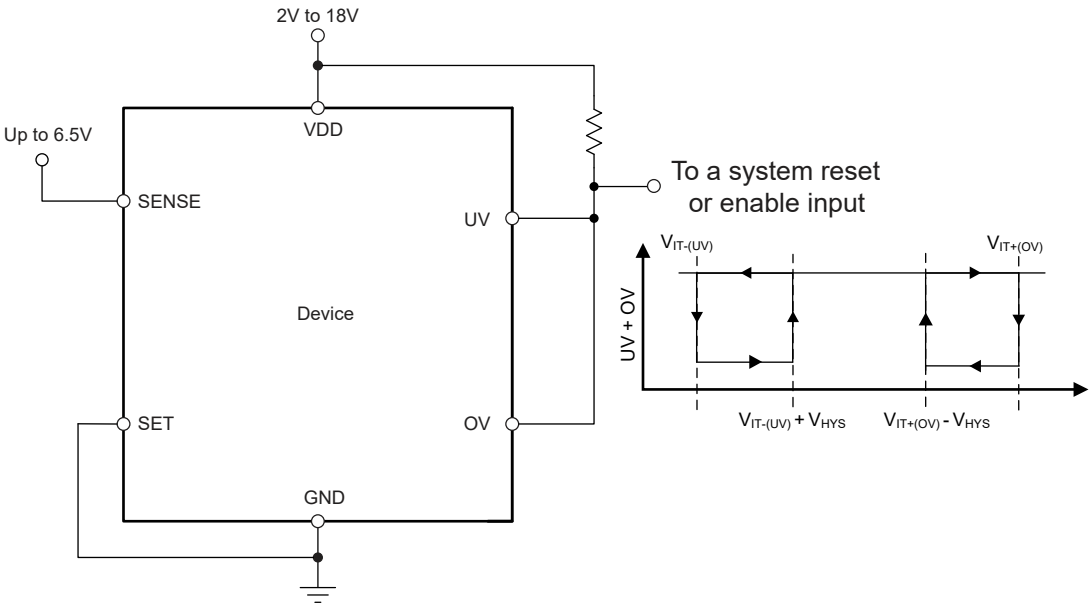


图 7-5. Monitoring a Voltage Other Than V_{DD} with Wired-OR Logic

Note that the SENSE input can also monitor voltages that are higher than $V_{SENSE\ (max)}$ or that may not be designed for rail voltages with the use of an external resistor divider network. If a resistor divider is used to reduce the voltage on the SENSE pin, make sure that the I_{SENSE} current is accounted for so the accuracy is not unexpectedly affected. As a general approximation, the current flowing through the resistor divider to ground must be greater than 100 times the current going into the SENSE pin. See application report *Optimizing Resistor Dividers at a Comparator Input* (SLVA450) for a more in-depth discussion on setting an external resistor divider.

7.1.3 Immunity to SENSE Pin Voltage Transients

The TPS3702-Q1 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient.

Overdrive is defined by how much the V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs (UV and OV). Threshold overdrive is calculated as a percent of the threshold in question, as shown in 方程式 1:

$$\text{Overdrive} = | (V_{SENSE} / V_{IT} - 1) \times 100\% | \quad (1)$$

where:

- V_{IT} is either V_{IT-} or V_{IT+} for UV or OV.

图 5-8 to 图 5-11 illustrate the V_{SENSE} minimum detectable pulse versus overdrive, and can be used to visualize the relationship that overdrive has on propagation delay.

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7.2 Typical Application

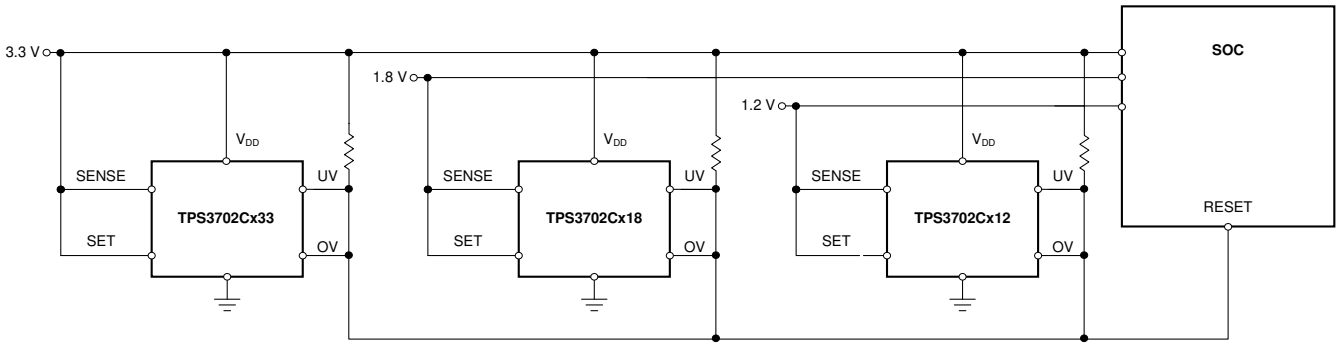


图 7-6. ±5% Window Voltage Detector for SOC Power Rails

7.2.1 Design Requirements

表 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored rails	3.3V nominal, with alerts if outside of ±5% of 3.3V (including device accuracy)	Worst case $V_{IT+(OV)}$ = 3.463V (4.94%), Worst case $V_{IT-(UV)}$ = 3.139V (4.86%)
	1.8V nominal, with alerts if outside of ±5% of 1.8V (including device accuracy)	Worst case $V_{IT+(OV)}$ = 1.889V (4.94%), Worst case $V_{IT-(UV)}$ = 1.712V (4.86%)
	1.2V nominal, with alerts if outside of ±5% of 1.2V (including device accuracy)	Worst case $V_{IT+(OV)}$ = 1.259V (4.94%), Worst case $V_{IT-(UV)}$ = 1.142V (4.86%)
Output logic voltage	3.3V CMOS	3.3V CMOS
Maximum device current consumption	50µA	40.5µA (maximum), 24µA (typical)

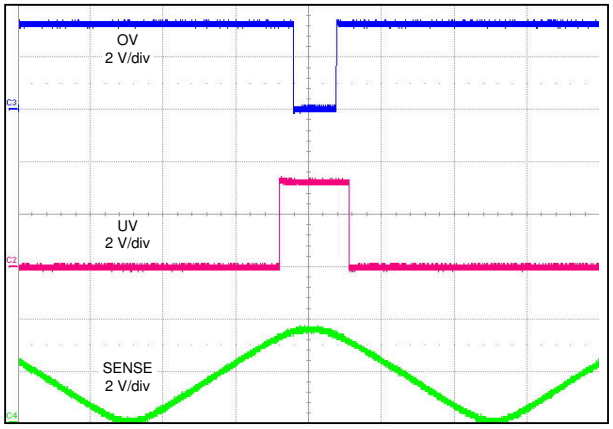
7.2.2 Detailed Design Procedure

Determine which version of the TPS3702-Q1 best suits the application nominal rail and window tolerances. See 表 8-1 for selecting the appropriate device number for the application needs. If the nominal rail voltage to be monitored is not listed as an option, a resistor divider can be used to reduce the voltage to a nominal voltage that is available. The current I_{SENSE} causes an error in the voltage detected at the SENSE pin because the SENSE current only flows through the resistor at the top of the resistor divider. The larger the current through the resistor divider to ground, the smaller this error can be. To optimize this resistor divider, refer to application report *Optimizing Resistor Dividers at a Comparator Input* (SLVA450) for more information.

When the outputs switch to the high-Z state, the rise time of the UV or OV node depends on the pull-up resistance and the capacitance on that node. Choose pull-up resistors that satisfy both the downstream timing requirements and the sink current required to have a V_{OL} low enough for the application; 10kΩ to 1MΩ resistors are a good choice for low-capacitive loads.

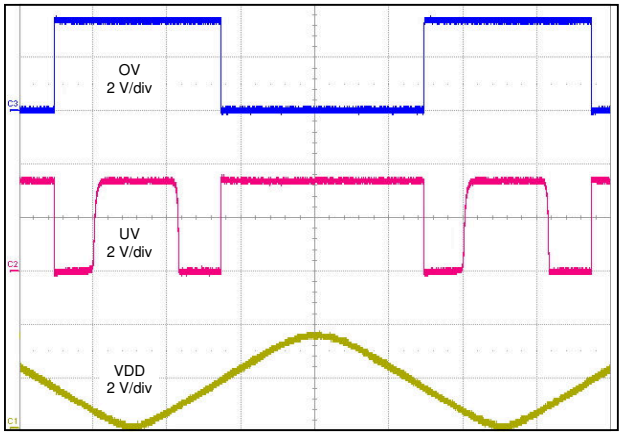
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7.2.3 Application Curves



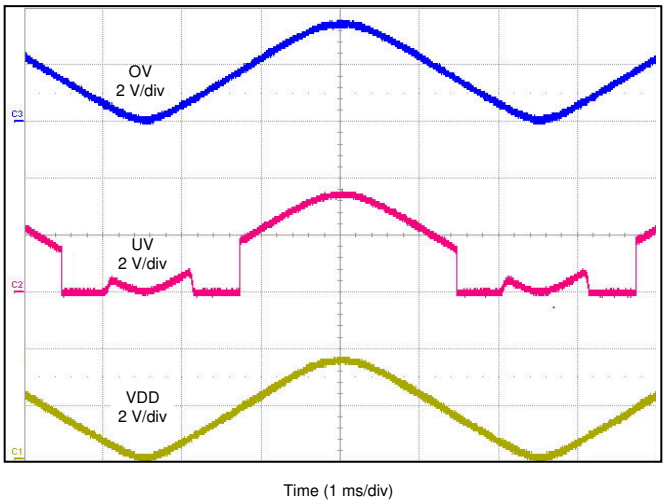
V_{SENSE} goes from 0V to 3.47V ($V_{IT+(OV)}$), V_{DD} = 3.3V, $V_{PULL-UP}$ = 3.3V

图 7-7. TPS3702CX33-Q1 Window Voltage Detector Function



V_{DD} goes from 0V to 3.3V, V_{SENSE} = 3.47V (above $V_{IT+(OV)}$)

图 7-8. TPS3702CX33-Q1 Startup with $V_{PULL-UP}$ = 3V



V_{DD} goes from 0V to 3.3V, V_{SENSE} = 3.3V

图 7-9. TPS3702CX33-Q1 Startup with $V_{PULL-UP}$ = V_{DD}

7.3 Power Supply Recommendations

The TPS3702-Q1 is designed to operate from an input voltage supply range between 2V and 18V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1µF capacitor between the VDD pin and the GND pin. This device has a 20V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 20V, additional precautions must be taken.

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7.4 Layout

7.4.1 Layout Guidelines

- Place the VDD decoupling capacitor close to the device.
- Avoid using long traces for the VDD supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum VDD voltage.

7.4.2 Layout Example

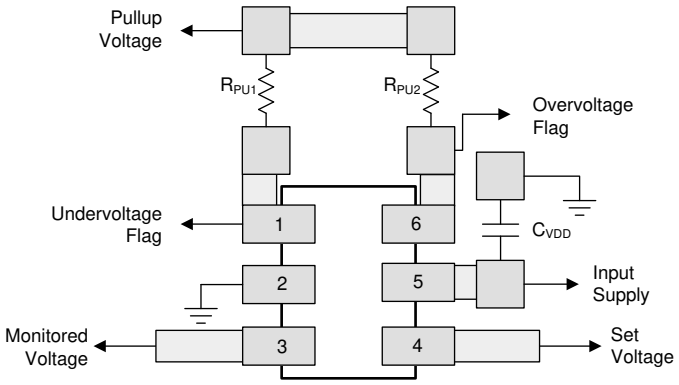


图 7-10. Recommended Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS3702. The TPS3702CX33EVM-683 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

8.1.2 Device Nomenclature

表 8-1 shows how to decode the function of the device based on the part number, with TPS3702CX33-Q1 used as an example.

表 8-1. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE
TPS3702 (high-accuracy window voltage detector family)	—	—
C (nominal thresholds as a percent of the nominal monitored voltage)	A	SET pin high = ±2%, SET pin low = ±6%
	B	SET pin high = ±3%, SET pin low = ±7%
	C	SET pin high = ±4%, SET pin low = ±9%
	D	SET pin high = ±5%, SET pin low = ±10%
X (hysteresis option)	X	0.55%
	Y	1.0%
33 (nominal monitored voltage option)	10	1.0V
	12	1.2V
	18	1.8V
	33	3.3V
	50	5.0V
Q1 (automotive version)	—	—

表 8-2 shows the released versions of the TPS3702, including the nominal undervoltage and overvoltage thresholds. Contact the factory for details and availability of other options shown in 表 8-1; minimum order quantities apply.

表 8-2. Released Device Thresholds

PRODUCT	NOMINAL SUPPLY (V)	HYSTERESIS (%)	UV THRESHOLD (V) SET ⩽ $V_{IL(SET)}$	UV THRESHOLD (V) SET ⩾ $V_{IH(SET)}$	OV THRESHOLD (V) SET ⩽ $V_{IL(SET)}$	OV THRESHOLD (V) SET ⩾ $V_{IH(SET)}$
TPS3702CX10	1.0	0.5	0.91	0.96	1.09	1.04
TPS3702CX12	1.2	0.5	1.09	1.15	1.31	1.25
TPS3702AX18	1.8	0.5	1.69	1.76	1.91	1.84
TPS3702CX18	1.8	0.5	1.64	1.73	1.96	1.87
TPS3702AX33	3.3	0.5	3.10	3.23	3.50	3.37
TPS3702CX33	3.3	0.5	3.00	3.17	3.60	3.43
TPS3702CX50	5.0	0.5	4.55	4.80	5.45	5.20

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8.2 Documentation Support

8.2.1 Related Documentation

Optimizing Resistor Dividers at a Comparator Input, SLVA450

TPS3702CX33EVM-683 Evaluation Module, SBVU026

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

Changes from Revision B (December 2015) to Revision C (March 2024)	Page
• 将整个数据表中的器件名称更改为“电压检测器”	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated timing diagram	6
• Changed device naming to voltage detector	10

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3702AX18QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFIO
TPS3702AX18QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFIO
TPS3702AX33QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFEO
TPS3702AX33QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFEO
TPS3702CX10QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFGO
TPS3702CX10QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFGO
TPS3702CX12QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFFO
TPS3702CX12QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFFO
TPS3702CX18QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFJO
TPS3702CX18QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFJO
TPS3702CX33QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFHO
TPS3702CX33QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFHO
TPS3702CX50QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFWO
TPS3702CX50QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZFWO

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3702-Q1 :

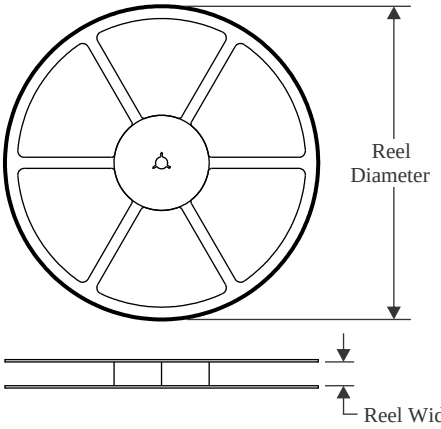
- Catalog : TPS3702

NOTE: Qualified Version Definitions:

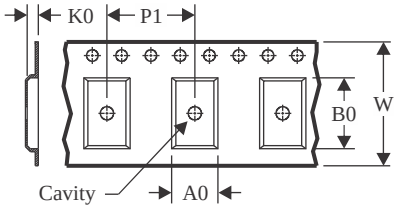
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

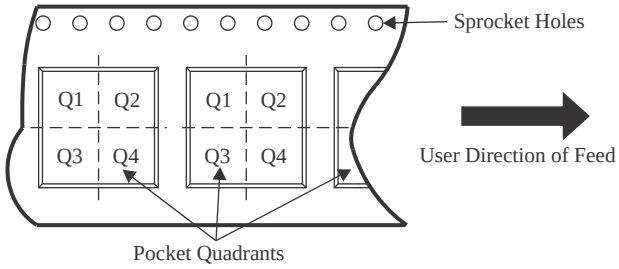


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

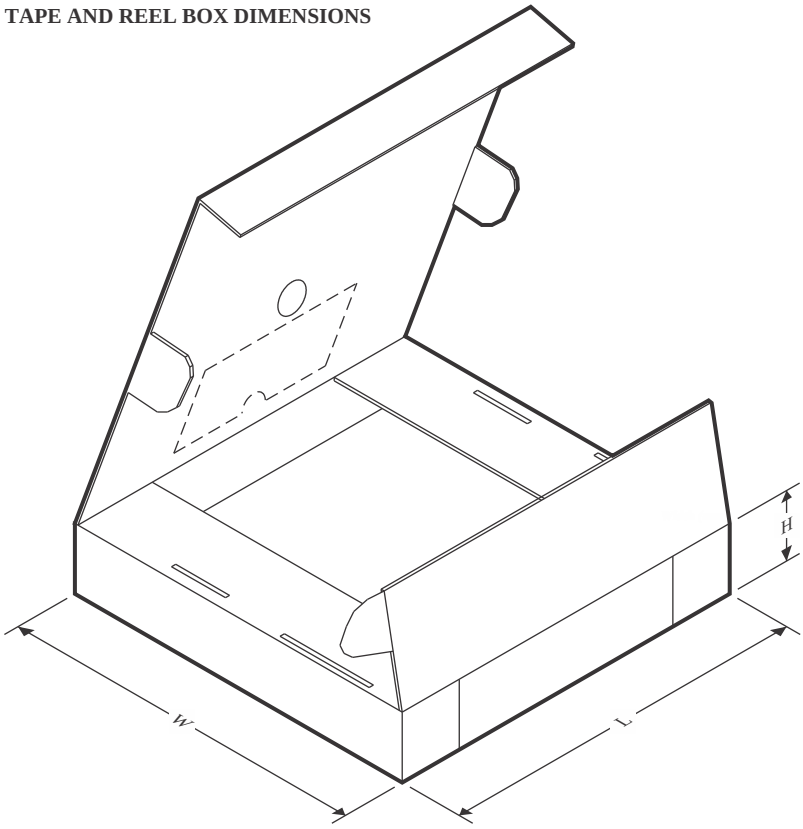
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3702AX18QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702AX33QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702CX10QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702CX12QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702CX18QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702CX33QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3702CX50QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

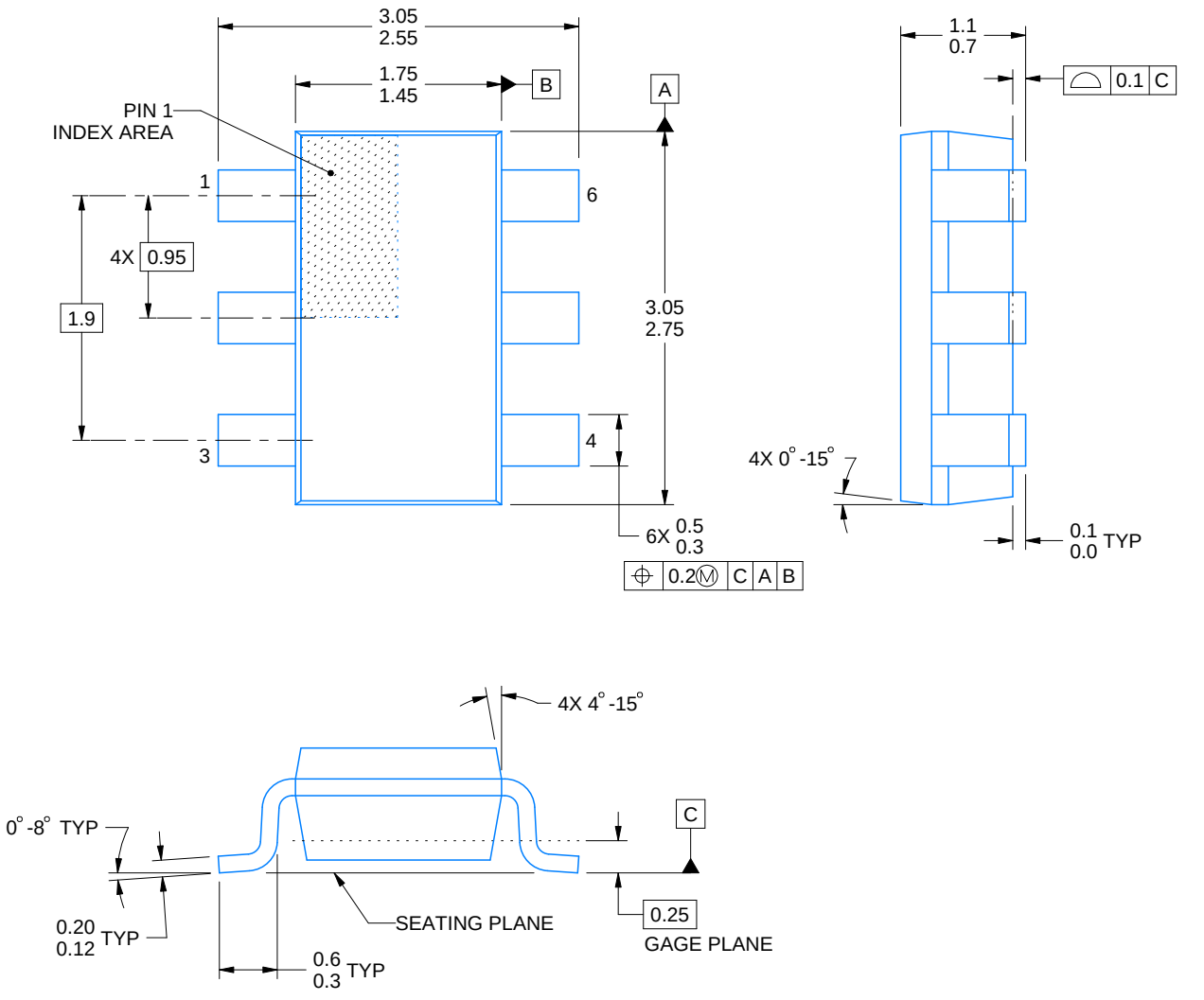
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3702AX18QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702AX33QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702CX10QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702CX12QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702CX18QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702CX33QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3702CX50QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

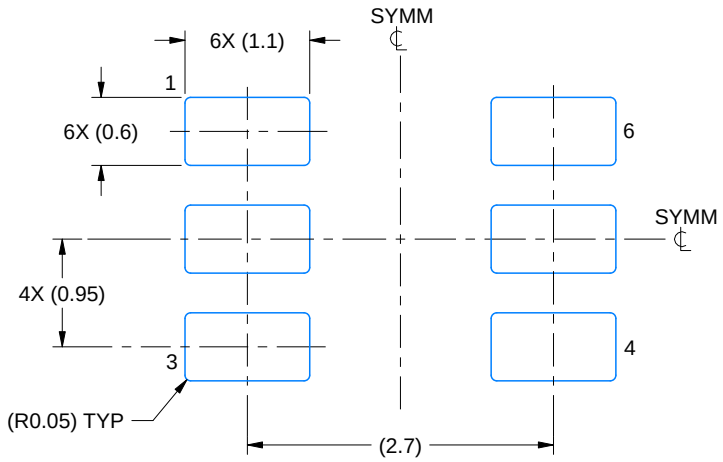
SMALL OUTLINE TRANSISTOR



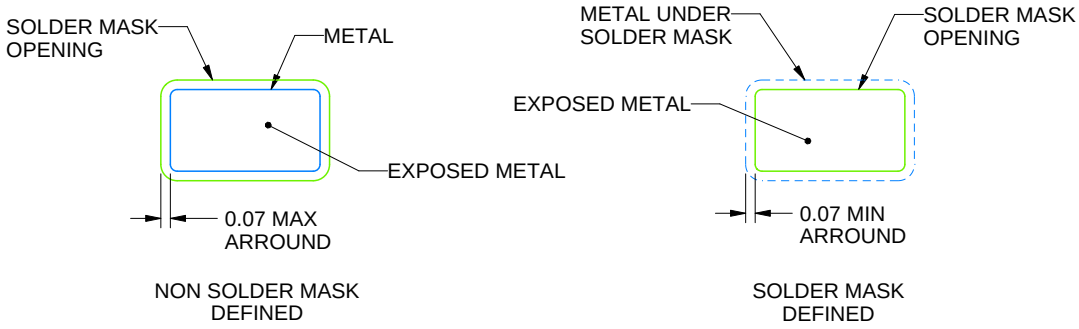
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

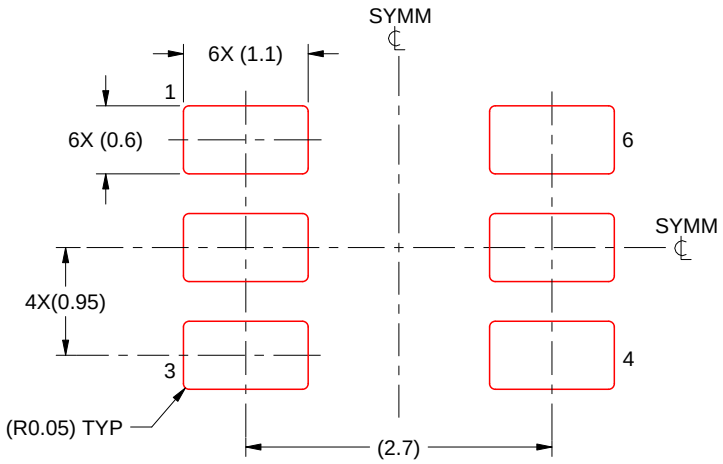


SOLDERMASK DETAILS

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NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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