

具有受控接通功能的超低导通电阻，4A 集成负载开关

 查询样品: [TPS22920L](#)

特性

- 输入电压范围: **0.75V 至 3.6V**
- 集成导通场效应晶体管 (FET)
 $R_{DS(ON)} = 2m\Omega$ (典型值), 此时 $V_{输入} = 3.6V$
- 超低导通电阻
 - $V_{输入} = 3.6V$ 时, $r_{导通} = 5.3m\Omega$
 - $V_{输入} = 2.5V$ 时, $r_{导通} = 5.4m\Omega$
 - $V_{输入} = 1.8V$ 时, $r_{导通} = 5.5m\Omega$
 - $V_{输入} = 1.2V$ 时, $r_{导通} = 5.8m\Omega$
 - $V_{输入} = 1.05V$ 时, $r_{导通} = 6.1m\Omega$
 - $V_{输入} = 0.75V$ 时, $r_{导通} = 7.3m\Omega$
- 超小型 8 引脚芯片级封装 (芯片级球栅阵列封装 (DSBGA)) 0.9mm x 1.9mm, 焊球间距 0.5mm
- **4A** 最大持续开关电流
- 关断电流最大值 **5.5 μ A**
- 低阈值 (**1.2V**) 通用输入输出 (GPIO) 控制输入
- 受控转换率以避免涌入电流
- 快速输出放电 (QOD) 晶体管
- 静电放电 (ESD) 性能测试符合 **JESD 22** 标准
 - **4000V** 人体模型 (A114-B, II 类)
 - **1000V** 充电器件模型 (C101)

应用范围

- **Thunderbolt™**
- 固态硬盘 (SSD)
- 笔记本/超薄
- 平板个人电脑
- 智能手机
- 便携式 GPS 器件
- **MP3** 播放器

说明

TPS22920L 是一款小型, 超低 $R_{导通}$ 负载开关, 此开关具有可控接通功能。此器件包含一个 N 通道金属氧化物半导体场效应晶体管 (MOSFET), 此 MOSFET 可运行在 0.75V 至 3.6V 的输入电压范围内, 并且开关电流高达 4A。一个集成的电荷泵把 NMOS 开关偏置, 以实现一个最小的开关导通电阻 ($R_{导通}$)。此开关可由一个打开/关闭输入 (ON) 控制, 此输入可与低压控制信号直接对接。

TPS22920L 包含一个 1250 Ω 片上负载电阻器用于在此开关被关闭时进行快速输出放电。

TPS22920L 有一个内部受控上升时间来减少涌入电流。电压为 3.6V 时, TPS22920L 特有一个 627 μ s 的上升时间。

TPS22920L 采用超小型、节省空间的 8 引脚芯片级封装并可在 -40 $^{\circ}$ C 至 85 $^{\circ}$ C 的自然通风温度范围内运行。

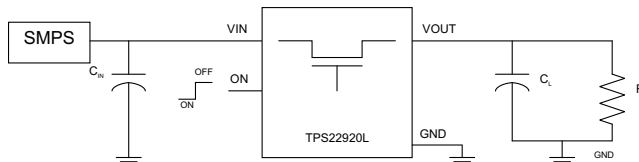


图 1. 典型应用

特性列表

	3.6V 时的 $r_{导通}$ (典型值)	3.6V 时的上升时间 (典型值)	快速输出放电 ⁽¹⁾	最大输出电压	使能
TPS22920L	5.3m Ω	627 μ s	是	4A	低电平有效

(1) 此特性可通过一个 1250 Ω 电阻器将开关的输出放电至接地水平, 从而防止此输出悬空。请见应用部分“输出下拉”



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com

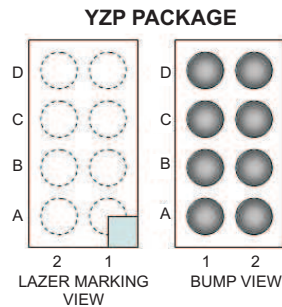


Figure 2. Bump Assignments

Bump Assignments (YZP Package)

D	GND	ON
C	VOUT	VIN
B	VOUT	VIN
A	VOUT	VIN
	1	2

Pin Description

TPS22920L	PIN NAME	DESCRIPTION
YZP		
D1	GND	Ground.
D2	ON	Switch control input, active low. Do not leave floating.
A1, B1, C1	VOUT	Switch output.
A2, B2, C2	VIN	Switch input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turn-on of the channel. See Application Information section for more information.

FUNCTIONAL BLOCK DIAGRAM

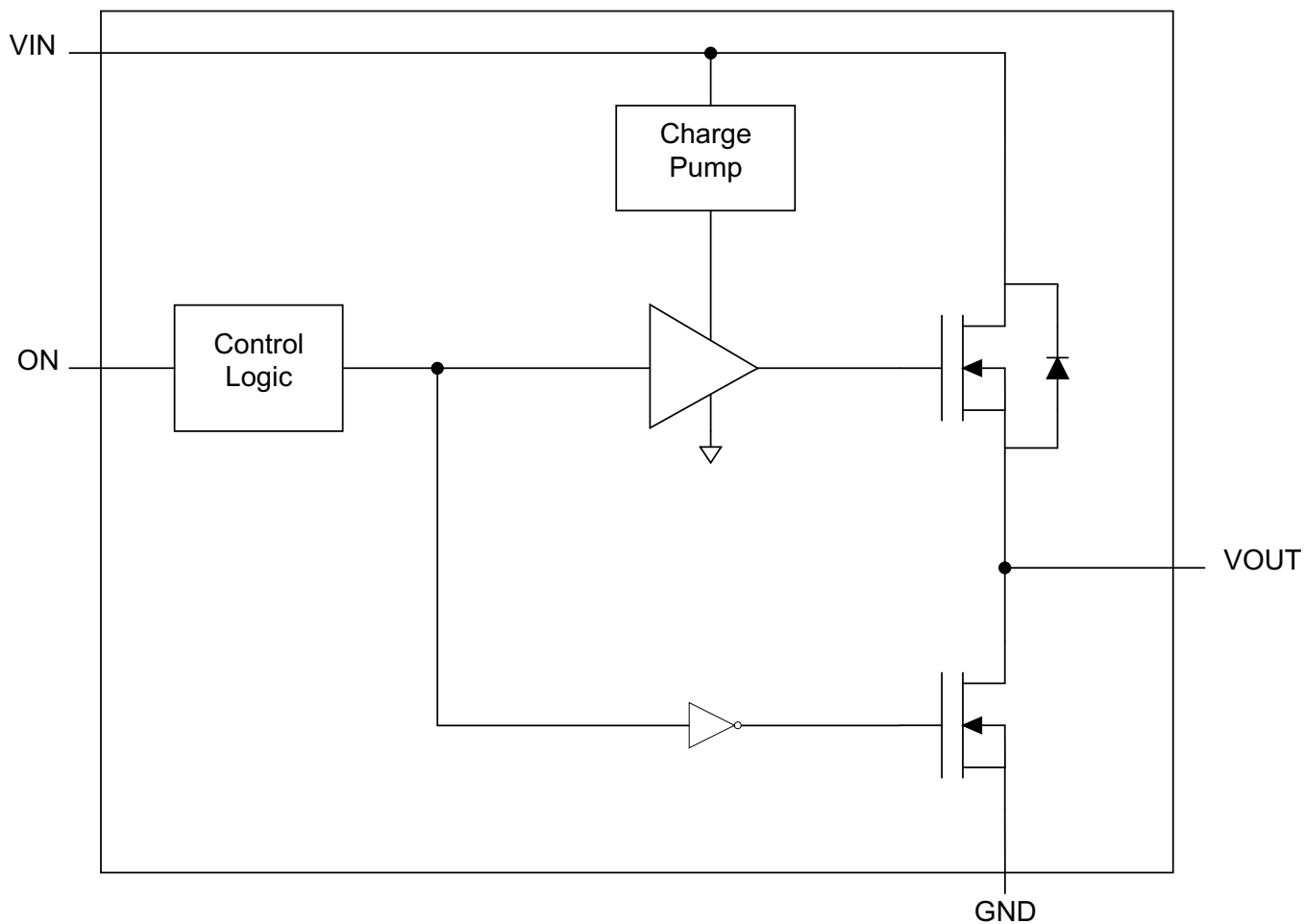


Figure 3. Functional block diagram of the TPS22920L

FUNCTION TABLE

ON	VIN to VOUT	VOUT to GND ⁽¹⁾
L	ON	OFF
H	OFF	ON

(1) See Application section 'Output Pull-Down'

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT	
V _{IN}	VIN voltage range	-0.3 to 4	V	
V _{OUT}	VOUT voltage range	V _{IN} + 0.3	V	
V _{ON}	ON-pin voltage range	-0.3 to 4	V	
I _{MAX}	Maximum continuous switch current	4	A	
I _{PLS}	Maximum pulsed switch current, pulse <300µS, 2% duty cycle	6	A	
T _A	Operating free-air temperature range	-40 to 85	°C	
T _J	Maximum junction temperature	125	°C	
T _{STG}	Storage temperature range	-65 to 150	°C	
T _{LEAD}	Maximum lead temperature (10-s soldering time)	300	°C	
ESD	Electrostatic discharge protection	Human-Body Model (HBM)	4000	V
		Charged Device Model (CDM)	1000	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS22920L	UNITS
		CSP (8 PINS)	
θ _{JA}	Junction-to-ambient thermal resistance	130	°C/W
θ _{JCtop}	Junction-to-case (top) thermal resistance	54	
θ _{JB}	Junction-to-board thermal resistance	51	
ψ _{JT}	Junction-to-top characterization parameter	1	
ψ _{JB}	Junction-to-board characterization parameter	50	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V _{IN}	VIN voltage range	0.75	3.6	V
V _{OUT}	VOUT voltage range		V _{IN}	V
V _{IH}	High-level input voltage, ON	V _{IN} = 2.5-V to 3.6 V		V
		V _{IN} = 0.75-V to 2.49 V		V
V _{IL}	Low-level input voltage, ON	V _{IN} = 2.5-V to 3.6 V		V
		V _{IN} = 0.75-V to 2.49 V		V
C _{IN}	Input Capacitor	1 ⁽¹⁾		µF

(1) See *Input Capacitor* section in Application Information.

ELECTRICAL CHARACTERISTICS

 $V_{IN} = 0.75\text{ V to }3.6\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP ⁽¹⁾	MAX	UNIT
$I_{Q,VIN}$	Quiescent current for VIN	$I_{OUT} = 0\text{ A}, V_{ON} = 0\text{ V}$	$V_{IN} = 3.6\text{ V}$	Full		68	160	μA
			$V_{IN} = 2.5\text{ V}$			40	70	
			$V_{IN} = 1.8\text{ V}$			25	350	μA
			$V_{IN} = 1.2\text{ V}$			103	200	
			$V_{IN} = 1.05\text{ V}$			78	110	μA
			$V_{IN} = 0.75\text{ V}$			37	70	
$I_{SD,VIN}$	Shutdown current for VIN	$V_{ON} = 3.6\text{ V}, V_{OUT} = 0\text{ V}$		Full			5.5	μA
R_{ON}	On-Resistance		$V_{IN} = 3.6\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		5.3	8.8	$\text{m}\Omega$
				Full			9.8	
			$V_{IN} = 2.5\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		5.4	8.9	$\text{m}\Omega$
				Full			9.9	
			$V_{IN} = 1.8\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		5.5	9.1	$\text{m}\Omega$
				Full			10.1	
			$V_{IN} = 1.2\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		5.8	9.4	$\text{m}\Omega$
				Full			10.4	
			$V_{IN} = 1.05\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		6.1	9.7	$\text{m}\Omega$
				Full			10.8	
			$V_{IN} = 0.75\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		7.3	11.0	$\text{m}\Omega$
				Full			12.4	
R_{PD}	Output pull down resistance ⁽²⁾	$V_{IN} = 3.3\text{ V}, V_{ON} = 3.6\text{ V}, I_{OUT} = 3\text{ mA}$		Full		1250	1500	Ω
I_{ON}	ON input leakage current	$V_{ON} = 0.9\text{ V to }3.6\text{ V or GND}$		Full			0.1	μA

(1) Typical values are at $V_{IN} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) See Output Pulldown in *Application Information*.

SWITCHING CHARACTERISTICS

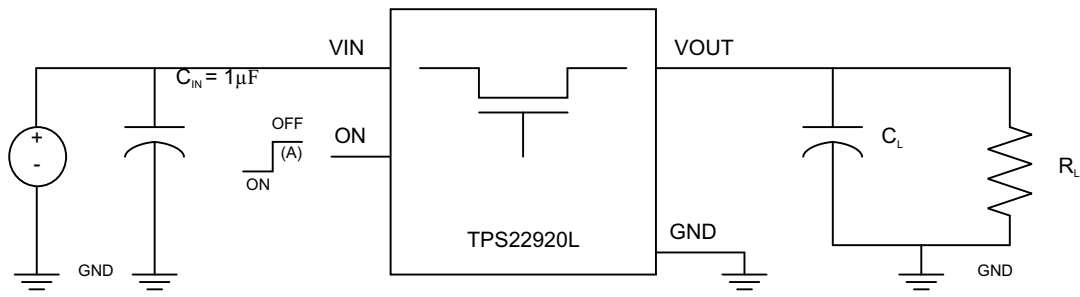
 $V_{IN} = 3.6\text{ V}, T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 3.6\text{ V}$		663		μs
t_{OFF}	Turn-OFF time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 3.6\text{ V}$		2		
t_R	VOUT Rise time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 3.6\text{ V}$		627		
t_F	VOUT Fall time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 3.6\text{ V}$		2		
t_D	ON delay time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 3.6\text{ V}$		380		

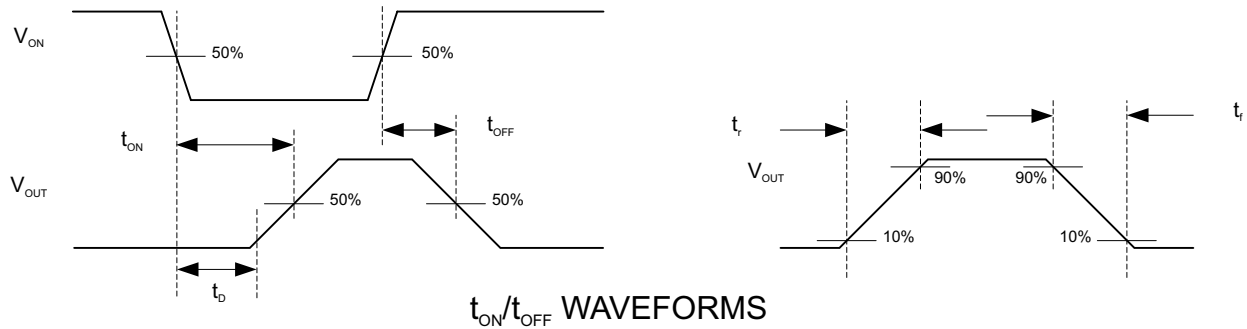
 $V_{IN} = 0.9\text{ V}, T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 0.9\text{ V}$		840		μs
t_{OFF}	Turn-OFF time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 0.9\text{ V}$		12		
t_R	VOUT Rise time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 0.9\text{ V}$		419		
t_F	VOUT Fall time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 0.9\text{ V}$		3		
t_D	ON delay time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 0.9\text{ V}$		611		

PARAMETRIC MEASUREMENT INFORMATION



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

A. Rise and fall times of the control signal is 100ns.

Figure 4. Test Circuit and t_{ON}/t_{OFF} Waveforms

TYPICAL CHARACTERISTICS

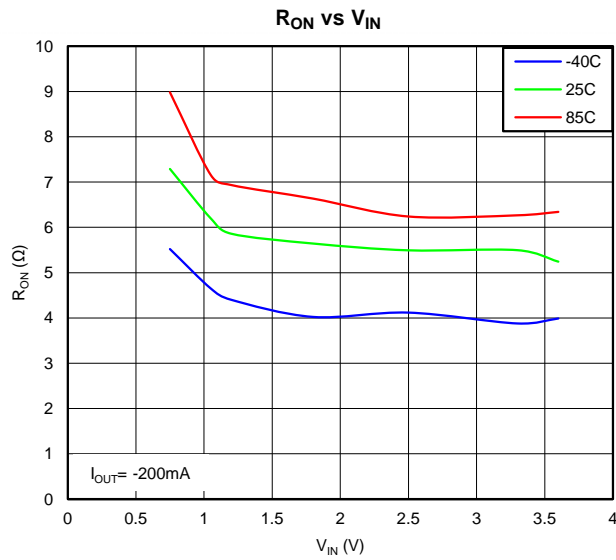


Figure 5.

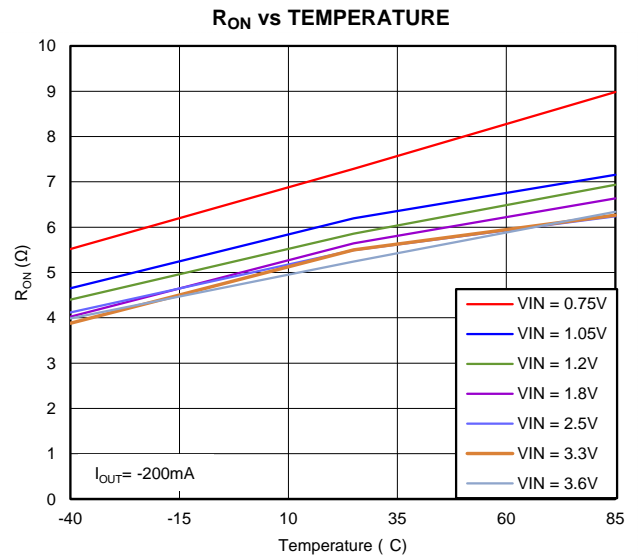


Figure 6.

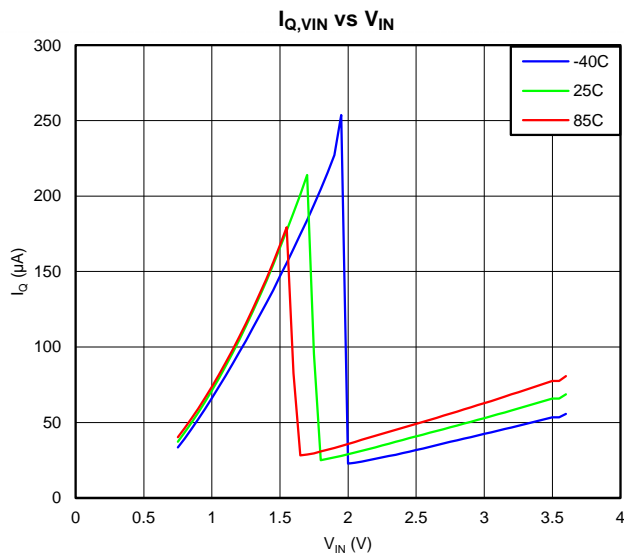


Figure 7.

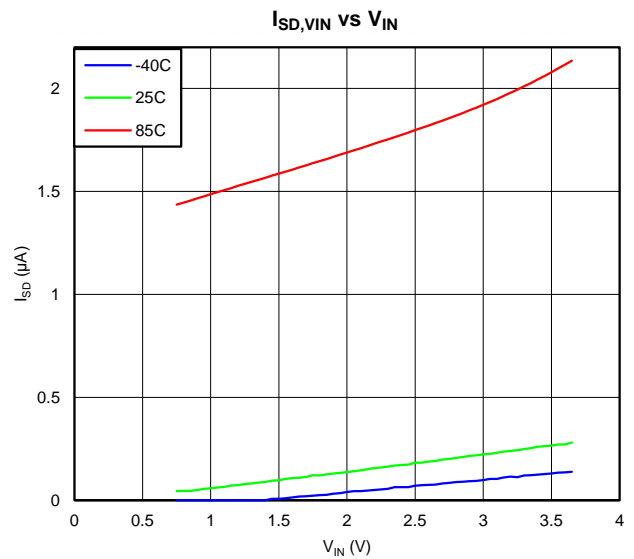


Figure 8.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE vs V_{ON} FALLING

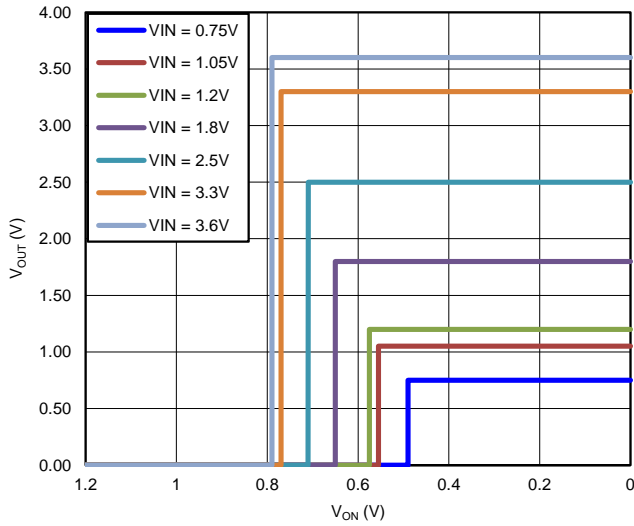


Figure 9.

OUTPUT VOLTAGE vs V_{ON} RISING

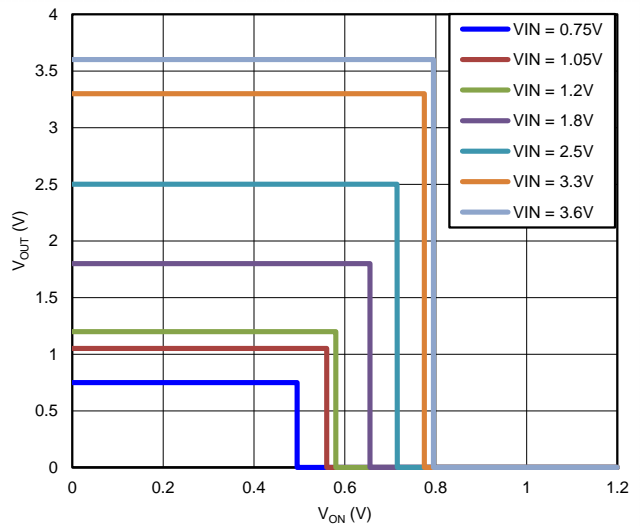


Figure 10.

t_{ON} vs TEMPERATURE

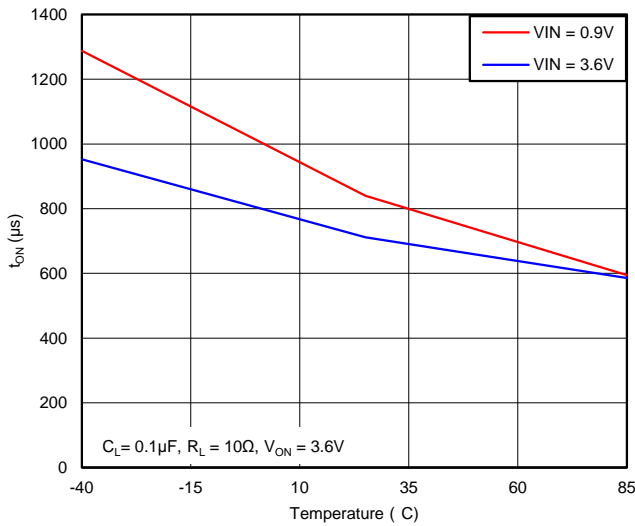


Figure 11.

t_{OFF} vs TEMPERATURE

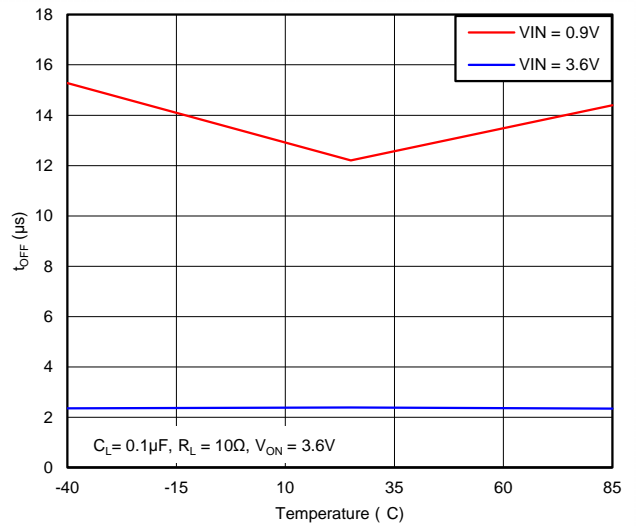


Figure 12.

TYPICAL CHARACTERISTICS (continued)

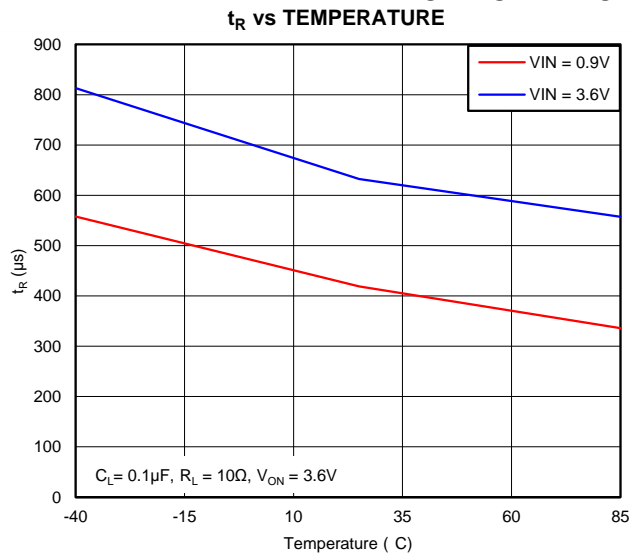


Figure 13.

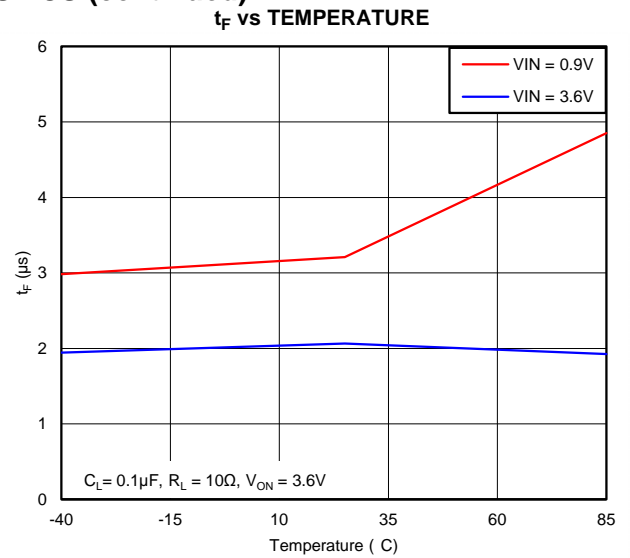


Figure 14.

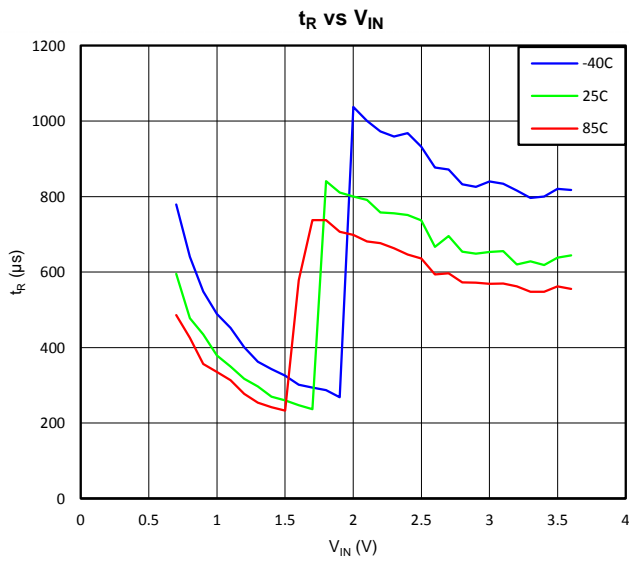


Figure 15.

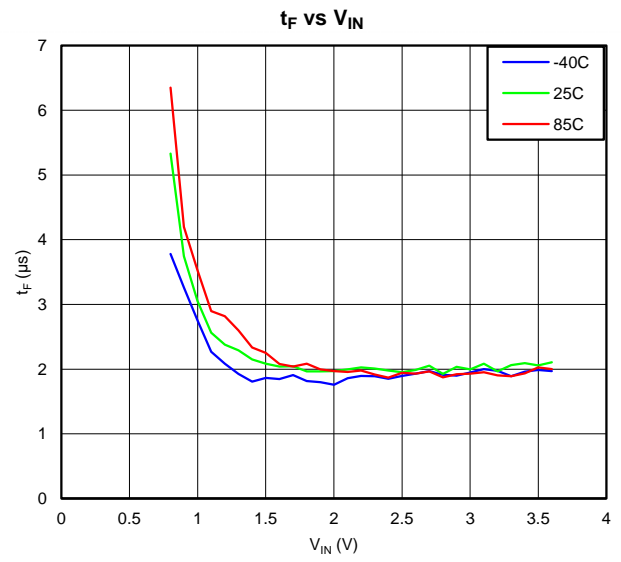


Figure 16.

TYPICAL CHARACTERISTICS (continued)

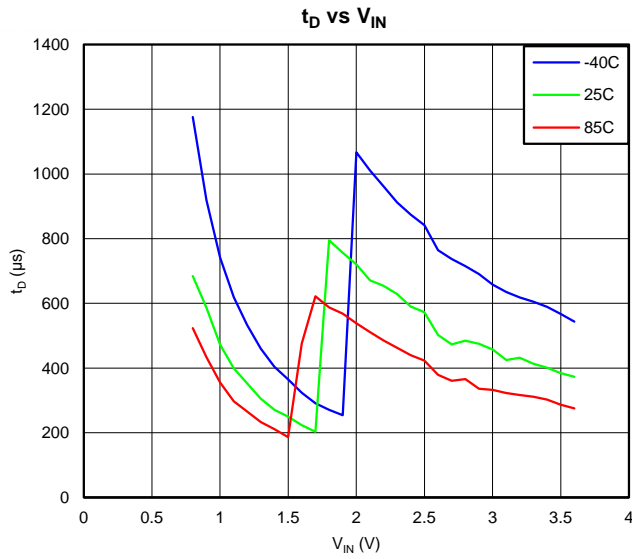


Figure 17.

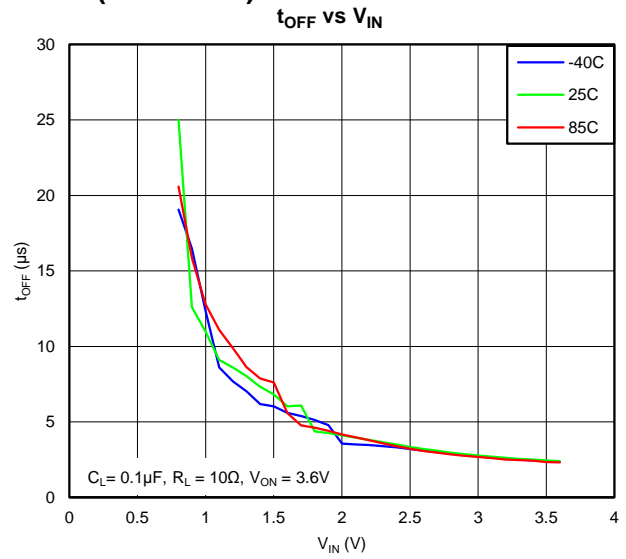


Figure 18.

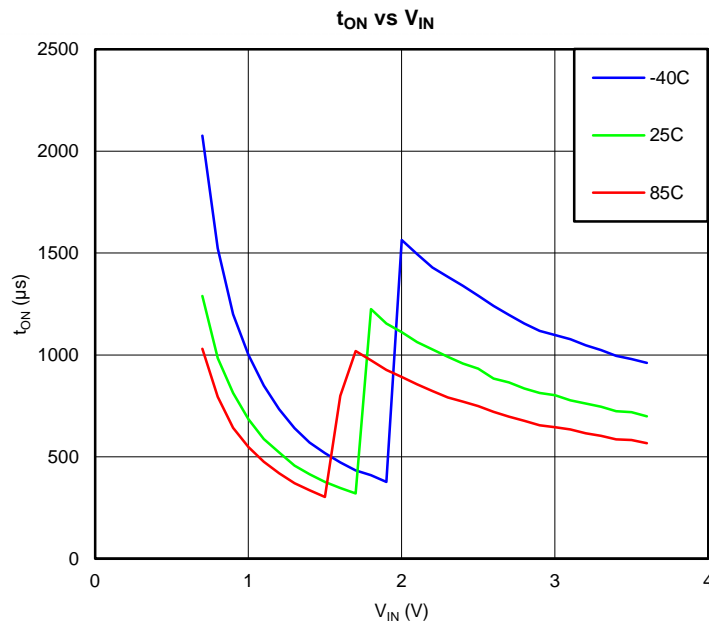


Figure 19.

TYPICAL CHARACTERISTICS (continued)

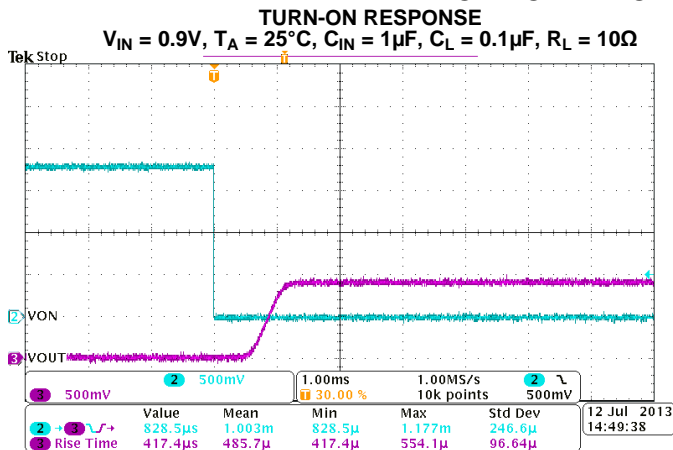


Figure 20.

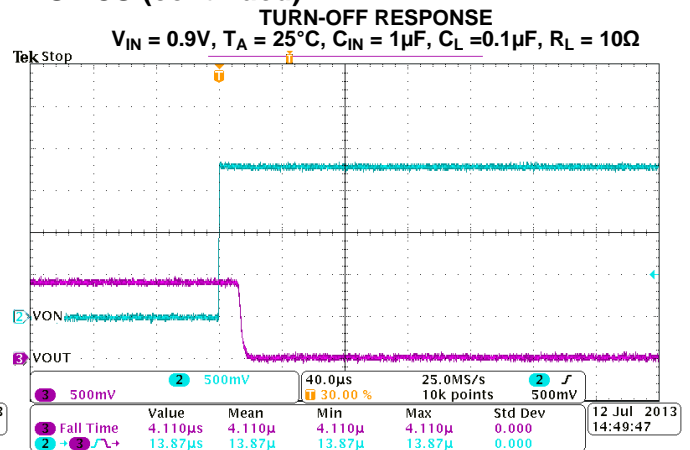


Figure 21.

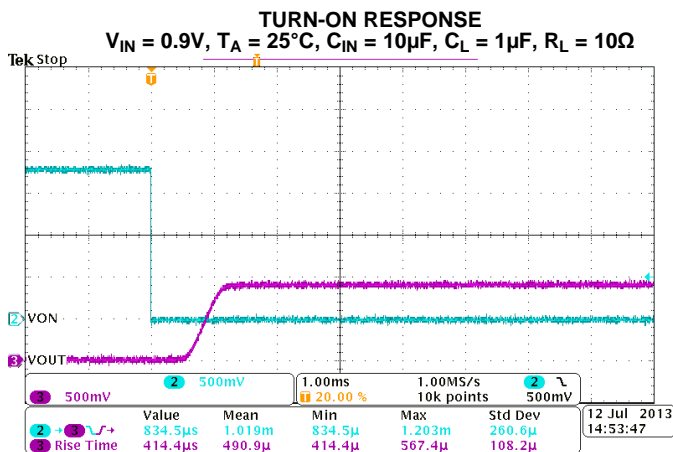


Figure 22.

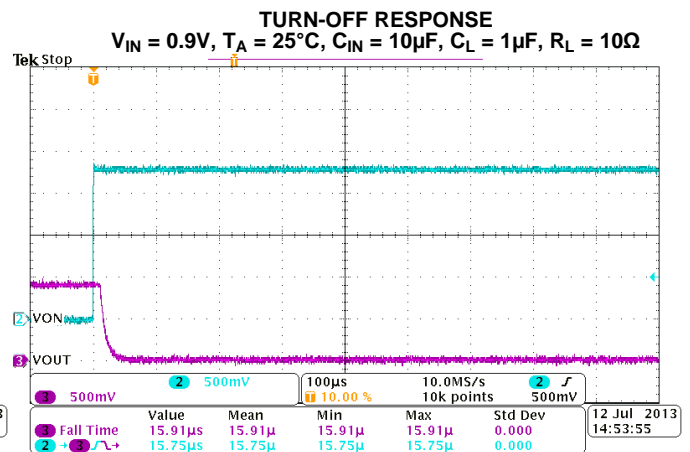


Figure 23.

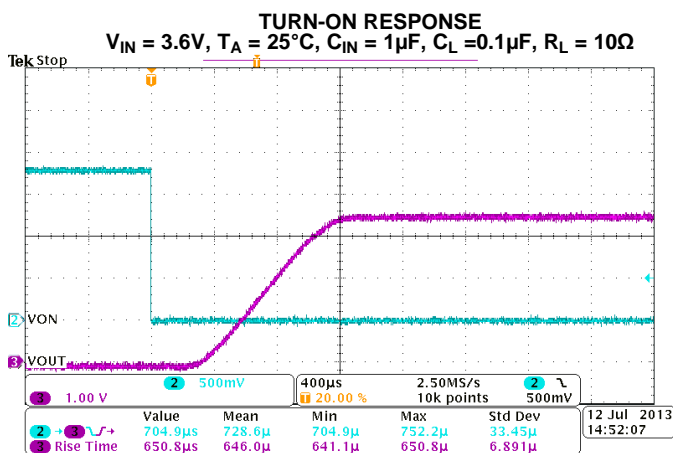


Figure 24.

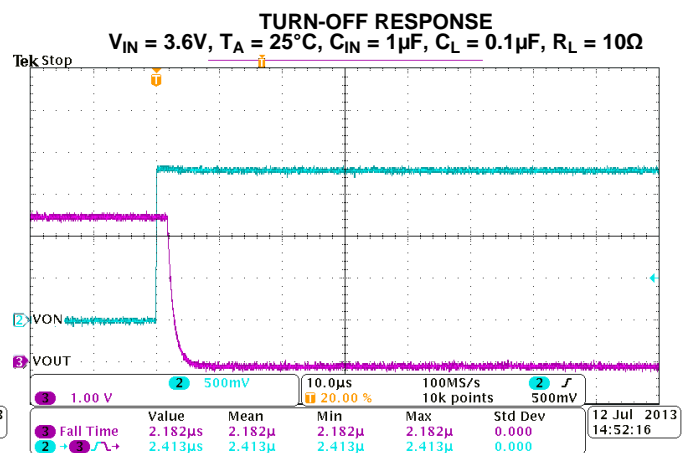


Figure 25.

TYPICAL CHARACTERISTICS (continued)

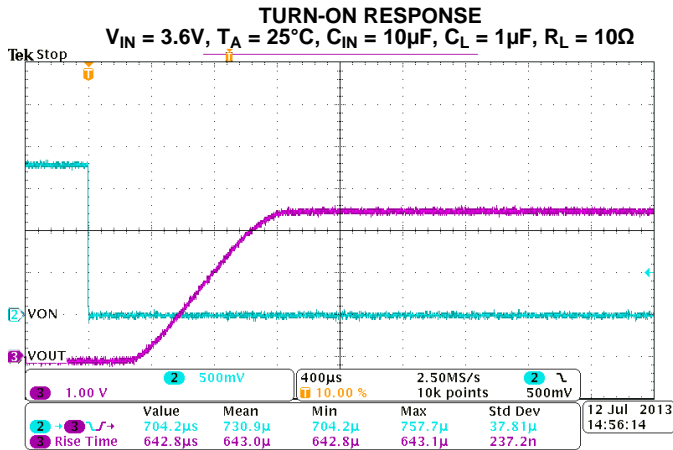


Figure 26.

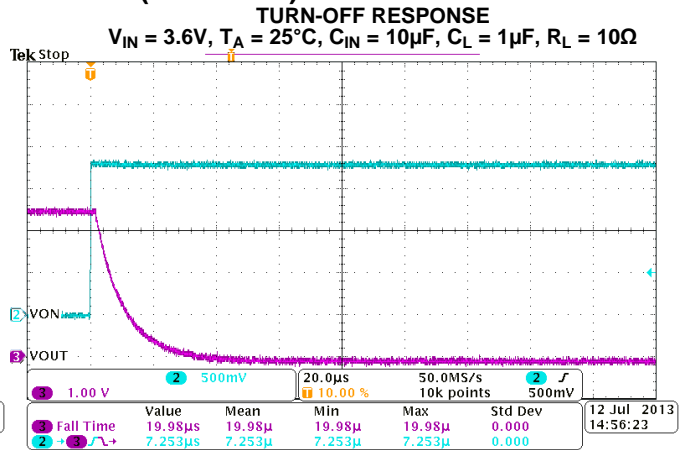


Figure 27.

APPLICATION INFORMATION

ON/OFF CONTROL

The ON pin controls the state of the switch. Asserting ON low enables the switch. ON is active low and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V, 1.8 V, 2.5 V or 3.3 V GPIOs.

INPUT CAPACITOR (OPTIONAL)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1 μ F ceramic capacitor, C_{IN} , placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

OUTPUT CAPACITOR (OPTIONAL)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

OUTPUT PULL-DOWN

The output pulldown is active when the user is turning off the main pass FET. The pulldown discharges the output rail to approximately 10% of the rail, and then the output pulldown is automatically disconnected to optimize the shutdown current.

BOARD LAYOUT

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN} , V_{OUT} , and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

REVISION HISTORY

Changes from Original (August 2013) to Revision A	Page
• 将预览文档更新为完全版本。	1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22920LYZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DV
TPS22920LYZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DV
TPS22920LYZPT	Active	Production	DSBGA (YZP) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DV
TPS22920LYZPT.B	Active	Production	DSBGA (YZP) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DV
TPS22920YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z
TPS22920YZPR.A	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z
TPS22920YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z
TPS22920YZPRB	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z
TPS22920YZPRB.A	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z
TPS22920YZPRB.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z
TPS22920YZPT	Active	Production	DSBGA (YZP) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z
TPS22920YZPT.A	Active	Production	DSBGA (YZP) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z
TPS22920YZPT.B	Active	Production	DSBGA (YZP) 8	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

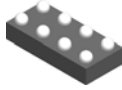
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22920LYZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920LYZPT	DSBGA	YZP	8	250	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPRB	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPRB	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPT	DSBGA	YZP	8	250	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPT	DSBGA	YZP	8	250	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22920LYZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22920LYZPT	DSBGA	YZP	8	250	182.0	182.0	20.0
TPS22920YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22920YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22920YZPRB	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22920YZPRB	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22920YZPT	DSBGA	YZP	8	250	182.0	182.0	20.0
TPS22920YZPT	DSBGA	YZP	8	250	182.0	182.0	20.0

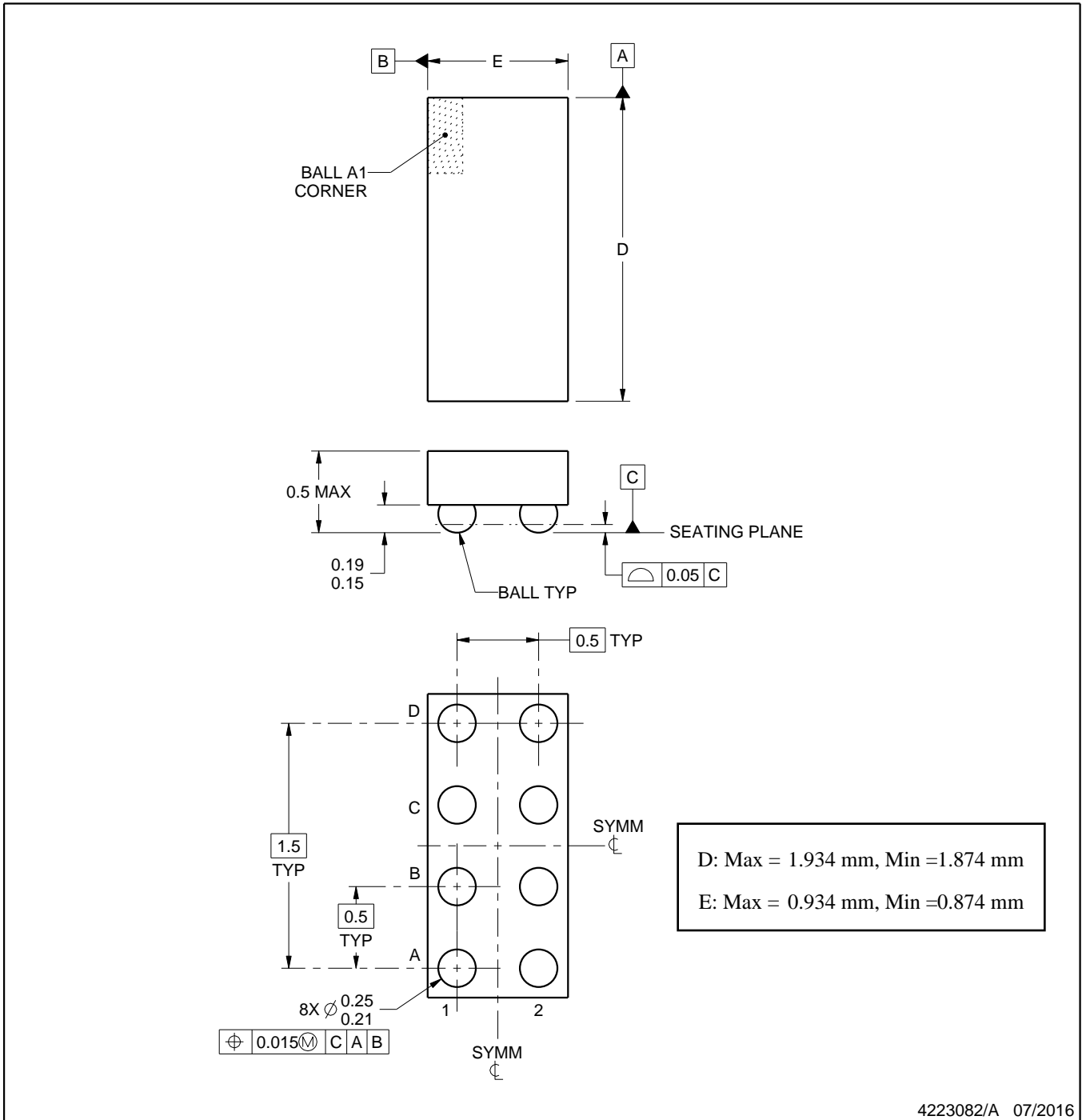
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

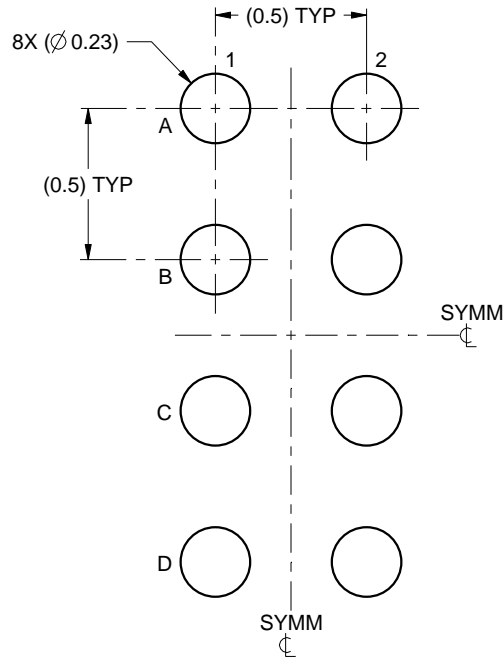
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

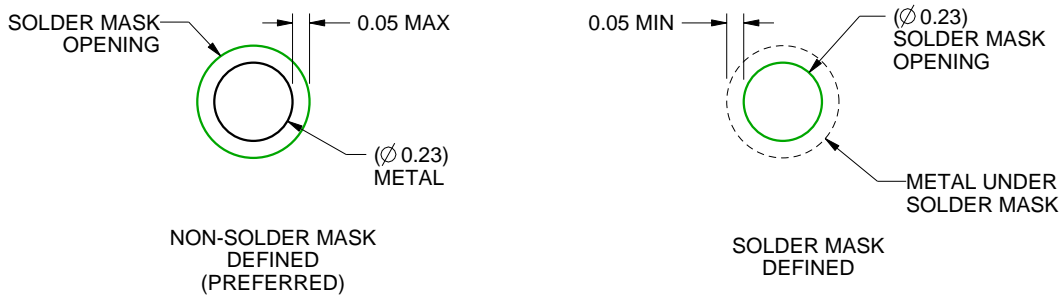
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

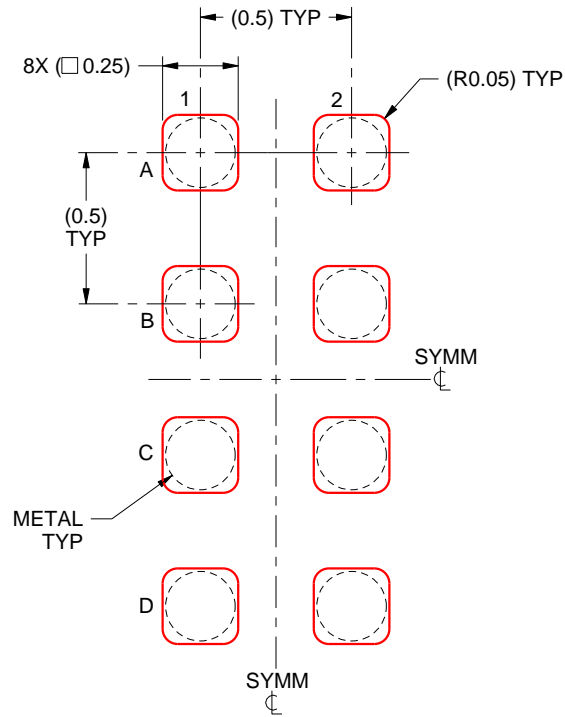
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月