具有可控接通功能的超小型、低导通电阻负载开关

查询样品: **TPS22912**

特性

- 集成单负载开关
- **0.9mm x 0.9mm**，锡球**/**焊盘间距 **0.5mm**，超小型晶片比例 **(CSP)-4** 封装
- 输入电压范围：**1.4V** 至 **5.5V**
- 低导通电阻
  - 在输入电压**(VIN) = 5V**时，r_{ON} **= 60mΩ**
  - 在输入电压**(VIN) = 3.3V**时，r_{ON} **= 61mΩ**
  - 在输入电压**(VIN) = 1.8V**时，r_{ON} **= 74mΩ**
  - 在输入电压**(VIN) = 1.5V**时，r_{ON} **= 84mΩ**
- **2A** 最大持续开关电流
- 低阈值控制输入
- 可控转换率选项
- 欠压闭锁
- 反向电流保护

应用范围

- 便携式工业**/**医疗设备
- 便携式媒体播放器
- **POS** 机终端
- 全球卫星定位系统 **(GPS)** 导航器件
- 数码摄像机
- 便携式仪表
- 智能电话 **/** 无线手持终端

说明

TPS22912 是一款具有可控接通功能的小型、低 r_{ON}负载开关，此开关包含一个可在 1.4V 至 5.5V 的输入电压范围内运行的 P 通道金属氧化物半导体场效应晶体管 (MOSFET)。此开关由一个高电平输入 (ON) 控制，此输入能够与低压控制信号直接接口相连。

为了避免涌入电流，此器件的转换率由内部控制。TPS22912 系列产品有多重上升时间选项并且工作态高电平启用。（参见表 1）

TPS22912 通过在反向电压情况期间锁存电源开关来提供电路断路器功能。 一个内部反向电压比较器在输出电压 (V_{OUT}) 高于输入电压 (V_{IN}) 时禁用此电源开关。 这一过程能够快速（典型值为 10µs）阻止流向开关输入端的电流。 反向电流保护一直有效，即便当器件被禁用时也是如此。 此外，如果此输入电压过低，欠压闭锁 (UVLO) 保护会将此开关关闭。

TPS22912 采用超小型、节省空间的 4 引脚 CSP 封装并可在 –40°C 至85°C 的大气环境温度范围内运行。

典型应用

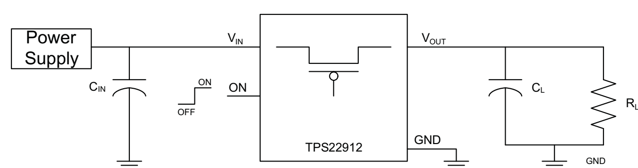


表 **1.** 特性列表

器件	**3.3V** 时的 r_{ON}（典型值）	**3.3V**（典型值）时的上升时间	快速输出放电 **(1)**	最大输出电压	使能
TPS22912A (2)	61mΩ	1µs	否	2A	高定平有效
TPS22912B (2)	61mΩ	100µs	否	2A	高定平有效
TPS22912C	61mΩ	1000µs	否	2A	高定平有效
TPS22912D (2)	61mΩ	4500µs	否	2A	高电平有效

(1) 此特性可通过一个 150Ω 电阻器将开关的输出放电至接地水平，从而防止此输出悬空。
(2) 请向当地销售商/分销商或者厂家查询产品供货信息。

English Data Sheet: SLVSB78

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

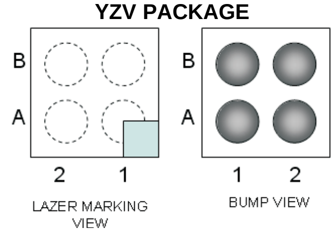
ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING/ STATUS[2]
–40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912AYZVR	Contact factory for availability
–40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912BYZVR	Contact factory for availability
–40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912CYZVR	_ _ _ _ 78
–40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912DYZVR	Contact factory for availability

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) Contact factory for details and availability for PREVIEW devices, minimum order quantities may apply.

DEVICE INFORMATION

YZV PACKAGE



TERMINAL ASSIGNMENTS

B	ON	GND
A	V_{IN}	V_{OUT}
	2	**1**

PIN FUNCTIONS

TPS22912 YZV	PIN NAME	DESCRIPTION
B1	GND	Ground
B2	ON	Switch control input, active high. Do not leave floating
A1	VOUT	Switch output
A2	VIN	Switch input. Use ceramic capacitor to GND for bypass.

BLOCK DIAGRAM

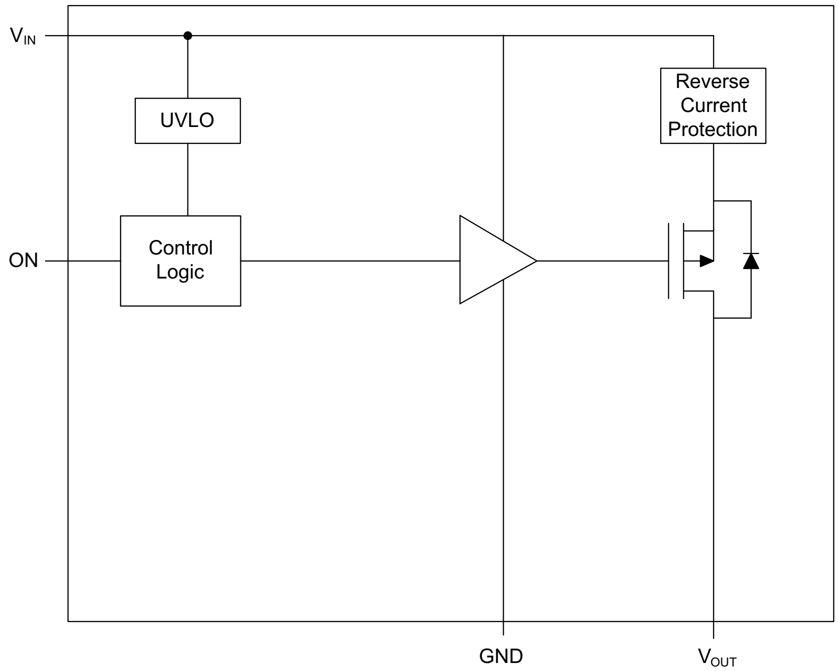


Table 2. FUNCTION TABLE

ON	VIN to VOUT
L	OFF
H	ON

ABSOLUTE MAXIMUM RATINGS

			VALUE	UNIT
V_{IN}	Input voltage range		–0.3 to 6	V
V_{OUT}	Output voltage range		–0.3 to 6	V
V_{ON}	Input voltage range		–0.3 to 6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse ≤500 ms, 50% duty cycle		3	A
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Maximum junction temperature		125	°C
T_{STG}	Storage temperature range		–65 to 150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM) (VIN, VOUT, GND pins)	2000	V
		Charged-Device Model (CDM) (VIN, VOUT, ON, GND pins)	1000	

THERMAL INFORMATION

THERMAL METRIC[1]		TPS22912 CSP 4 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	189.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	1.9	
θ_{JB}	Junction-to-board thermal resistance	36.8	
ψ_{JT}	Junction-to-top characterization parameter	11.3	
ψ_{JB}	Junction-to-board characterization parameter	36.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{IN}	Input voltage range		1.4	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range (Note: V_{OUT} greater than V_{IN} will cause the reverse current protection of this device to trigger. See application section.)			V_{IN} [1]	
V_{IH}	High-level input voltage, ON	VIN = 3.61 V to 5.5 V	1.1	5.5	V
		VIN = 1.4 V to 3.6 V	1.1	5.5	V
V_{IL}	Low-level input voltage, ON	VIN = 3.61 V to 5.5 V		0.6	V
		VIN = 1.4 V to 3. 6V		0.4	V
C_{IN}	Input Capacitor		1 [1]		µF

(1) Refer to the application section.

ELECTRICAL CHARACTERISTICS

VIN = 1.4 V to 5.5 V, T_A = –40ºC to 85ºC (unless otherwise noted)

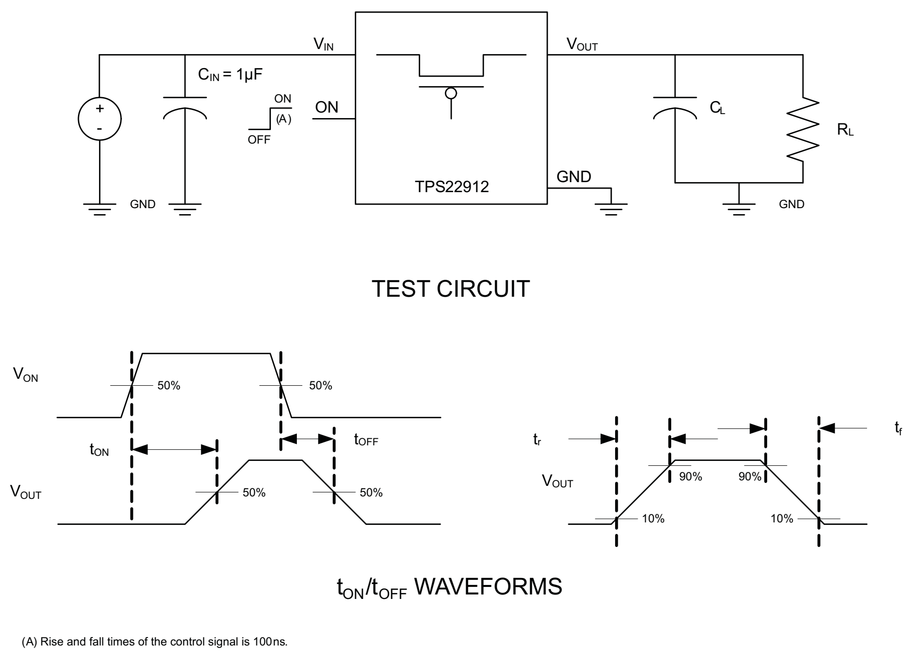
PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{IN}	Quiescent current	I_{OUT} = 0, V_{ON} = V_{IN} = 5.25 V	Full		2	10	µA
		I_{OUT} = 0, V_{ON} = V_{IN} = 4.2 V			2	7.0	
		I_{OUT} = 0, V_{ON} = V_{IN} = 3.6 V			2	7.0	
		I_{OUT} = 0, V_{ON} = V_{IN} = 2.5 V			0.9	5	
		I_{OUT} = 0, V_{ON} = V_{IN} = 1.5 V			0.7	5	
$I_{IN(off)}$ (1)	Off supply current	R_L = 1 MΩ, V_{IN} = 5.25 V, V_{ON} = GND	Full		1.2	10	µA
		R_L = 1 MΩ, V_{IN} = 4.2 V, V_{ON} = GND			0.2	7.0	
		R_L = 1 MΩ, V_{IN} = 3.6 V, V_{ON} = GND			0.1	7.0	
		R_L = 1 MΩ, V_{IN} = 2.5 V, V_{ON} = GND			0.1	5	
		R_L = 1 MΩ, V_{IN} = 1.5 V, V_{ON} = GND			0.1	5	
$I_{IN(Leakage)}$	Leakage current	V_{OUT} = 0, V_{IN} = 5.25 V, V_{ON} = GND	Full		1.2	10	µA
		V_{OUT} = 0, V_{IN} = 4.2 V, V_{ON} = GND			0.2	7.0	
		V_{OUT} = 0, V_{IN} = 3.6 V, V_{ON} = GND			0.1	7.0	
		V_{OUT} = 0, V_{IN} = 2.5 V, V_{ON} = GND			0.1	5	
		V_{OUT} = 0, V_{IN} = 1.5 V, V_{ON} = GND			0.1	5	
r_{ON}	On-resistance	V_{IN} = 5.25 V, I_{OUT} = –200 mA	25°C		60	80	mΩ
			Full			110	
		V_{IN} = 5.0 V, I_{OUT} = –200 mA	25°C		60	80	
			Full			110	
		V_{IN} = 4.2 V, I_{OUT} = –200 mA	25°C		60	80	
			Full			110	
		V_{IN} = 3.3 V, I_{OUT} = –200 mA	25°C		60.7	80	
			Full			110	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA	25°C		63.4	90	
			Full			120	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA	25°C		74.2	100	
			Full			130	
		V_{IN} = 1.5 V, I_{OUT} = –200 mA	25°C		83.9	120	
			Full			150	
UVLO	Under voltage lockout	V_{IN} increasing, V_{ON} = 3.6 V, I_{OUT} = –100 mA	Full			1.2	V
		V_{IN} decreasing, V_{ON} = 3.6 V, I_{OUT} = –100 mA		0.50			
I_{ON}	ON input leakage current	V_{ON} = 1.4 V to 5.25 V or GND	Full			1	µA
V_{RCP}	Reverse Current Voltage Threshold	V_{OUT} > V_{IN}	25°C		54		mV
I_{RCP}(leak)	Reverse Current Protection Leakage after Reverse Current event	V_{OUT} – V_{IN} > V_{RCP}	25°C		0.3		µA
t_{DELAY}	Reverse Current Response Delay	V_{IN} = 5V			10		µs

(1) Verified by characterization, not production tested.

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITION	TPS22912 TYP	UNIT
VIN = 5 V, T_A = 25ºC (unless otherwise noted)				
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF	840	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF	6.6	
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF	912	
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF	3	
VIN = 3.3 V, T_A = 25ºC (unless otherwise noted)				
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF	1147	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF	8.6	
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF	1030	
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF	3	
VIN = 1.5 V, T_A = 25ºC (unless otherwise noted)				
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF	2513	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF	17.4	
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF	1970	
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF	6.5	

PARAMETRIC MEASUREMENT INFORMATION



A. Rise and fall times of the control signal are 100 ns.

Figure 1. Test Circuit and t_{ON}/t_{OFF} Waveforms

TYPICAL CHARACTERISTICS

ON-STATE RESISTANCE vs INPUT VOLTAGE

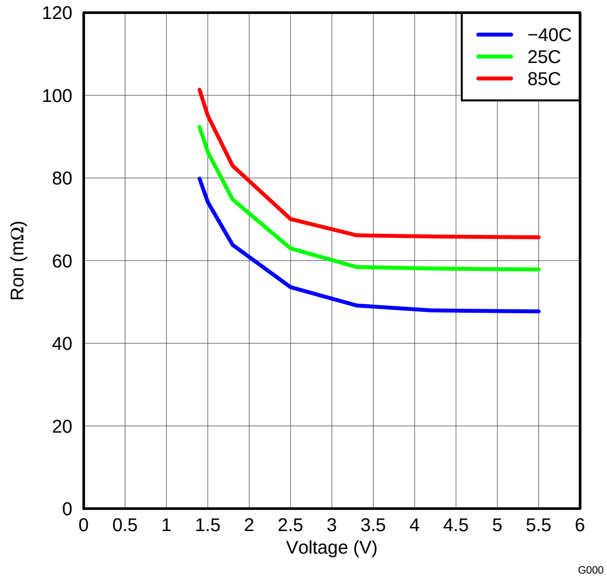


Figure 2.

ON INPUT THRESHOLD

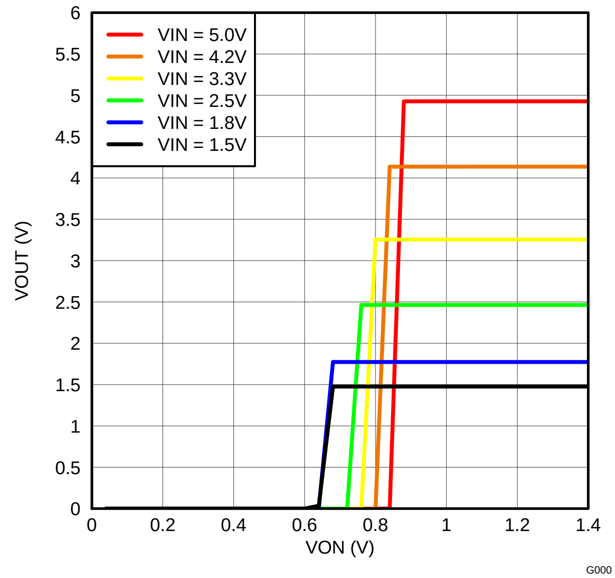


Figure 3.

INPUT CURRENT, QUIESCENT vs INPUT VOLTAGE

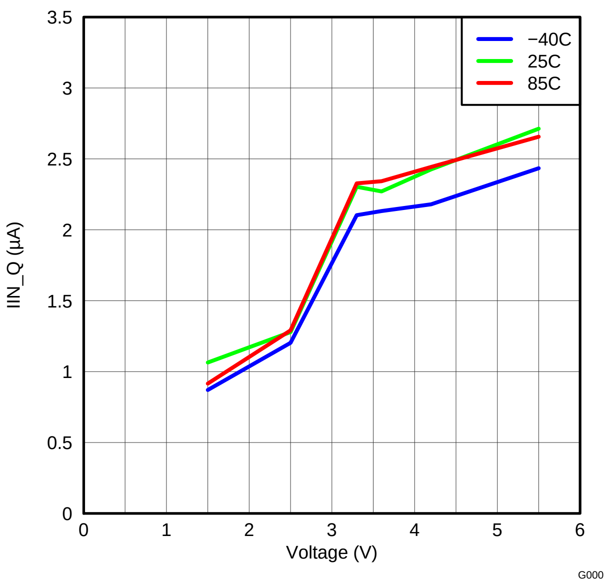


Figure 4.

INPUT CURRENT, LEAK vs INPUT VOLTAGE

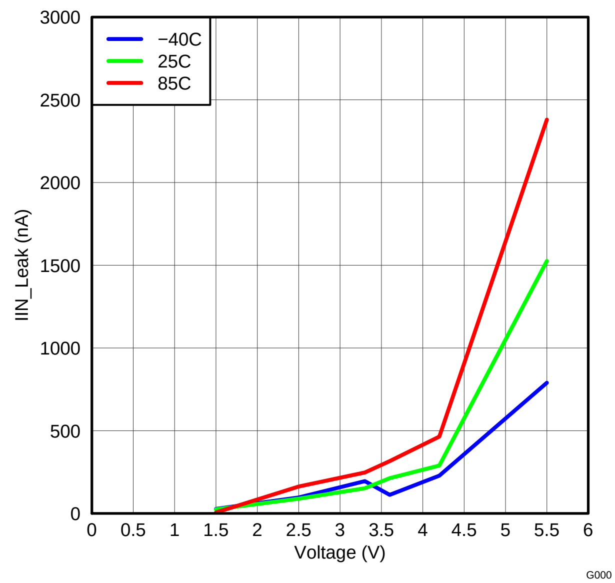


Figure 5.

TYPICAL CHARACTERISTICS (continued)

ON-STATE RESISTANCE vs TEMPERATURE

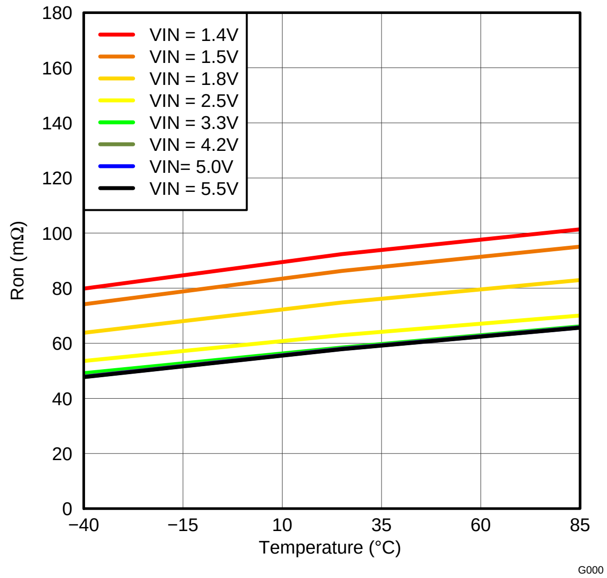


Figure 6.

INPUT CURRENT, OFF vs INPUT VOLTAGE

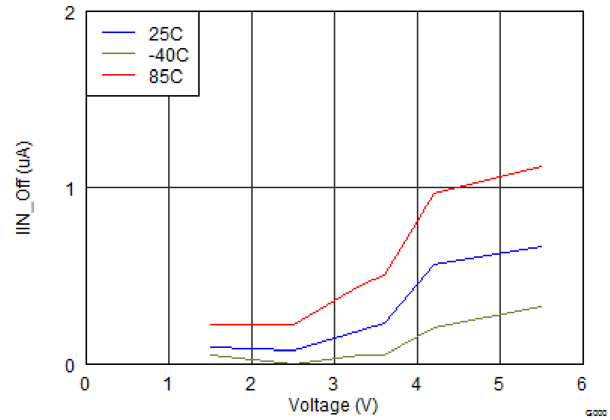


Figure 7.

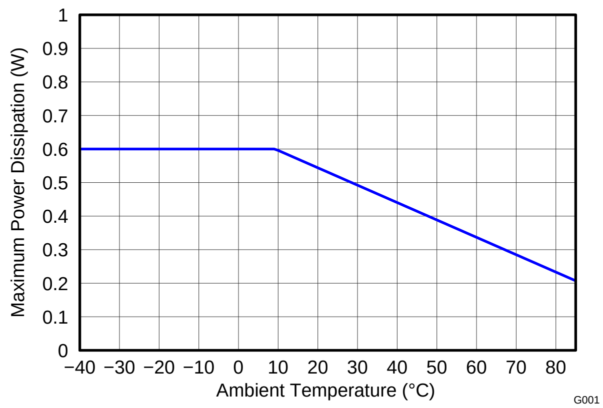


Figure 8. Allowable Power Dissipation

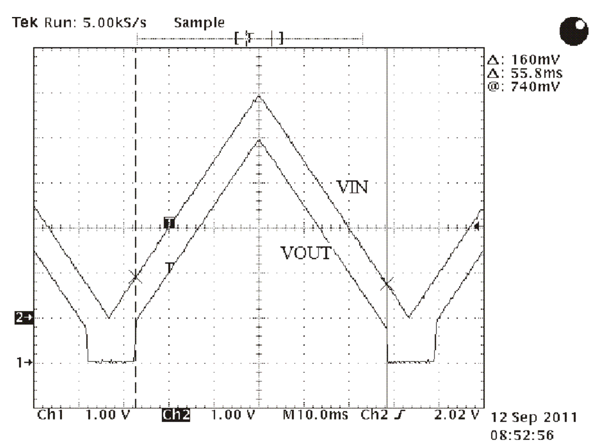


Figure 9. ULVO Response I_{OUT} = -100mA

TYPICAL CHARACTERISTICS (continued)

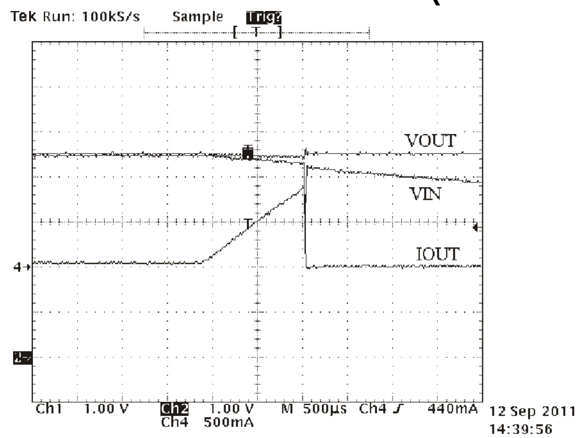


Figure 10. Reverse Current Protection V_{OUT} = 3.3V, V_{IN} = 3.3V Decreasing to 0V

TYPICAL AC CHARACTERISTICS FOR TPS22912C

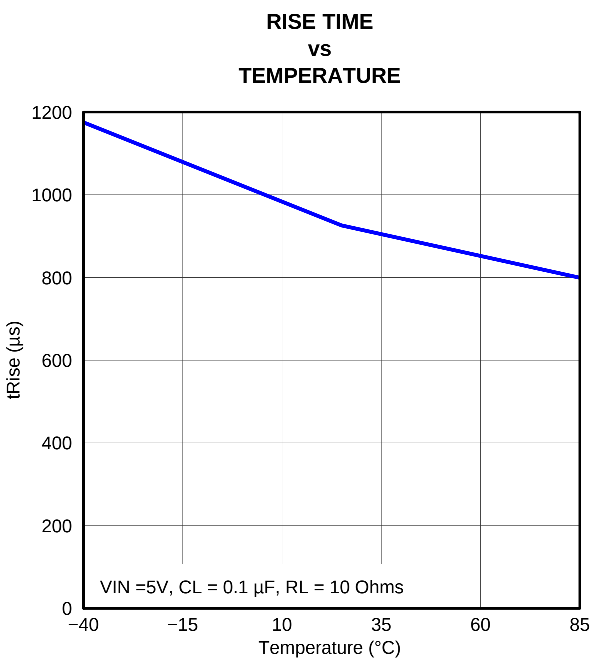


Figure 11.

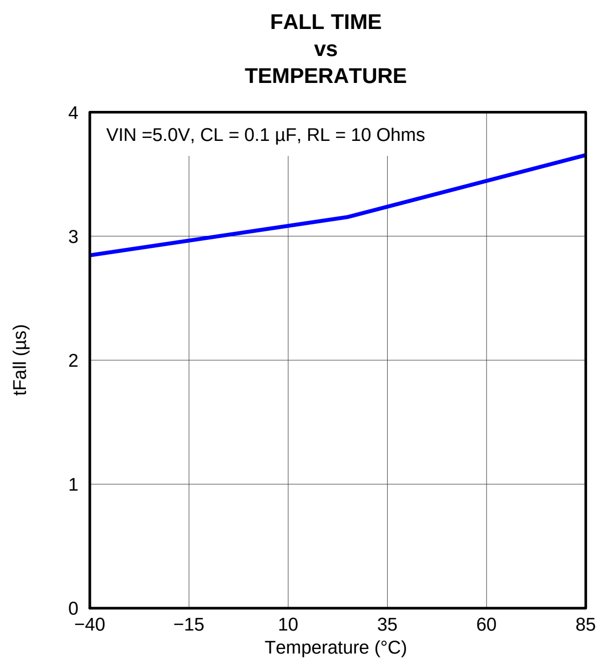


Figure 12.

TYPICAL CHARACTERISTICS (continued)

RISE TIME vs TEMPERATURE

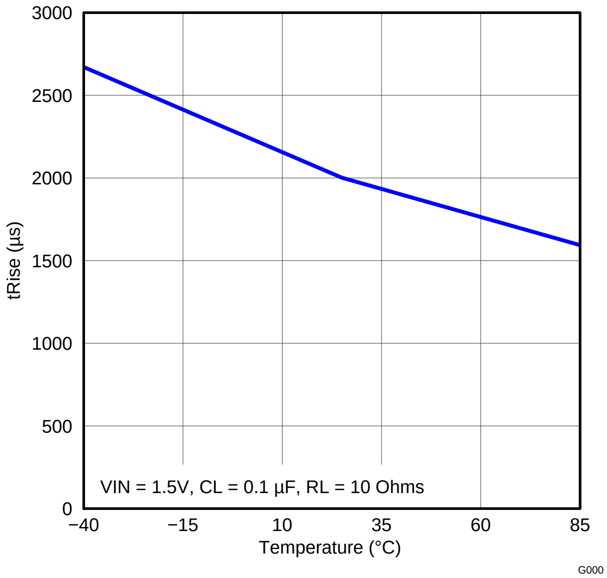


Figure 13.

FALL TIME vs TEMPERATURE

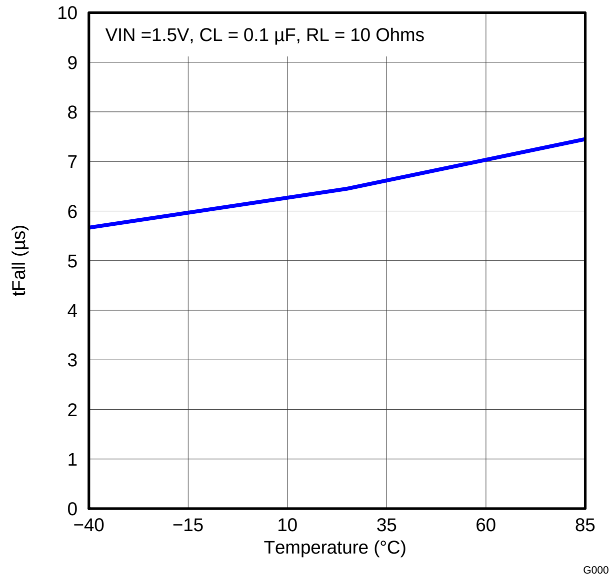


Figure 14.

TURN-ON TIME vs TEMPERATURE

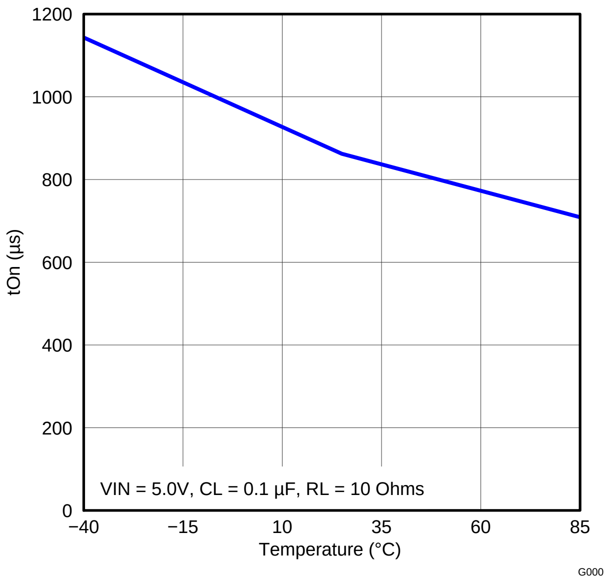


Figure 15.

TURN-OFF TIME vs TEMPERATURE

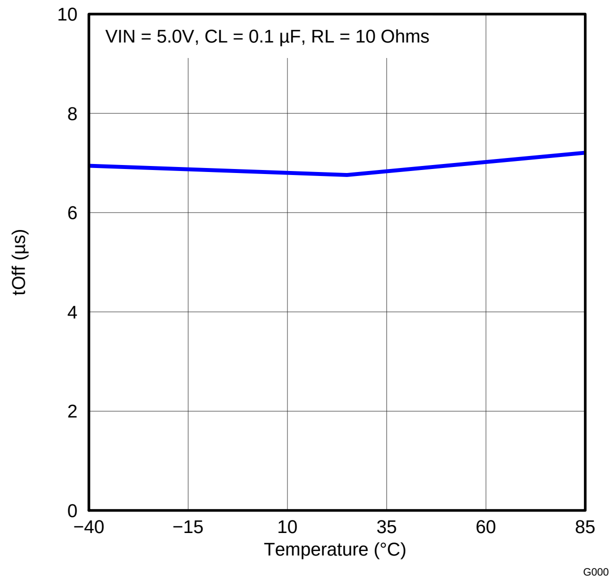


Figure 16.

TYPICAL CHARACTERISTICS (continued)

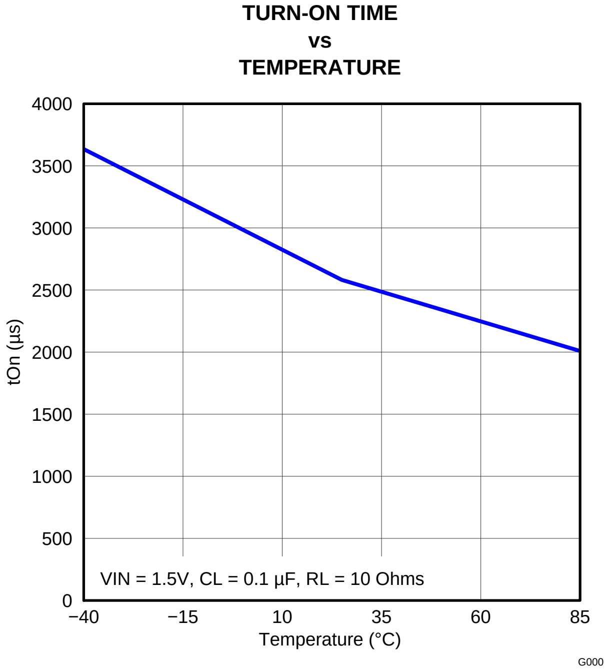


Figure 17.

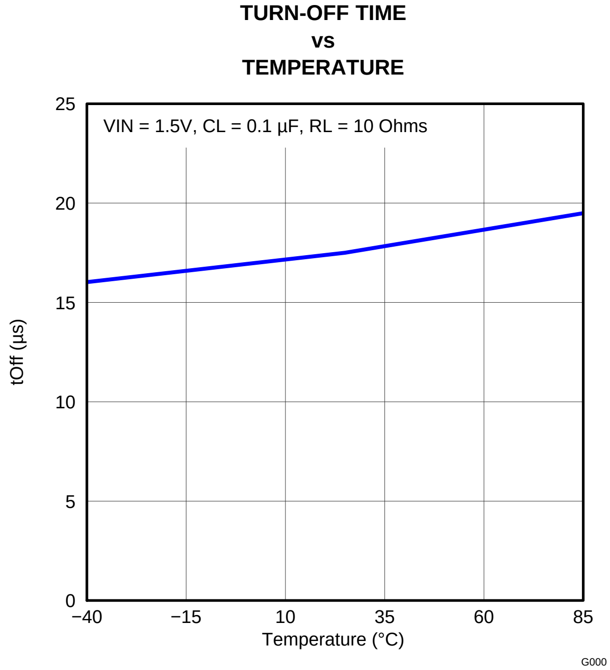


Figure 18.

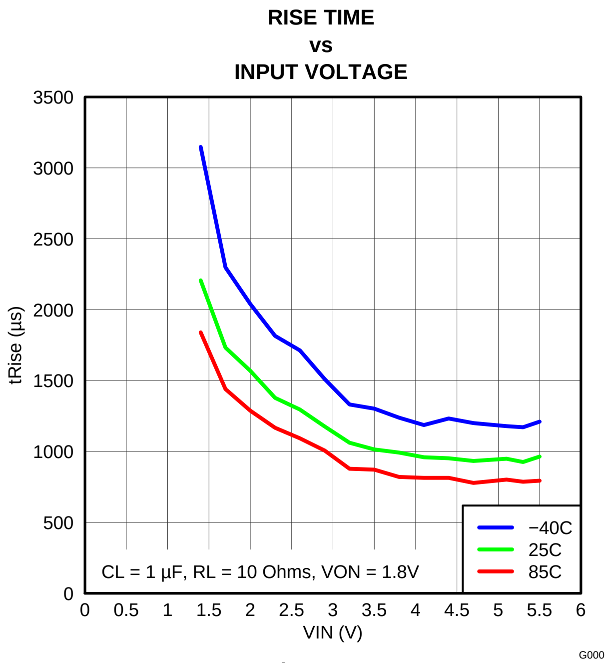


Figure 19.

TYPICAL CHARACTERISTICS (continued)

TURN-ON RESPONSE
V_{IN} = 5V, T_A = 25°C, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω

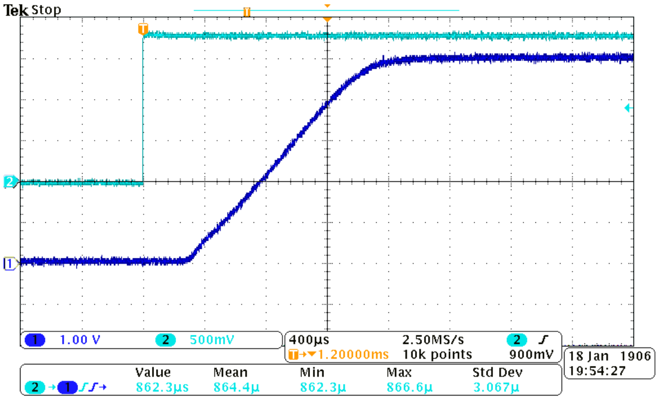


Figure 20.

TURN-OFF RESPONSE
V_{IN} = 5V, T_A = 25°C, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω

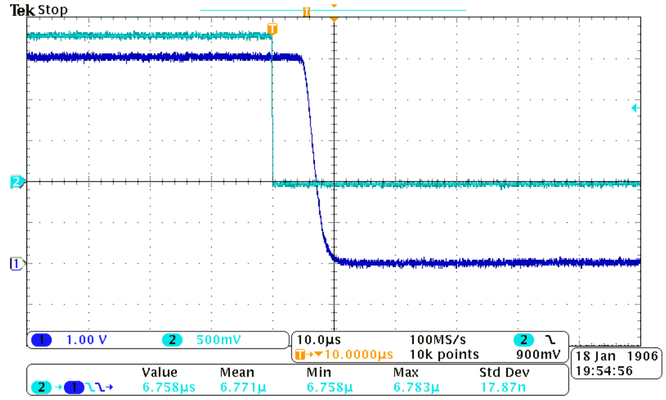


Figure 21.

TURN-ON RESPONSE TIME
V_{IN} = 5V, T_A = 25°C, C_{IN} =10µF, C_L = 1µF, R_L = 10Ω

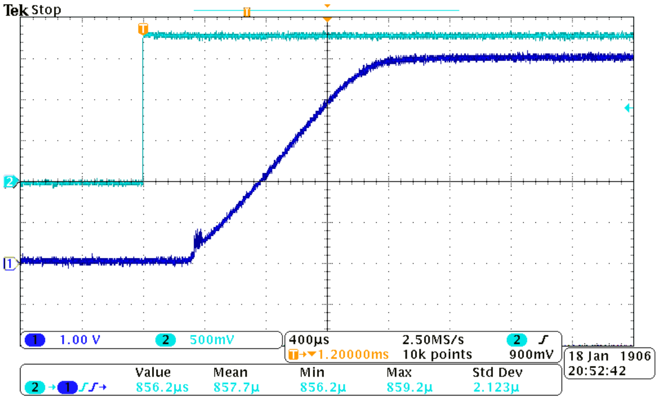


Figure 22.

TURN-OFF RESPONSE TIME
V_{IN} = 5V, T_A = 25°C, C_{IN} = 10µF, C_L = 1µF, R_L = 10Ω

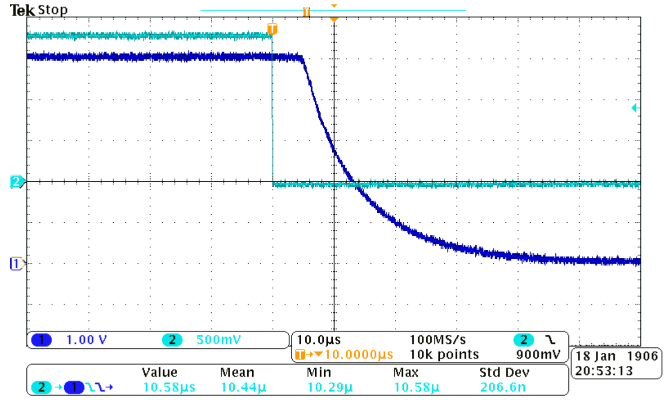


Figure 23.

TURN-ON RESPONSE TIME
V_{IN} = 1.5V, T_A = 25°C, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω

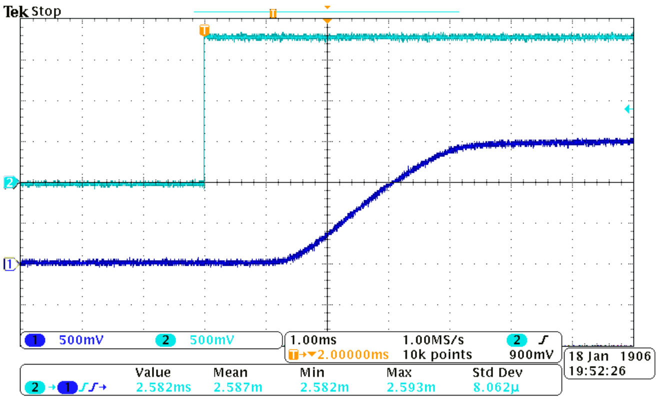


Figure 24.

TURN-OFF RESPONSE TIME
V_{IN} = 1.5V, T_A = 25°C, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω

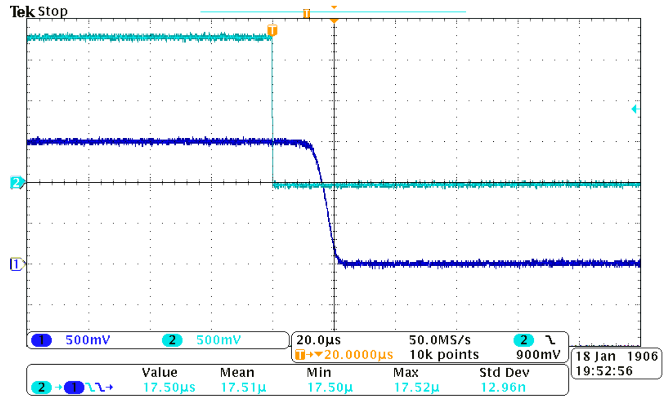


Figure 25.

TYPICAL CHARACTERISTICS (continued)

TURN-ON RESPONSE TIME
V_{IN} = 1.5V, T_A = 25°C, C_{IN} = 10µF, C_L = 1µF, R_L = 10Ω

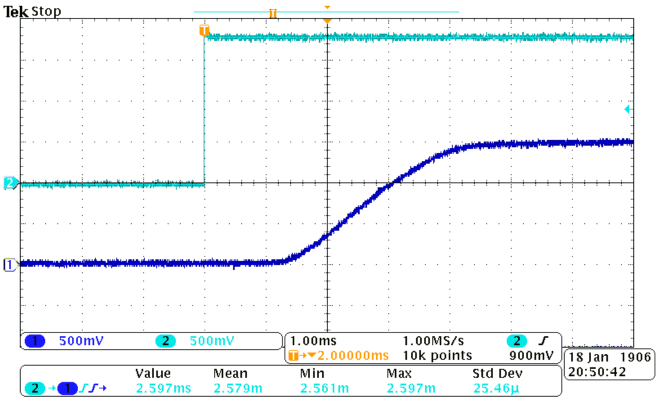


Figure 26.

TURN-OFF RESPONSE TIME
V_{IN} = 1.5V, T_A = 25°C, C_{IN} = 10µF, C_L = 1µF, R_L = 10Ω

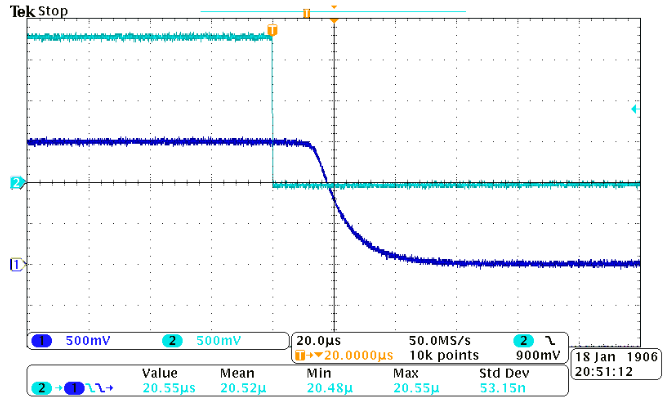


Figure 27.

APPLICATION INFORMATION

On/Off Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making the pin capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIO.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents, a capacitor needs to be placed between VIN and GND. A 1-μF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

Output Capacitor

A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup. Devices with faster rise times may require a larger ratio to minimize V_{IN} dip.

Under-Voltage Lockout

Under-voltage lockout protection turns off the switch if the input voltage is below the under-voltage lockout threshold. During under-voltage lockout (UVLO), if the voltage level at V_{OUT} exceeds the voltage level at V_{IN} by the Reverse Current Voltage Threshold (V_{RVP}), the body diode will be disengaged to prevent any current flow to V_{IN}. With the ON pin active, the input voltage rising above the under-voltage lockout threshold will cause a controlled turn-on of the switch to limit current over-shoot.

Reverse Current Protection

In a scenario where V_{OUT} is greater than V_{IN}, there is potential for reverse current to flow through the pass FET or the body diode. The TPS22912 monitors V_{IN} and V_{OUT} voltage levels. When the reverse current voltage threshold (V_{RCP}) is exceeded, the switch is disabled (within 10μs typ). Additionally, the body diode is disengaged so as to prevent any reverse current flow to V_{IN}. The FET, and the output (V_{OUT}), will resume normal operation when the reverse current scenario is no longer present. The peak instantaneous reverse current is the current it takes to trip the reverse current protection. After the reverse current protection has tripped due to the peak instantaneous reverse current, the DC (off-state) leakage current from V_{OUT} and V_{IN} is referred to as I_{RCP}(leak) (see figure below).

Use the following formula to calculate the amount of peak instantaneous reverse current for a particular application:

$$I_{RC} = \frac{V_{RCP}}{R_{ON(VIN)}}$$

Where,

I_{RC} is the amount of reverse current,

$R_{ON(VIN)}$ is the on-resistance at the VIN of the reverse current condition.

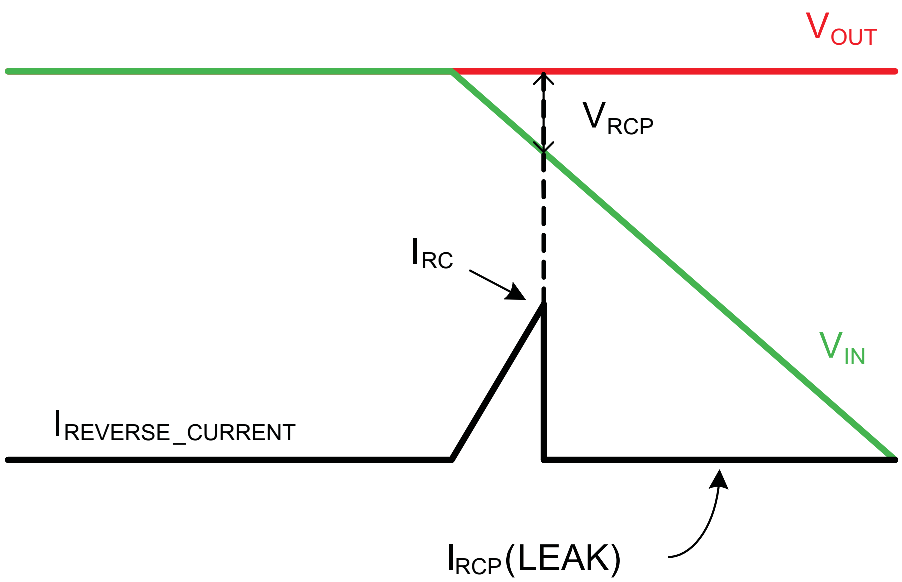


Figure 28. Reverse Current

Board Layout

For best performance, all traces should be as short as possible. The input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22912CYZVR	ACTIVE	DSBGA	YZV	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	78	Samples
TPS22912CYZVT	ACTIVE	DSBGA	YZV	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	78	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

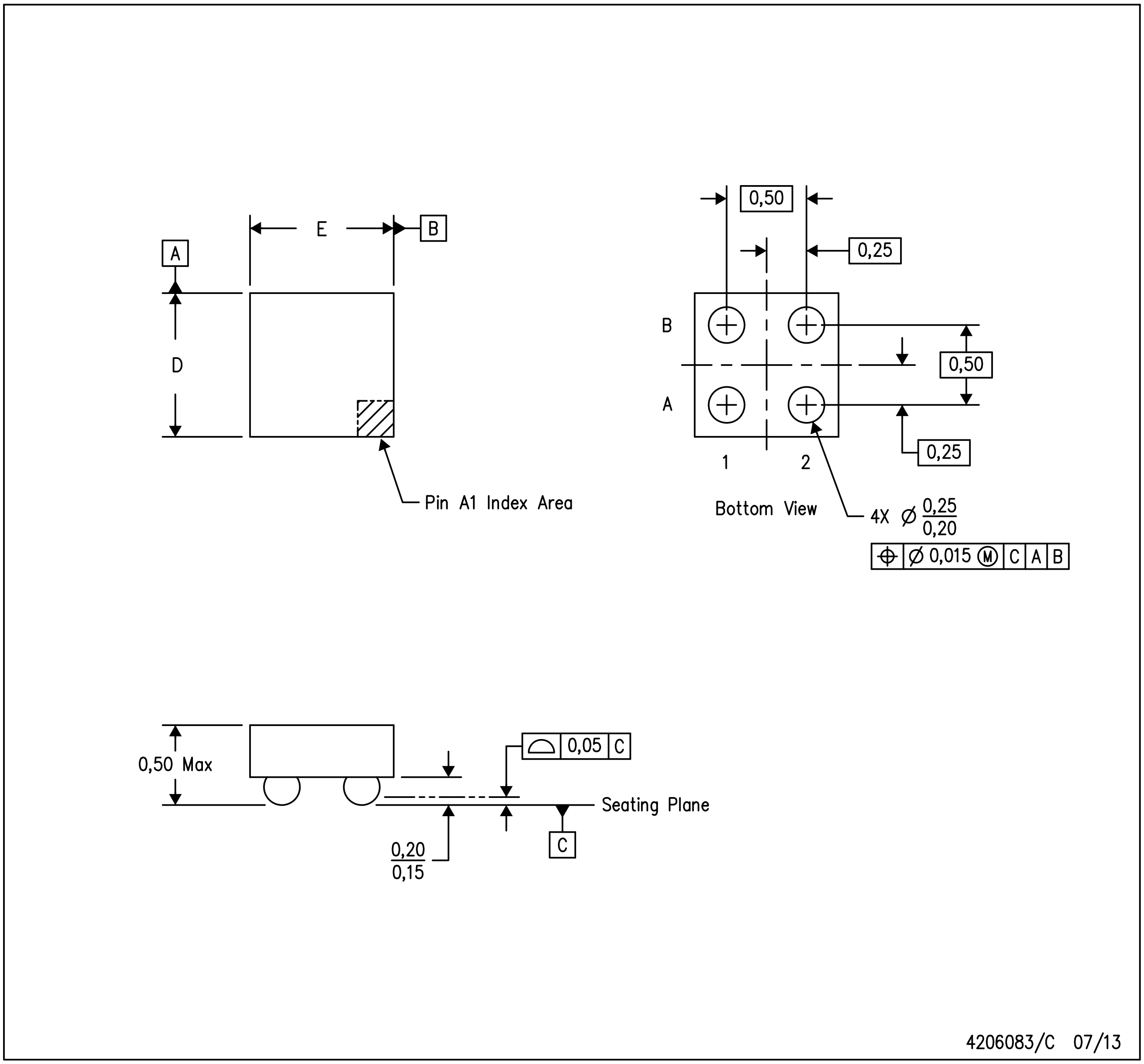
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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