TPD4E110 4 通道保护解决方案，用于超高速（高达 6GBPS）接口

1 特性

- 为低压输入输出 (IO) 接口提供系统级静电放电 (ESD) 保护
- IO 电容值 0.45pF（典型值）
- IEC 61000-4-2 4 级
  - ±12kV（接触放电）
  - ±15kV（空气间隙放电)
- IEC 61000-4-5（浪涌）：2.5A (8/20μs)
- 直流击穿电压 6.5V（最小值）
- 超低泄露电流 1nA（最大值）
- 低 ESD 钳位电压
- 工业温度范围：-40°C 至 125°C
- 最大限度减少空间的 0.8mm x 0.8mm DPW 封装

2 应用范围

- USB 3.0
- HDMI 2.0
- 低压差分信令 (LVDS)
- DisplayPort
- PCI Express 接口
- eSata 接口

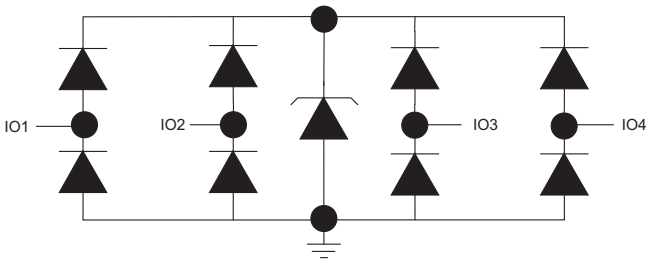
3 说明

TPD4E110 是一款具有超低电容值的单向静电放电 (ESD) 保护器件。 此器件由一个中央 ESD 钳位组成，并且在每个通道中特有两个隐藏的二极管，以减少电容负载。 每条通道额定 ESD 冲击消散值高于 IEC61000-4-2 4 级国际标准中规定的最高水平。 TPD4E110 的超低负载电容值使得此器件非常适合于保护高速信号引脚。

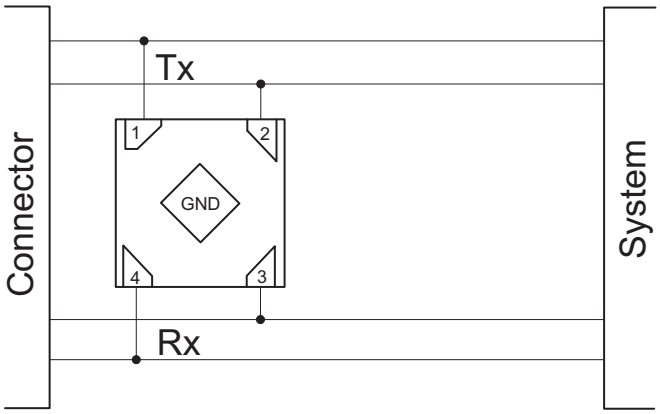
器件信息

订货编号	封装	封装尺寸
TPD4E110DPW	X2SON (4)	0.8mm x 0.8mm

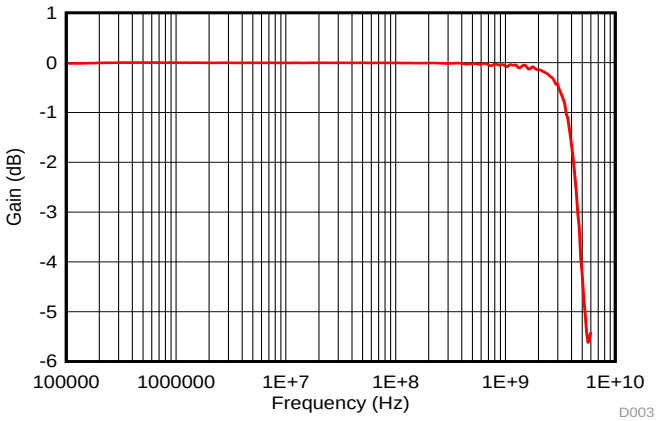
电路保护系统



4 简化电路原理图



插入损耗



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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5 修订历史记录

Changes from Revision A (March 2014) to Revision B **Page**

- 已修改超低泄露电流排印错误。 ... 1
- Updated I_{LEAK} max value. ... 4

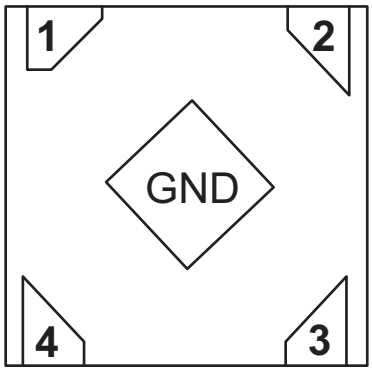
Changes from Original (July 2013) to Revision A **Page**

- 已将首页数据表更新为完全版。 ... 1

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6 Terminal Configuration and Functions

4 Terminal DPW Package
Bottom View



Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
IOX	1, 2, 3, 4	IO	ESD-protected channel
GND	5	G	Ground

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Operating temperature range	-40	125	°C
I_{PP}	Peak pulse current (t_p = 8/20μs)		2.5	A
P_{PP}(forward)	Peak pulse power (t_p = 8/20μs)		35	W
P_{PP}(reverse)	Peak pulse power (t_p = 8/20μs)		18	W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature	–65	155	°C
ESD(1)	IEC 61000-4-2 contact ESD		±12	kV
	IEC 61000-4-2 air-gap ESD		±15	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}		0.0	5.5	V
T_A	Operating free-air temperature	–40	125	°C

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7.4 Thermal Information

THERMAL METRIC(1)		TPD4E110 DPW (4 TERMINALS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	291.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	224.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	245.8	
ψ_{JT}	Junction-to-top characterization parameter	31.4	
ψ_{JB}	Junction-to-board characterization parameter	245.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	195.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} = 10 µA			5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	I = 1A, TLP, I/O to GND		10		V
		I = 5A, TLP, I/O to GND		13		V
		I = 1A, TLP, GND to I/O		3		V
		I = 5A, TLP, GND to I/O		6		V
V_{BR}	Break-down voltage	I_{IO} = 1mA	6.5	7.5	8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5V		0.02	1	nA
R_{DYN}	Dynamic resistance	Any I/O to GND Terminal(1)		0.8		Ω
		GND to any I/O Terminal(1)		0.7		Ω
C_L	Line capacitance	V_{IO} = 2.5V, f = 1MHz, I/O to GND		0.45	0.55	pF
C_{CROSS}	Channel to channel input capacitance	GND Terminal = 0V, f = 1MHz, V_{BIAS} = 2.5 V, between channel terminals		0.003		pF
$\Delta C_{IO\text{-}TO\text{-}GND}$	Variation of channel input capacitance	GND Terminal = 0V, f = 1MHz, V_{BIAS} = 2.5 V, Channel_x terminal to GND – Channel_y terminal to GND		0.05		pF

(1) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10A and I = 20A.

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7.6 Typical Characteristics

At T_A = 25°C, unless otherwise noted

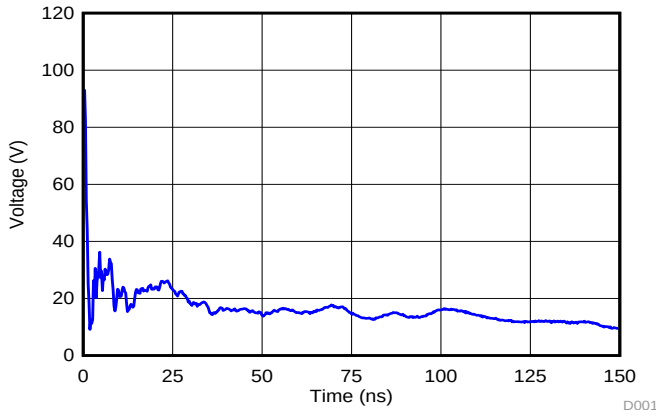


Figure 1. IEC 61000-4-2 Clamping Voltage, +8kV Contact

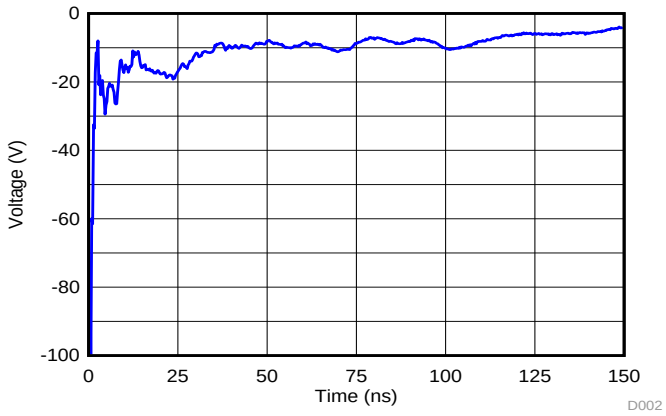


Figure 2. IEC 61000-4-2 Clamping Voltage, -8kV Contact

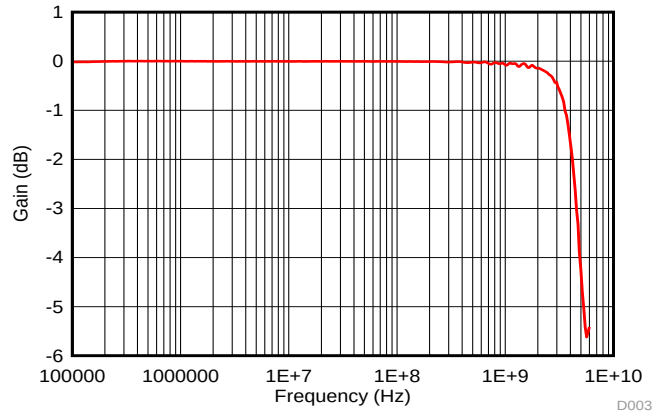


Figure 3. Insertion Loss

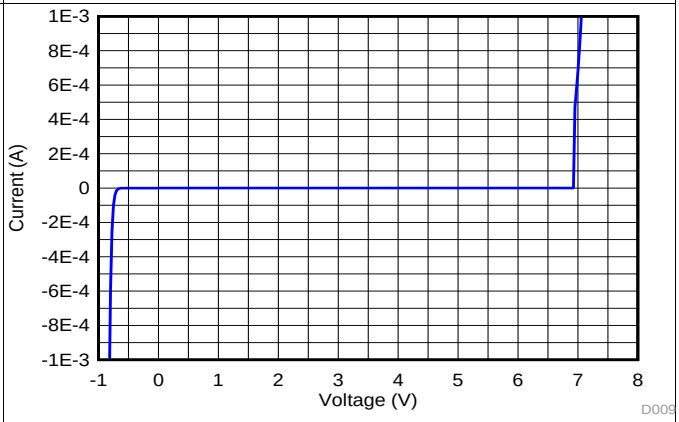


Figure 4. IV Curve

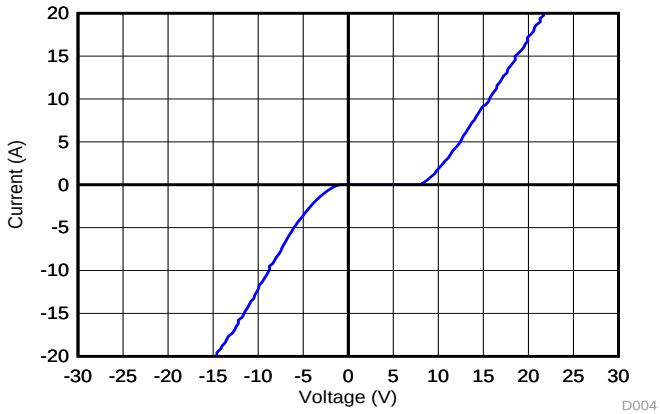


Figure 5. TLP, t_{PW} = 100 nS, t_{RISE} = 10 nS

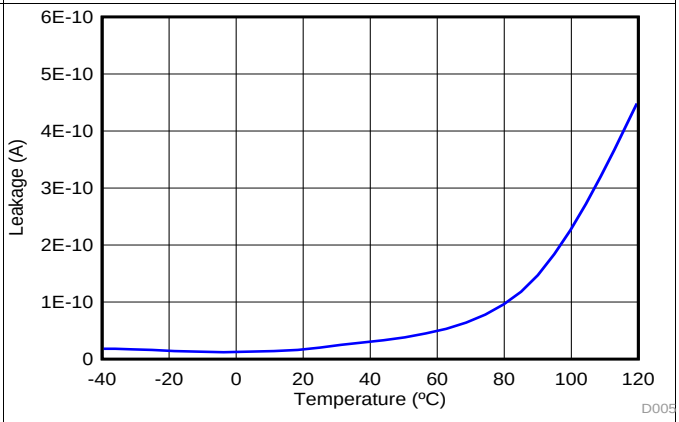


Figure 6. Leakage vs Temperature

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Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted

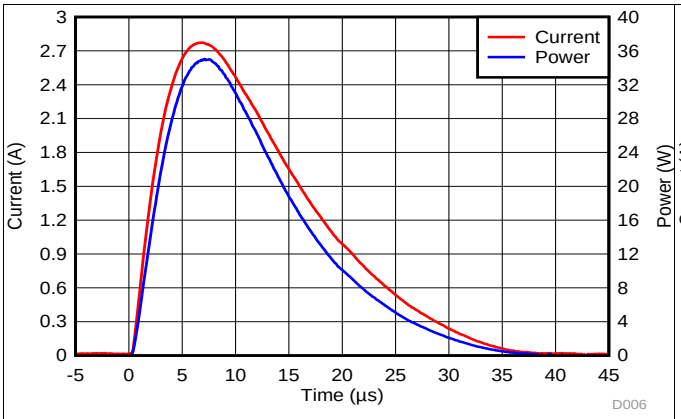


Figure 7. Surge Curves, IO to GND

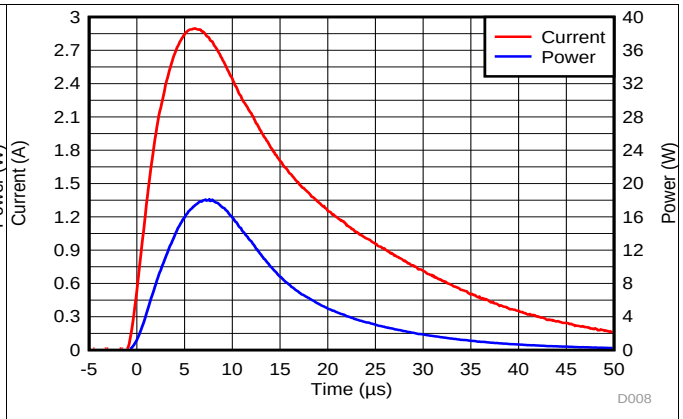


Figure 8. Surge Curves, GND to IO

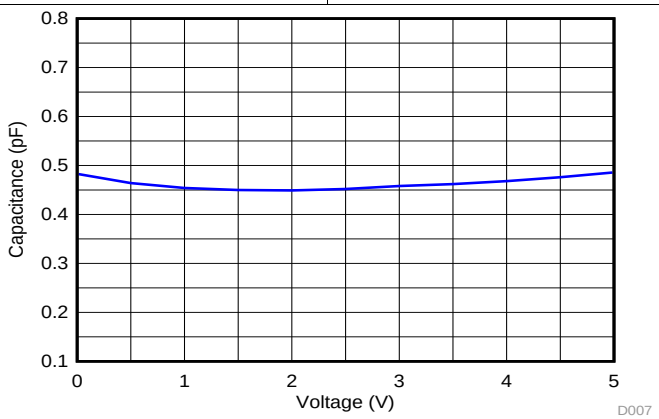


Figure 9. IO Terminal Capacitance vs V_{BIAS}

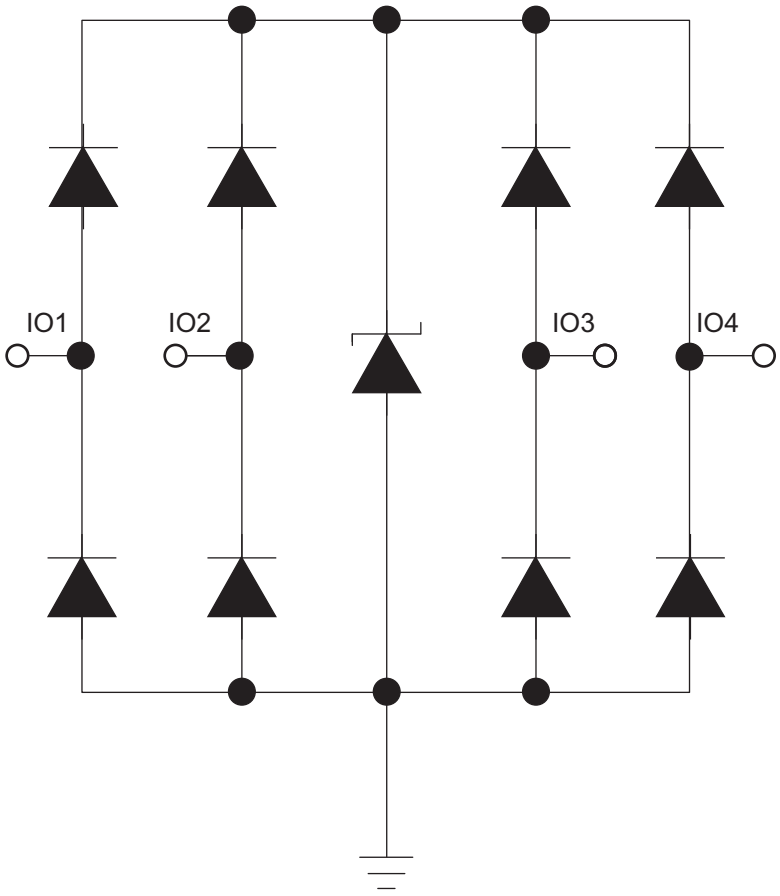
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8 Detailed Description

8.1 Overview

TPD4E110DPW is a uni-directional ESD protection device with ultra-low capacitance. The device is constructed with a central ESD clamp that features two hiding diodes per channel to reduce the capacitive loading. Each channel is rated to dissipate ESD strikes above the maximum level specified in the IEC61000-4-2 level 4 international standard. The TPD4E110DPW's ultra-low loading capacitance makes the device ideal for protecting high-speed signal terminals. The 0.8 mm x 0.8 mm package is designed for space saving designs. The pinout allows for straight through routing of 2 differential pairs when PCB manufacturing which feature sizes of 2.8 mils (0.071 mm).

8.2 Functional Block Diagram



8.3 Feature Description

TPD4E110 is a uni-directional Electrostatic Discharge (ESD) protection device with ultra-low capacitance. The device is constructed with a central ESD clamp that features two hiding diodes per line to reduce the capacitive loading. Each line is rated to dissipate ESD strikes above the maximum level specified in the IEC61000-4-2 level 4 international standard. The TPD4E110's ultra-low loading capacitance makes it ideal for protecting high-speed signal terminals.

8.4 Device Functional Modes

TPD4E110 is a passive integrated circuit that activates whenever voltages above V_{BR} or below the lower diodes $V_{forward}$ (–0.6V) are present upon the circuit being protected. During ESD events, voltages as high as ±15 kV can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E110 (usually within 10’s of nano-seconds) the device reverts to passive.

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9 Applications and Implementation

9.1 Application Information

TPD4E110 is a diode array type Transient Voltage Suppressor (TVS) which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

9.2 Typical Application

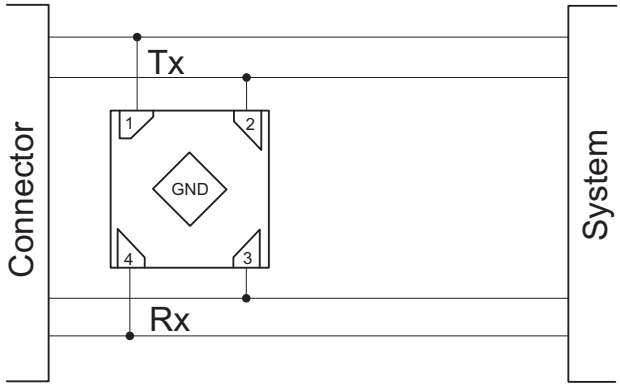


Figure 10. Protecting a Pair of Super-Speed Data Lines

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Signal range on Pin 1, 2, 3, or 4	0V to 5.5V
Operating Frequency	3.0 GHz

9.2.2 Detailed Design Procedure

To begin the design process some parameters must be decided upon. The designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

9.2.2.1 Signal range on Terminal 1, 2, 3, or 4

TPD4E110 has 4 identical protection channels for signal lines. The symmetry of TPD4E110 provides flexibility when selecting which of the 4 IO channels will protect which signal lines. Any IO will support a signal range of 0V to 5.5V.

9.2.2.2 Operating Frequency

The 0.45pF capacitance of each IO channel supports data rates up to 6Gbps.

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9.2.3 Application Curves

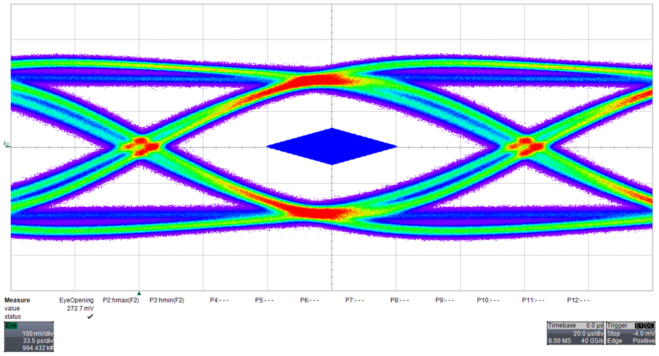


Figure 11. Eye Diagram for USB 3.0 Super-Speed Data Lines Using Single Layer Routing with Device Installed

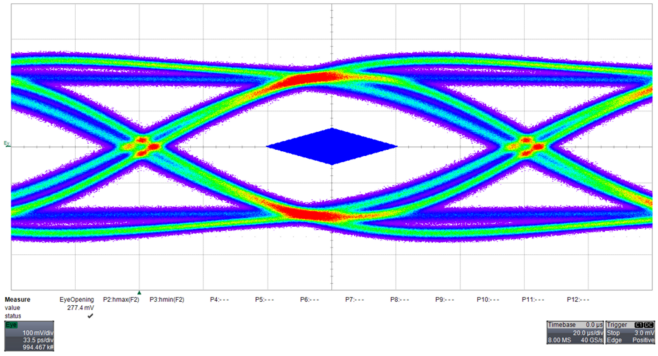


Figure 12. Eye Diagram for USB 3.0 Super-Speed Data Lines Using Single Layer Routing without Device Installed

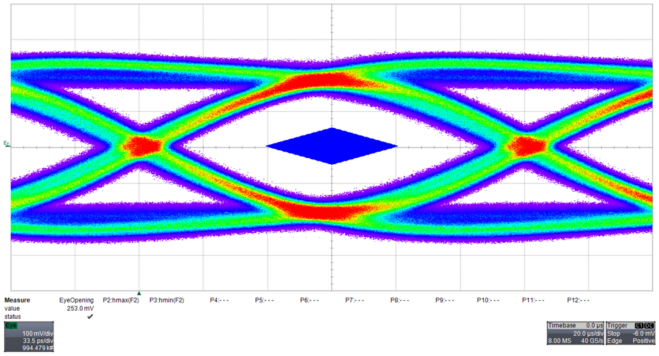


Figure 13. Eye Diagram for USB 3.0 Super-Speed Data Lines Using Double Layer Routing with Device Installed

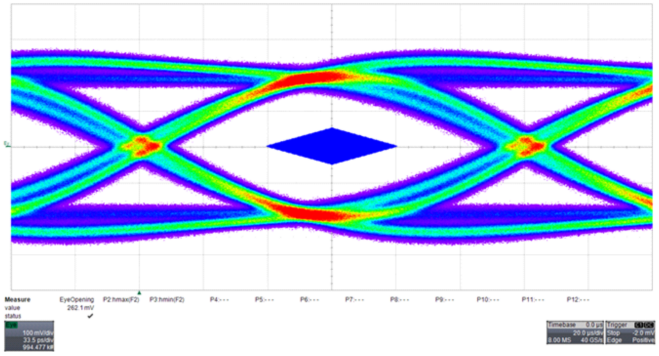


Figure 14. Eye Diagram for USB 3.0 Super-Speed Data Lines Using Double Layer Routing with Device Installed

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10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

10.2.1 Single Layer Routing

PCB manufacturing technologies allowing 2.8 mil (0.071 mm) clearances can route two Super-Speed data line pairs through TPD4E110 on a single layer.

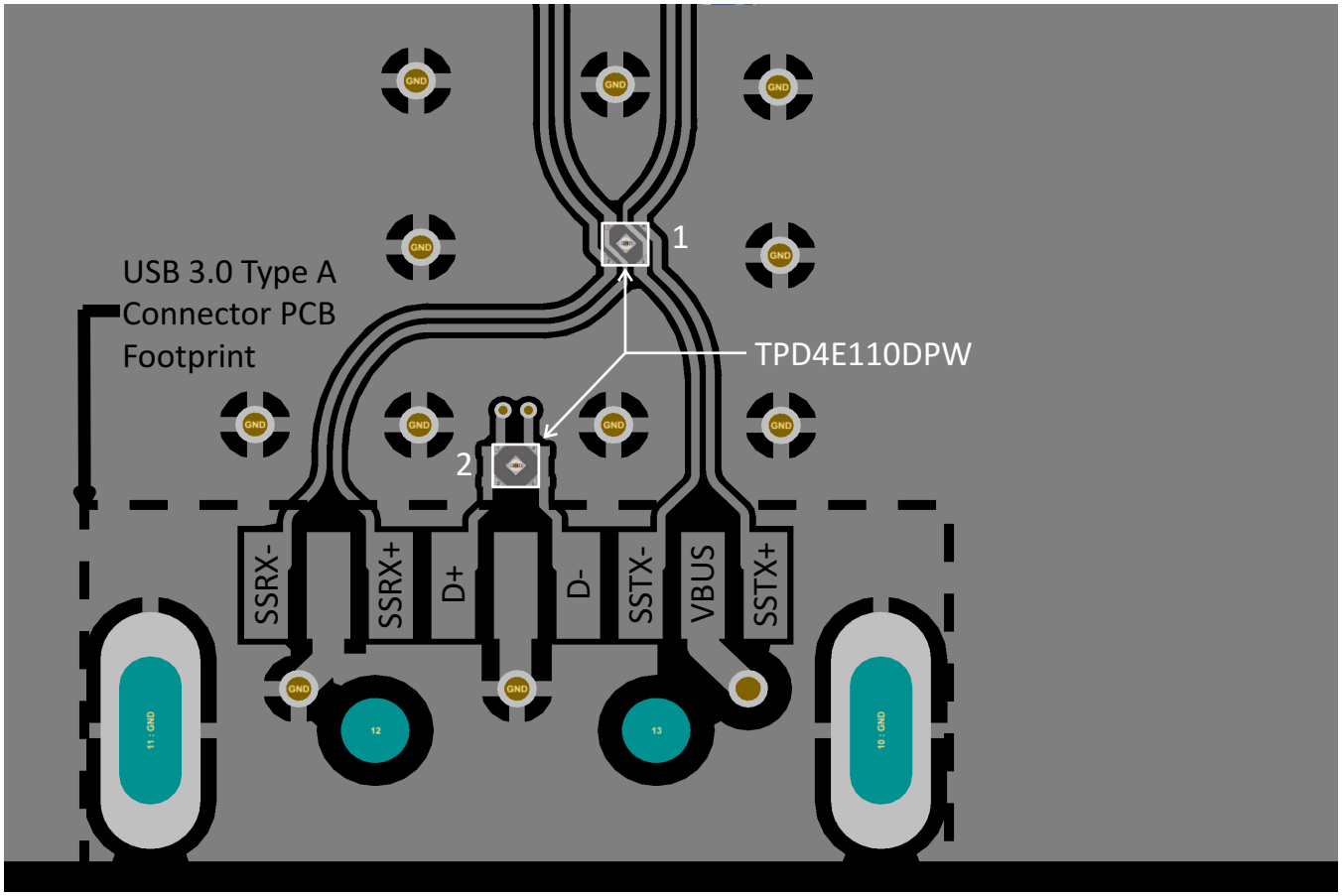


Figure 15. Example Layout for USB 3.0 Type A connector using two TPD4E110s

In Figure 15, Figure 16 and Figure 17 an example layout shows the use of two TPD4E110s to protect the USB 3.0 port. TPD4E110 Number 1 is protecting the two Super-Speed data pairs used for Super Speed data transfer, and TPD4E110 Number 2 protects the USB 2.0 D+/D– Hi-Speed data lines. Number 2 uses two channels to protect each line in the pair, thus affording a more robust protection and simpler layout.

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Layout Example (continued)

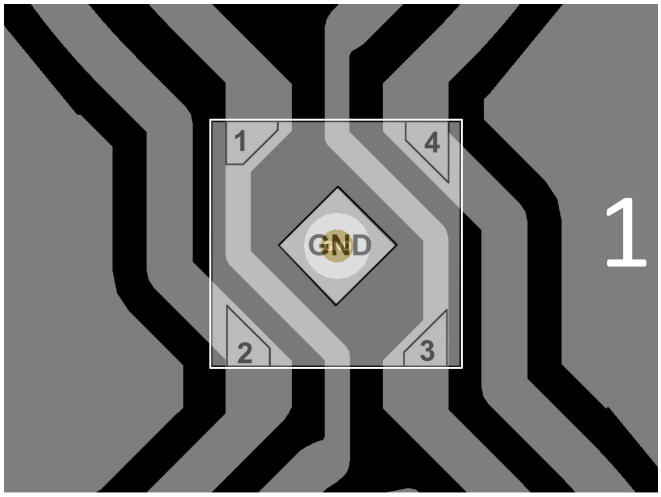


Figure 16. Close-up of Routing for TPD4E110 for Super-Speed Data Lines

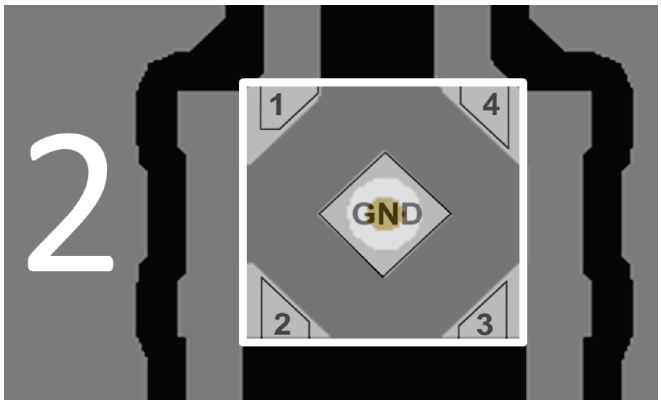


Figure 17. Close-up of Routing for TPD4E110 for USB 2.0 D+/D– Hi-Speed Data Lines

10.2.2 Double Layer Routing

PCB manufacturing technologies allowing 4.0 mil (0.1 mm) clearances can route two Super-Speed data line pairs through TPD4E110 using two layers.

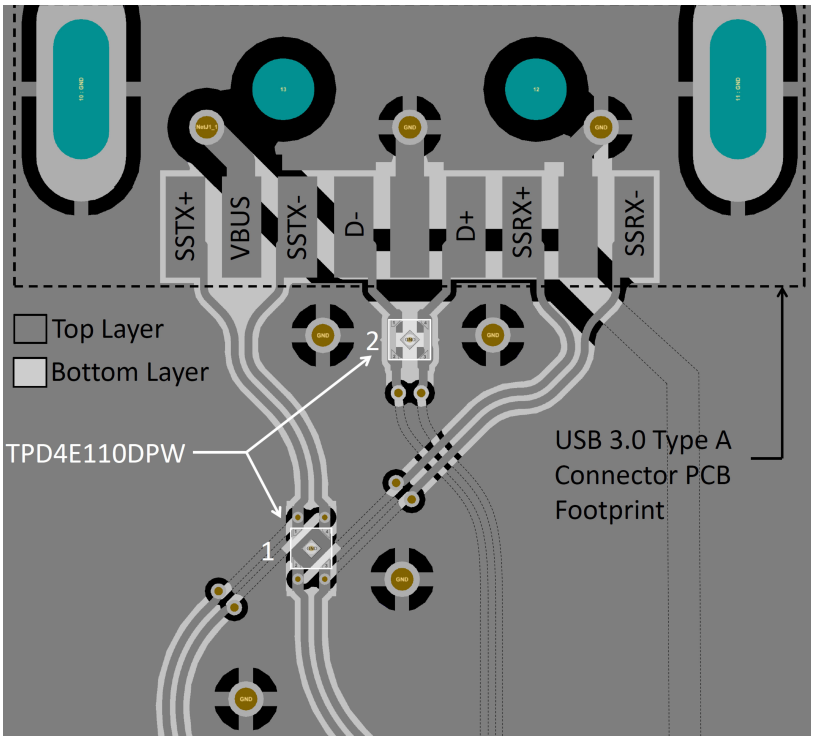


Figure 18. Example Layout for USB 3.0 Type A Connector Using Two TPD4E110s

In Figure 18 an example layout shows the use of two TPD4E110s to protect the USB 3.0 port. TPD4E110 Number 1 is protecting the two Super-Speed data pairs used for high speed data transfer, and TPD4E110 Number 2 protects the USB 2.0 D+/D– Hi-Speed lines. Number 2 uses two channels to protect each line in the pair, thus affording a more robust protection and simpler layout.

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11 器件和文档支持

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E110DPWR	Active	Production	X2SON (DPW) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D2
TPD4E110DPWR.B	Active	Production	X2SON (DPW) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

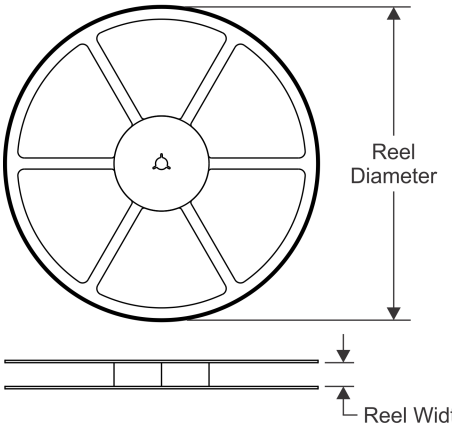
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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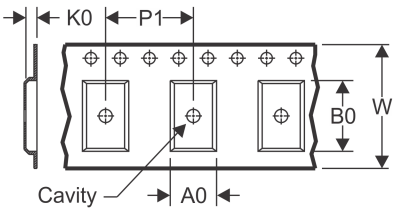
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

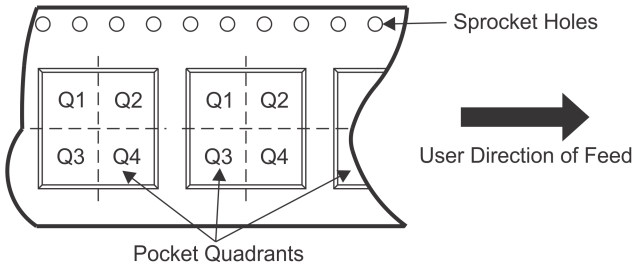


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

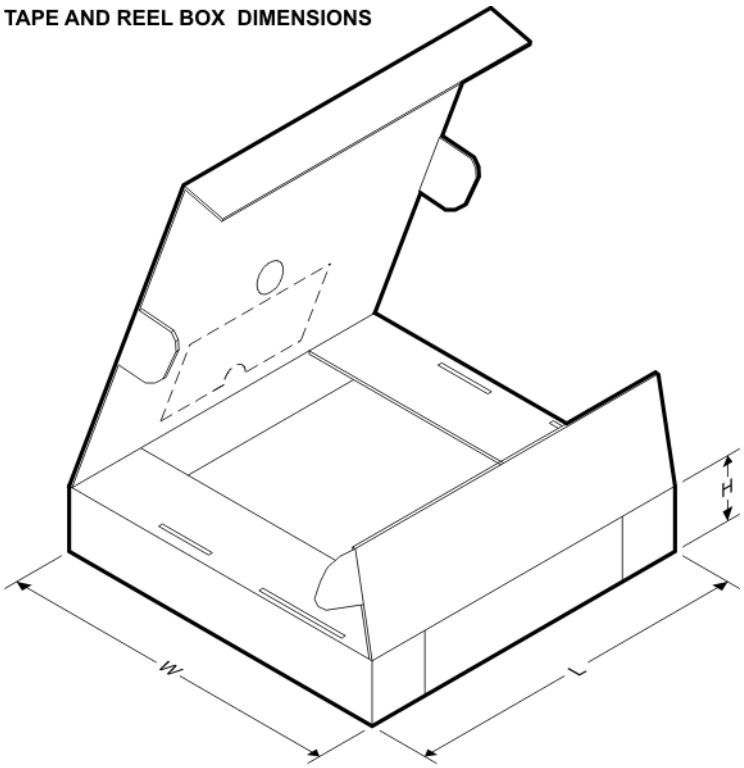
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E110DPWR	X2SON	DPW	4	3000	180.0	9.5	0.91	0.91	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E110DPWR	X2SON	DPW	4	3000	184.0	184.0	19.0

GENERIC PACKAGE VIEW

DPW 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

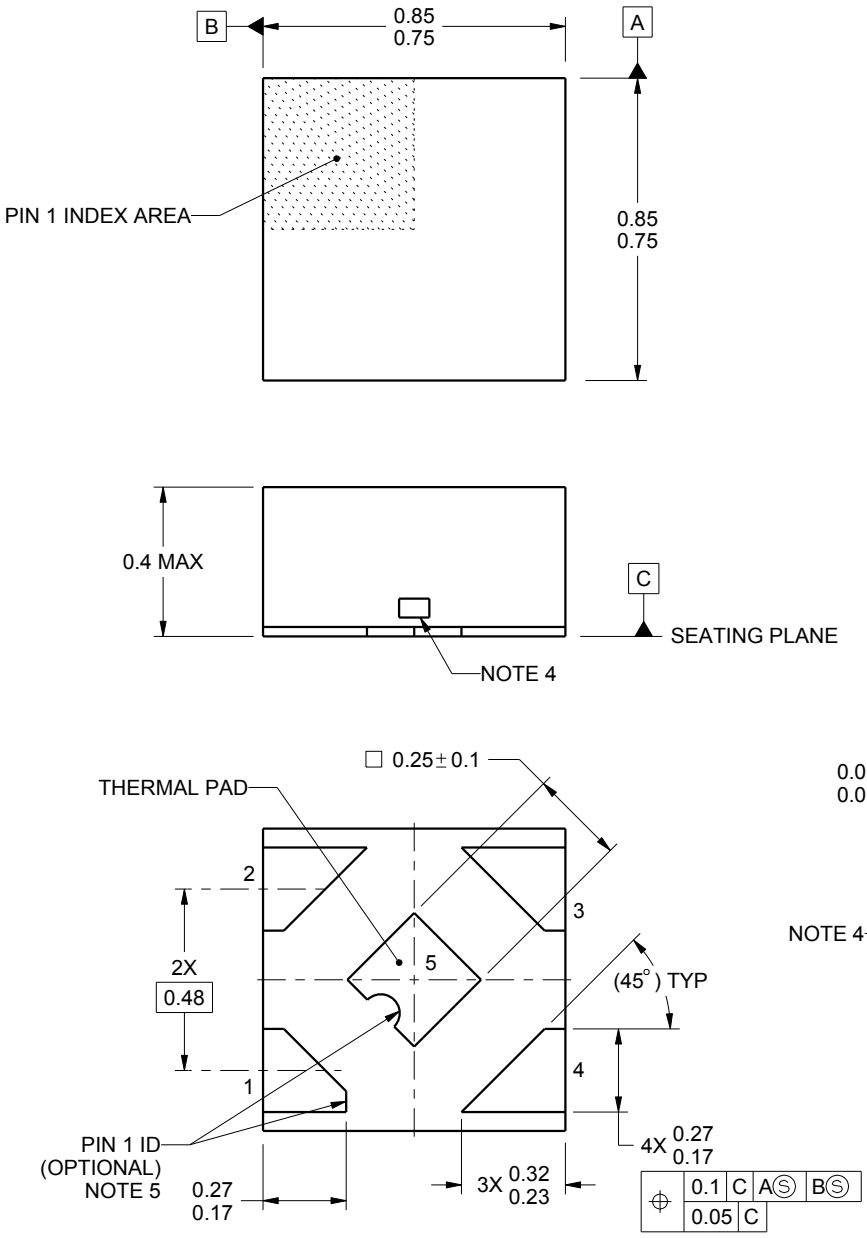
4211218-2/D

PACKAGE OUTLINE

DPW0004A

X2SON - 0.4 mm max height

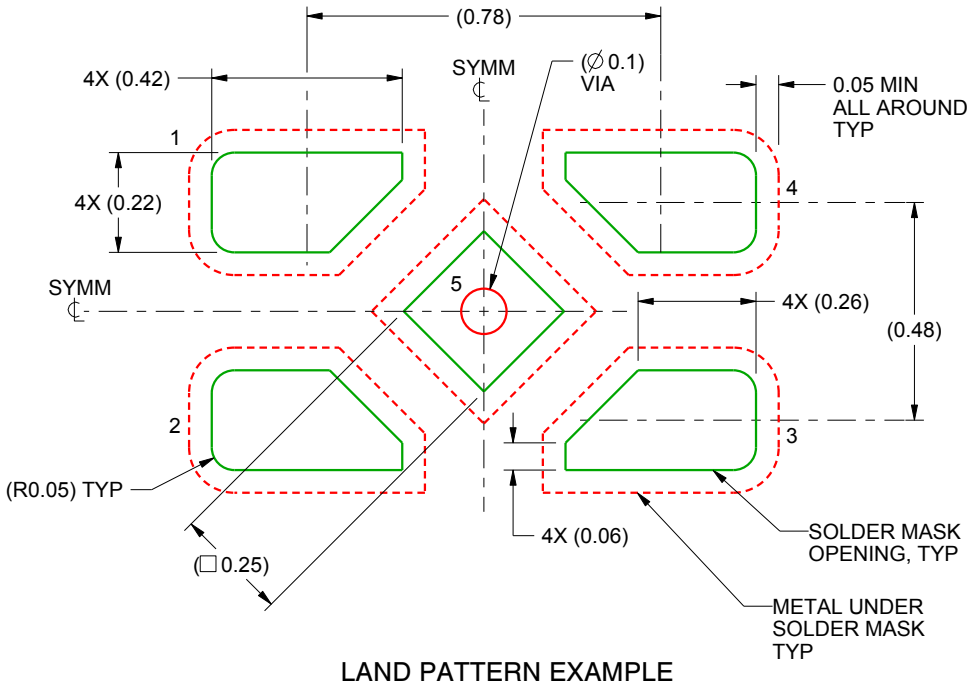
PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

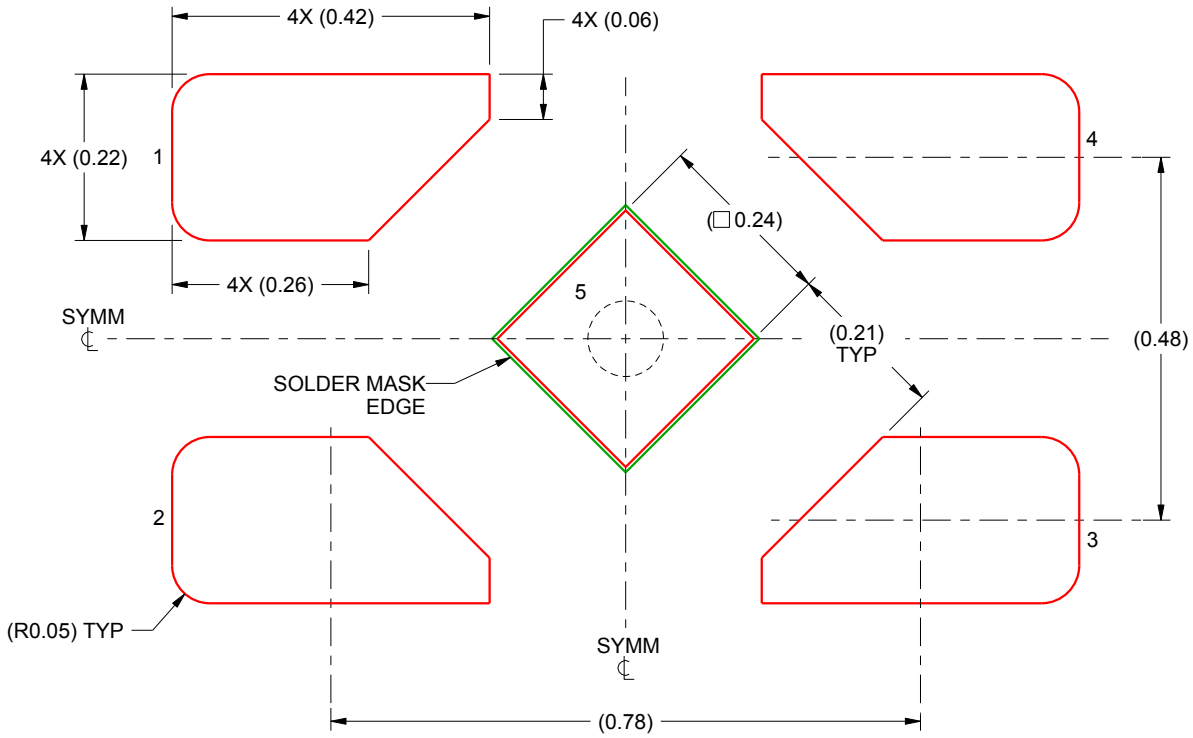


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

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NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5:
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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