

TPD4E001-Q1 具有 1.5pF I/O 电容的 4 通道 ESD 保护阵列

1 特性

- 符合 AEC-Q100 标准，其中包括以下内容：
 - 器件温度等级 1: -40°C 至 +125°C 运行环境温度范围
 - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 3B
 - HBM 电平 15kV
 - 器件带电器件模型 (CDM) ESD 分类等级 C5
- IEC 61000-4-2 4 级 ESD 保护
 - ±8kV 接触放电
 - ±15kV 气隙放电
- IEC 61000-4-5 浪涌保护
 - 5.5A (8/20μs)
- 输入电容低至 1.5pF
- 最大泄漏电流低至 10nA
- 电源电压范围：0.9V 至 5.5V

2 应用

- 终端设备
 - 汽车音响主机
 - 汽车后座娱乐系统
 - 汽车后置摄像头系统
- 接口
 - USB 2.0
 - 以太网
 - 精密模拟接口

3 说明

TPD4E001-Q1 器件是一款低电容 TVS 二极管阵列，设计用于为通信线路中连接的敏感电子元件提供 ESD 保护。每个通道包含一对将 ESD 脉冲引导至 V_{CC} 或者 GND 的瞬态电压抑制二极管。根据 IEC 61000-4-2 国际标准规定，TPD4E001-Q1 可防止接触放电电压高达 ±8kV 和气隙放电高达电压 ±15kV 的 ESD 事件发生。该器件每通道的电容低至 1.5pF，因此非常适用于高速数据接口。低泄露电流（最大 10nA）确保了系统的最低功耗和模块接口的高精度。

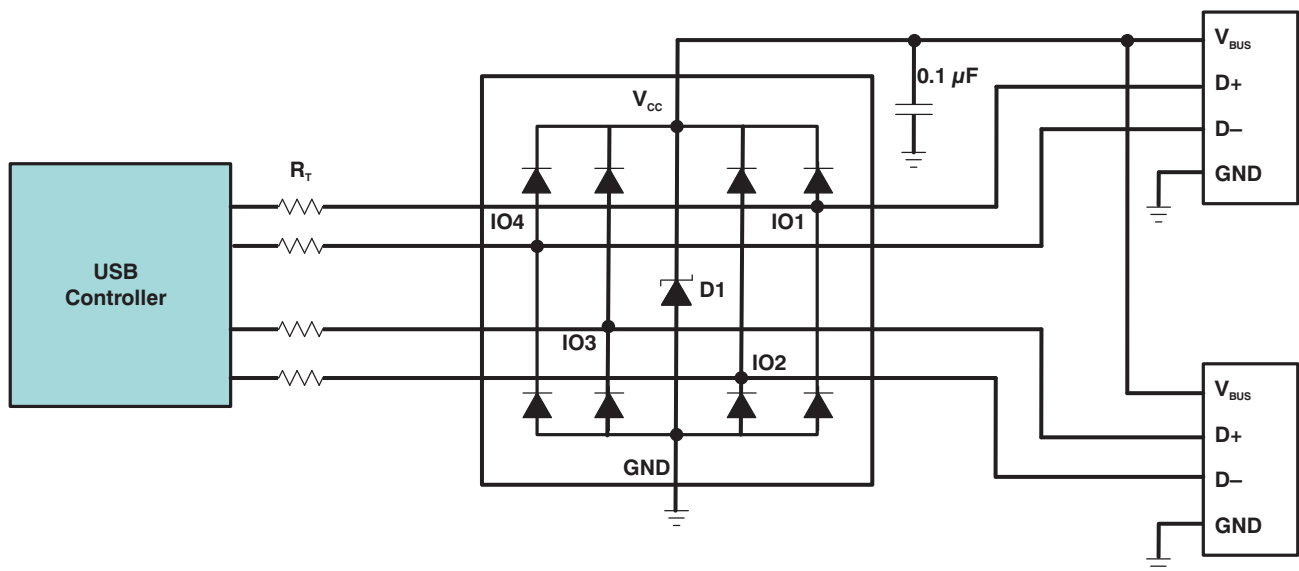
此外，此器件还适用于为使用 USB 2.0、以太网或高精度模拟接口的汽车音响主机、后座娱乐系统以及后座摄像机系统提供保护。

器件信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
TPD4E001-Q1	SOT-23 (6)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型电路原理图



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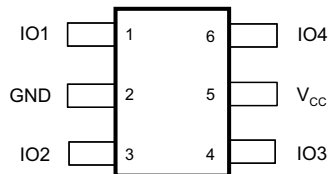
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (June 2017) to Revision F	Page
• Added ISO Specification.....	4
Changes from Revision D (March 2015) to Revision E	Page
• Updated <i>Typical Application Schematic</i>	9
Changes from Revision C (June 2013) to Revision D	Page
• 已添加 引脚配置和功能部分, ESD 额定值表, 特性 描述部分, 器件功能模式, 应用和实施部分, 电源相关建议部分, 布局部分, 器件和文档支持部分以及机械、封装和可订购信息部分	1
• 已更改 器件 CDM ESD 分类等级, 从 C4B 改为 C5	1
Changes from Revision B (February 2012) to Revision C	Page
• Changed maximum I_{CC} supply current in Electrical Characteristics	5
Changes from Revision A (April 2013) to Revision B	Page
• 已修改 说明 部分的文本.....	1
• Revised Figure 2 graph	5
• Revised APPLICATION INFORMATION schematic	9

5 Pin Configuration and Functions

**DBV Package
6-Pin SOT-23
Top View**



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	GND	Ground
IO1	1	I/O	ESD-protected channel
IO2	3		
IO3	4		
IO4	6		
V _{CC}	5	I	Power-supply input. Bypass V _{CC} to GND with a 0.1-μF ceramic capacitor

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	−0.3	7	V
V _{IO}	I/O voltage tolerance	−0.3	V _{CC} + 0.3	V
I _{PP}	Peak pulse current (T _p = 8/20 μs) ⁽²⁾		5.5	A
P _{PP}	Peak pulse power (T _p = 8/20 μs) ⁽²⁾		100	W
T _A	Free air operating temperature	−40	125	°C
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5.

6.2 ESD Ratings—AEC Specification

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±15000
		Charged-device model (CDM), per AEC Q100-011	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 contact discharge	±8000
		IEC 61000-4-2 air-gap discharge	±15000

6.4 ESD Ratings—ISO Specification

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	ISO 10605 (330 pF, 330 Ω) contact discharge	±8000
		ISO 10605 (330 pF, 330 Ω) air-gap discharge	±15000

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T _A	Free air operating temperature	–40	125	°C
V _{CC} pin	Operating voltage	0.9	5.5	V
IO1, IO2, IO3, IO4 pins	Operating voltage	0	V _{CC}	V

6.6 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD4E001-Q1	UNIT
		DBV (SOT-23)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	202.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	146.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	47.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	37.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	46.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Electrical Characteristics

V_{CC} = 5 V ± 10%, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
I _{CC}	Supply current			1	200	nA
V _F	Diode forward voltage	I _F = 10 mA	0.65		0.95	V
V _{BR}	Breakdown voltage	I _{BR} = 10 mA	11			V
V _{CLAMP}	Clamping voltage	Surge strike ⁽²⁾ on IO pin, GND pin grounded, V _{CC} = 5.5 V, I _{PP} = 5.5 A		16		V
V _{RWM}	Reverse standoff voltage	IO pin to GND pin			5.5	V
I _{IO}	Channel leakage current	V _{IO} = GND to V _{CC}			±10	nA
C _{IO}	Channel input capacitance	V _{CC} = 5 V, bias of V _{CC} /2, f = 10 MHz		1.5		pF

(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.

(2) Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5.

6.8 Typical Characteristics

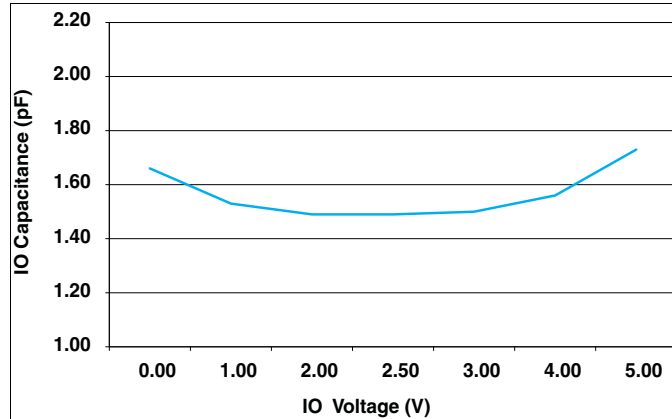


Figure 1. IO Capacitance vs IO Voltage ($V_{CC} = 5\text{ V}$)

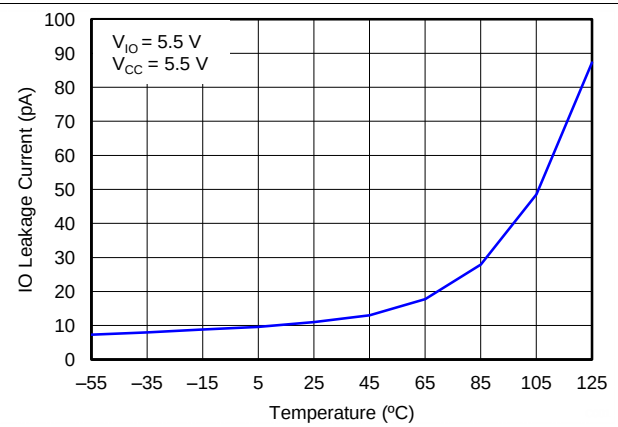


Figure 2. IO Leakage Current vs Temperature

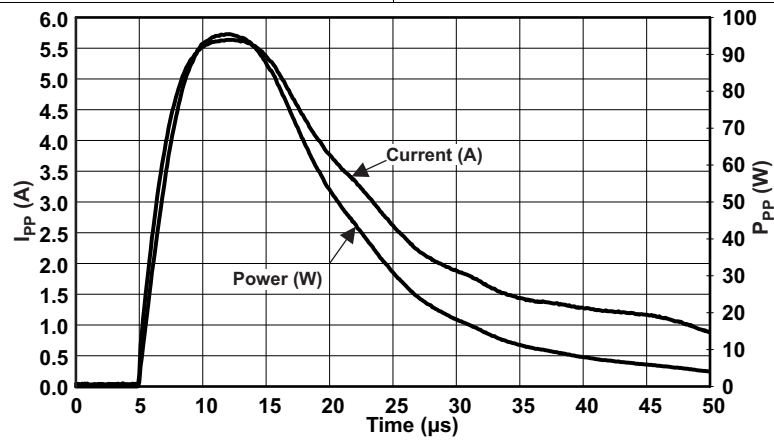


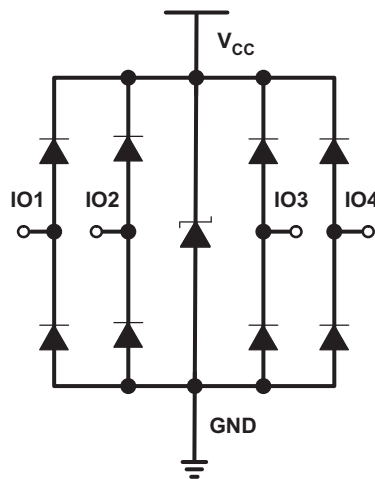
Figure 3. Peak Pulse Waveform, $V_{CC} = 5.5\text{ V}$

7 Detailed Description

7.1 Overview

The TPD4E001-Q1 device is a low-capacitance, TVS diode array designed for ESD protection in sensitive electronics connected to communication lines. Each channel consists of a pair of transient voltage suppression diodes that steer ESD pulses to V_{CC} or GND. The TPD4E001-Q1 device protects against ESD events up to ± 8 -kV contact discharge and ± 15 -kV air-gap discharge, as specified in IEC 61000-4-2 international standard. This device has a low capacitance of 1.5-pF per channel making it ideal for use in high-speed data interfaces. The low-leakage current (10 nA maximum) ensures minimum power consumption for the system and high accuracy for analog interfaces.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 AEC-Q100 Qualified

This device is qualified according to the AEC-Q100 standard. The device temperature rating is Grade 1 (-40°C to $+125^{\circ}\text{C}$). The HBM Classification Level passed is 3B (> 8 kV). The CDM Classification Level passed is C5 (all pins 750 V to < 1000 V).

7.3.2 IEC 61000-4-2 Level 4 ESD Protection

The device is specified at ± 8 -kV contact discharge and ± 15 -kV air gap discharge.

7.3.3 IEC 61000-4-5 Surge Protection

This device is rated to pass at least 5.5-A of peak pulse current according to the IEC 61000-4-5 (8/20- μs pulse) standard.

7.3.4 Low 1.5-pF Input Capacitance

This device has a typical capacitance of 1.5-pF on each of the four IO pins. This allows for high speed signals on the IO pins in excess of 1 Gbps.

7.3.5 Low 10-nA (Maximum) Leakage Current

This device is rated to have a maximum leakage current of 10-nA on each of the four IO pins.

7.3.6 0.9-V to 5.5-V Supply Voltage Range

This device is specified to operate with a supply voltage (on V_{CC}) between 0.9-V and 5.5-V to ensure sufficient signal integrity.

7.4 Device Functional Modes

The TPD4E001-Q1 device is a passive integrated circuit that triggers when voltages are above V_{BR} or below the lower diodes V_F (-0.6 V). During ESD events, voltages as high as ± 8 kV (contact) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E001-Q1 (usually within 10s of nano-seconds) the device reverts back to its high-impedance state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E001-Q1 device is a TVS diode array which is typically used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The triggered TVS holds this voltage, V_{CLAMP} , to a safe level for the protected IC.

8.2 Typical Application

For this design example, one TPD4E001-Q1 device is being used in a dual USB 2.0 application. This provides a complete port protection scheme.

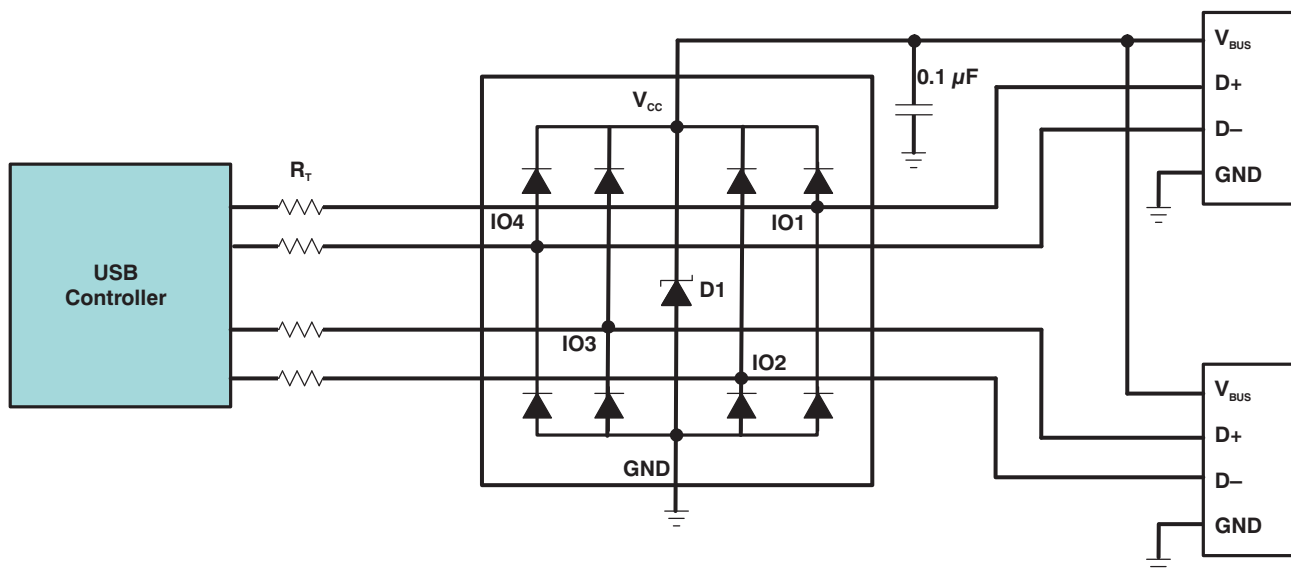


Figure 4. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

For this design example, a single TPD4E001-Q1 device is used to protect all the pins on two USB2.0 connectors. Given the USB application, known parameters are listed in the [Table 1](#).

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, or IO4	0 V to 3.6 V
Voltage range on V_{CC}	0 V to 5.25 V
Operating Frequency on IO1, IO2, IO3, or IO4	240 MHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all protected lines
- Operating frequency on all protected lines

8.2.2.1 Signal Range on IO1 Through IO4

The TPD4E001-Q1 device has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 IO channels protects which signal lines. Any IO supports a signal range of 0 to $(V_{CC} + 0.3)$ V. Therefore, this device supports the USB 2.0 signal swing assuming V_{CC} is set appropriately.

8.2.2.2 Voltage Range on V_{CC}

The V_{CC} pin can be connected in one of two ways:

- If the V_{CC} pin connects to the system power supply, the TPD4E001-Q1 device works as a transient suppressor for any signal swing above $V_{CC} + V_F$. TI recommends a 0.1- μ F capacitor on the device V_{CC} pin for ESD bypass.
- If the V_{CC} pin does not connect to the system power supply, the TPD4E001-Q1 device can tolerate higher signal swing in the range up to 10 V. Note that TI still recommends a 0.1- μ F capacitor at the V_{CC} pin for ESD bypass.

If this pin is connected to the USB 2.0 V_{BUS} supply or left floating, the allowable signal swing is enough for a USB 2.0 application.

8.2.2.3 Bandwidth on IO1 Through IO4

Each IO pin on the TPD4E001-Q1 device has a typical capacitance of 1.5 pF. This capacitance is low enough to easily support USB 2.0 data rates.

8.2.3 Application Curve

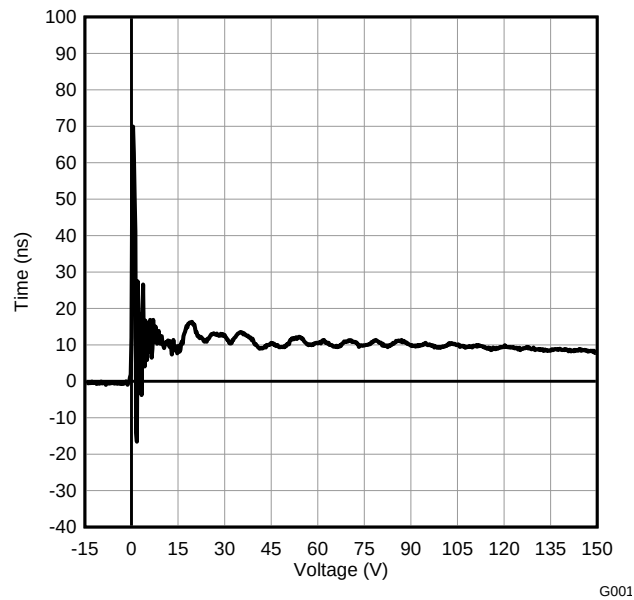


Figure 5. IEC 61000-4-2 Voltage Clamp Waveform 8-kV Contact

9 Power Supply Recommendations

This device is a passive ESD protection device so there is no need to power it. Do not violate the maximum voltage specifications for each pin.

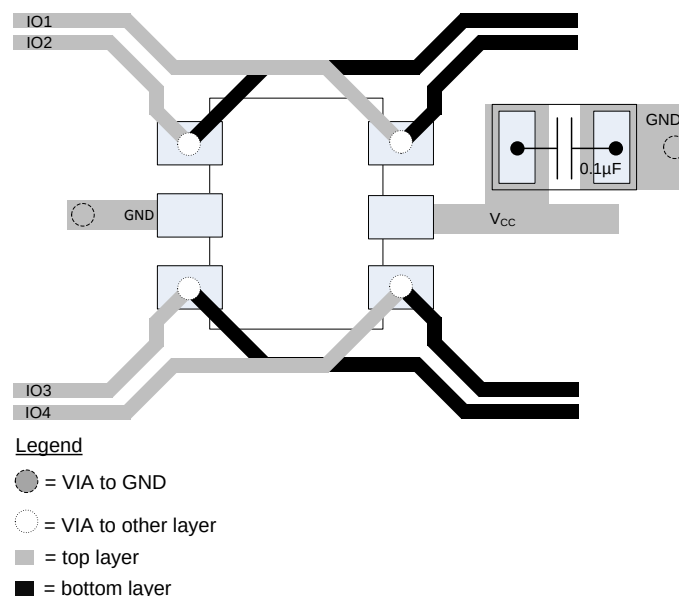
10 Layout

10.1 Layout Guidelines

When placed near the connector, the TPD4E001-Q1 device's ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage-current specifications. The TPD4E001-Q1 device ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, observe the following layout and design guidelines:

- Place the TPD4E001-Q1 device close to the connector. This allows the device to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
- Place a 0.1- μ F capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
- Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD4E001-Q1 device consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
- Leave the unused IO pins floating.
- One can connect the V_{CC} pin in two different ways:
 - a. If the V_{CC} pin connects to the system power supply, the TPD4E001-Q1 works as a transient suppressor for any signal swing above $V_{CC} + V_F$. TI recommends a 0.1- μ F capacitor on the device V_{CC} pin for ESD bypass.
 - b. If the V_{CC} pin does not connect to the system power supply, the TPD4E001-Q1 can tolerate higher signal swing in the range up to 10 V. Note that TI still recommends a 0.1- μ F capacitor at the V_{CC} pin for ESD bypass.
- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example



11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- [阅读和理解 ESD 保护数据表](#)
- [《ESD 布局指南》](#)

11.2 接收文档更新通知

如需接收文档更新通知，请访问 [ti.com](#) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E001QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AAXQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

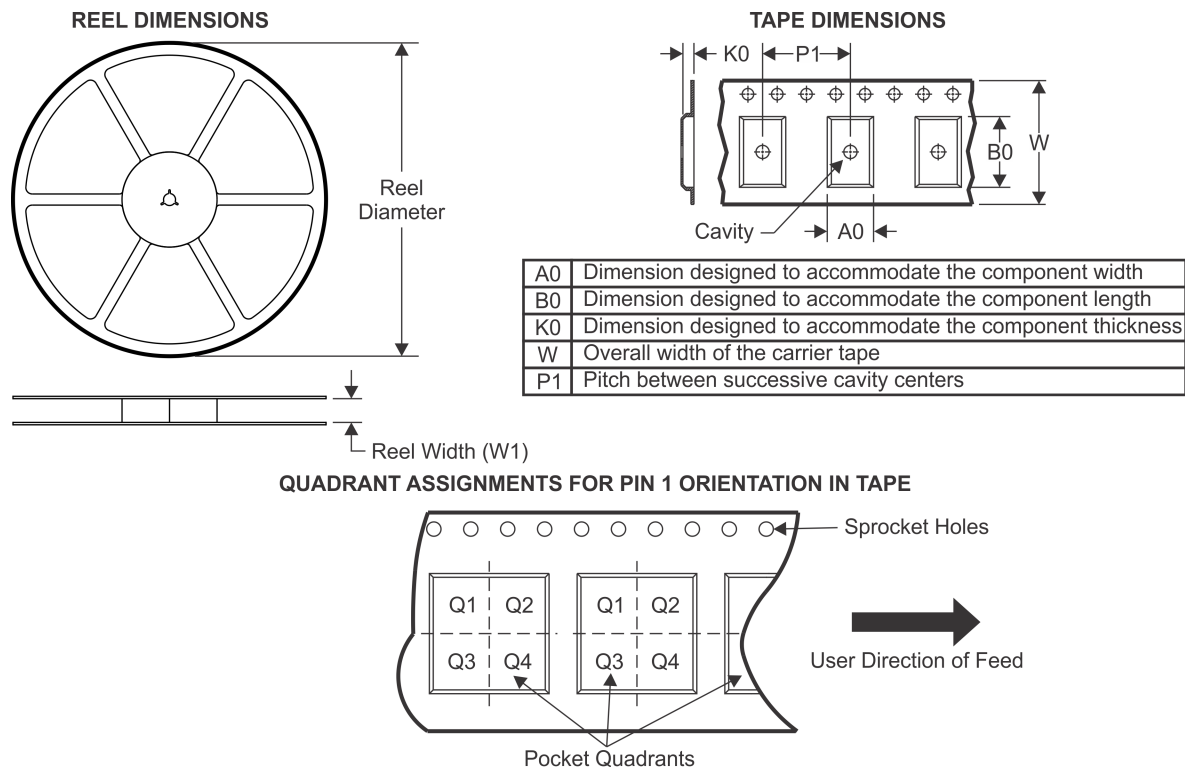
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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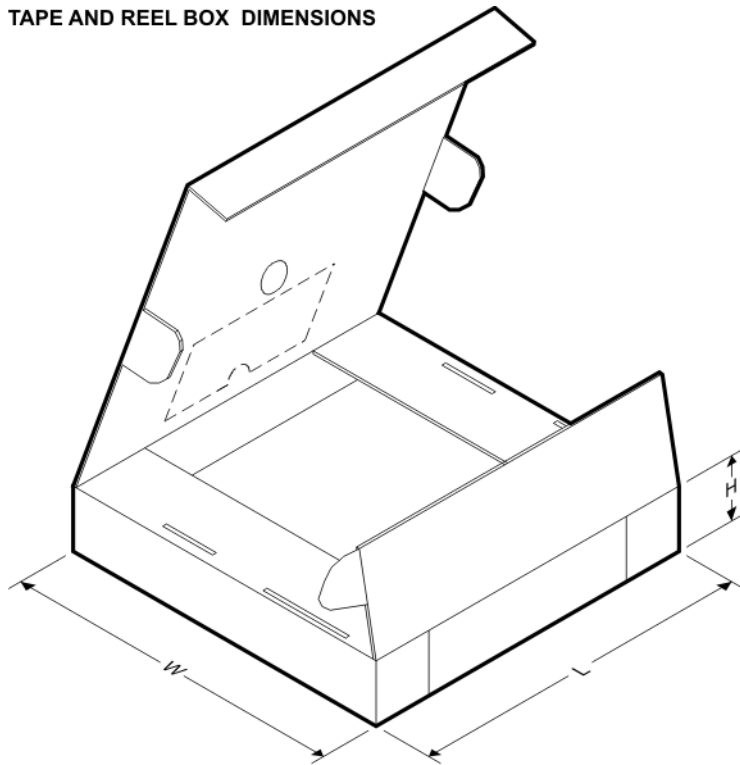
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E001QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



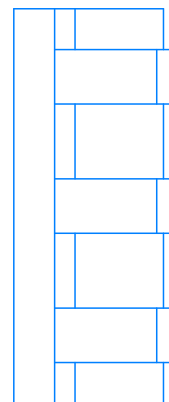
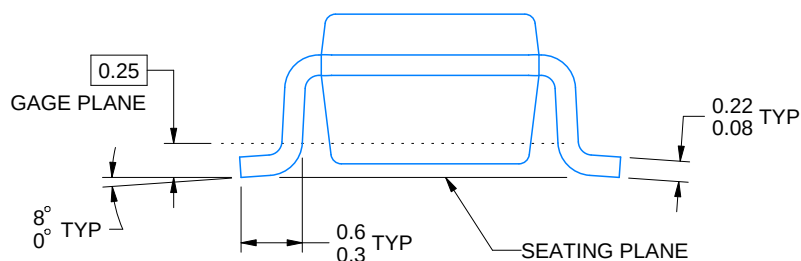
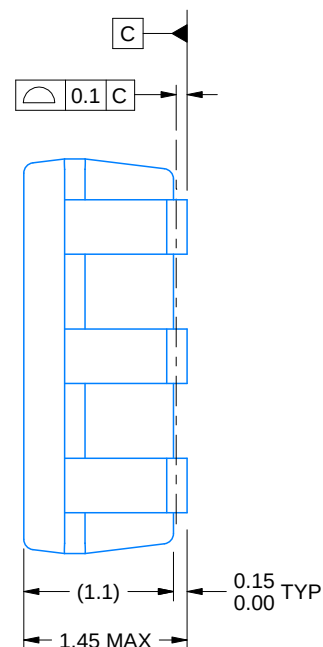
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E001QDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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NOTES:

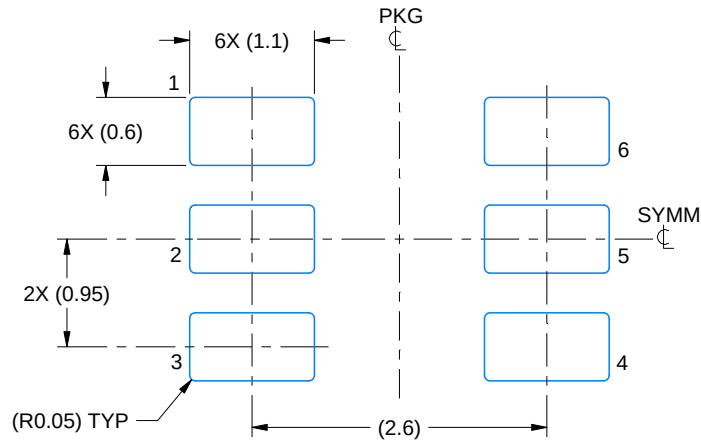
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

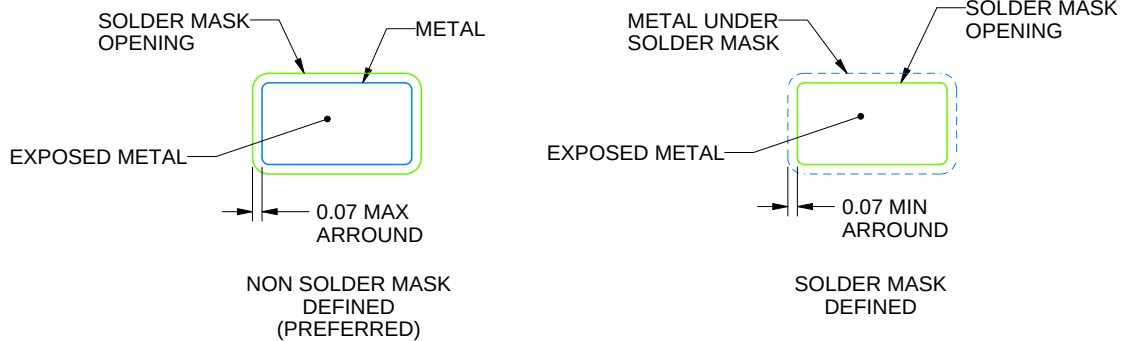
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

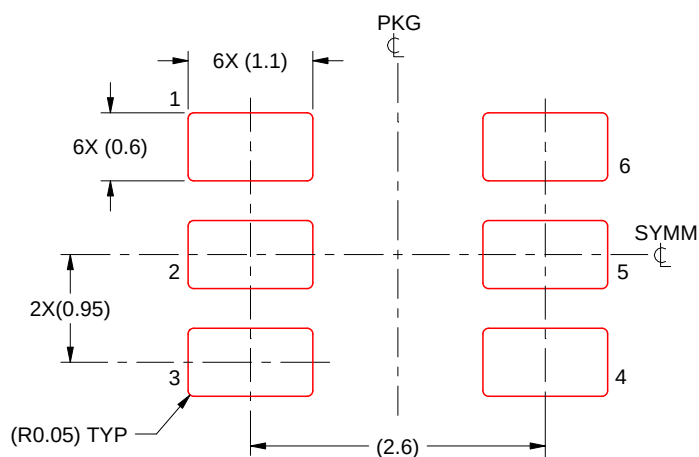
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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