# TPD1E10B09-Q1 采用 0402 封装、具有 10pF 电容和 9V 击穿电压的汽车类单通道 ESD 保护二极管

## 1 特性

- 符合 AEC-Q101 标准
- IEC 61000-4-2 4 级 ESD 保护
  - ±20kV 接触放电
  - ±20kV 气隙放电
- ISO 10605（330pF，330Ω）ESD 保护
  - ±8kV 接触放电
  - ±15kV 气隙放电
- IEC 61000-4-5 浪涌保护
  - 4.5A (8/20μs)
- I/O 电容 10pF（典型值）
- $R_{DYN}$：0.5Ω（典型值）
- 直流击穿电压 ±9.5V（最小值）
- 超低泄漏电流 100nA（最大值）
- 13V 钳位电压（$I_{PP}$ = 1A 时的典型值）
- 工业温度范围：–40°C 至 +125°C
- 节省空间的 0402 外形尺寸

## 2 应用

- 终端设备：
  - 音响主机
  - 高端音响
  - 外部放大器
  - 车身控制模块
  - 网关
  - 远程信息处理系统
  - 摄像头模块
- 接口：
  - 音频线路
  - 按钮
  - 存储器接口
  - GPIO

## 3 说明

TPD1E10B09-Q1 器件是一款采用小型 0402 业界通用封装的双向静电放电 (ESD) 瞬态电压抑制 (TVS) 二极管。该 TVS 保护二极管可方便在节省空间的应用中进行元件放置，并且具有低 $R_{DYN}$ 和高 IEC 等级。TPD1E10B09-Q1 的额定 ESD 冲击消散值高于 IEC 61000-4-2 国际标准中规定的最高级别（4 级），可以提供 ±20kV 接触放电和 ±20kV IEC 气隙保护。ESD 电压可轻松达到 5kV，并且在极端条件下，这些电压能够显著升高，从而对许多集成电路造成损坏。例如，在湿度较低的环境下，电压可超过 20kV。

低动态电阻 (0.5Ω) 和低钳位电压（1A IPP 时为 13V）可确保提供系统级瞬变事件保护，从而为暴露于 ESD 事件下的设计提供强大的保护。该器件还具有 10pF IO 电容，因此非常适用于音频线路、按钮、存储器接口或 GPIO。

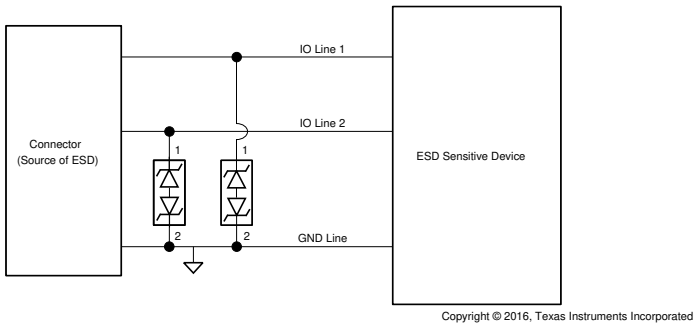
该器件还具有未经过汽车认证的型号：TPD1E10B09。

**封装信息**

| 器件型号 | 封装(1) | 封装尺寸(2) |
|---|---|---|
| TPD1E10B09-Q1 | DPY（X1SON，2） | 1mm × 0.6mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。




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**应用原理图**

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision A (September 2016) to Revision B (September 2023) | Page |
|---|---|
| • 更改了*封装信息* 表的格式以包含封装引线尺寸 | 1 |
| • 更改了整个文档中的表格、图和交叉参考的编号格式 | 1 |

| Changes from Revision * (August 2016) to Revision A (September 2016) | Page |
|---|---|
| • 将器件状态从*产品预发布* 更改为*量产数据* | 1 |


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# 5 Pin Configuration and Functions

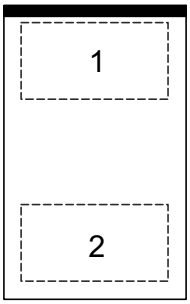



图 5-1. DPY Package, 2-Pin X1SON (Top View)

表 5-1. Pin Functions

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | IO | I/O | ESD protected I/O |
| 2 | GND | Ground | Ground. Connect to ground |

(1) I = input, O = output, GND = ground

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $I_{PP}$ | Peak pulse current (tp = 8/20 µs, positive) | | 5.5 | A |
| $I_{PP}$ | Peak pulse current (tp = 8/20 µs, negative) | | 4.5 | A |
| $P_{PP}$ | Peak pulse power (tp = 8/20 µs) | | 90 | W |
| P | Power Dissipation(2) | | 162 | mW |
| | Operating temperature | –40 | 125 | °C |
| $T_{stg}$ | Storage temperature | –65 | 155 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Max junction temperature: 125°C; power dissipation calculated at 25°C ambient temperature using JEDEC High K board Standard. Not to be used for steady state power dissipation in the breakdown region.

## 6.2 ESD Ratings—AEC Specification

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2500 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1000 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 ESD Ratings—IEC Specification

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 Contact Discharge | ±20000 | V |
| | | IEC 61000-4-2 Air-Gap Discharge | ±20000 | |

## 6.4 ESD Ratings—ISO Specification

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | ISO 10605 (330 pF, 330 Ω) Contact Discharge | ±8000 | V |
| | | ISO 10605 (330 pF, 330 Ω) Air-Gap Discharge | ±15000 | |

## 6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |
| | Operating voltage | Pin 1 to 2 or pin 2 to 1 | –9 | 9 | V |


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## 6.6 Thermal Information

| THERMAL METRIC[1] | | TPD1E10B09-Q1 DPY (X1SON) 2 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 615.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 404.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 493.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 127.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 493.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse stand-off voltage | Pin 1 to 2 or pin 2 to 1 | | | 9 | V |
| $I_{LEAK}$ | Leakage current | Pin 1 = 5 V, pin 2 = 0 V | | | 100 | nA |
| VClamp1,2 | Clamp voltage with ESD strike on pin 1, pin 2 grounded | $I_{PP}$ = 1 A, tp = 8/20 μs[2] | | 13 | | V |
| | | $I_{PP}$ = 5 A, tp = 8/20 μs[2] | | 17 | | |
| VClamp2,1 | Clamp voltage with ESD strike on pin 2, pin 1 grounded | $I_{PP}$ = 1 A, tp = 8/20 μs[2] | | 13 | | V |
| | | $I_{PP}$ = 4.5 A, tp = 8/20 μs[2] | | 20 | | |
| $R_{DYN}$ | Dynamic resistance | Pin 1 to pin 2[1] | | 0.5 | | Ω |
| | | Pin 2 to pin 1[1] | | 0.5 | | |
| $C_{IO}$ | I/O capacitance | $V_{IO}$ = 2.5 V; *f* = 1 MHz | | 10 | | pF |
| $V_{BR1,2}$ | Break-down voltage, pin 1 to pin 2 | $I_{IO}$ = 1 mA | 9.5 | | | V |
| $V_{BR2,1}$ | Break-down voltage, pin 2 to pin 1 | $I_{IO}$ = 1 mA | 9.5 | | | V |

(1) Extraction of $R_{DYN}$ using least squares fit of TLP characteristics from $I_{PP}$ = 10 A to $I_{PP}$ = 20 A.
(2) Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5.

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## 6.8 Typical Characteristics

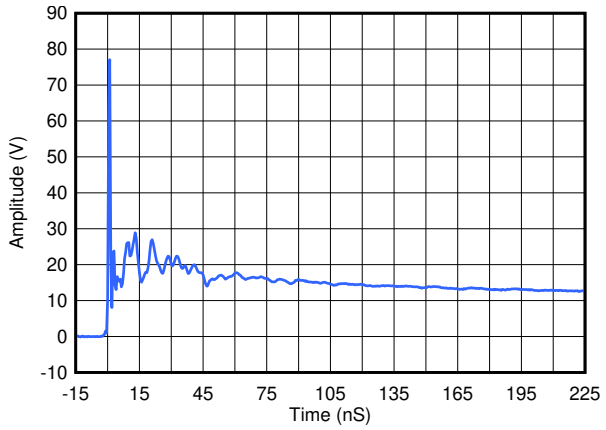



图 6-1. ESD Clamp Voltage 8-kV Contact ESD

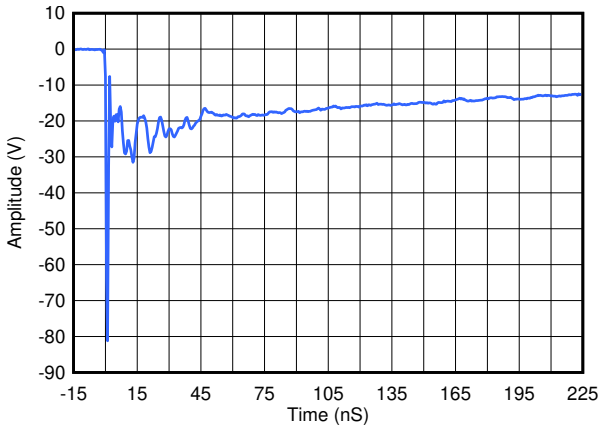



图 6-2. ESD Clamp Voltage – 8-kV Contact ESD

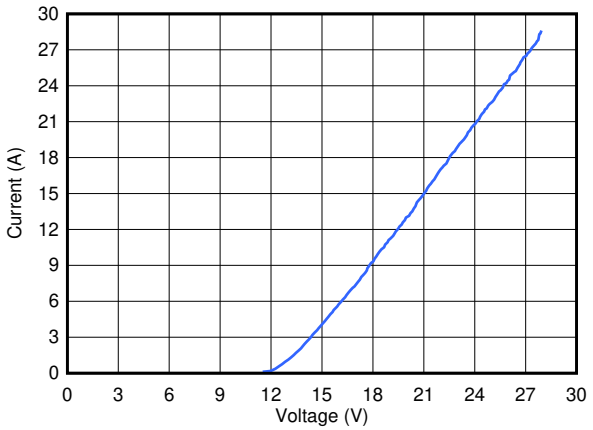



图 6-3. Transmission Line Pulse (TLP) Waveform Pin 1 to Pin 2

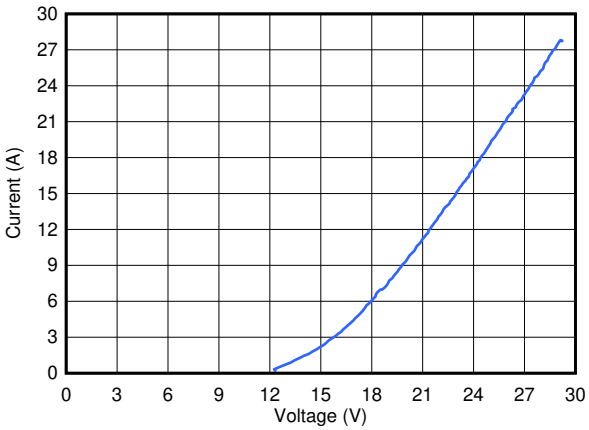



图 6-4. Transmission Line Pulse (TLP) Waveform Pin 2 to Pin 1

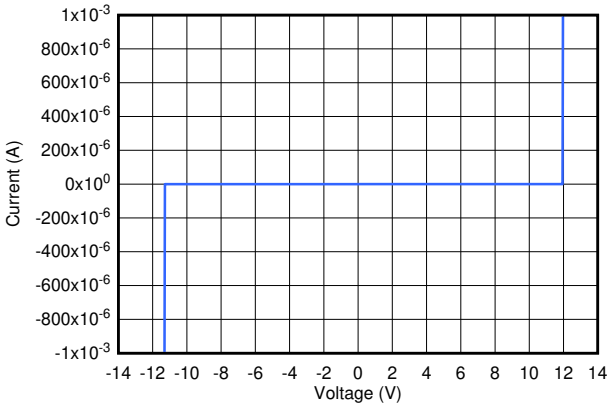



图 6-5. IV Curve

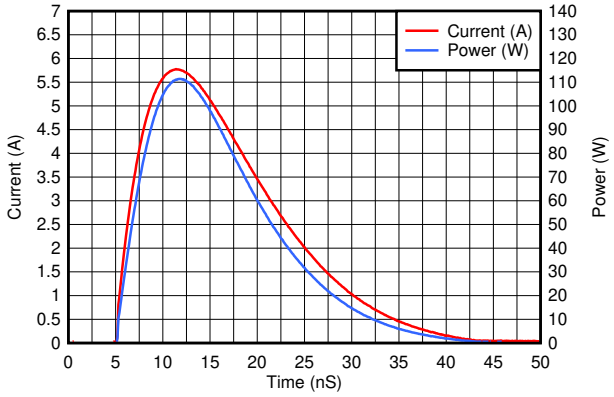



图 6-6. Positive Surge Waveform 8/20 µs


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## 6.8 Typical Characteristics (continued)

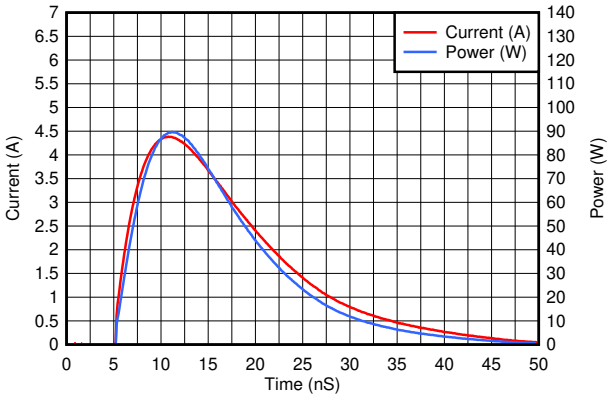



图 6-7. Negative Surge Waveform 8/20 µs

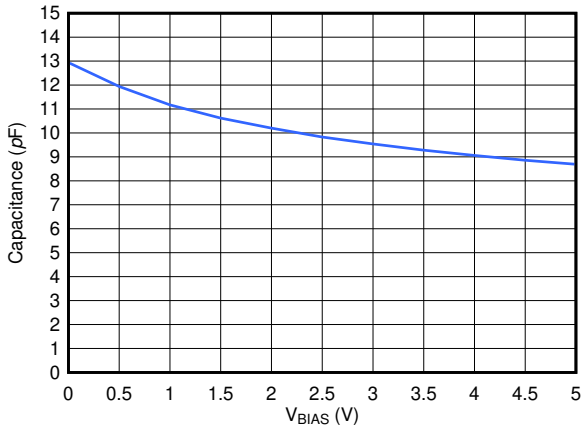



图 6-8. Pin Capacitance Across $V_{BIAS}$

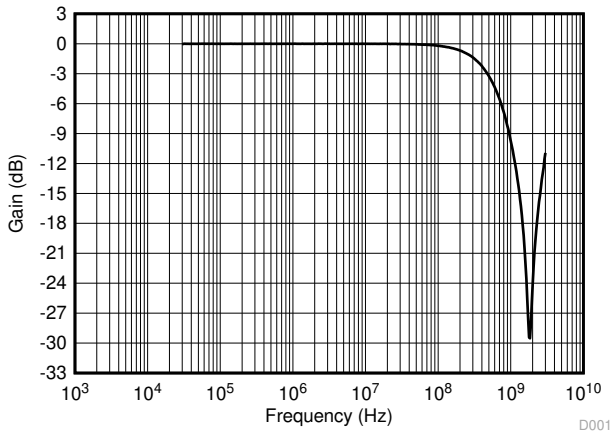


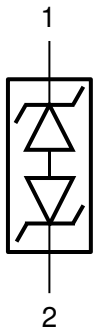

图 6-9. Insertion Loss

# 7 Detailed Description

## 7.1 Overview

The TPD1E10B09-Q1 is a single-channel ESD TVS that provides ±20-kV IEC 61000-4-2 (Level 4) contact and air-gap ESD protection. The 10-pF back-to-back diode architecture is suitable for signals that range from –9 V to 9 V and supports data rates up to 500 Mbps. The industry-standard 0402 package is convenient for placement in applications with limited space.

## 7.2 Functional Block Diagram




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## 7.3 Feature Description

The TPD1E10B09-Q1 is a bidirectional TVS with high ESD protection level. This device protects circuit from ESD strikes up to ±20-kV contact and ±20-kV air-gap specified in the IEC 61000-4-2 level 4 international standard. The device can also handle up to 4.5-A surge current (IEC 61000-4-5 8/20 µs). The I/O capacitance of 10 pF supports a data rate up to 500 Mbps. This clamping device has a small dynamic resistance of 0.5 Ω typically. This makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 13 V when the device is taking 1-A transient current. The breakdown is bidirectional so that this protection device is a good fit for GPIO, especially audio lines which carry bidirectional signals. Low leakage allows the diode to conserve power when working below the $V_{RWM}$. The industrial temperature range of –40°C to +125°C makes this ESD device work at extensive temperatures in most environments. The space-saving 0402 package can fit into small electronic devices like mobile equipment and wearables.

### 7.3.1 AEC-Q101 Qualified

This device is qualified to AEC-Q101 standards and is qualified to operate from –40°C to +125°C.

### 7.3.2 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±20-kV contact and ±20-kV air according to the IEC 61000-4-2 standard. An ESD-surge clamp diverts the current to ground.

### 7.3.3 ISO 10605 ESD Protection

The I/O pins can withstand ESD events at least ±8-kV contact and ±15-kV air according to the ISO 10605 (330 pF, 330 Ω) standard. An ESD-surge clamp diverts the current to ground.

### 7.3.4 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 5.5 A positive and 4.5 A negative (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

### 7.3.5 IO Capacitance

The capacitance between the I/O pins 10 pF. This capacitance support data rates up to 500 Mbps.


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### 7.3.6 Dynamic Resistance

The IO pins feature an ESD clamp that has a low $R_{DYN}$ of 0.50 Ω which prevents system damage during ESD events.

### 7.3.7 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of 9.5 V, which protects sensitive equipment from surges above the reverse standoff voltage of 9 V.

### 7.3.8 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of 100 nA (maximum) with a bias of 5 V.

### 7.3.9 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 13 V ($I_{PP}$ = 1 A) and 17 V ($I_{PP}$ = 5 A).

### 7.3.10 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

### 7.3.11 Space-Saving Footprint

This device features a space-saving, industry standard 0402 footprint.

## 7.4 Device Functional Modes

The TPD1E10B09-Q1 is a passive clamp that has low leakage during normal operation when the voltage between pin 1 and pin 2 is below $V_{RWM}$ and activates when the voltage between pin 1 and pin 2 goes above $V_{BR}$. During IEC ESD events, transient voltages as high as ±20 kV can be clamped between the two pins. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

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# 8 Application and Implementation

**备注**

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## 8.1 Application Information

The TPD1E10B09-Q1 is a single-channel back-to-back diode that protects one bidirectional signal line from electrostatic discharge and surge pulses. Because the diode is bidirectional, the TPD1E10B09-Q1 protects signals that have positive or negative polarity. During normal operation, the diode behaves as a 10-pF capacitance to ground. Board layout is critical for optimal performance of any diode.

Placement: The diode must be placed very close to the external connector for optimal performance. Ideally, the diode must be placed on the line that it is protecting.

Layout: Pin 1 of the diode must be right over the protected signal line. There must a thick and short trace from pin 2 to ground. An example is shown in the *Layout* section.

## 8.2 Typical Application

A system with a human interface is vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these connectors. The TPD1E10B09-Q1 is a single-channel ESD protection device containing back-to-back TVS diodes, which is typically used to provide a path to ground for dissipating ESD events on bidirectional signal lines between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low $R_{DYN}$ of the triggered TVS holds this voltage, $V_{CLAMP}$, to a tolerable level to the protected IC.

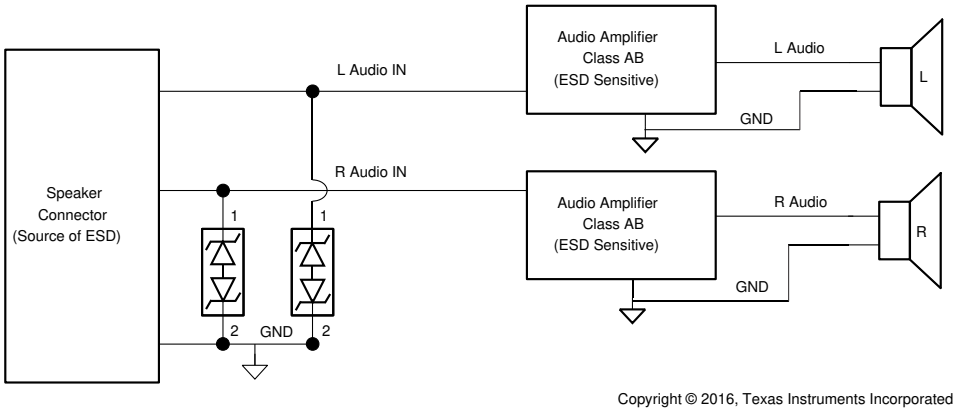



**图 8-1. Typical Application Schematic**


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### 8.2.1 Design Requirements

For this design example, two TPD1E10B09-Q1s are used to protect left and right audio channels. 表 8-1 lists the known system parameters for this audio application.

**表 8-1. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Audio amplifier class | AB |
| Audio signal voltage range | – 8 V to 8 V |
| Audio frequency content | 20 Hz to 20 kHz |
| Required IEC 61000-4-2 ESD protection | ±15-kV Contact, ±15-kV Air-Gap |

### 8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer must make sure:

- The voltage range on the protected line does not exceed the reverse standoff voltage of the TVS diode(s) ($V_{RWM}$).
- The operating frequency is supported by the I/O capacitance, $C_{IO}$, of the TVS diode.
- The IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, the audio signal voltage range is – 8 V to 8 V. The $V_{RWM}$ for the TVS is – 9.5 V to 9.5 V; therefore, the bidirectional TVS does not break down during normal operation, and normal operation of the audio signal is not affected due to the signal voltage range. In this application, a bidirectional TVS like the TPD1E10B09-Q1 is required.

Next, consider the frequency content of this audio signal. In this application with the class AB amplifier, the frequency content is from 20 Hz to 20 kHz; ensure that the TVS I/O capacitance does not distort this signal by filtering it. With the TPD1E10B09-Q1 typical capacitance of 10 pF, which leads to a typical cutoff frequency of just under 500 MHz, this diode has sufficient bandwidth to pass the audio signal without distorting it.

Finally, the human interface in this application requires protection for ±15-kV Contact and ±15-kV Air-Gap ESD, which is above the standard Level 4 IEC 61000-4-2 system-level ESD protection. A standard TVS cannot survive this level of IEC ESD stress. However, the TPD1E10B09-Q1 can survive at least ±20-kV Contact and ±20-kV Air-Gap ESD. Therefore, the device can provide sufficient ESD protection for the interface, even though the requirements are stringent. For any TVS diode to provide its full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, it is crucial that a system designer uses proper board layout of their TVS ESD protection diodes. See the *Layout* section for instructions on properly laying out the TPD1E10B09-Q1.

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### 8.2.3 Application Curves

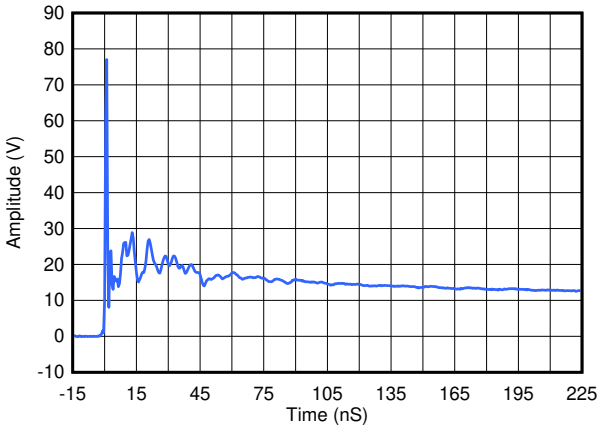



图 8-2. ESD Clamp Voltage 8-kV Contact ESD

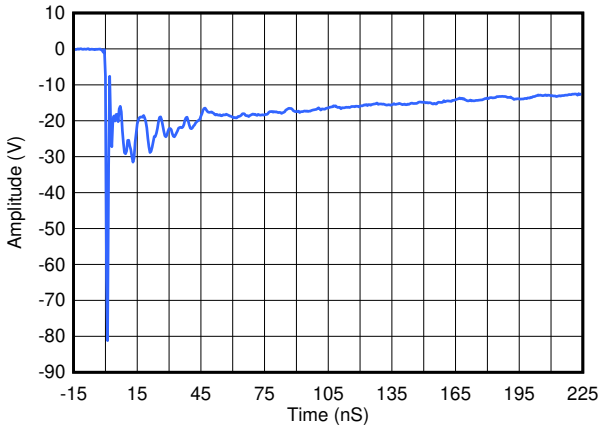



图 8-3. ESD Clamp Voltage – 8-kV Contact ESD

## 8.3 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, so there is no need to power it. Do not violate the maximum specifications for each pin.

## 8.4 Layout

### 8.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Use rounded corners with the largest radii possible on the protected traces between the TVS and the connector, thus eliminating any sharp corners.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or pin 2 is connected to ground, use a thick and short trace for this return path.


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### 8.4.2 Layout Example

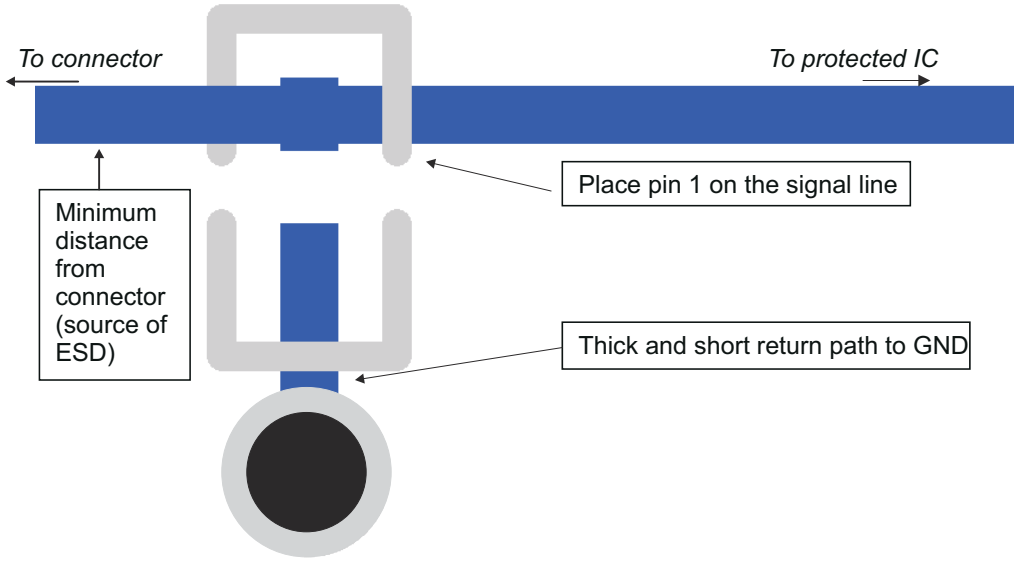



**图 8-4. Layout Example**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPD1E10B09-Q1 Evaluation Module*
- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet*
- Texas Instruments, *ESD Layout Guide*
- Texas Instruments, *ESD PROTECTION DIODES EVM*

## 9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 9.4 Trademarks

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## 9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPD1E10B09QDPYRQ1 | Active | Production | X1SON (DPY) \| 2 | 10000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 4N |
| TPD1E10B09QDPYRQ1.B | Active | Production | X1SON (DPY) \| 2 | 10000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 4N |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPD1E10B09-Q1 :**

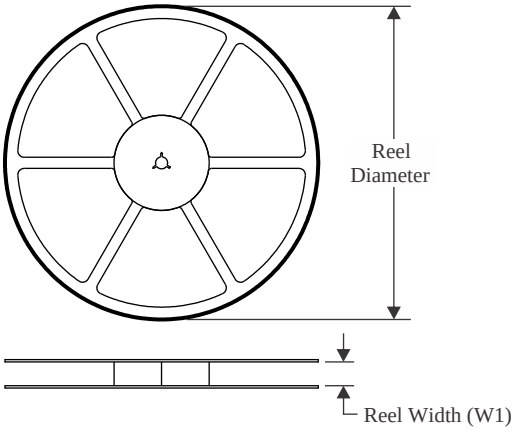
- Catalog : TPD1E10B09

NOTE: Qualified Version Definitions:

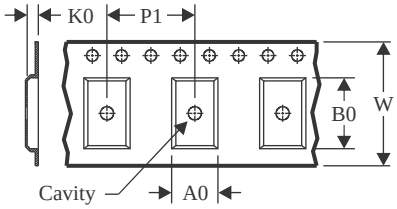
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

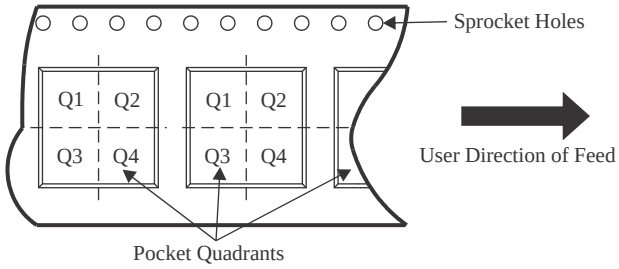



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

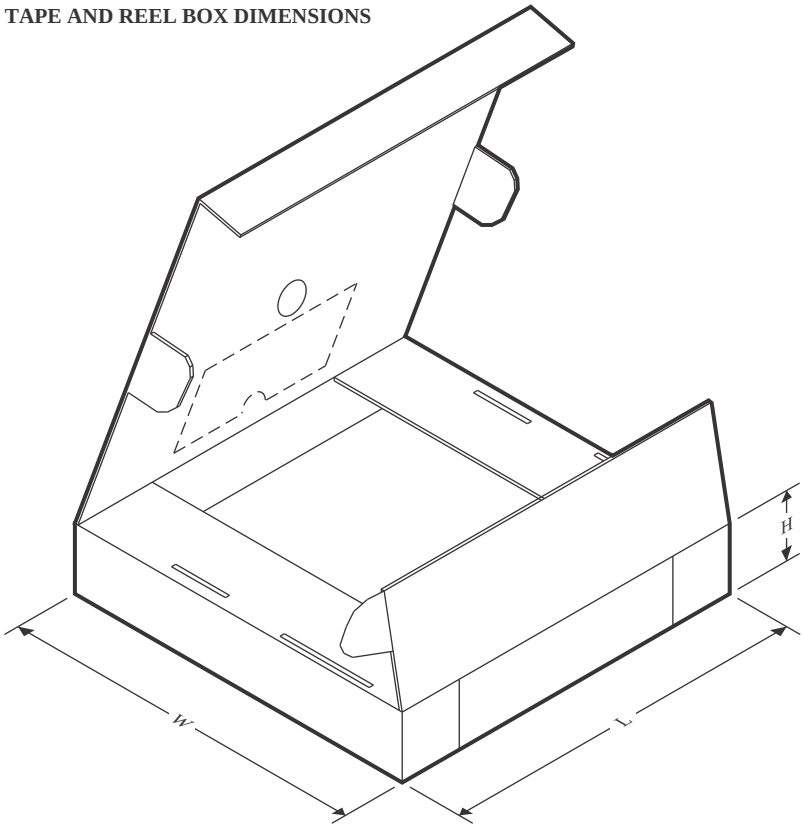
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD1E10B09QDPYRQ1 | X1SON | DPY | 2 | 10000 | 180.0 | 9.5 | 0.73 | 1.13 | 0.5 | 2.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPD1E10B09QDPYRQ1 | X1SON | DPY | 2 | 10000 | 189.0 | 185.0 | 36.0 |

# GENERIC PACKAGE VIEW

## DPY 2

## X1SON - 0.45 mm max height

**1 x 0.6 mm**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



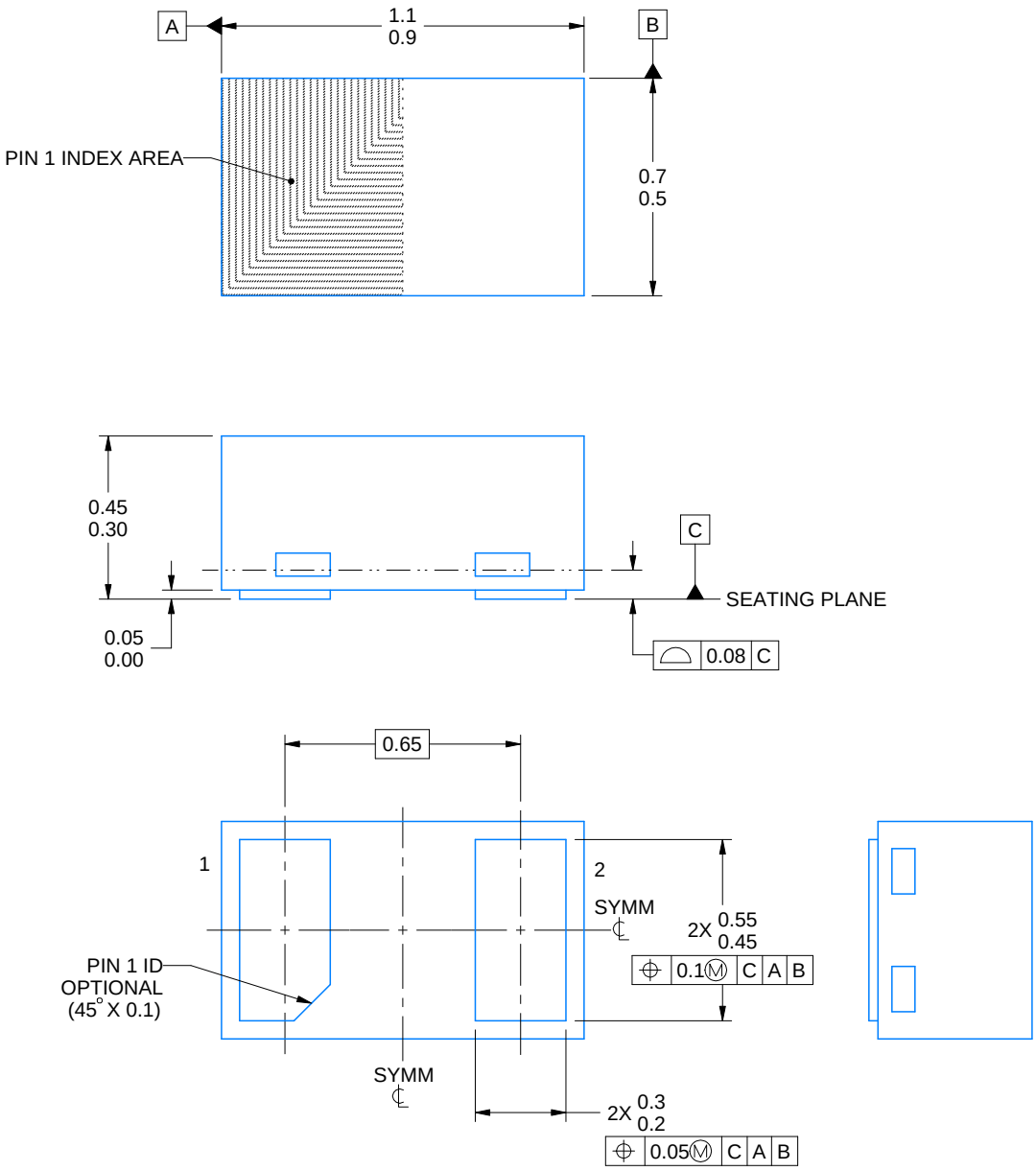

4231484/A

# PACKAGE OUTLINE

## DPY0002A

## X1SON - 0.45 mm max height

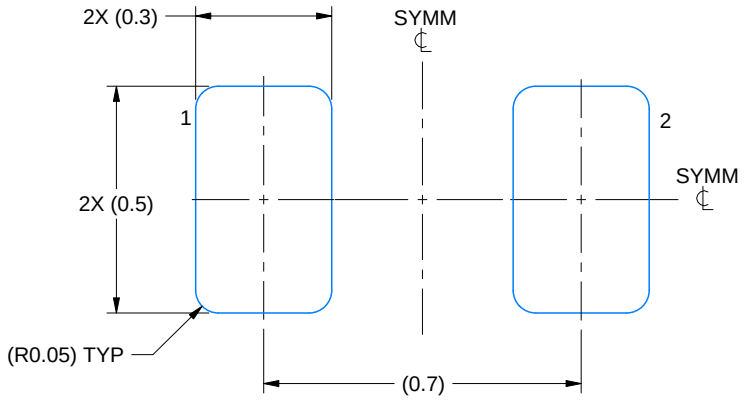
PLASTIC SMALL OUTLINE - NO LEAD



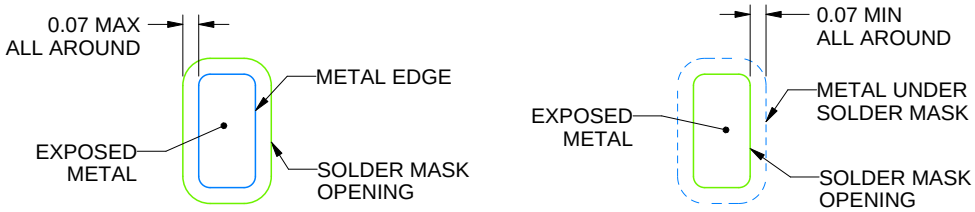

4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

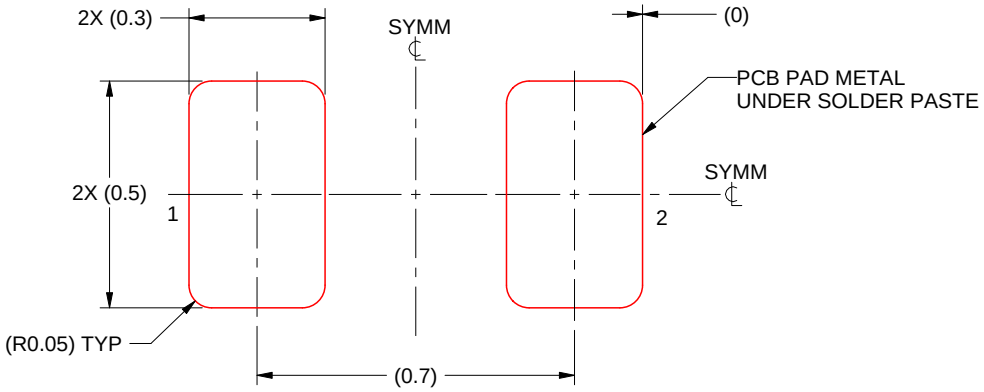



SOLDER MASK DETAILS

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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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