TEXAS INSTRUMENTS
TMUXHS221
ZHCSQZ0A – AUGUST 2022 – REVISED NOVEMBER 2022

TMUXHS221 USB 2.0 480Mbps 2:1/1:2 多路复用器/多路信号分离器开关

1 特性

- 与 USB 2.0 以及 eUSB2 LS、FS 和 HS 物理层兼容
- 模拟开关可支持大多数高达 3.3V 和 3Gbps 的 CMOS 或差分信号
- 数据引脚可承受 5V 电压
- $V_{I/O}$ = 0.2V 时，RON 低至 3Ω
- 高 -3dB 带宽为 3.3GHz
- 非常适合 240MHz 下的 USB 2.0 或 eUSB2 HS 信号：
  - 插入损耗 = -0.4dB
  - 回损 = -22dB
  - 关断隔离/串扰 = –32dB
- 超低的垂直和水平 USB 2.0 HS 眼图衰减
- 3.3V 电源电压
- 1.8V 或 3.3V 控制逻辑输入
- 工业级工作温度范围：-40°C 至 125°C
- 小型 10 引脚 1.4mm × 1.8mm UQFN 封装
- 具有多个源的引脚对引脚和 BOM 对 BOM

2 应用

- PC 和笔记本电脑
- 游戏、电视、家庭影院和娱乐系统
- 数据中心和企业级计算
- 医疗应用
- 测试和测量
- 工厂自动化和控制
- 手机和平板电脑

3 说明

TMUXHS221 是一款针对 USB 2.0 以及 eUSB2 LS、FS 和 HS 信号传输进行优化的高速双向 2:1/1:2 多路复用器/多路信号分离器。TMUXHS221 是一款适用于诸多数据速率高达 3Gbps 的高速接口的模拟无源开关。TMUXHS221 支持电压范围为 −0.3V 至 3.6V 的差分或单端 CMOS 信号传输。

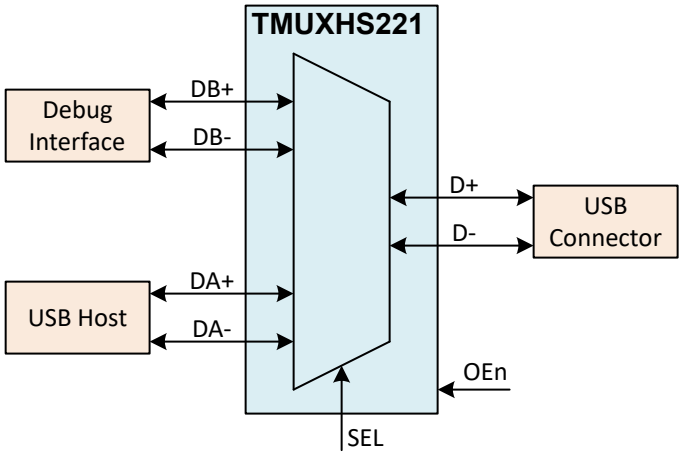
TMUXHS221 的出色高速性能可将 USB 2.0 或 eUSB2 HS 信号眼图的衰减降至超低水平，具有非常低的通道导通电阻、高带宽、低反射和低附加抖动。该器件经过优化，可实现出色的高频响应，从而更容易通过 USB 2.0 HS 电气合规性测试。该器件的数据路径也经过匹配，可实现出色的差分对内延迟性能。

TMUXHS221 的工作温度范围适用于多种严苛应用，包括工业和高可靠性用例。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
TMUXHS221	NKG（UQFN，10）	1.40mm × 1.80mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



应用用例

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (August 2022) to Revision A (November 2022)	Page
• 将数据表的状态从*预告信息*更改为*量产数据*	1

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5 Pin Configuration and Functions

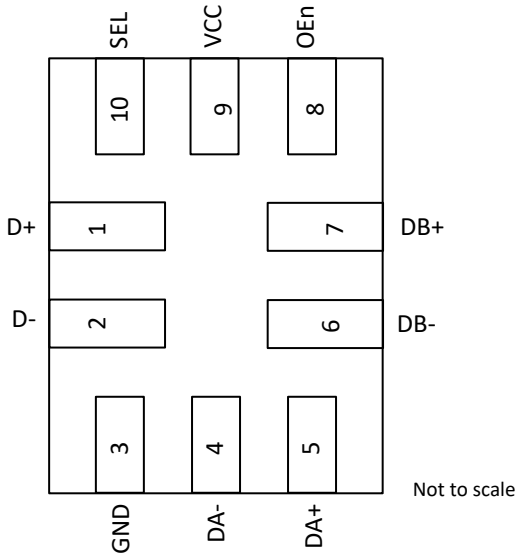


图 5-1. TMUXHS221 NKG Package, 10-Pin UQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
D+	1	I/O	Data signals Common Port, positive
D-	2	I/O	Data signals Common Port, negative
DA+	5	I/O	Data signals Port A, positive
DA-	4	I/O	Data signals Port A, negative
DB+	7	I/O	Data signals Port B, positive
DB-	6	I/O	Data signals Port B, negative
SEL	10	IN	Switch control configuration signal as provided in 表 7-1.
OEn	8	IN	
VCC	9	P	3.3 V power supply
GND	3	G	Ground

(1) IN = input, I/O = input or output, P = power, G = ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{CC-ABSMAX}$	Supply voltage		-0.5	4.0	V
$V_{I/O-ABSMAX}$	Voltage	Data pins	-0.5	5.5	V
$V_{IN-ABSMAX}$	Voltage	Control pins	-0.5	4.0	V
$I_{I/O-ABSMAX}$	ON-state switch current	Data pins		100	mA
$T_{J-ABSMAX}$	Junction temperature		-40	125	°C
T_{STG}	Storage temperature		-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±5000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
VCC	Supply voltage	DC plus AC power should not exceed these limits	3.0	3.3	3.6	V
VCC_{RAMP}	Supply voltage ramp time		0.1		100	ms
$V_{I/O}$	Voltage range for data signals ($V_{I/O}$)	D, DA, DB	-0.3		3.6	V
T_A	Operating free-air/ambient temperature		-40		125	°C
T_J	Device junction temperature		-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMUXHS221 NKG (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance - High K	225.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	147.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	147.1	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package ThermalMetrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	OEn = L		11	30	µA
I_{STDN}	Device shutdown current	OEn = H		1.3	4	µA
C_{ON}	Output ON capacitance to GND	OEn = L		1.7		pF
R_{ON}	Channel ON resistance	$V_{I/O}$ =0 V , I_O = – 8 mA		3	5.4	Ω
		$V_{I/O}$ = 2.4 V, I_O = – 8 mA		3.9	8	Ω
$R_{ON,FLAT}$	Channel ON resistance flatness defined as difference of R_{ON} over input voltage range	$V_{I/O}$ = 0 V and $V_{I/O}$ = 2.4 V; I_O = – 8 mA		1		Ω
ΔR_{ON}	On-resistance match between pairs for the same channel at same $V_{I/O}$, VCC and T_A,	$V_{I/O}$ = 0 V; I_O = – 8 mA			0.5	Ω
		$V_{I/O}$ = 2.4 V; I_O = – 8 mA			0.5	Ω
V_{IH}	Input high voltage, control pins (OEn, SEL)		1.4		3.6	V
VIL	Input low voltage, control pins (OEn, SEL)		-0.3		0.4	
I_{IH}	Input high current, control pins (OEn, SEL)	V_{IN} = 3.6 V			1	µA
I_{IL}	Input low current, control pins (OEn, SEL)	V_{IN} = 0 V			0.2	µA
$I_{I/O,H}$	Input high current, data pins (Dx, DAx, DBx)	$V_{I/O}$ = 3.6 V			2	µA
$I_{I/O,L}$	Input low current, data pins (Dx, DAx, DBx)	$V_{I/O}$ = 0 V			0.2	µA
$I_{HIZ,I/O}$	Leakage current through turned off switch	OEn = H; $V_{I/O}$ = 3.6 V			2	µA
$I_{OFF,IN}$	Failsafe leakage current for control pins (IN)	VCC = 0 V, V_{IN} = 3.6 V			10	µA
$I_{OFF,I/O}$	Failsafe leakage current for data pins (I/O)	VCC = 0 V, $V_{I/O}$ = 3.6 V			10	µA

6.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
BW	– 3-dB bandwidth	Relative to DC		3.3		GHz
I_L	Differential insertion loss	f = 10 MHz		-0.3		dB
		f = 240 MHz		-0.4		
R_L	Differential return loss	f = 10 MHz		-32		dB
		f = 240 MHz		-22		
O_{IRR}	Differential OFF isolation (D to DA/DB)	f = 10 MHz		-56		dB
		f = 240 MHz		-32		
XT	Differential cross-talk (DA to DB or DB to DA)	f = 10 MHz		-64		dB
		f = 240 MHz		-32		dB

6.7 Switching Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay			60	80	ps
t_{SW}	Switching time CTRL-to-Switch ON (SEL toggles in between H, L)	R_L = 50 Ω, C_L = 10 pF			1	µs
t_{OFF}	Time required for device ON-to-OFF transition (OEn = L to H)	R_L = 50 Ω, C_L = 10 pF			0.5	µs
t_{ON}	Time required for device OFF-to-ON transition (OEn = H to L)	R_L = 50 Ω, C_L = 10 pF			16	µs
t_{SK_INTRA}	Intra-pair output skew between positive and negative for same differential channel	For Dx to DAx or DBx channels		2	10	ps
t_{SK_INTER}	Inter-pair output skew between channels	For Dx to DAx or DBx channels		2	10	ps

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6.8 Typical Characteristics – S-Parameters

图 6-1 and 图 6-2 show differential insertion loss and return loss repectively for a typical TMUXHS221 channel. The excellent high speed performance at 240 MHz results in minimal attenuation to the USB 2.0 or eUSB2 HS signal eye diagrams. Note: measurements are performed in TI evaluation board with board and equipment parasitics calibrated out.

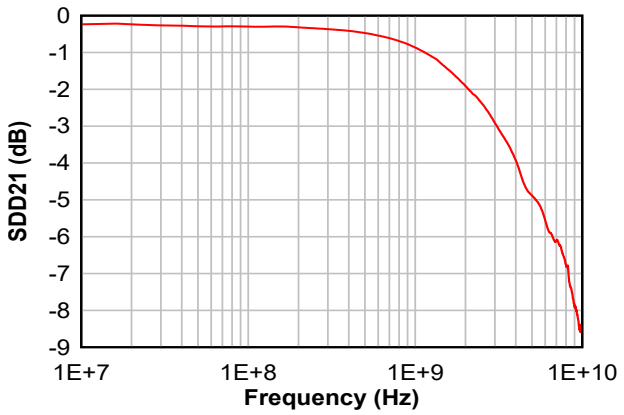


图 6-1. Typical Differential Insertion Loss vs Frequency

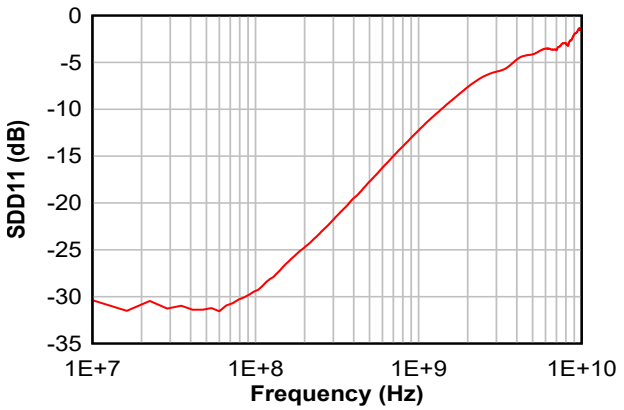


图 6-2. Typical Differential Return Loss vs Frequency

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6.9 Typical Characteristics – Eye Diagrams

图 6-3 and 图 6-4 show a side by side comparison of 480 Mbps USB 2.0 HS signals through calibration traces (without the device) and a typical TMUXHS221 channel. Attenuation of the vertical and horizonal eye opening through the device is minimal. The mux device also adds a very negligble amount of jitter to the signals.

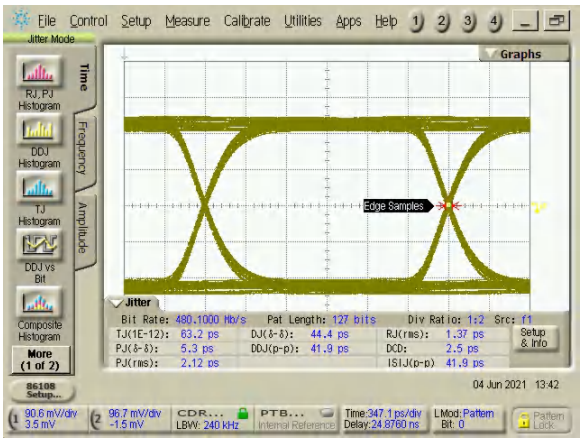


图 6-3. Through Calibration Traces at 480 Mbps

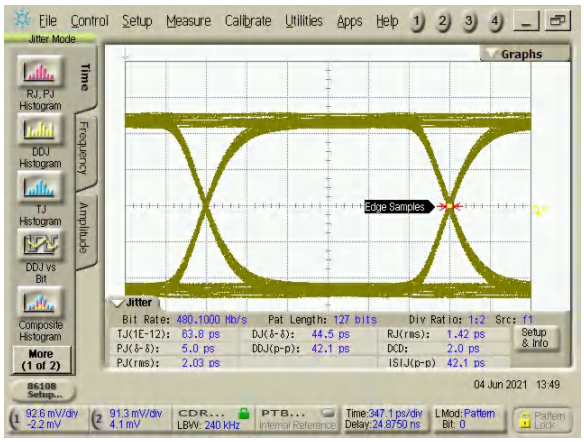


图 6-4. Through a Typical TMUXHS221 Channel at 480 Mbps

图 6-5 and 图 6-6 show a side by side eye diagram comparison at 3 Gbps signals through calibration traces (without the device) and a typical TMUXHS221 channel. Attenuation of the vertical and horizonal eye opening through the device is minimal. The mux device adds only a small amount of jitter at 3 Gbps.

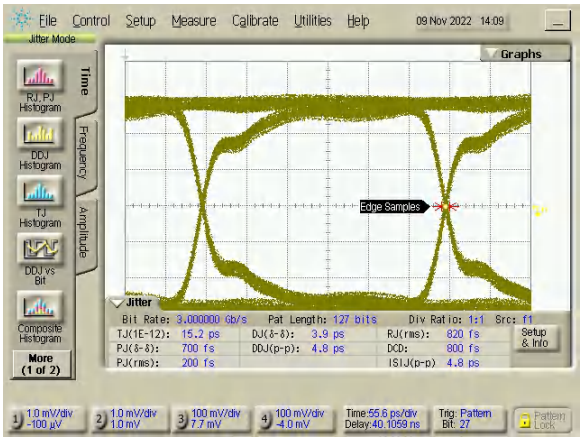


图 6-5. Through Calibration Traces at 3 Gbps

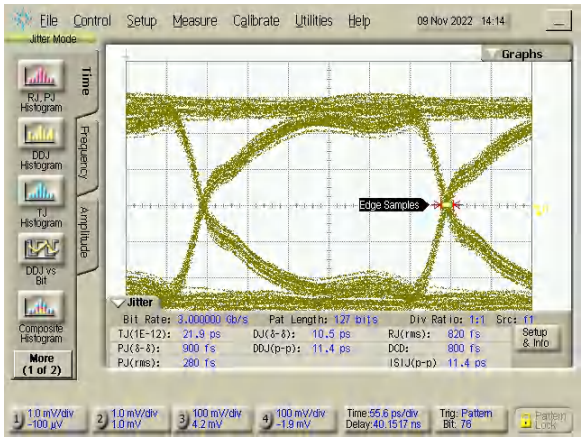


图 6-6. Through a Typical TMUXHS221 Channel at 3 Gbps

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6.10 Typical Characteristics – R_{ON}

图 6-7, 图 6-8, and 图 6-9 show switch ON resistance R_{ON} versus common mode voltage VCM, supply voltage VCC, and ambient temperature respectively. All curves are at nominal PVT conditions unless specified.

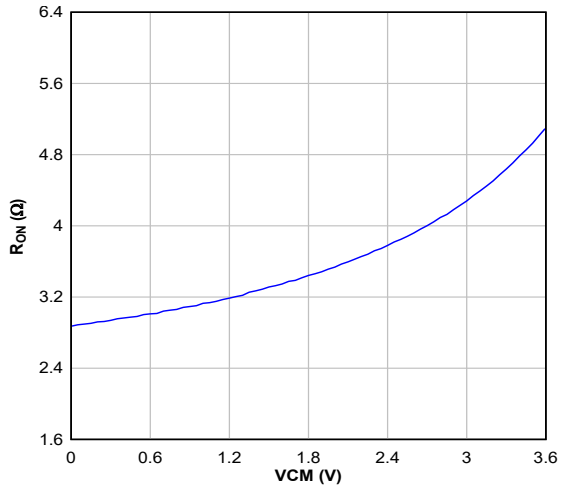


图 6-7. R_{ON} vs Common Mode Voltage VCM

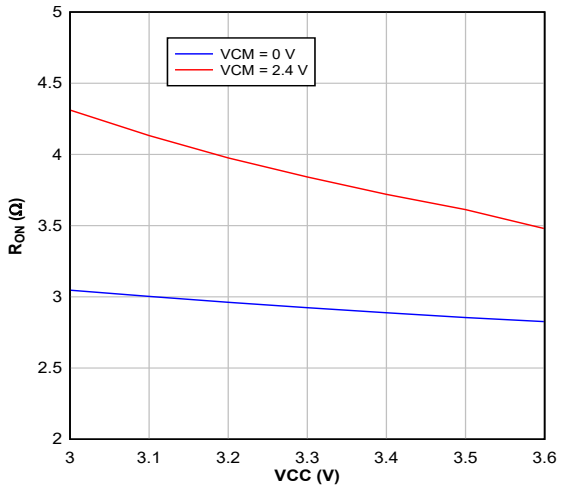


图 6-8. R_{ON} vs Supply Voltage VCC

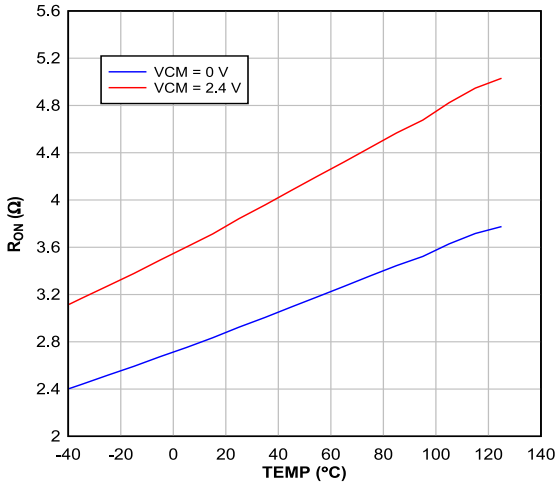


图 6-9. R_{ON} vs Ambient Temperature

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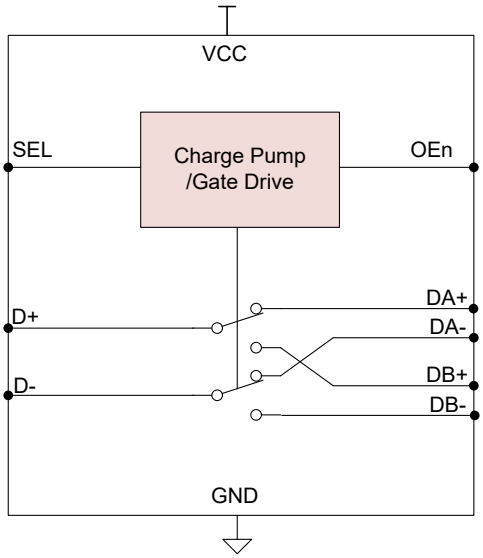
7 Detailed Description

7.1 Overview

The TMUXHS221 is an analog passive mux with 2:1/1:2 multiplexer/demultiplexer that can work for any low-speed, high-speed, differential or single ended signals. The signals must be within the allowable voltage range of −0.3 to 3.6 V. The device is optimized for eUSB2 and USB 2.0 LS, FS, and HS signaling.

Excellent dynamic characteristics of the device allow high speed switching with minimal attenuation to the signal eye diagram with very little added jitter. While the device is recommended for the interfaces up to 3 Gbps, actual data rate where the device can be used highly depends on the electrical channels. For low loss channels where adequate margin is maintained, the device can potentially be used for higher data rates.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Enable and Power Savings

The TMUXHS221 has two power modes: Active or Normal operating mode and Standby or Shutdown mode. During Standby mode, the device consumes very-little current to achieve ultra low power in systems where saving power is critical. To enter Standby mode, OEn must be pulled high.

7.3.2 Data Line Biasing

The TMUXHS221 does not contain any internal biasing. All channels of the device must be biased from either of the two sides to avoid floating channels.

7.4 Device Functional Modes

表 7-1. Mux Configuration Control Logic for TMUXHS221(1)

SEL	OEn	Mux Configuration
L	L	D to DA
H	L	D to DB
X	H	All channels are disabled and Hi-Z

(1) The TMUXHS221 can tolerate polarity inversions for differential signals. Ensure that the polarity consistency is maintained for all differential pairs.

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8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TMUXHS221 is an analog high-speed mux/demux that can be used for routing differential as well as single ended CMOS signals through it. The device can be used for many high speed and low speed interfaces up to 3 Gbps including the following:

- Universal Serial Bus (USB) 2.0 HS, FS, and LS
- Embedded Universal Serial Bus (eUSB) 2.0 HS, FS, and LS
- I^2C
- System Management Bus (SMBus™)
- Universal Asynchronous Receiver-Transmitter (UART™)
- Debug interface signals
- Mipi® Camera Serial Interface (CSI-2), Display Serial Interface (DSI)
- PCIe® clock
- DisplayPort™ Auxiliary and Hot Plug Detect Signals
- USB-C™ SBU signals
- Low Voltage Differential Signalling (LVDS)

An available GPIO pin of a controller or hard tie to voltage level H or L can easily control the mux or demux selection pin (SEL) of the device as an application requires.

Many interfaces require AC coupling capacitors between the transmitter and receiver. The 0201 or 0402 capacitors are the preferred option, but other capacitors can also be used depending on interface speed and signal integrity needs. If AC coupling capacitors are used on both sides of the TMUXHS221, then ensure the device is biased from either side, as there is no internal biasing to the device.

8.2 Typical Applications

8.2.1 Routing Debug Signals to USB Port

Many electronic end-equipment such as PCs, media players, point of sales registers, printers, cameras, headphones, smartphones, tablets, and so forth use USB ports (such as USB Type-A, USB Type-B, or USB Type-C™) for in-field or factory debug interface. In such use cases debug signals are routed to USB 2.0 pins of a USB port through a mux or demux device. TMUXHS221 is a good fit for such use cases with its flexible data handling capability. TMUXHS221 virtually can handle any debug interface signals as long as they are limited to −0.3 V (minimum) to 3.6 V (maximum). The device also provides very low attenuation to both USB 2.0 and debug signals with its very low channel ON resistance, high bandwidth, and low reflection.

图 8-1 shows a system implementation where USB 2.0 signals are multiplexed with debug interface signals into DP/DM wires of a USB port.

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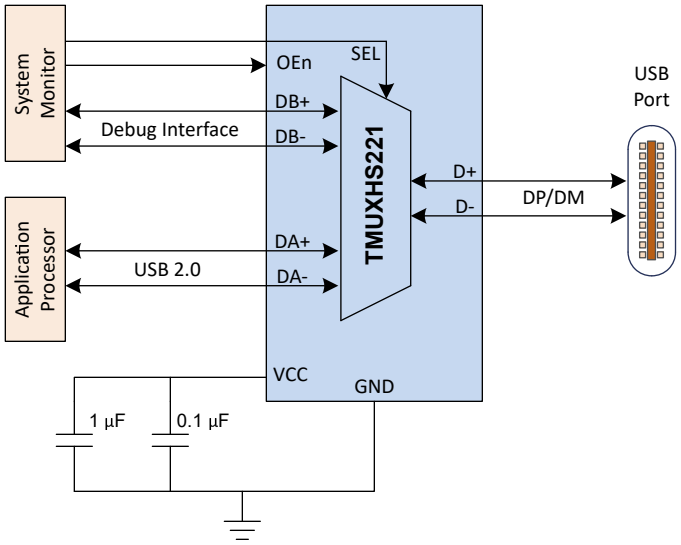


图 8-1. Routing Debug Signals to USB Port

8.2.1.1 Design Requirements

表 8-1 provides various parameters and their expected values to implement the routing debug signals into the USB port. Note that the recommendation is for illustration purpose only.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
DA+, DA-, DB+, and DB−	Direct connect to processors, −0.3 – 3.6 V
SEL/OEn pin maximum voltage for low	0.4 V
SEL/OEn pin minimum voltage for high	1.4 V
Decoupling capacitor for VCC	0.1 µF and 1 µF

8.2.1.2 Detailed Design Procedure

The TMUXHS221 is a high-speed passive switch device that can behave as a mux or demux. Signal integrity is important because as a passive switch, the device provides no signal conditioning capability. The TMUXHS221 has an excellent electrical performance with very low channel ON resistance, high bandwidth, low reflection, and low added jitter for both debug signals and USB 2.0 signals.

- Determine the loss profile between circuits that are to be muxed or demuxed.
- Provide clean impedance and electrical length matched board traces.
- Provide a control signal for the SEL and OEn pins.
- Provide good ground connection to the board ground plane.
- See the application schematics for the recommended decouple capacitors from VCC pins to ground.

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8.2.1.3 Application Curves

图 8-2 and 图 8-3 show eye diagrams for USB 2.0 signals through calibration traces (without device) and TMUXHS221 channel. A combination of very low channel ON resistance, high bandwidth, very low reflection (retun loss), and low added jitter from the device allows 480 MBps USB 2.0 HS signals to stay almost unattenuated. Many system platforms struggle to pass USB 2.0 compliance due to high loss. TMUXHS221 allows insertion of an analog mux device in the signal path without creating any additional signal integrity challenge.

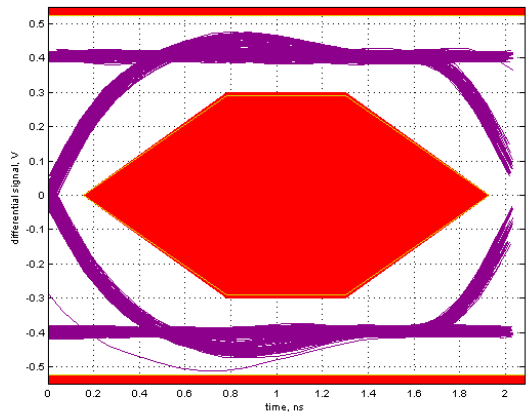


图 8-2. USB 2.0 HS Compliance Eye in TI Evaluation Board – Through Calibration Traces

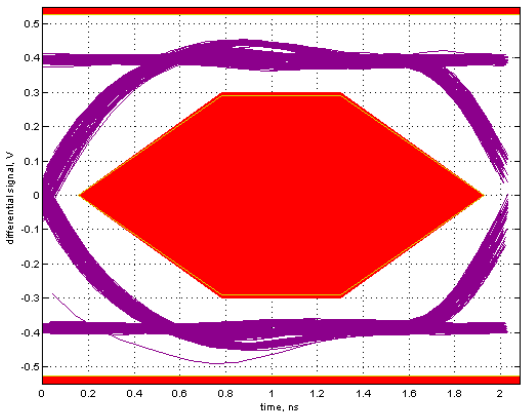


图 8-3. USB 2.0 HS Compliance Eye in TI Evaluation Board – Through TMUXHS221 Channel

8.3 Systems Examples

8.3.1 PCIe Clock Muxing

图 8-4 shows an application where TMUXHS221 is used to switch the PCIe clock. The device is measured in a TI evaluation board with an available clock source to show an added jitter less than 10 fs for all NOISE_FOLD and PCIe 5.0 CK filter versions, which is well below PCIe 5.0 clock specifications.

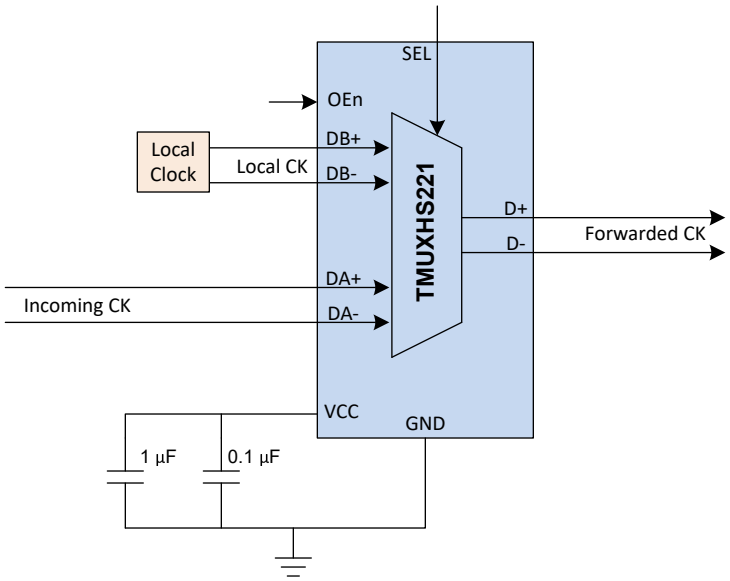


图 8-4. PCIe Clock Muxing

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8.3.2 USB-C SBU Muxing

图 8-5 shows an application block diagram that implements SBU cross-muxing in a USB Type-C interface for implementing DisplayPort (DP) Alternate mode using the TMUXHS221. Note that the device has adequate bandwidth to support fast Auxiliary (AUX) signals. It is also capable of handling asymetric biasing for DP AUX signals.

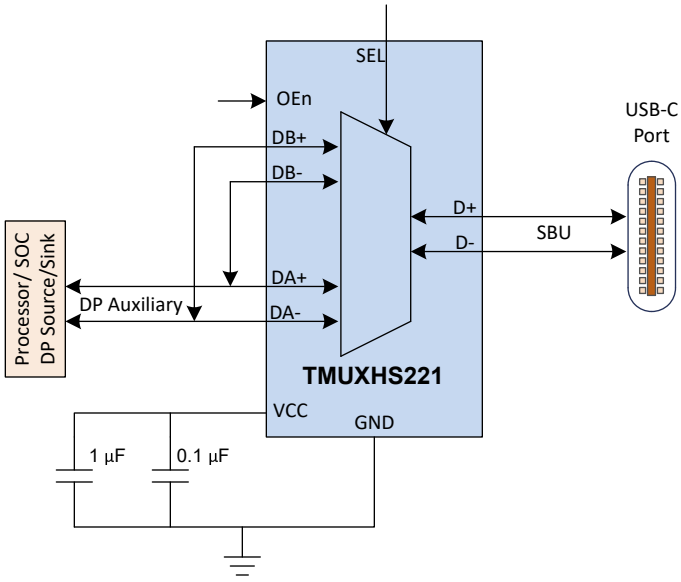


图 8-5. USB Type-C SBU Signals Muxing

8.3.3 Switching USB Port

图 8-6 shows an application block diagram where TMUXHS221 is used to switch the USB port in between a handheld portable device and its connected dock.

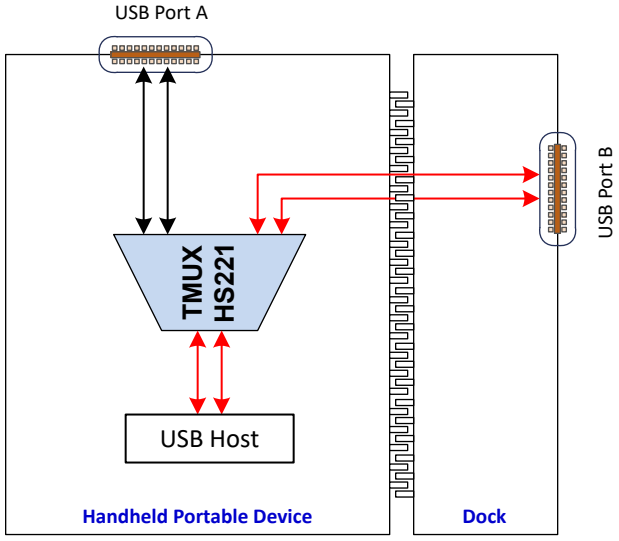


图 8-6. Switching USB Port

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9 Power Supply Recommendations

The TMUXHS221 does not require a power supply sequence. However, TI recommends that the device is enabled after VCC is stable and in specification. TI also recommends to place ample decoupling capacitors at the device VCC near the pin.

10 Layout

10.1 Layout Guidelines

Place supply bypass capacitors as close to the VCC pin as possible. Avoid placing the bypass capacitors near the D+/D – traces. The high-speed D+/D – traces should always be matched and must be no more than 4 inches, otherwise the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In the layout, the impedance of D+ and D – traces should match the cable characteristic differential impedance for optimal performance. Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC's that use or duplicate clock signals. Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm. Route all high-speed USB signal traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch, commonly found with plane split.

For high speed layout guidelines, refer to *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs* application note.

10.2 Layout Example

图 10-1 shows TMUXHS221 layout example.

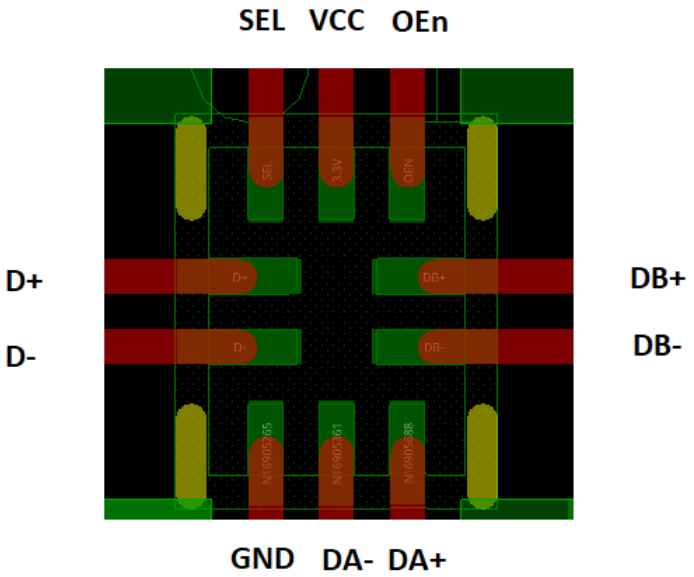


图 10-1. TMUXHS221 Layout Example

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11 Device and Documentation Support

11.1 Related Documentation

For related documenattion, see the following:

- Texas Instruments, *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs* application note

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要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUXHS221NKGR	Active	Production	UQFN (NKG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	21
TMUXHS221NKGR.A	Active	Production	UQFN (NKG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	21
TMUXHS221NKGT	Active	Production	UQFN (NKG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	21
TMUXHS221NKGT.A	Active	Production	UQFN (NKG) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	21

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

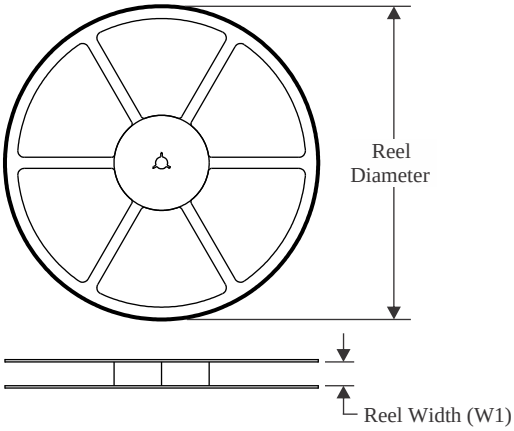
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

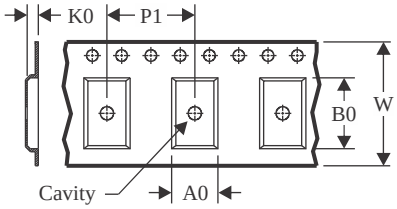
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

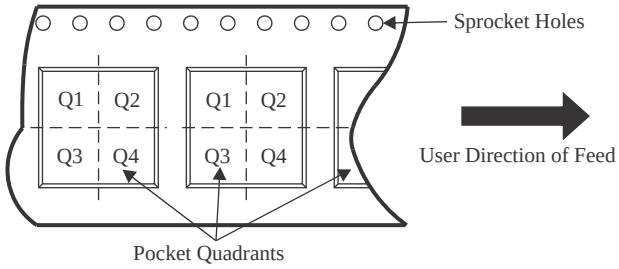


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

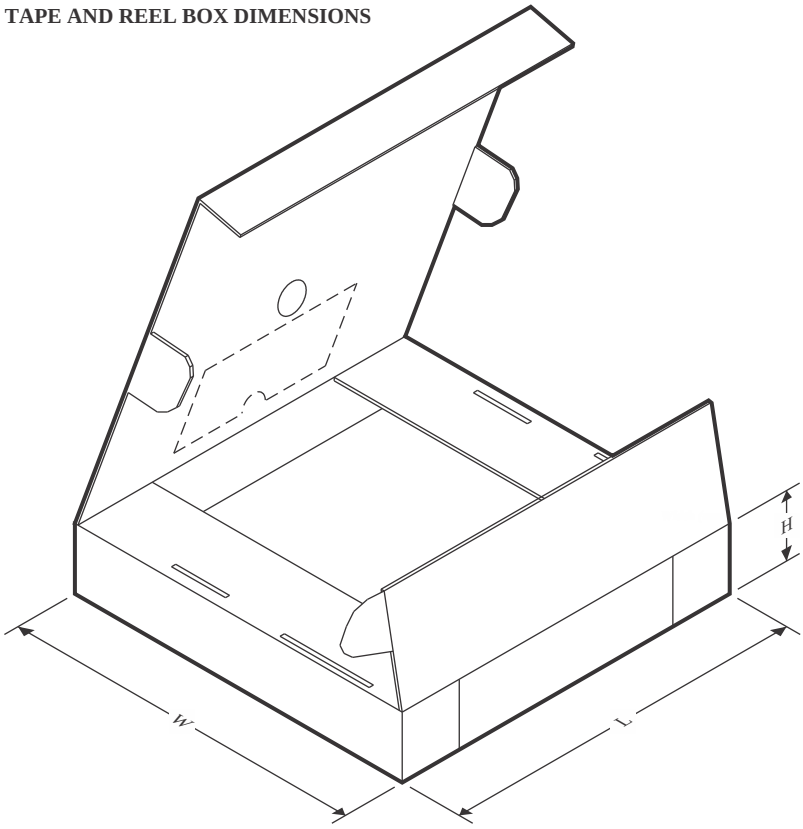
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUXHS221NKGR	UQFN	NKG	10	3000	180.0	8.4	1.6	2.0	0.7	4.0	8.0	Q1
TMUXHS221NKGT	UQFN	NKG	10	250	180.0	8.4	1.6	2.0	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

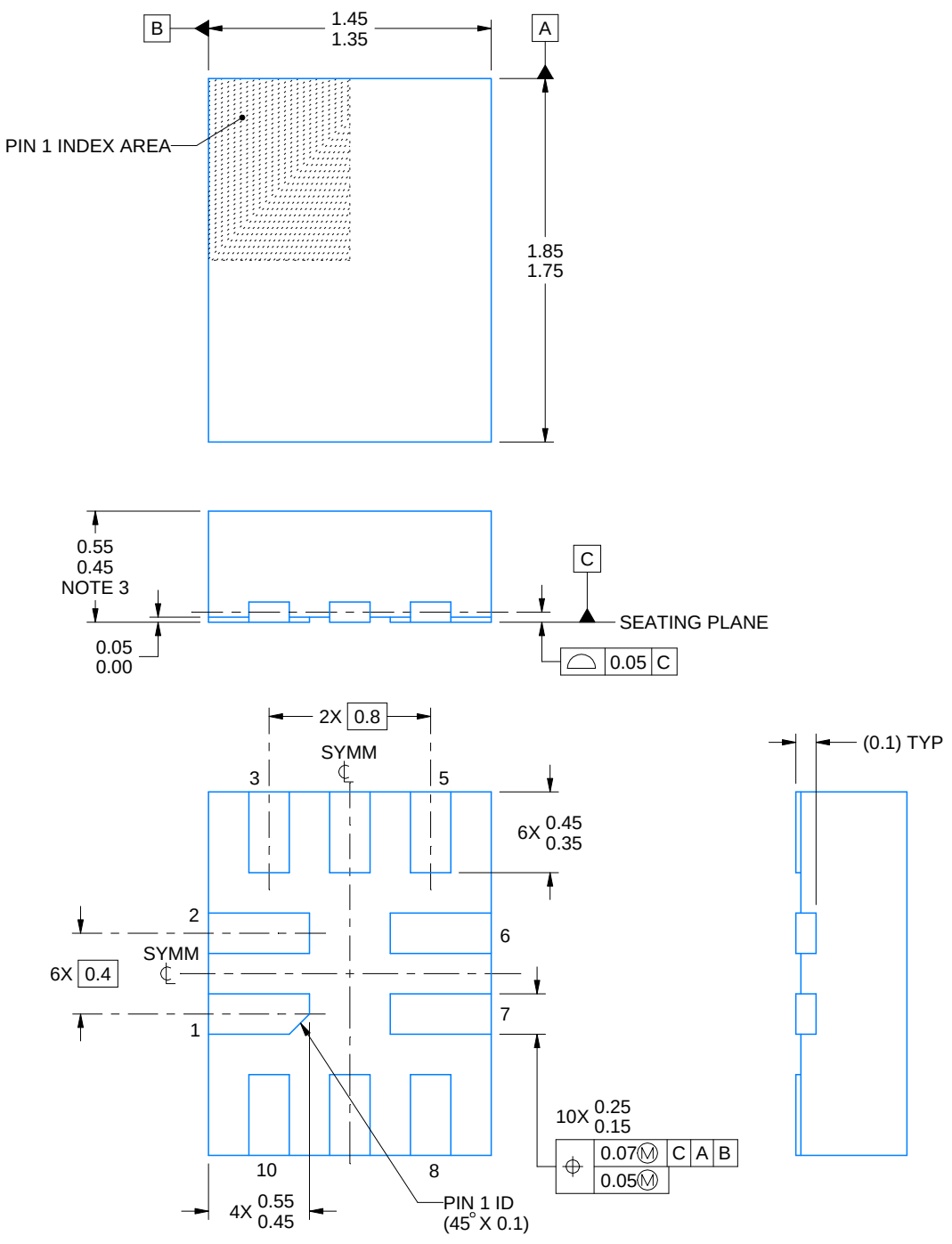
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUXHS221NKGR	UQFN	NKG	10	3000	210.0	185.0	35.0
TMUXHS221NKGT	UQFN	NKG	10	250	210.0	185.0	35.0

PACKAGE OUTLINE

NKG0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

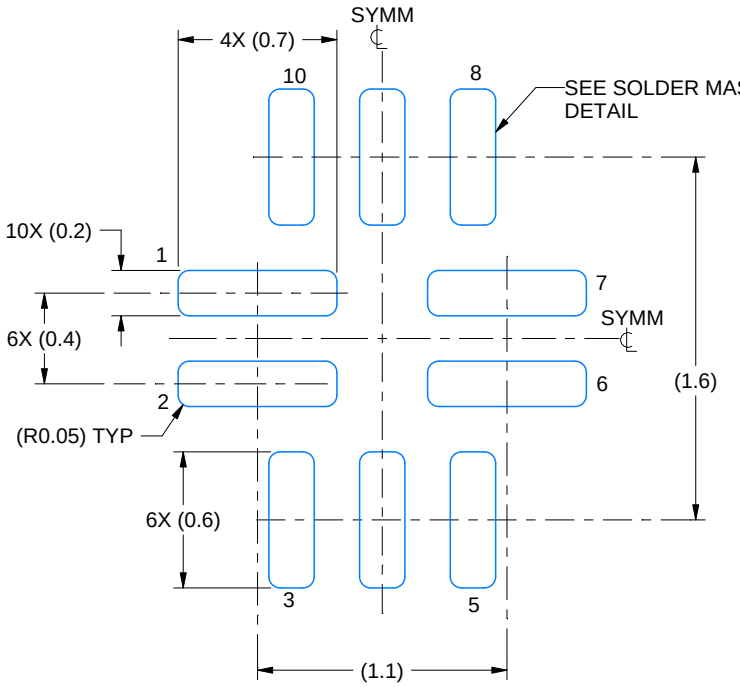
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.

EXAMPLE BOARD LAYOUT

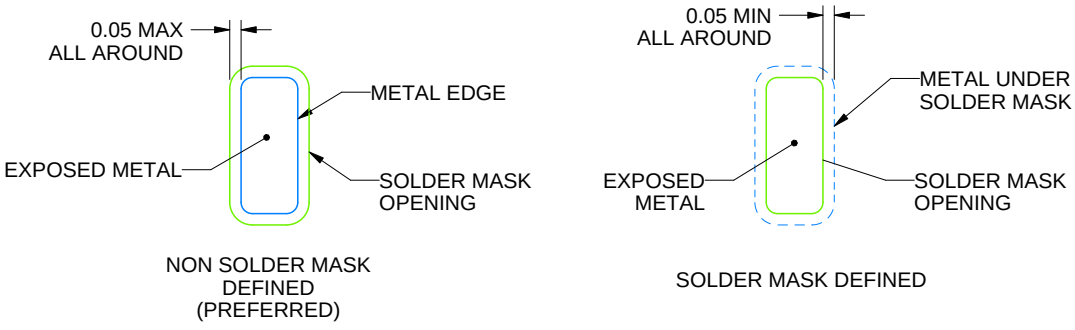
NKG0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

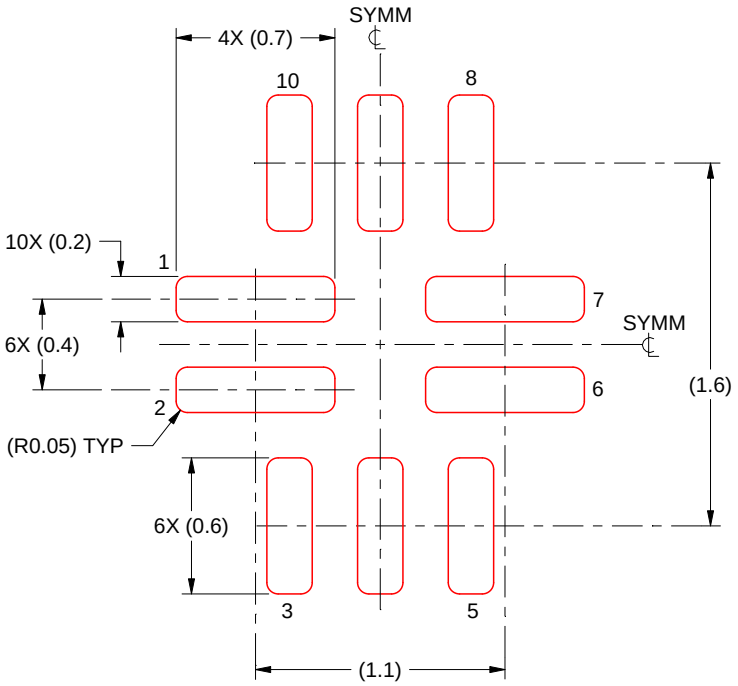


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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