TMUX113x 5V、低漏电流、2:1 (SPDT)、3 或 4 通道精密开关

1 特性

- 单电源电压范围：1.08V 至 5.5V
- 双电源电压范围：±2.75V
- 低漏电流：3pA
- 低电荷注入：-1pC
- 低导通电阻：2Ω
- 工作温度范围：-40°C 至 +125°C
- 兼容 1.8V 逻辑电平
- 失效防护逻辑
- 轨到轨运行
- 双向信号路径
- 先断后合开关
- ESD 保护 HBM：2000V

2 应用

- 现场发送器
- 可编程逻辑控制器 (PLC)
- 工厂自动化和控制
- 超声波扫描仪
- 患者监护和诊断
- 心电图 (ECG)
- 数据采集系统 (DAQ)
- ATE 测试设备
- 电池测试设备
- 仪表：实验、分析、便携
- 智能仪表：水表和燃气表
- 光纤网络
- 光学测试设备
- 便携式 POS
- 远程无线电单元
- 有源天线系统 (mMIMO)

3 说明

TMUX113x 器件是具有多个通道的精密互补金属氧化物半导体 (CMOS) 开关。TMUX1133 是 2:1 单极双投 (SPDT) 开关，具有三个独立控制的通道和一个 $\overline{EN}$ 引脚，用于启用或禁用全部三个开关。TMUX1134 包含四个独立控制的 SPDT 开关。1.08V 至 5.5V 或 ±2.75V 双电源的宽工作电源电压范围使其适用于从医疗设备到工业系统的各种应用。该器件可支持源极 (Sx) 和漏极 (Dx) 引脚上 V_{SS} 到 V_{DD} 范围的双向模拟和数字信号。对于单电源应用，V_{SS} 必须连接至 GND。

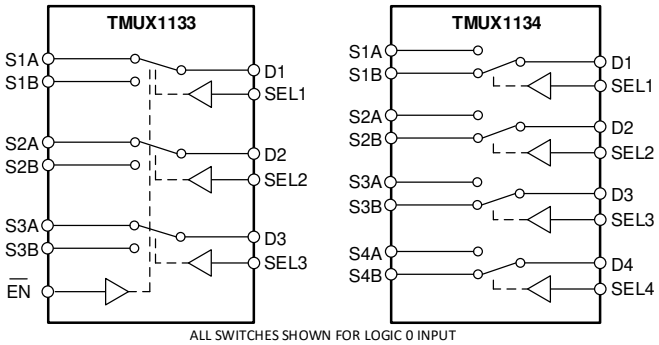
所有逻辑输入均具有兼容 1.8V 逻辑的阈值，当器件在有效电源电压范围内运行时，这些阈值可实现 TTL 和 CMOS 逻辑兼容性。失效防护逻辑电路允许先在控制引脚上施加电压，然后在电源引脚上施加电压，从而保护器件免受潜在的损害。

TMUX113x 器件是精密开关和多路复用器器件系列中的一部分。此类器件具有非常低的导通和关断漏电流以及较低的电荷注入，因此可用于高精度测量应用。8nA 的低电源
电流使其可用于便携式应用。

器件信息

器件型号	通道数(1)	封装(2)
TMUX1133	3 通道	PW（TSSOP，16）
TMUX1134	4 通道	PW（TSSOP，20）

(1) 请参阅器件比较
(2) 有关更多信息，请参阅节 12。



TMUX113x 方框图

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4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX1133	2:1 (SPDT), 3-Channel Switch
TMUX1134	2:1 (SPDT), 4-Channel Switch

5 Pin Configuration and Functions

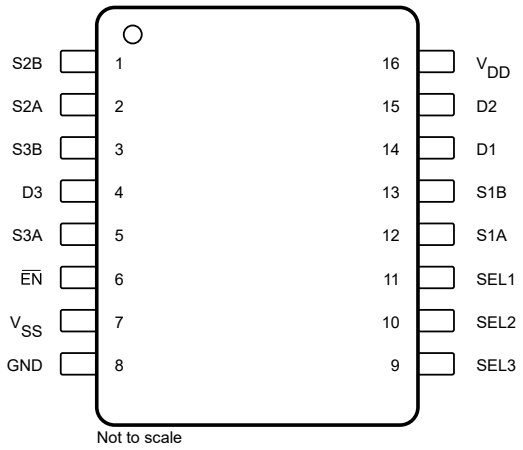


图 5-1. TMUX1133: PW Package, 16-Pin TSSOP (Top View)

表 5-1. Pin Functions TMUX1133

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
S2B	1	I/O	Source pin 2B. Can be an input or output.
S2A	2	I/O	Source pin 2A. Can be an input or output.
S3B	3	I/O	Source pin 3B. Can be an input or output.
D3	4	I/O	Drain pin 3. Can be an input or output.
S3A	5	I/O	Source pin 3A. Can be an input or output.
$\overline{EN}$	6	I	Active low logic enable. When this pin is high, all switches are turned off. When this pin is low, the SELx inputs determine switch connection as listed in 表 8-1.
V_{SS}	7	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{SS} and GND. V_{SS} must be connected to ground for single supply voltage applications.
GND	8	P	Ground (0V) reference
SEL3	9	I	Logic control select pin 3. Controls switch 3 connection as listed in 表 8-1.
SEL2	10	I	Logic control select pin 2. Controls switch 2connection as listed in 表 8-1.
SEL1	11	I	Logic control select pin 1. Controls switch 1 connection as listed in 表 8-1.
S1A	12	I/O	Source pin 1A. Can be an input or output.
S1B	13	I/O	Source pin 1B. Can be an input or output.
D1	14	I/O	Drain pin 1. Can be an input or output.
D2	15	I/O	Drain pin 2. Can be an input or output.
V_{DD}	16	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.

(1) I = input, O = output, I/O = input and output, P = power
(2) Refer to 节 8.4 for what to do with unused pins

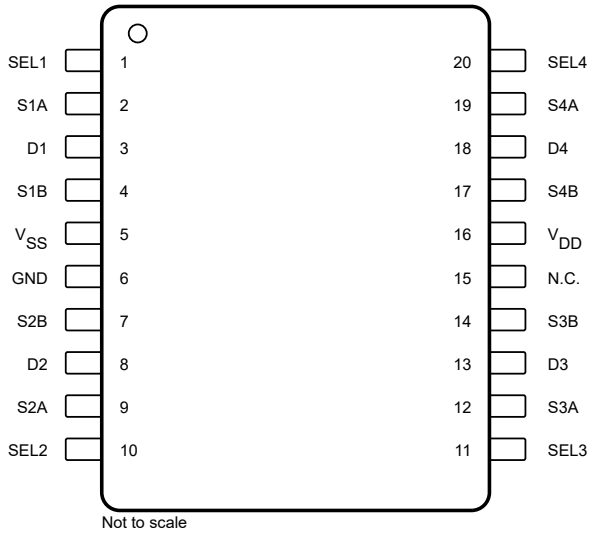


图 5-2. TMUX1134: PW Package, 20-Pin TSSOP (Top View)

表 5-2. Pin Functions TMUX1134

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
SEL1	1	I	Logic control select pin 1. Controls switch 1 connection as listed in 表 8-2.
S1A	2	I/O	Source pin 1A. Can be an input or output.
D1	3	I/O	Drain pin 1. Can be an input or output.
S1B	4	I/O	Source pin 1B. Can be an input or output.
V_{SS}	5	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{SS} and GND. V_{SS} must be connected to ground for single supply voltage applications.
GND	6	P	.Ground (0V) reference.
S2B	7	I/O	Source pin 2B. Can be an input or output.
D2	8	I/O	Drain pin 2. Can be an input or output.
S2A	9	I/O	Source pin 2A. Can be an input or output.
SEL2	10	I	Logic control select pin 2. Controls switch 2 connection as listed in 表 8-2.
SEL3	11	I	Logic control select pin 3. Controls switch 3 connection as listed in 表 8-2.
S3A	12	I/O	Source pin 3A. Can be an input or output.
D3	13	I/O	Drain pin 3. Can be an input or output.
S3B	14	I/O	Source pin 3B. Can be an input or output.
N.C.	15	Not Connected	Not Connected. Can be shorted to GND or left floating.
V_{DD}	16	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.
S4B	17	I/O	Source pin 4B. Can be an input or output.
D4	18	I/O	Drain pin 4. Can be an input or output.
S4A	19	I/O	Source pin 4A. Can be an input or output.
SEL4	20	I	Logic control select pin 4. Controls switch 4 connection as listed in 表 8-2.

(1) I = input, O = output, I/O = input and output, P = power
(2) Refer to 节 8.4 for what to do with unused pins

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
V_{DD} – V_{SS}	Supply voltage	– 0.5	6	V
V_{DD}		– 0.5	6	V
V_{SS}		– 3.0	0.3	V
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, SELx)	– 0.5	6	V
I_{SEL} or I_{EN}	Logic control input pin current ($\overline{EN}$, SELx)	– 30	30	mA
V_S or V_D	Source or drain voltage (SxA, SxB, Dx)	– 0.5	V_{DD} + 0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (SxA, SxB, Dx)	IDC ± 10 %(4)	IDC ± 10 %(4)	mA
I_S or $I_{D\ (PEAK)}$	Source and drain peak current: (1 ms period max, 10% duty cycle maximum) (Sx, SxA, SxB, D, DA, DB)	Ipeak ± 10 %(4)	Ipeak ± 10 %(4)	mA
T_{stg}	Storage temperature	– 65	150	°C
P_{tot}	Total power dissipation(5) (6)		500	mW
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Refer to Recommended Operating Conditions for IDC and IPeak ratings.
(5) For TSSOP(16)(PW) package: Ptot derates linearly above TA=89°C by 8.29mW/°C
(6) For TSSOP(20)(PW) package: Ptot derates linearly above TA=98°C by 9.78mW/°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Positive power supply voltage (single)		1.08		5.5	V
V_{SS}	Negative power supply voltage (dual)		– 2.75		0	V
V_{DD} - V_{SS}	Supply rail voltage difference		1.08		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (SxA, SxB, Dx)		V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, SELx)		0		5.5	V
T_A	Ambient temperature		– 40		125	°C
I_{DC}	Continuous current through switch	Tj = 25°C		150		mA
		Tj = 85°C		120		mA
		Tj = 125°C		60		mA
		Tj = 130°C		50		mA

6.3 Recommended Operating Conditions（续）

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
I_{peak}	Peak current through switch(1 ms period max, 10% duty cycle maximum)	Tj = 25°C		300		mA
		Tj = 85°C		300		mA
		Tj = 125°C		180		mA
		Tj = 130°C		160		mA

6.4 Thermal Information

THERMAL METRIC(1)		TMUX1133 PW (TSSOP) 16 PINS	TMUX1134 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.6	102.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.0	43.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.8	53.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.7	6.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	66.2	53.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics (V_{DD} = 5V ±10 %)

At T_A = 25°C, V_{DD} = 5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		2	4	Ω
			– 40°C to +85°C			4.5	Ω
			– 40°C to +125°C			4.9	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		0.18		Ω
			– 40°C to +85°C			0.4	Ω
			– 40°C to +125°C			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		0.85		Ω
			– 40°C to +85°C			1.6	Ω
			– 40°C to +125°C			1.6	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 5V Switch Off V_D = 4.5V / 1.5V V_S = 1.5V / 4.5V Refer to 节 7.2	25°C	– 0.08	±0.003	0.08	nA
			– 40°C to +85°C	– 0.3		0.3	nA
			– 40°C to +125°C	– 0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 5V Switch Off V_D = 4.5V / 1.5V V_S = 1.5V / 4.5V Refer to 节 7.2	25°C	– 0.1	±0.003	0.1	nA
			– 40°C to +85°C	– 0.35		0.35	nA
			– 40°C to +125°C	– 2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5V Switch On V_D = V_S = 4.5V / 1.5V Refer to 节 7.3	25°C	– 0.1	±0.003	0.1	nA
			– 40°C to +85°C	– 0.35		0.35	nA
			– 40°C to +125°C	– 2		2	nA
LOGIC INPUTS ($\overline{EN}$, SELx)							

6.5 Electrical Characteristics (V_{DD} = 5V ±10 %)（续）

At T_A = 25°C, V_{DD} = 5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
V_{IH}	Input logic high		–40°C to +125°C	1.49		5.5	V
V_{IL}	Input logic low			0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.008		µA
			–40°C to +125°C			1	µA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 3V R_L = 200Ω, C_L = 15pF Refer to 节 7.4	25°C		12		ns
			–40°C to +85°C			18	ns
			–40°C to +125°C			19	ns
t_{OPEN} (BBM)	Break before make time	V_S = 3V R_L = 200Ω, C_L = 15pF Refer to 节 7.5	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time (TMUX1133 Only)	V_S = 3V R_L = 200Ω, C_L = 15pF Refer to 节 7.6	25°C		12		ns
			–40°C to +85°C			21	ns
			–40°C to +125°C			22	ns
$t_{OFF(EN)}$	Enable turn-off time (TMUX1133 Only)	V_S = 3V R_L = 200Ω, C_L = 15pF Refer to 节 7.6	25°C		6		ns
			–40°C to +85°C			11	ns
			–40°C to +125°C			12	ns
Q_C	Charge Injection	V_S = 1V R_S = 0Ω, C_L = 1nF Refer to 节 7.7	25°C		–1		pC
O_{ISO}	Off Isolation	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to 节 7.8	25°C		–65		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to 节 7.8	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to 节 7.9	25°C		–100		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to 节 7.9	25°C		–90		dB
BW	Bandwidth	R_L = 50Ω, C_L = 5pF Refer to 节 7.10	25°C		220		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1MHz	25°C		17		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		20		pF

(1) When V_S is 4.5V, V_D is 1.5V or when V_S is 1.5V, V_D is 4.5V.

6.6 Electrical Characteristics (V_{DD} = 3.3V ±10 %)

At T_A = 25°C, V_{DD} = 3.3V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		3.7	8.8	Ω
			– 40°C to +85°C			9.5	Ω
			– 40°C to +125°C			9.8	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		0.13		Ω
			– 40°C to +85°C			0.4	Ω
			– 40°C to +125°C			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		1.9		Ω
			– 40°C to +85°C		2		Ω
			– 40°C to +125°C		2.2		Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 3.3V Switch Off V_D = 3V / 1V V_S = 1V / 3V Refer to 节 7.2	25°C	– 0.05	±0.001	0.05	nA
			– 40°C to +85°C	– 0.1		0.1	nA
			– 40°C to +125°C	– 0.7		0.7	nA
$I_{D(OFF)}$	Drain off leakage current(1) (TMUX1133 Only)	V_{DD} = 3.3V Switch Off V_D = 3V / 1V V_S = 1V / 3V Refer to 节 7.2	25°C	– 0.1	±0.005	0.1	nA
			– 40°C to +85°C	– 0.35		0.35	nA
			– 40°C to +125°C	– 2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 3.3V Switch On V_D = V_S = 3V / 1V Refer to 节 7.3	25°C	– 0.1	±0.005	0.1	nA
			– 40°C to +85°C	– 0.35		0.35	nA
			– 40°C to +125°C	– 2		2	nA
LOGIC INPUTS ($\overline{EN}$, SELx)							
V_{IH}	Input logic high		– 40°C to +125°C	1.35		5.5	V
V_{IL}	Input logic low			0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		– 40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			– 40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.006		µA
			– 40°C to +125°C			1	µA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 2V R_L = 200Ω, C_L = 15pF Refer to 节 7.4	25°C		14		ns
			– 40°C to +85°C			22	ns
			– 40°C to +125°C			22	ns
$t_{OPEN\ (BBM)}$	Break before make time	V_S = 2V R_L = 200Ω, C_L = 15pF Refer to 节 7.5	25°C		9		ns
			– 40°C to +85°C	1			ns
			– 40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time (TMUX1133 Only)	V_S = 2V R_L = 200Ω, C_L = 15pF Refer to 节 7.6	25°C		15		ns
			– 40°C to +85°C			22	ns
			– 40°C to +125°C			23	ns

6.6 Electrical Characteristics (V_{DD} = 3.3V ±10 %) （续）

At T_A = 25°C, V_{DD} = 3.3V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
$t_{OFF(EN)}$	Enable turn-off time (TMUX1133 Only)	V_S = 2V R_L = 200Ω, C_L = 15pF Refer to 节 7.6	25°C		8		ns
			–40°C to +85°C			13	ns
			–40°C to +125°C			14	ns
Q_C	Charge Injection	V_S = 1V R_S = 0Ω, C_L = 1nF Refer to 节 7.7	25°C		–1		pC
O_{ISO}	Off Isolation	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to 节 7.8	25°C		–65		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to 节 7.8	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to 节 7.9	25°C		–100		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to 节 7.9	25°C		–90		dB
BW	Bandwidth	R_L = 50Ω, C_L = 5pF Refer to 节 7.10	25°C		220		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1MHz	25°C		17		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		20		pF

(1) When V_S is 3V, V_D is 1V or when V_S is 1V, V_D is 3V.

6.7 Electrical Characteristics (V_{DD} = 2.5V ±10 %), (V_{SS} = –2.5V ±10 %)

At T_A = 25°C, V_{DD} = +2.5V, V_{SS} = –2.5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = V_{SS} to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		2	4	Ω
			–40°C to +85°C			4.5	Ω
			–40°C to +125°C			4.9	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = V_{SS} to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		0.18		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = V_{SS} to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		0.85		Ω
			–40°C to +85°C			1.6	Ω
			–40°C to +125°C			1.6	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = +2.5V, V_{SS} = –2.5V Switch Off V_D = +2V / –1V V_S = –1V / +2V Refer to 节 7.2	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA

6.7 Electrical Characteristics (V_{DD} = 2.5V ±10 %), (V_{SS} = – 2.5V ±10 %) （续）

At T_A = 25°C, V_{DD} = +2.5V, V_{SS} = – 2.5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = +2.5V, V_{SS} = – 2.5V Switch Off V_D = +2V / – 1V V_S = – 1V / +2V Refer to 节 7.2	25°C	– 0.1	±0.01	0.1	nA
			– 40°C to +85°C	– 0.35		0.35	nA
			– 40°C to +125°C	– 2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = +2.5V, V_{SS} = – 2.5V Switch On V_D = V_S = +2V / – 1V Refer to 节 7.3	25°C	– 0.1	±0.01	0.1	nA
			– 40°C to +85°C	– 0.35		0.35	nA
			– 40°C to +125°C	– 2		2	nA
LOGIC INPUTS ($\overline{EN}$, SELx)							
V_{IH}	Input logic high		– 40°C to +125°C	1.2		2.75	V
V_{IL}	Input logic low			0		0.73	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		– 40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			– 40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 2.75V	25°C		0.008		µA
			– 40°C to +125°C			1	µA
I_{SS}	V_{SS} supply current	Logic inputs = 0V or 2.75V	25°C		0.008		µA
			– 40°C to +125°C			1	µA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1.5V R_L = 200Ω, C_L = 15pF Refer to 节 7.4	25°C		12		ns
			– 40°C to +85°C			20	ns
			– 40°C to +125°C			21	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1.5V R_L = 200Ω, C_L = 15pF Refer to 节 7.5	25°C		8		ns
			– 40°C to +85°C	1			ns
			– 40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time (TMUX1133 Only)	V_S = 1.5V R_L = 200Ω, C_L = 15pF Refer to 节 7.6	25°C		12		ns
			– 40°C to +85°C			21	ns
			– 40°C to +125°C			22	ns
$t_{OFF(EN)}$	Enable turn-off time (TMUX1133 Only)	V_S = 1.5V R_L = 200Ω, C_L = 15pF Refer to 节 7.6	25°C		6		ns
			– 40°C to +85°C			14	ns
			– 40°C to +125°C			15	ns
Q_C	Charge Injection	V_S = – 1V R_S = 0Ω, C_L = 1nF Refer to 节 7.7	25°C		– 1		pC
O_{ISO}	Off Isolation	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to 节 7.8	25°C		– 65		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to 节 7.8	25°C		– 45		dB

6.7 Electrical Characteristics (V_{DD} = 2.5V ±10 %), (V_{SS} = –2.5V ±10 %) （续）

At T_A = 25°C, V_{DD} = +2.5V, V_{SS} = –2.5V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
X_{TALK}	Crosstalk	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to 节 7.9	25°C		–100		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to 节 7.9	25°C		–90		dB
BW	Bandwidth	R_L = 50Ω, C_L = 5pF Refer to 节 7.10	25°C		220		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1MHz	25°C		17		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		20		pF

(1) When V_S is positive, V_D is negative or when V_S is negative, V_D is positive.

6.8 Electrical Characteristics (V_{DD} = 1.8V ±10 %)

At T_A = 25°C, V_{DD} = 1.8V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		40		Ω
			–40°C to +85°C			80	Ω
			–40°C to +125°C			80	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.98V Switch Off V_D = 1.62V / 1V V_S = 1V / 1.62V Refer to 节 7.2	25°C	–0.05	±0.003	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.98V Switch Off V_D = 1.62V / 1V V_S = 1V / 1.62V Refer to 节 7.2	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.98V Switch On V_D = V_S = 1.62V / 1V Refer to 节 7.3	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS ($\overline{EN}$, SELx)							
V_{IH}	Input logic high		–40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low			0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			–40°C to +125°C			2	pF
POWER SUPPLY							

6.8 Electrical Characteristics (V_{DD} = 1.8V ±10 %)（续）

At T_A = 25°C, V_{DD} = 1.8V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.001		µA
			–40°C to +125°C			0.85	µA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to 节 7.4	25°C		28		ns
			–40°C to +85°C			48	ns
			–40°C to +125°C			48	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to 节 7.5	25°C		16		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time (TMUX1133 Only)	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to 节 7.6	25°C		28		ns
			–40°C to +85°C			48	ns
			–40°C to +125°C			48	ns
$t_{OFF(EN)}$	Enable turn-off time (TMUX1133 Only)	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to 节 7.6	25°C		16		ns
			–40°C to +85°C			27	ns
			–40°C to +125°C			27	ns
Q_C	Charge Injection	V_S = 1V R_S = 0Ω, C_L = 1nF Refer to 节 7.7	25°C		–1		pC
O_{ISO}	Off Isolation	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to 节 7.8	25°C		–65		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to 节 7.8	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to 节 7.9	25°C		–100		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to 节 7.9	25°C		–90		dB
BW	Bandwidth	R_L = 50Ω, C_L = 5pF Refer to 节 7.10	25°C		220		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1MHz	25°C		17		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		20		pF

(1) When V_S is 1.62V, V_D is 1V or when V_S is 1V, V_D is 1.62V.

6.9 Electrical Characteristics (V_{DD} = 1.2V ±10 %)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		70		Ω
			–40°C to +85°C			105	Ω
			–40°C to +125°C			105	Ω

6.9 Electrical Characteristics (V_{DD} = 1.2V ±10 %) （续）

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to 节 7.1	25°C		0.4		Ω
			-40°C to +85°C			1.5	Ω
			-40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.32V Switch Off V_D = 1V / 0.8V V_S = 0.8V / 1V Refer to 节 7.2	25°C	-0.05	±0.003	0.05	nA
			-40°C to +85°C	-0.1		0.1	nA
			-40°C to +125°C	-0.5		0.5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.32V Switch Off V_D = 1V / 0.8V V_S = 0.8V / 1V Refer to 节 7.2	25°C	-0.1	±0.005	0.1	nA
			-40°C to +85°C	-0.5		0.5	nA
			-40°C to +125°C	-2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.32V Switch On V_D = V_S = 1V / 0.8V Refer to 节 7.3	25°C	-0.1	±0.005	0.1	nA
			-40°C to +85°C	-0.5		0.5	nA
			-40°C to +125°C	-2		2	nA
LOGIC INPUTS ($\overline{EN}$, SELx)							
V_{IH}	Input logic high		-40°C to +125°C	0.96		5.5	V
V_{IL}	Input logic low			0		0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		-40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			-40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.001		µA
			-40°C to +125°C			0.7	µA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to 节 7.4	25°C		55		ns
			-40°C to +85°C			201	ns
			-40°C to +125°C			201	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to 节 7.5	25°C		28		ns
			-40°C to +85°C	1			ns
			-40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time (TMUX1133 Only)	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to 节 7.6	25°C		60		ns
			-40°C to +85°C			201	ns
			-40°C to +125°C			201	ns
$t_{OFF(EN)}$	Enable turn-off time (TMUX1133 Only)	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to 节 7.6	25°C		45		ns
			-40°C to +85°C			150	ns
			-40°C to +125°C			150	ns
Q_C	Charge Injection	V_S = 1V R_S = 0Ω, C_L = 1nF Refer to 节 7.7	25°C		-1		pC

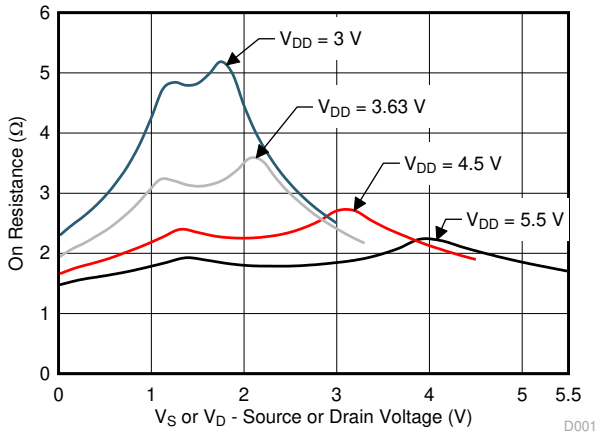
6.9 Electrical Characteristics (V_{DD} = 1.2V ±10 %) （续）

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
O_{ISO}	Off Isolation	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to 节 7.8	25°C		-65		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to 节 7.8	25°C		-45		dB
X_{TALK}	Crosstalk	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to 节 7.9	25°C		-100		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to 节 7.9	25°C		-90		dB
BW	Bandwidth	R_L = 50Ω, C_L = 5pF Refer to 节 7.10	25°C		220		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		6		pF
C_{DOFF}	Drain off capacitance	f = 1MHz	25°C		17		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		20		pF

(1) When V_S is 1V, V_D is 0.8V or when V_S is 0.8V, V_D is 1V.

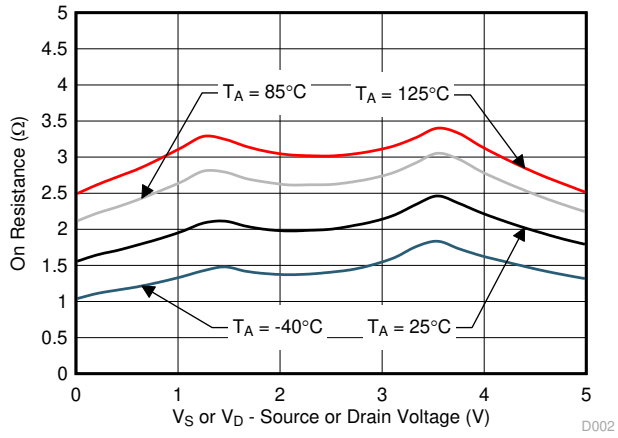
6.10 Typical Characteristics

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



T_A = 25°C

图 6-1. On-Resistance vs Source or Drain Voltage

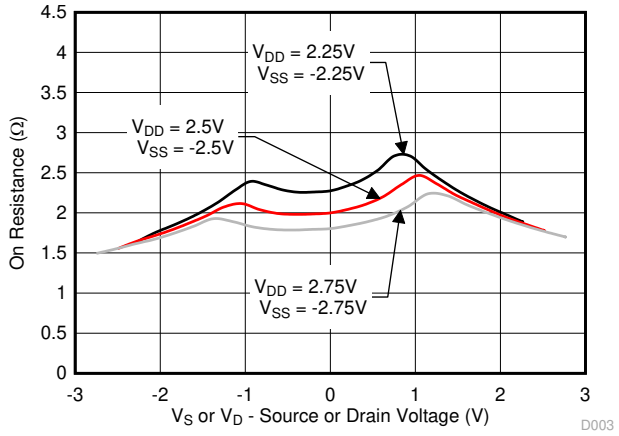


V_{DD} = 5V

图 6-2. On-Resistance vs Temperature

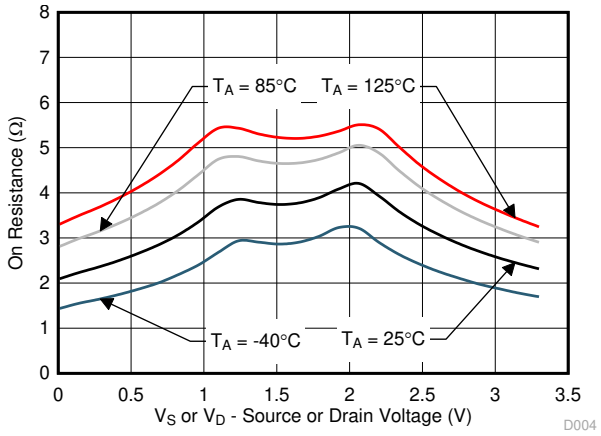
6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



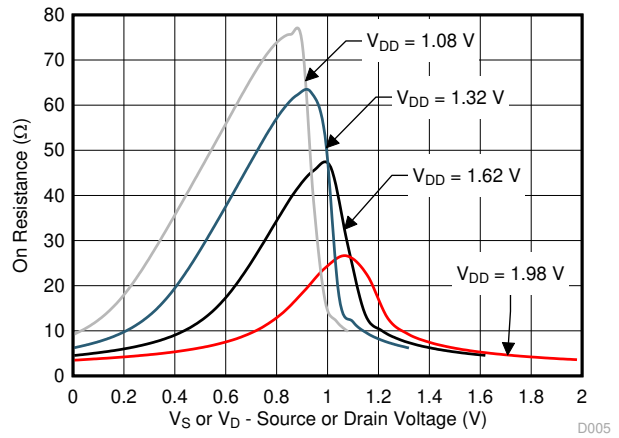
V_{DD} = ±2.5V

图 6-3. On-Resistance vs Temperature



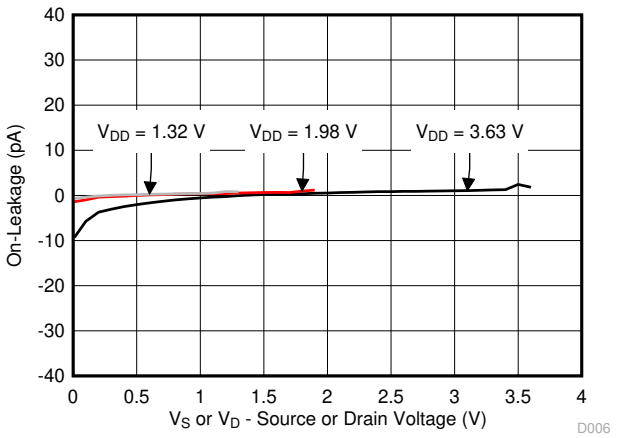
V_{DD} = 3.3V

图 6-4. On-Resistance vs Temperature



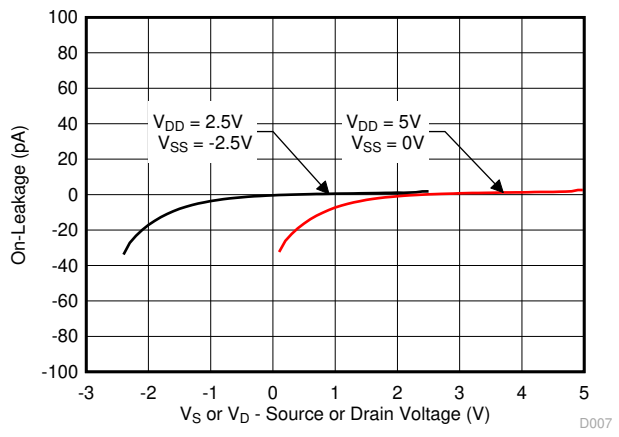
T_A = 25°C

图 6-5. On-Resistance vs Source or Drain Voltage



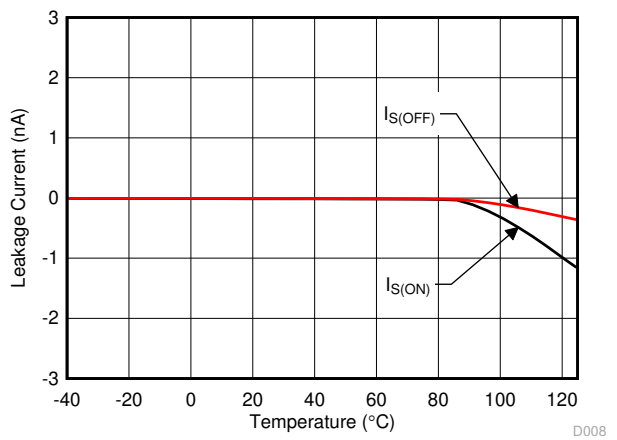
T_A = 25°C

图 6-6. On-Leakage vs Source or Drain Voltage



V_{DD} = 5V

图 6-7. On-Leakage vs Source or Drain Voltage

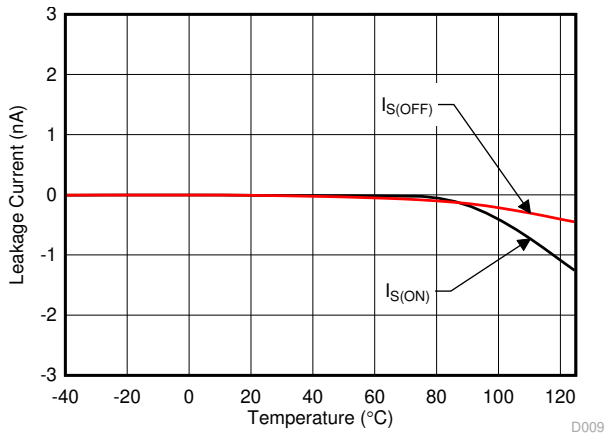


V_{DD} = 3.3V

图 6-8. Leakage Current vs Temperature

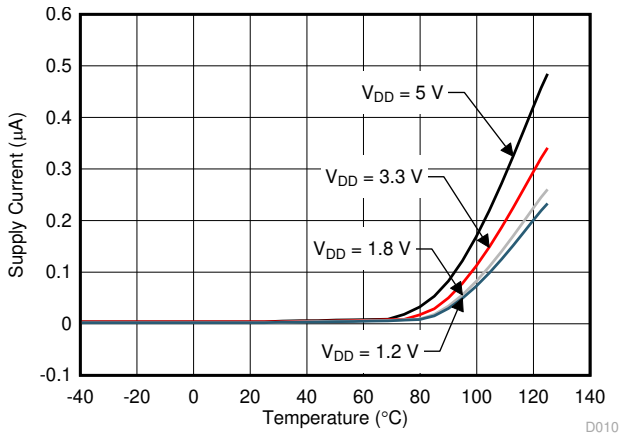
6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



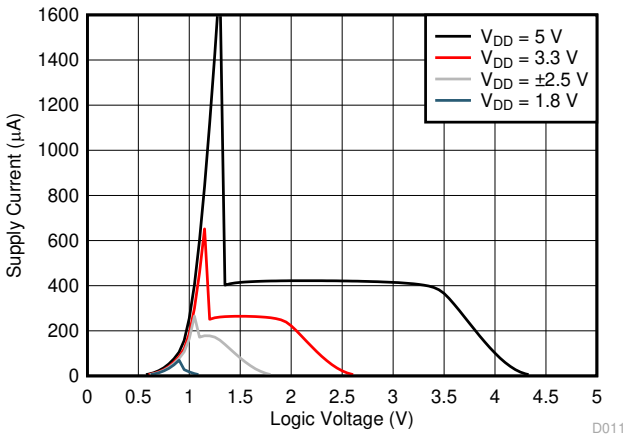
V_{DD} = 5V

图 6-9. Leakage Current vs Temperature



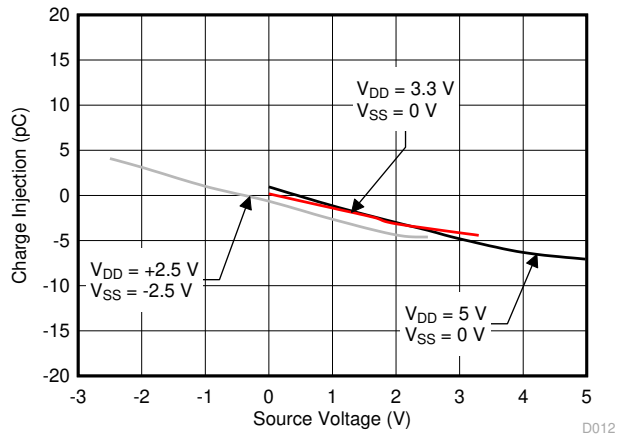
V_{SEL} = V_{DD}

图 6-10. Supply Current vs Temperature



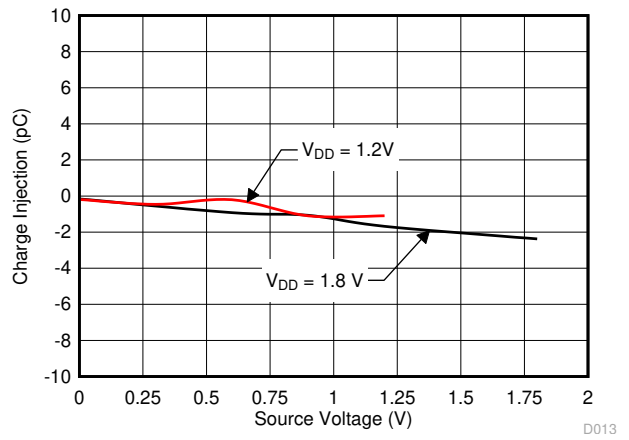
T_A = 25°C

图 6-11. Supply Current vs Logic Voltage



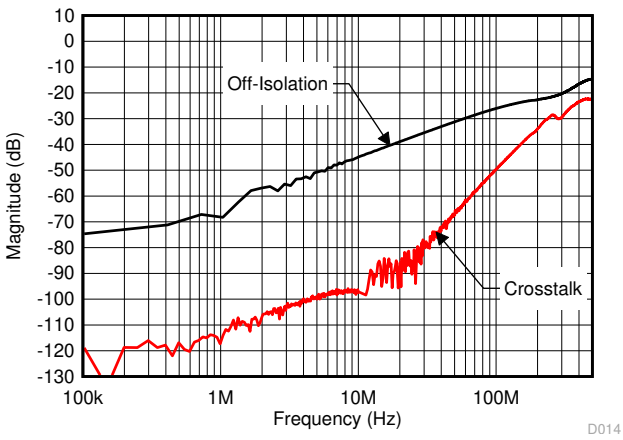
T_A = -40°C to 125°C

图 6-12. Charge Injection vs Source Voltage



T_A = -40°C to 125°C

图 6-13. Charge Injection vs Source Voltage

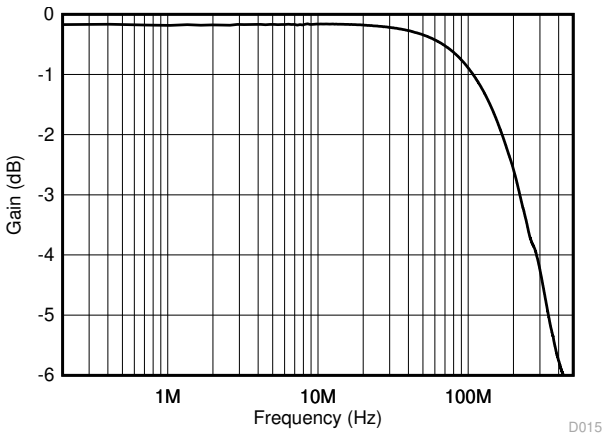


T_A = -40°C to +125°C

图 6-14. Xtalk and Off-Isolation vs Frequency

6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



T_A = -40°C to +125°C

图 6-15. On Response vs Frequency

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 图 7-1. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

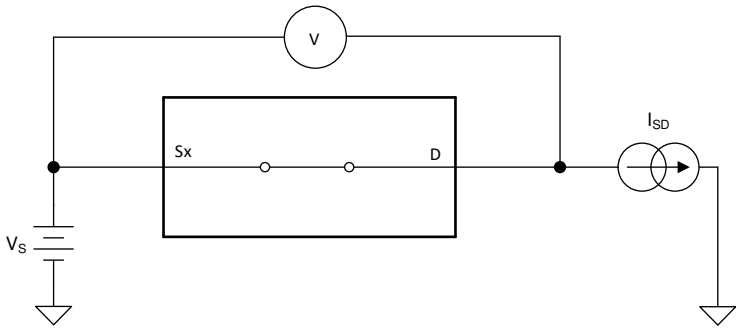


图 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 图 7-2.

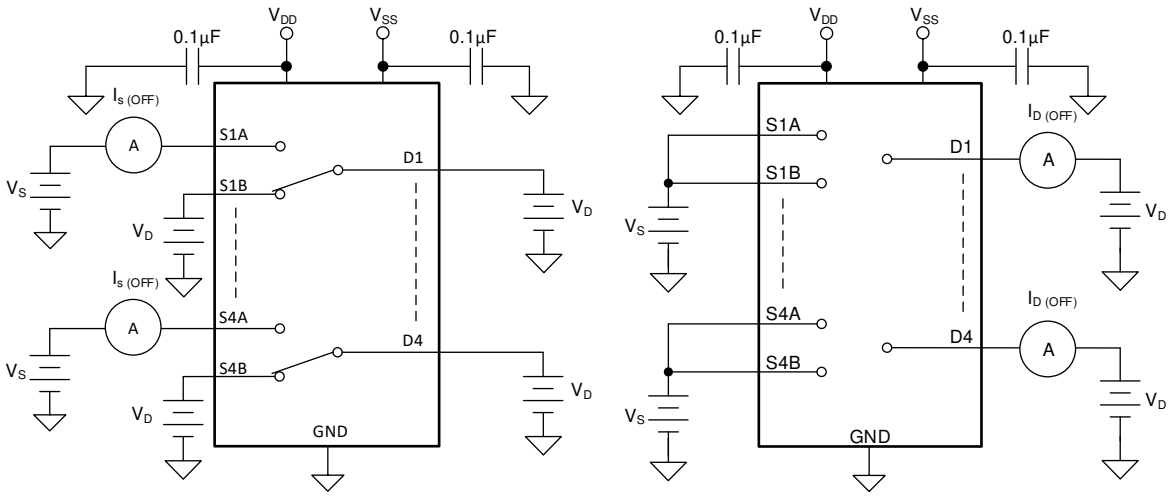


图 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

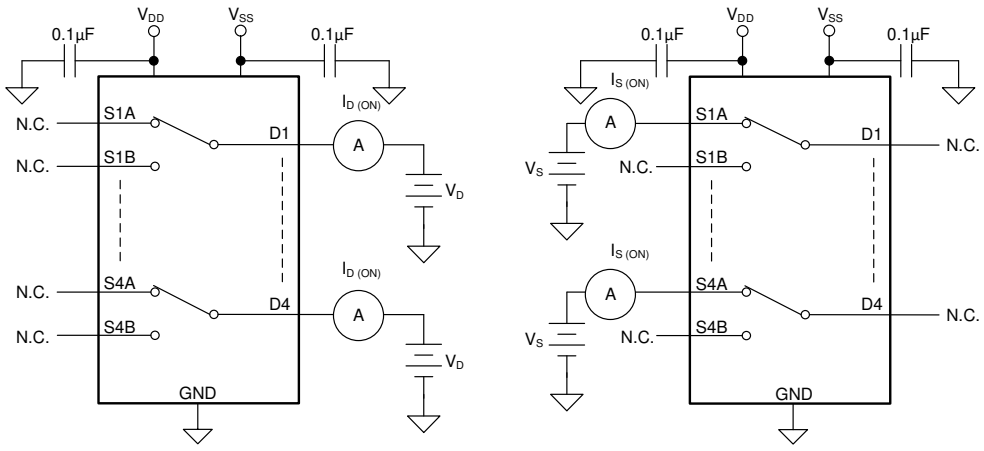


图 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

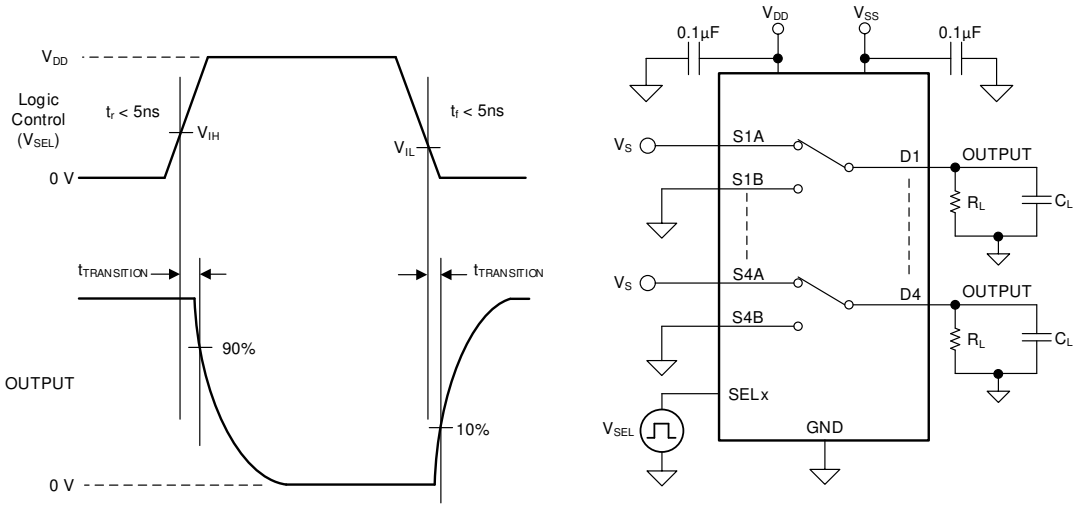


图 7-4. Transition-Time Measurement Setup

7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

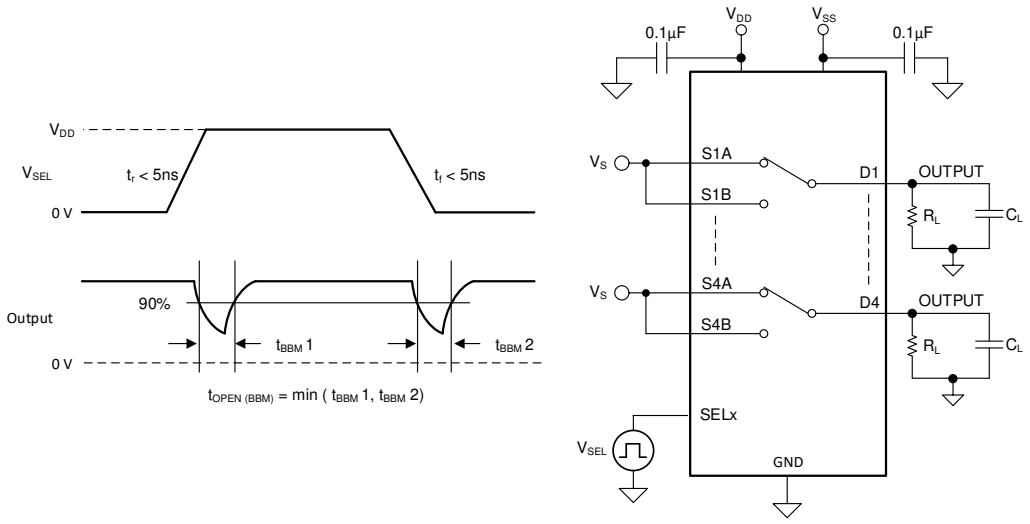


图 7-5. Break-Before-Make Delay Measurement Setup

7.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-6 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-6 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

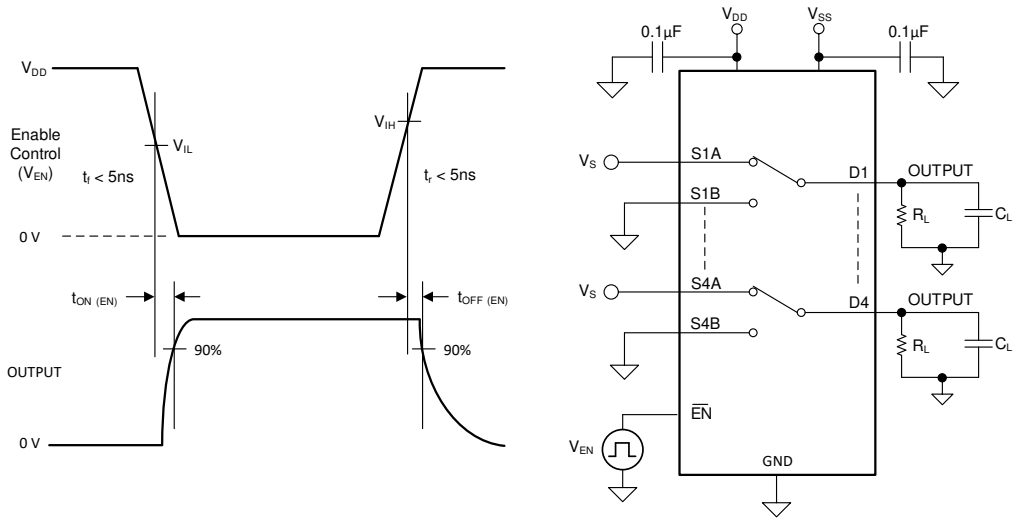


图 7-6. Turn-On and Turn-Off Time Measurement Setup

7.7 Charge Injection

The TMUX1133 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. 图 7-7 shows the setup used to measure charge injection from source (Sx) to drain (D).

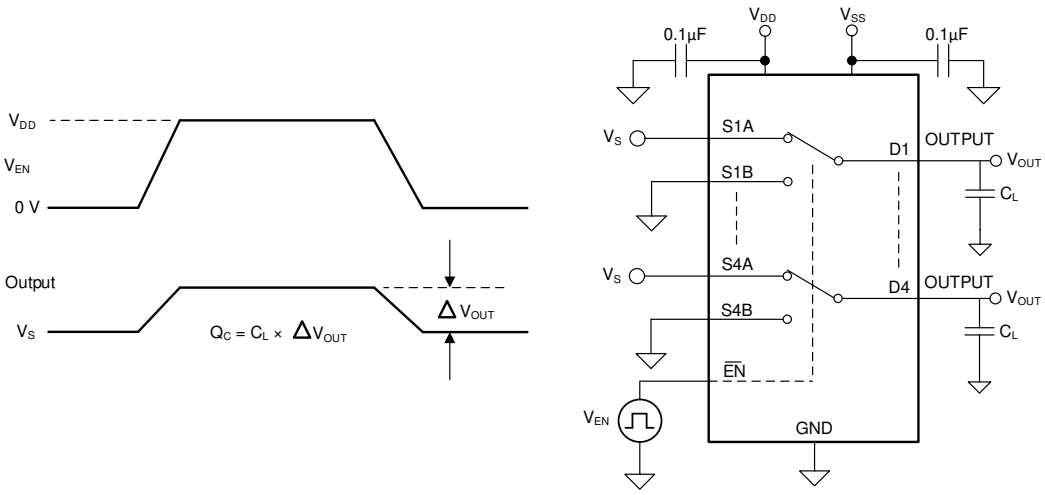


图 7-7. Charge-Injection Measurement Setup

7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 图 7-8 shows the setup used to measure, and the equation used to calculate off isolation.

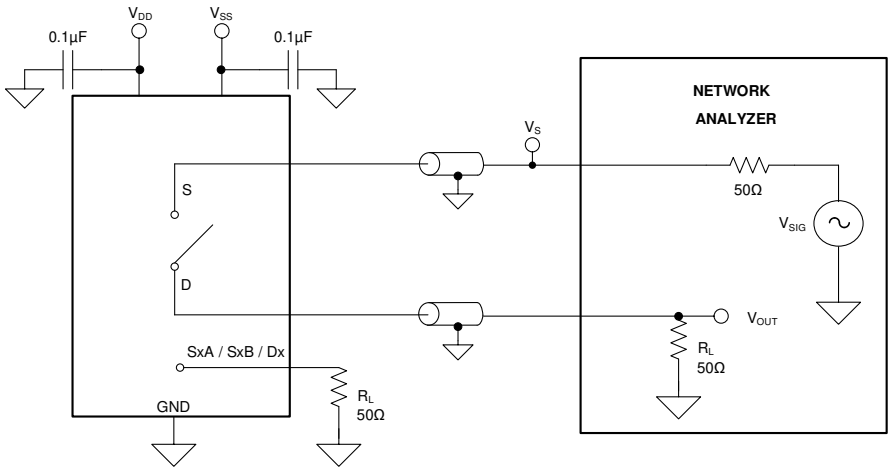


图 7-8. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

7.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 7-9 shows the setup used to measure, and the equation used to calculate crosstalk.

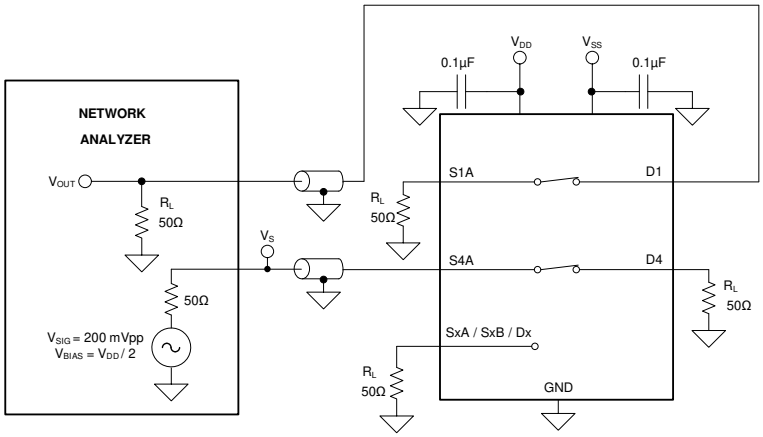


图 7-9. Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 7-10 shows the setup used to measure bandwidth.

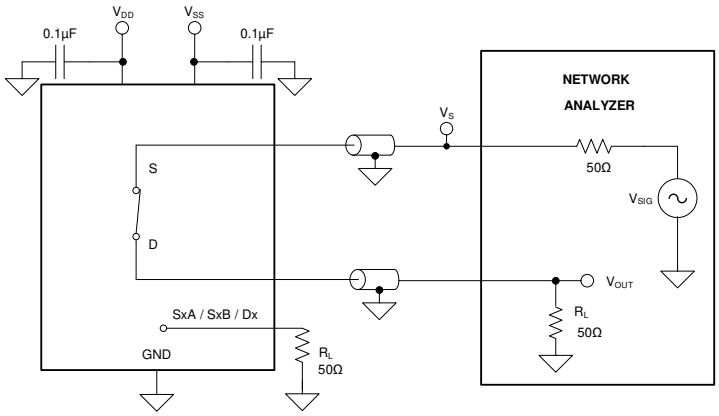


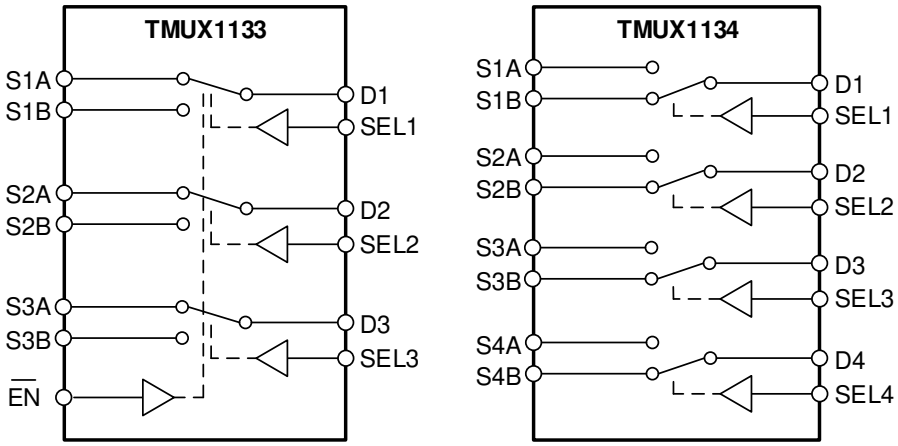
图 7-10. Bandwidth Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX1133 contains three independently controlled single-pole double-throw (SPDT) switches and has an active low $\overline{EN}$ pin to enable or disable all three switches simultaneously. The TMUX1134 contains four independently controlled SPDT switches.

8.2 Functional Block Diagram



ALL SWITCHES SHOWN FOR LOGIC 0 INPUT

8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX113x devices conduct equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX113x ranges from V_{SS} to V_{DD}. For single supply applications V_{SS} can be connected to GND.

8.3.3 1.8V Logic Compatible Inputs

The TMUX113x devices have 1.8V logic compatible control for all logic control inputs. The logic input thresholds scale with supply but still provide 1.8V logic control when operating at 5.5V supply voltage. 1.8V logic level inputs allows the TMUX113x devices to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. The current consumption of the TMUX113x devices increase when using 1.8V logic with higher supply voltage as shown in 图 6-11. For more information on 1.8V logic implementations refer to *Simplifying Design with 1.8V logic Muxes and Switches*

8.3.4 Fail-Safe Logic

The TMUX113x devices support Fail-Safe Logic on the control input pins (SELx and $\overline{EN}$) allowing for operation up to 5.5V, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pins, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX113x devices to be ramped to 5.5V while V_{DD} = 0V. Additionally, the feature enables operation of the TMUX113x devices with V_{DD} = 1.2V while allowing the select pins to interface with a logic level of another device up to 5.5V.

8.3.5 Ultra-low Leakage Current

The TMUX1133 and TMUX1134 provide extremely low on-leakage and off-leakage currents. The TMUX113x devices are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. 图 8-1 shows typical leakage currents of the TMUX113x devices versus input voltage.

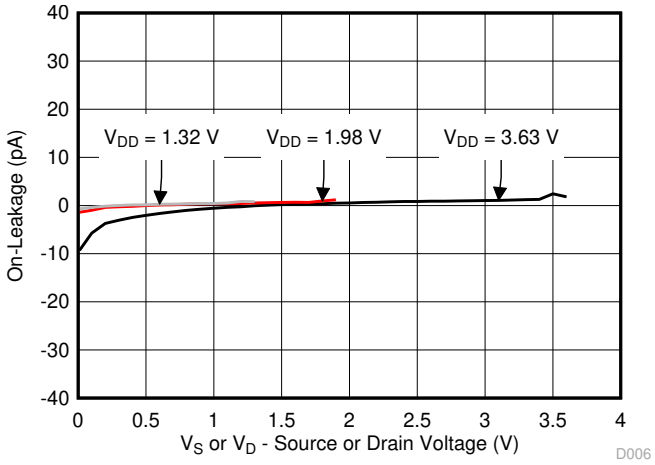


图 8-1. Leakage Current vs Input Voltage

8.3.6 Ultra-Low Charge Injection

The TMUX113x devices have a transmission gate topology, as shown in 图 8-2. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

The TMUX113x devices have special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to -1pC at V_S = 1V as shown in 图 8-3.

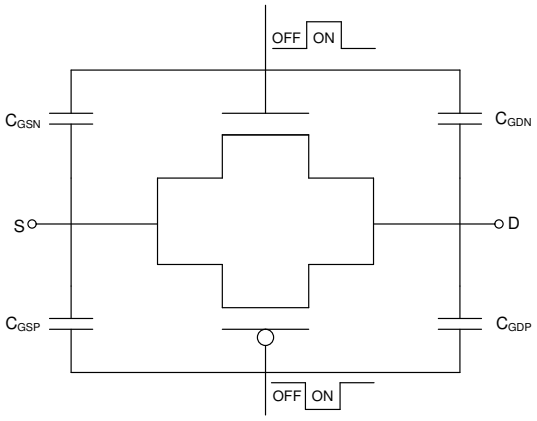


图 8-2. Transmission Gate Topology

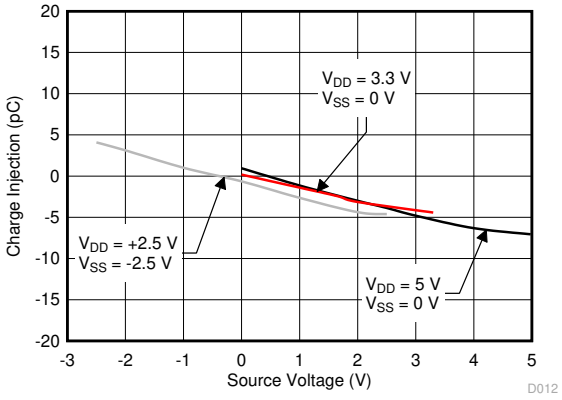


图 8-3. Charge Injection vs Source Voltage

8.4 Device Functional Modes

The select (SELx) pins are logic pins that control the connection between the source (SxA and SxB) and drain (Dx) pins of the TMUX113x devices. When a source pin is not selected that pin is in an open state (HI-Z). When a source pin is selected the switch conducts to drain. The logic control pins can be as high as 5.5V.

When the $\overline{EN}$ pin of the TMUX1133 is pulled low the SELx logic control inputs determine which source input is selected. When the $\overline{EN}$ pin is pulled high, all of the switches are in an open state regardless of the state of the SELx logic control inputs. The TMUX1134 SELx logic control inputs determine which source pin is connected to the drain pin for each channel.

The TMUX113x devices can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins must be tied to GND or V_{DD} so that the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (SxA, SxB, or Dx) should be connected to GND.

8.5 Truth Tables

表 8-1 and 表 8-2 lists the truth tables for the TMUX1133 and TMUX1134 respectively.

表 8-1. TMUX1133 Truth Table

$\overline{EN}$	SEL1(1)	SEL2	SEL3	Selected Source Pins Connected To Drain Pins
0	0	X	X	S1A to D1
0	1	X	X	S1B to D1
0	X	0	X	S2A to D2
0	X	1	X	S2B to D2
0	X	X	0	S3A to D3
0	X	X	1	S3B to D3
1	X	X	X	Hi-Z (OFF)

表 8-2. TMUX1134 Truth Table

SEL1	SEL2	SEL3	SEL4	Selected Source Pins Connected To Drain Pins
0	X	X	X	S1B to D1
1	X	X	X	S1A to D1
X	0	X	X	S2B to D2
X	1	X	X	S2A to D2
X	X	0	X	S3B to D3
X	X	1	X	S3A to D3
X	X	X	0	S4B to D4
X	X	X	1	S4A to D4

(1) X denotes *do not care*.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

9.1 Application Information

The TMUX11xx family offers ultra-low input/output leakage currents and low charge injection. These devices operate up to 5.5V, and offer true rail-to-rail input and output switching of both analog and digital signals. The TMUX113x devices have low on-capacitance which allows faster settling time when switching between inputs in the time domain. These features make the TMUX11xx devices a family of precision, high-performance switches and multiplexers for low-voltage applications.

9.2 Typical Application

图 9-1 shows an example circuit where the TMUX1133 or TMUX1134 can be used to minimize board space by integrating various applications into a multi-channel 2:1 (SPDT) switch. The application uses a 3-channel, or 4-channel SPDT switch to optimize the tradeoffs of system flexibility and board space.

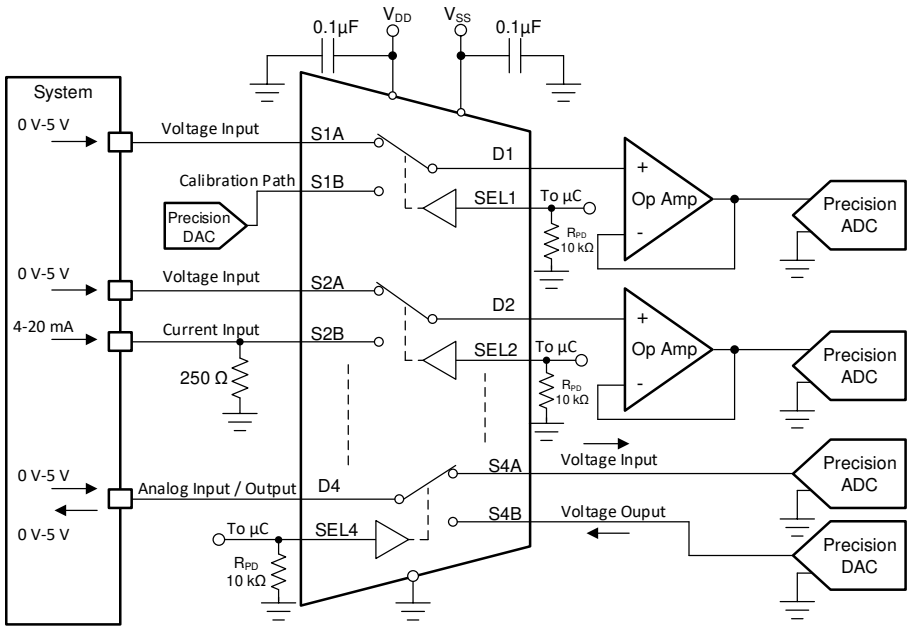


图 9-1. Multi-channel 2:1, Switching Applications

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	5V
Input / Output Voltage range	0V to 5V
Input / Output Current range	4mA to 20mA
Control logic thresholds	1.8V compatible

9.2.2 Detailed Design Procedure

The TMUX113x devices can be operated without any external components except for the supply decoupling capacitors, however pull-down or pull-up resistors are recommended on the logic control inputs so that each channel is in a known state. All inputs passing through the switch must fall within the recommend operating conditions, including signal range and continuous current. For this design with a single supply of 5V the signal range can be 0V to 5V, and the maximum continuous current can be 30mA.

Industrial applications such as in factory automation and control; test and measurement benefit from using a multi-channel 2:1 switch, because it allows additional flexibility in the design.
A single 2:1 switch has numerous applications such as:

1. Switching between an analog signal path and a calibration path so that the system is calibrated across the life of a product or after installation.
2. Configuring a single channel to accept either a voltage or current input through software - allowing for system flexibility across applications where the end users input signals may differ.
3. Allowing a single channel to be configured as either an analog input or analog output. Providing additional control to a system while minimizing the number of physical connectors

图 9-1 shows how to configure a multi-channel analog switch to address these design implementations for additional control and flexibility in the system. The on-resistance of the TMUX113x devices is very low, 2Ω typical, and has a maximum on-leakage current of 2nA which allows the devices to be used in precision measurement applications. A system with a 4mA to 20mA signal can achieve >20bits of precision due to the extremely low leakage current of the TMUX113x devices.

9.2.3 Application Curve

The TMUX113x devices are capable of switching signals with minimal distortion because of the ultra-low leakage currents and low on-resistance. 图 9-2 shows how the leakage current of the TMUX113x varies with different input voltages.

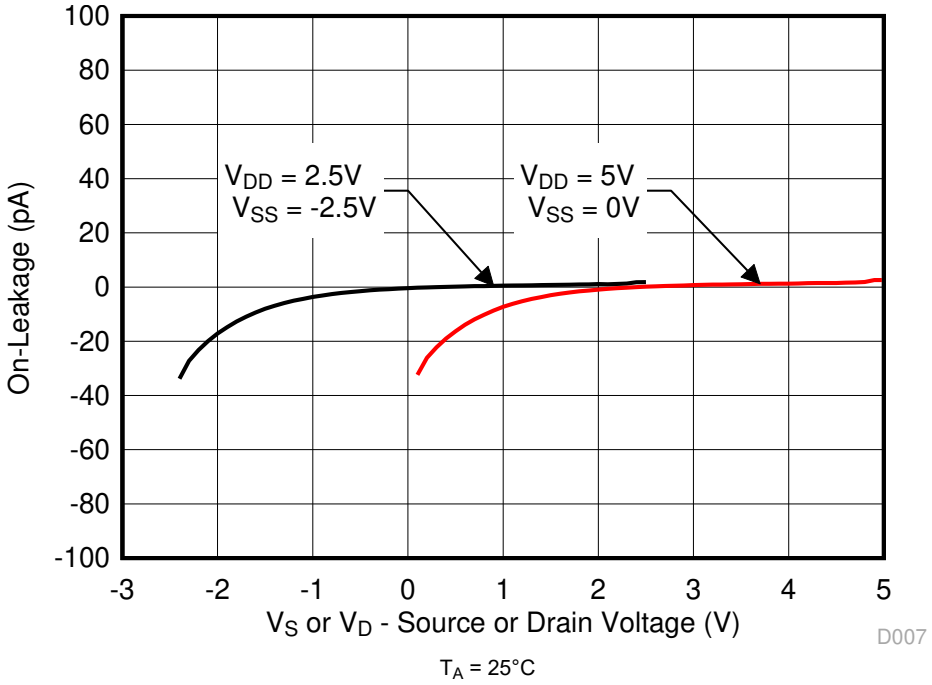


图 9-2. On-Leakage vs Source or Drain Voltage

9.3 Power Supply Recommendations

The TMUX113x devices operate across a wide supply range of 1.08V to 5.5V single supply, or ±2.75V for dual supply applications. For single supply voltage applications V_{SS} must be connected to GND. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} and V_{SS} supplies to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} and V_{SS} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

9.4 Layout

9.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self‐inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 9-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

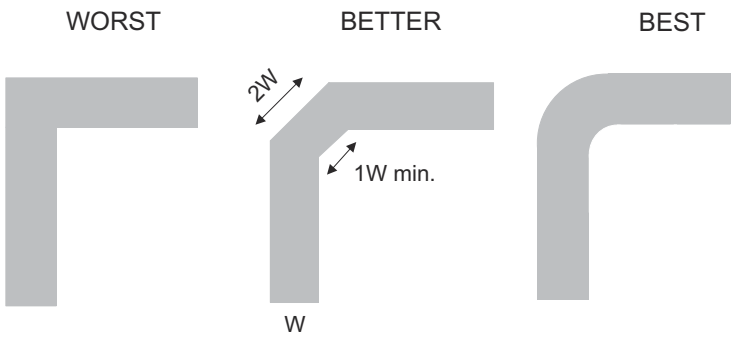


图 9-3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 9-4 and 图 9-5 shows examples of a PCB layout with the TMUX1133 and TMUX1134 respectively. Some key considerations are:

- Decouple the V_{DD} and V_{SS} pins with a 0.1μF capacitor, placed as close to the pin as possible. Ensure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

9.4.2 Layout Example

图 9-4 shows an example board layout for the TMUX1133.

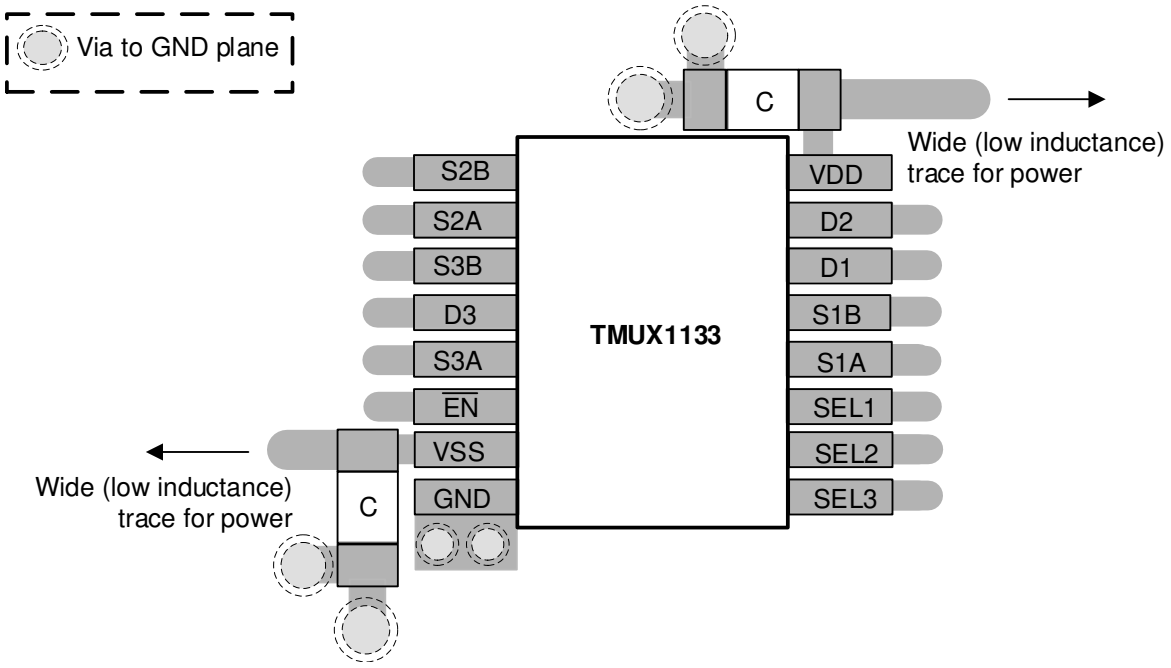


图 9-4. TMUX1133 Layout Example

图 9-5 shows an example board layout for the TMUX1134.

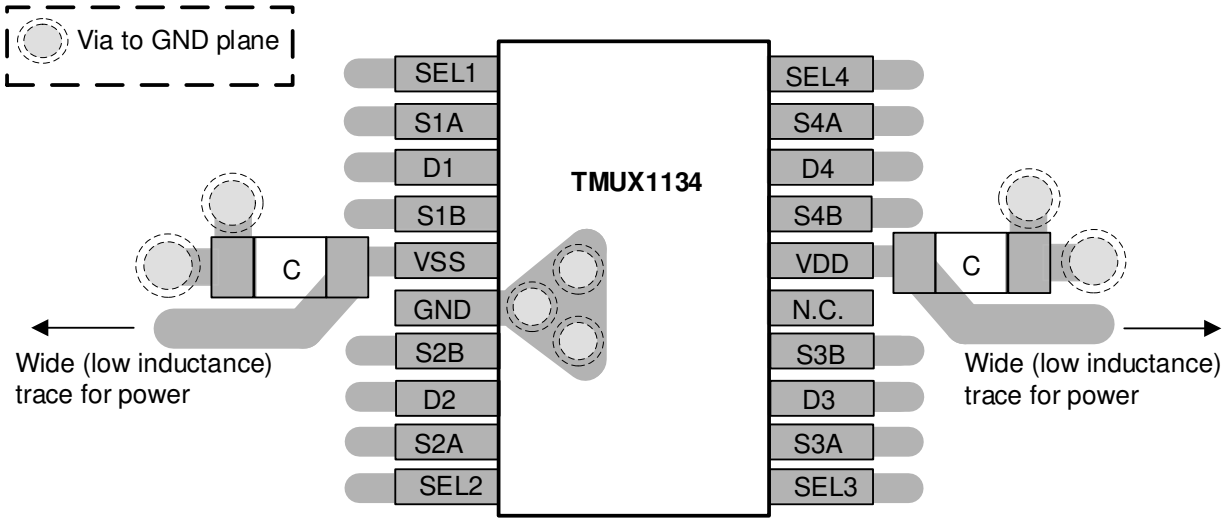


图 9-5. TMUX1134 Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Ultrasonic Gas Meter Front-End With MSP430™ Reference Design*.
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit*.
- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches*.
- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.
- Texas Instruments, *QFN/SON PCB Attachment*.
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages*.

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (August 2019) to Revision B (January 2024)	Page
• 编辑了“功能方框图”图像以显示逻辑状态。	1
• Updated Is or Id (Continuous Current) values	5
• Added Ipeak values to recommended operating conditions table	5

Changes from Revision * (June 2019) to Revision A (August 2019)	Page
• 将器件状态从*预告信息* 更改为*量产* 数据	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX1133PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1133	Samples
TMUX1134PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1134	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

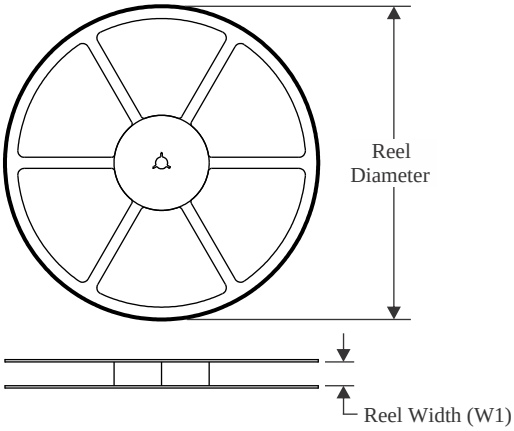
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

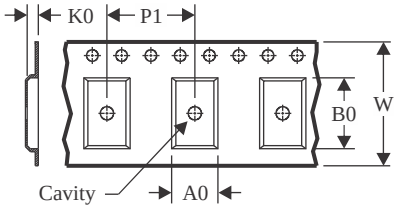
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

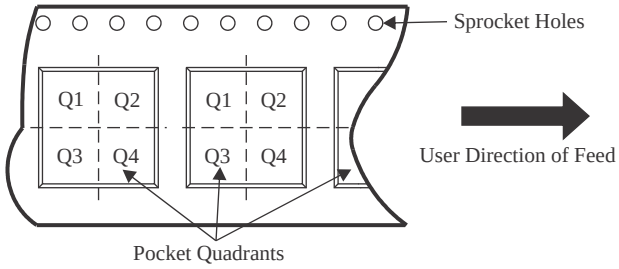


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

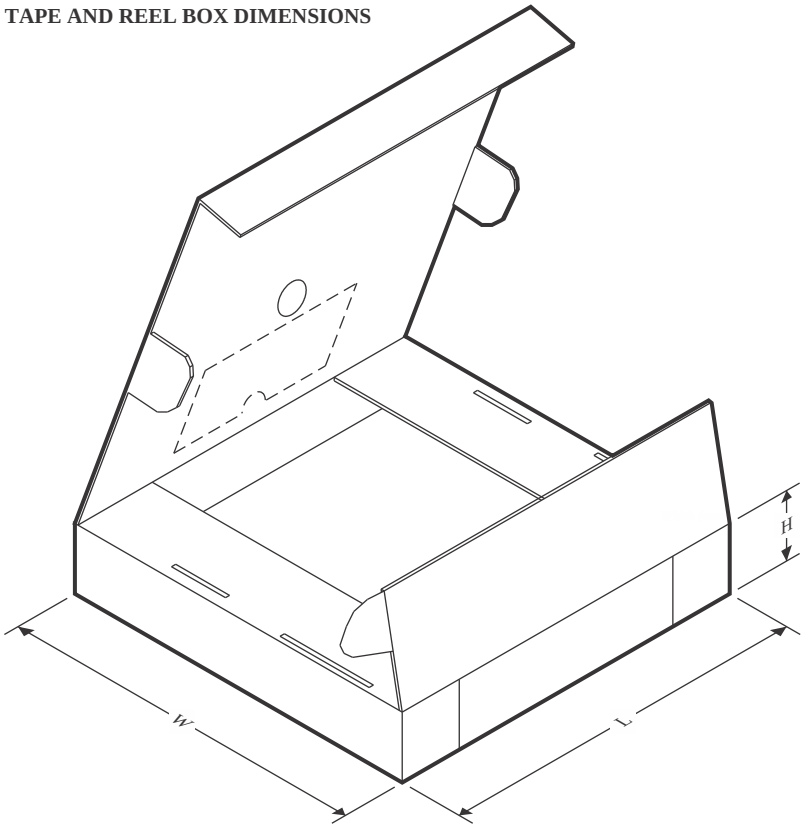
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1133PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1134PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

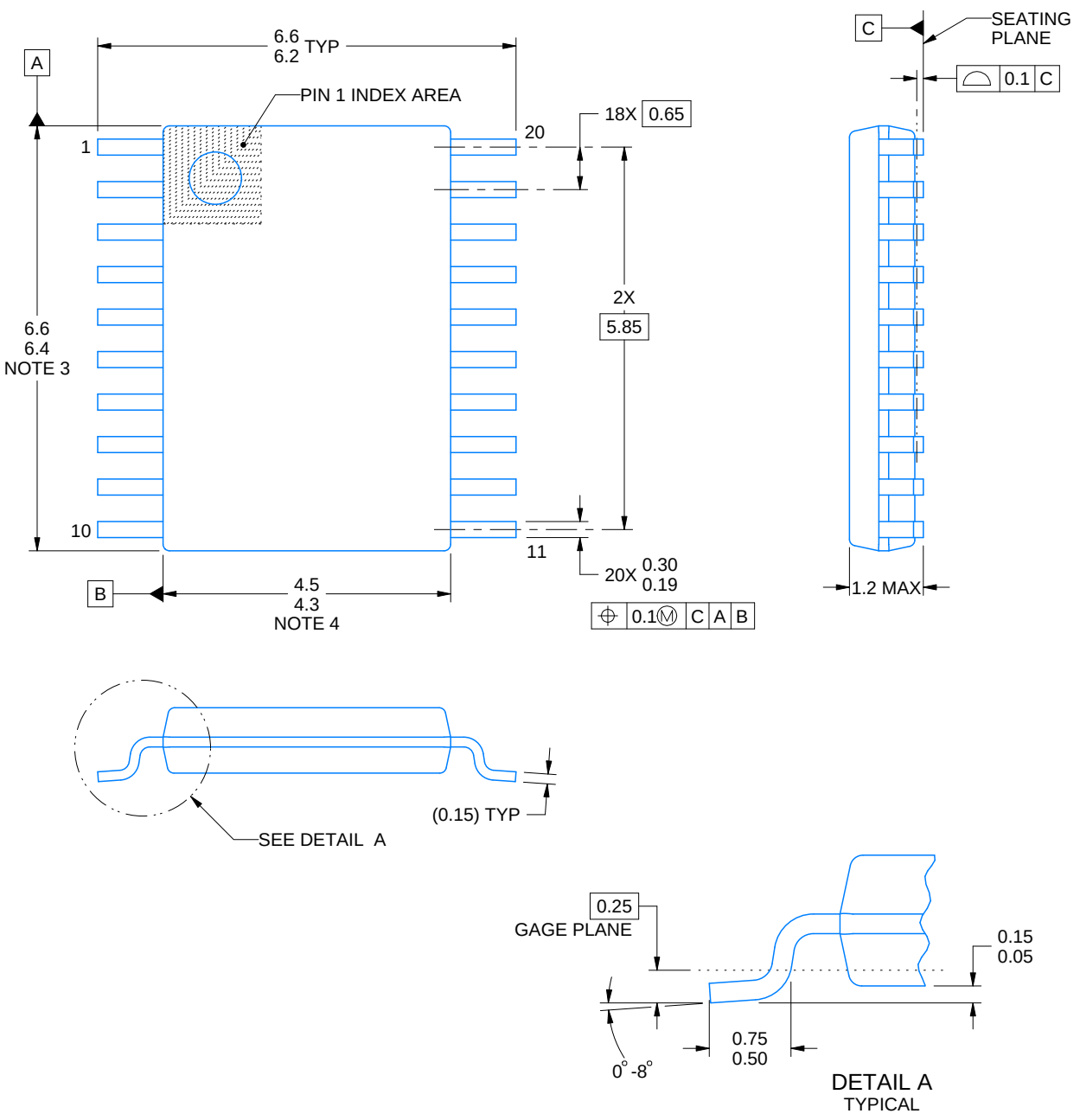
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1133PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TMUX1134PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0020A

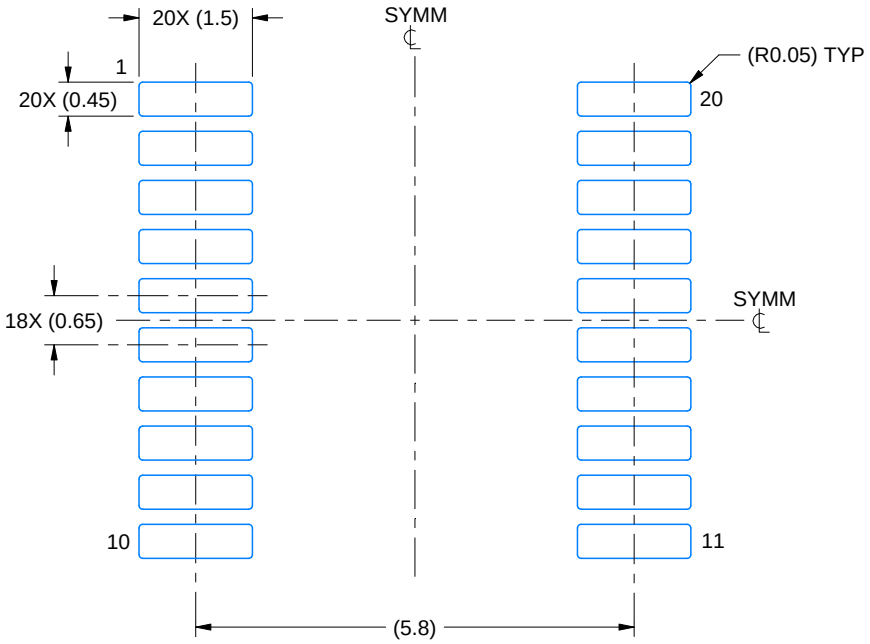
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



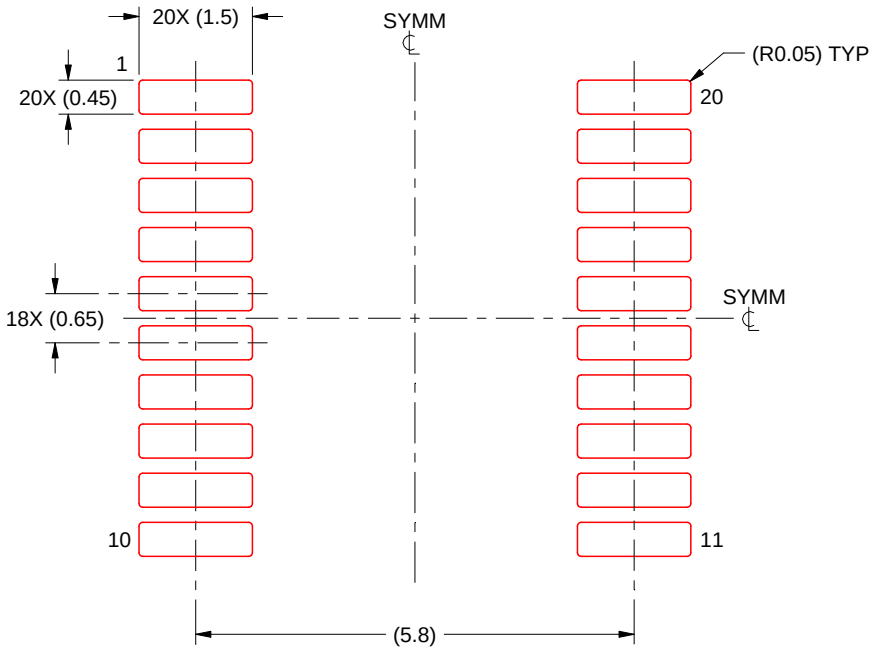
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



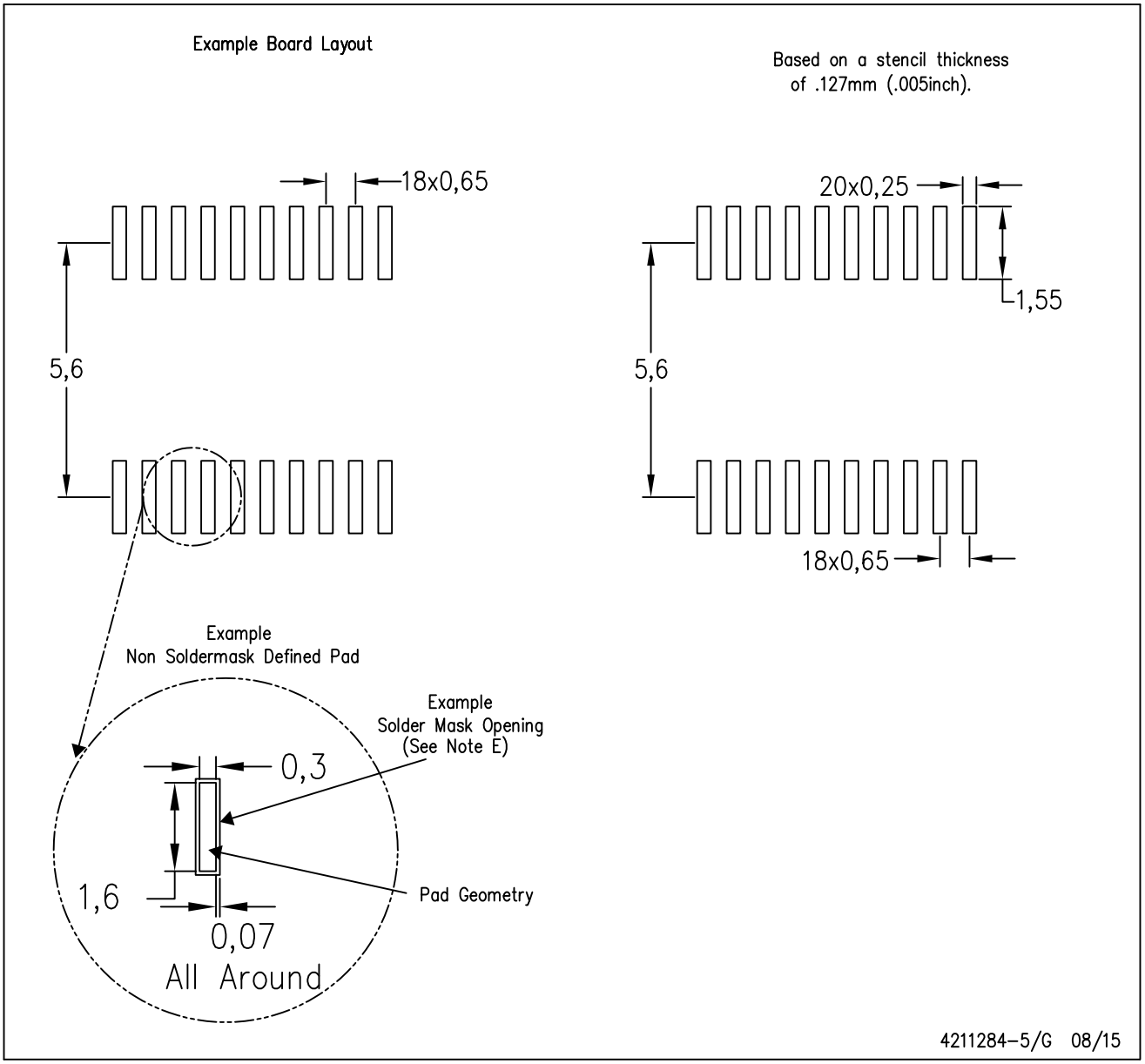
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



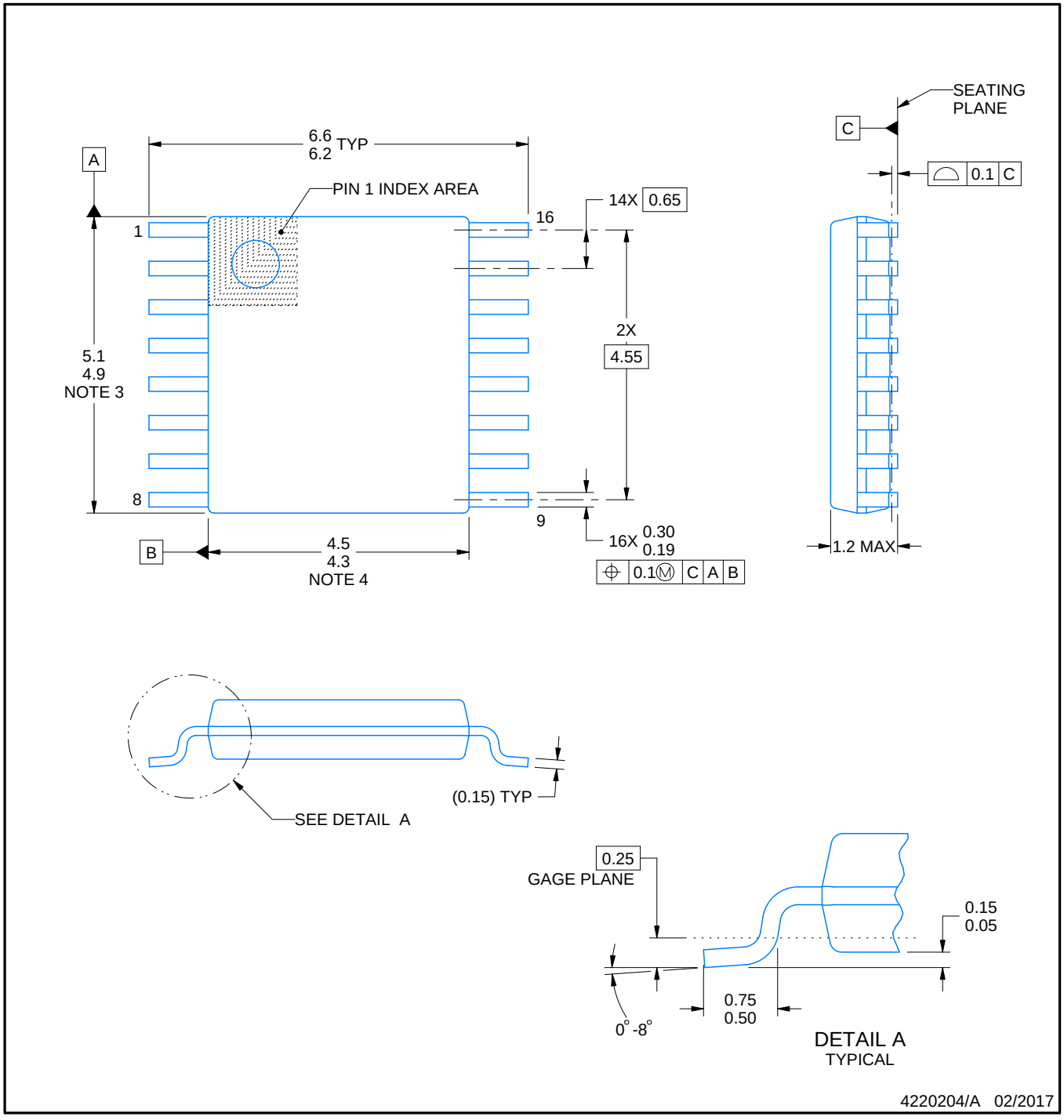
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

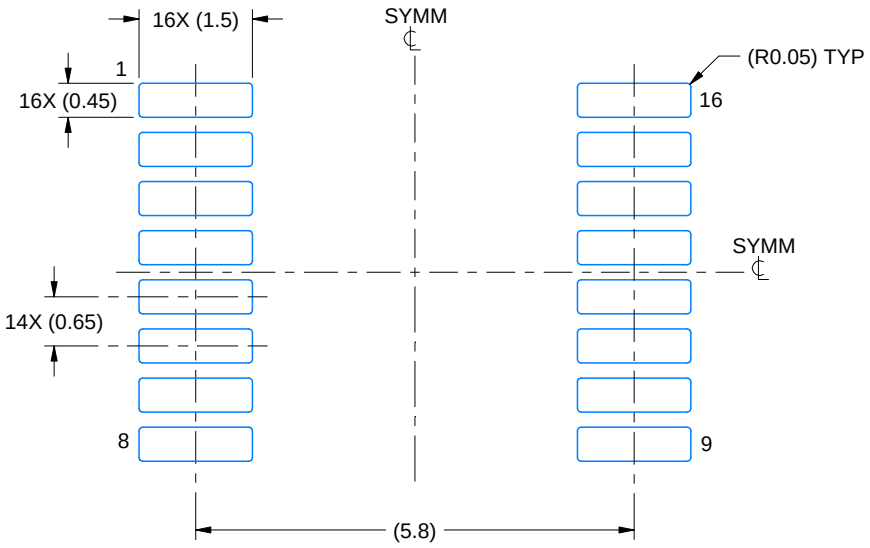
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

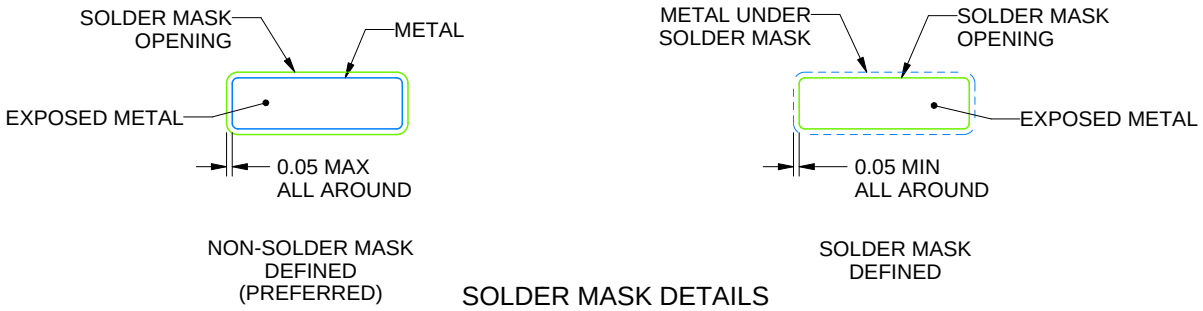


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

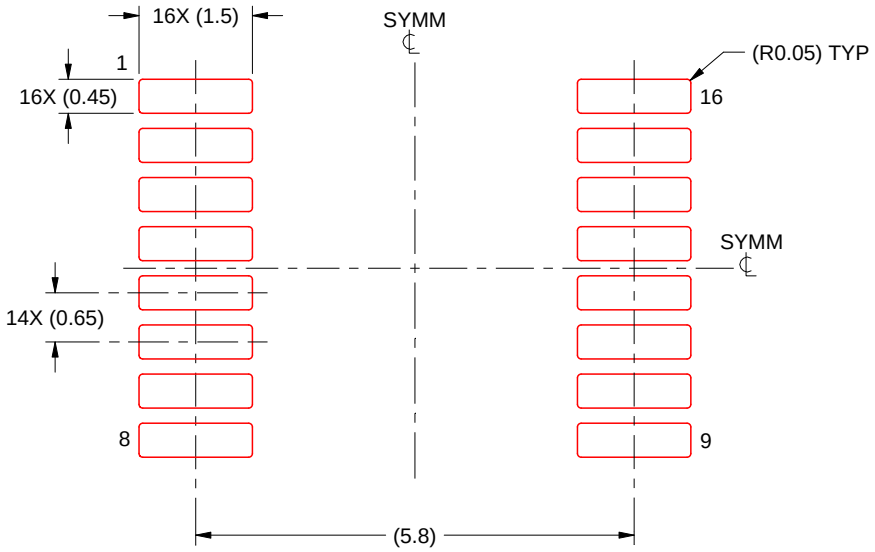


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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