

## TMS320F2802x 微控制器

### 1 特性

- 高效 32 位 CPU (TMS320C28x)
  - 60MHz ( 16.67ns 周期时间 )
  - 50MHz ( 20ns 周期时间 )
  - 40MHz ( 25ns 周期时间 )
  - 16 × 16 和 32 × 32 MAC 操作
  - 16 × 16 双 MAC
  - 哈佛 (Harvard) 总线架构
  - 连动运算
  - 快速中断响应和处理
  - 统一存储器编程模型
  - 高效代码 ( 使用 C/C++ 和汇编语言 )
- 字节序：小端字节序
- 器件和系统均可实现低成本：
  - 3.3V 单电源
  - 无需电源时序
  - 集成型加电和欠压复位
  - 可采用低至 38 引脚小型封装
  - 低功耗
  - 无模拟支持引脚
- 时钟：
  - 两个内部零引脚振荡器
  - 片上晶振振荡器和外部时钟输入
  - 看门狗计时器模块
  - 丢失时钟检测电路
- 多达 22 个具有输入滤波功能且可单独编程的多路复用 GPIO 引脚
- 可支持所有外设中断的外设中断扩展 (PIE) 模块
- 三个 32 位 CPU 计时器
- 每个增强型脉宽调制器 (ePWM) 中均有一个独立的 16 位计时器
- 片上存储器
  - 闪存, SARAM, OTP, 引导 ROM 可用
- 代码安全模块
- 128 位安全密钥和锁
  - 保护安全内存块
  - 防止固件逆向工程

- 串行端口外设
  - 一个串行通信接口 (SCI) 通用异步接收器/发送器 (UART) 模块
  - 一个串行外设接口 (SPI) 模块
  - 一个内部集成电路 (I2C) 模块
- 增强型控制外设
  - ePWM
  - 高分辨率 PWM (HRPWM)
  - 增强型捕捉 (eCAP) 模块
  - 模数转换器 (ADC)
  - 片上温度传感器
  - 比较器
- 高级仿真特性
  - 分析和断点功能
  - 通过硬件进行实时调试
- 封装选项
  - 38 引脚 DA Thin Shrink Small-Outline Package (TSSOP)
  - 48 引脚 PT Low-Profile Quad Flatpack (LQFP)
- 温度选项
  - T：-40°C 至 105°C
  - S：-40°C 至 125°C
  - Q：-40°C 至 125°C 的环境温度范围 ( 通过针对汽车应用的 AEC Q100 认证 )

### 2 应用

- 空调室外机
- 逆变器和电机控制
- 纺织机
- 微型逆变器
- 交流驱动器功率级模块
- 交流输入 BLDC 电机驱动器
- 直流输入 BLDC 电机驱动器
- 工业交流/直流电源
- 三相 UPS
- 商用直流/直流电源
- 商用网络和服务服务器 PSU
- 商用通信电源整流器



### 3 说明

C2000™ 32 位微控制器针对处理、感应和驱动进行了优化，可提高实时控制应用（如工业电机驱动器、光伏逆变器和数字电源、电动汽车和运输、电机控制以及感应和信号处理）的闭环性能。C2000 系列包括高级性能 MCU 和入门级性能 MCU。

F2802x 微控制器系列提供 C28xx 内核的强大功能，同时结合低引脚数器件中高度集成的控制外设。该系列器件的代码与基于 C28x 的旧版代码兼容，同时具有较高的模拟集成度。

内部稳压器实现了单电源轨运行。HRPWM 模块经过强化，可实现双边沿控制（调频）。增设了具有 10 位内部基准的模拟比较器，可直接进行路由以控制 PWM 输出。ADC 可在 0V 至 3.3V 的固定满量程范围内实施转换，支持  $V_{REFHI}/V_{REFLO}$  基准的比例运算。ADC 接口已针对低开销和延迟进行了优化。

如需详细了解 C2000 MCU，请访问“C2000 概述”，地址为 [www.ti.com/c2000](http://www.ti.com/c2000)。

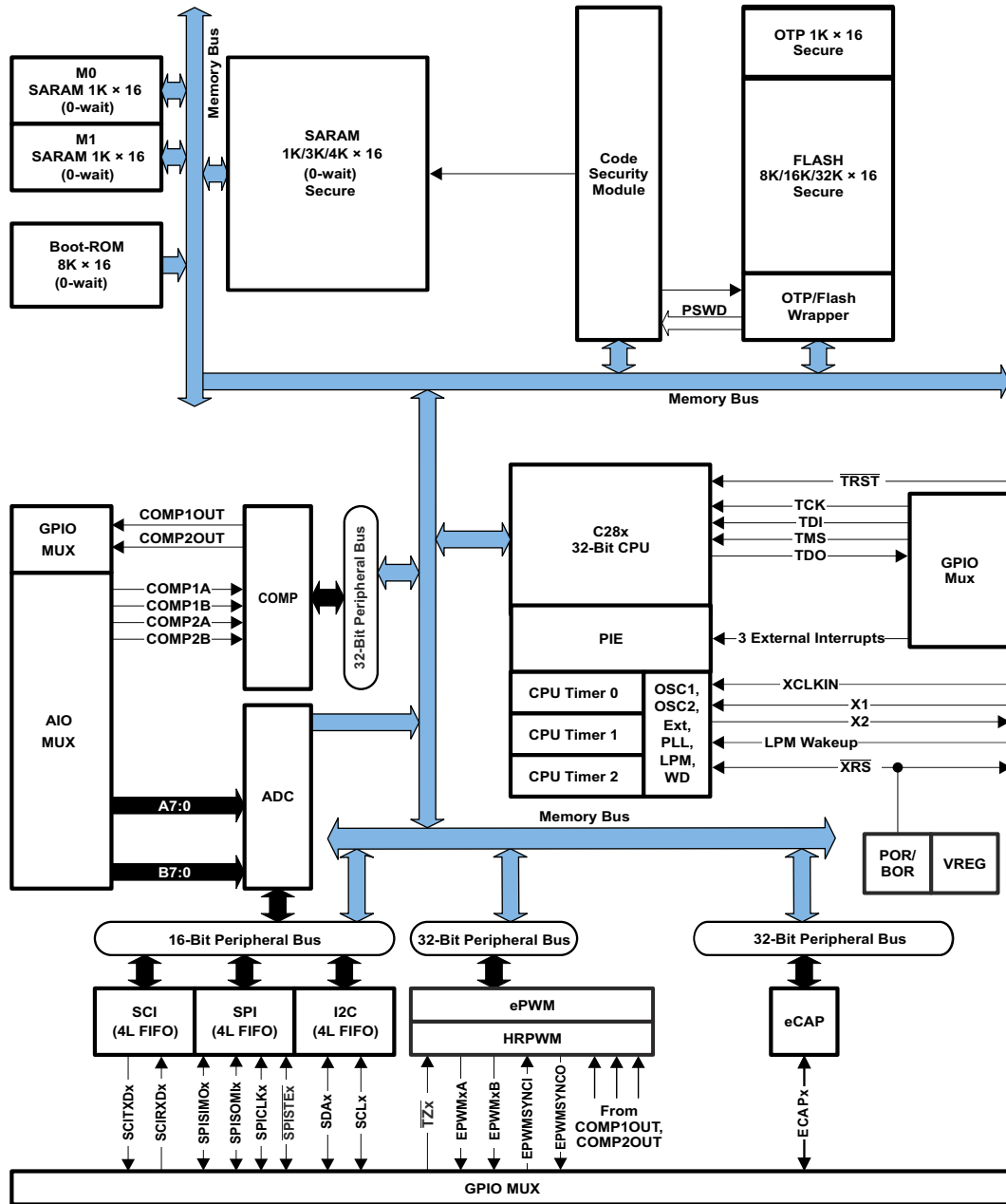
器件信息

| 器件型号 <sup>(1)</sup> | 封装         | 封装尺寸           |
|---------------------|------------|----------------|
| TMS320F28027PT      | LQFP (48)  | 7.0mm × 7.0mm  |
| TMS320F28026PT      | LQFP (48)  | 7.0mm × 7.0mm  |
| TMS320F28023PT      | LQFP (48)  | 7.0mm × 7.0mm  |
| TMS320F28022PT      | LQFP (48)  | 7.0mm × 7.0mm  |
| TMS320F28021PT      | LQFP (48)  | 7.0mm × 7.0mm  |
| TMS320F28020PT      | LQFP (48)  | 7.0mm × 7.0mm  |
| TMS320F280200PT     | LQFP (48)  | 7.0mm × 7.0mm  |
| TMS320F28027DA      | TSSOP (38) | 12.5mm × 6.2mm |
| TMS320F28026DA      | TSSOP (38) | 12.5mm × 6.2mm |
| TMS320F28023DA      | TSSOP (38) | 12.5mm × 6.2mm |
| TMS320F28022DA      | TSSOP (38) | 12.5mm × 6.2mm |
| TMS320F28021DA      | TSSOP (38) | 12.5mm × 6.2mm |
| TMS320F28020DA      | TSSOP (38) | 12.5mm × 6.2mm |
| TMS320F280200DA     | TSSOP (38) | 12.5mm × 6.2mm |

(1) 有关这些器件的详细信息，请参阅机械、封装和可订购信息。

## 4 功能方框图

功能方框图展示了器件的功能方框图。



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A. 由于多路复用，所有外设引脚不能同时使用。

图 4-1. 功能方框图

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## 5 修订历史记录

Changes from OCTOBER 30, 2020 to JANUARY 18, 2021 (from Revision O (October 2020) to Revision P (January 2021))

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## 6 Device Comparison

表 6-1 lists the features of the TMS320F2802x devices.

表 6-1. Device Comparison

| FEATURE                                                 |                                   | TYPE<br>(1) | 28027<br>28027-Q1<br>28027F<br>28027F-Q1<br>(60 MHz) <sup>(2)</sup> |                      | 28026<br>28026-Q1<br>28026F<br>28026F-Q1<br>(60 MHz) <sup>(2)</sup> |                      | 28023<br>28023-Q1<br>(50 MHz) |                      | 28022<br>28022-Q1<br>(50 MHz) |                      | 28021<br>(40 MHz)     |                      | 28020<br>(40 MHz)     |                      | 280200<br>(40 MHz)    |                      |
|---------------------------------------------------------|-----------------------------------|-------------|---------------------------------------------------------------------|----------------------|---------------------------------------------------------------------|----------------------|-------------------------------|----------------------|-------------------------------|----------------------|-----------------------|----------------------|-----------------------|----------------------|-----------------------|----------------------|
|                                                         |                                   |             | 38-Pin<br>DA<br>TSSOP                                               | 48-Pin<br>PT<br>LQFP | 38-Pin<br>DA<br>TSSOP                                               | 48-Pin<br>PT<br>LQFP | 38-Pin<br>DA<br>TSSOP         | 48-Pin<br>PT<br>LQFP | 38-Pin<br>DA<br>TSSOP         | 48-Pin<br>PT<br>LQFP | 38-Pin<br>DA<br>TSSOP | 48-Pin<br>PT<br>LQFP | 38-Pin<br>DA<br>TSSOP | 48-Pin<br>PT<br>LQFP | 38-Pin<br>DA<br>TSSOP | 48-Pin<br>PT<br>LQFP |
| Instruction cycle                                       |                                   | –           | 16.67 ns                                                            |                      | 16.67 ns                                                            |                      | 20 ns                         |                      | 20 ns                         |                      | 25 ns                 |                      | 25 ns                 |                      | 25 ns                 |                      |
| On-chip flash (16-bit word)                             |                                   | –           | 32K                                                                 |                      | 16K                                                                 |                      | 32K                           |                      | 16K                           |                      | 32K                   |                      | 16K                   |                      | 8K                    |                      |
| On-chip SARAM (16-bit word)                             |                                   | –           | 6K                                                                  |                      | 6K                                                                  |                      | 6K                            |                      | 6K                            |                      | 5K                    |                      | 3K                    |                      | 3K                    |                      |
| Code security for on-chip flash/SARAM/OTP blocks        |                                   | –           | Yes                                                                 |                      | Yes                                                                 |                      | Yes                           |                      | Yes                           |                      | Yes                   |                      | Yes                   |                      | Yes                   |                      |
| Boot ROM (8K x 16)                                      |                                   | –           | Yes                                                                 |                      | Yes                                                                 |                      | Yes                           |                      | Yes                           |                      | Yes                   |                      | Yes                   |                      | Yes                   |                      |
| One-time programmable (OTP) ROM (16-bit word)           |                                   | –           | 1K                                                                  |                      | 1K                                                                  |                      | 1K                            |                      | 1K                            |                      | 1K                    |                      | 1K                    |                      | 1K                    |                      |
| ePWM channels                                           |                                   | 1           | 8 (ePWM1/2/3/4)                                                     |                      | 8 (ePWM1/2/3/4)                                                     |                      | 8 (ePWM1/2/3/4)               |                      | 8 (ePWM1/2/3/4)               |                      | 8 (ePWM1/2/3/4)       |                      | 8 (ePWM1/2/3/4)       |                      | 8 (ePWM1/2/3/4)       |                      |
| eCAP inputs                                             |                                   | 0           | 1                                                                   |                      | 1                                                                   |                      | 1                             |                      | 1                             |                      | 1                     |                      | 1                     |                      | –                     |                      |
| Watchdog timer                                          |                                   | –           | Yes                                                                 |                      | Yes                                                                 |                      | Yes                           |                      | Yes                           |                      | Yes                   |                      | Yes                   |                      | Yes                   |                      |
| 12-Bit ADC                                              | MSPS                              | 3           | 4.6                                                                 |                      | 4.6                                                                 |                      | 3                             |                      | 3                             |                      | 2                     |                      | 2                     |                      | 2                     |                      |
|                                                         | Conversion Time                   |             | 216.67 ns                                                           |                      | 216.67 ns                                                           |                      | 260 ns                        |                      | 260 ns                        |                      | 500 ns                |                      | 500 ns                |                      | 500 ns                |                      |
|                                                         | Channels                          |             | 7                                                                   | 13                   | 7                                                                   | 13                   | 7                             | 13                   | 7                             | 13                   | 7                     | 13                   | 7                     | 13                   | 7                     | 13                   |
|                                                         | Temperature Sensor                |             | Yes                                                                 |                      | Yes                                                                 |                      | Yes                           |                      | Yes                           |                      | Yes                   |                      | Yes                   |                      | Yes                   |                      |
|                                                         | Dual Sample-and-Hold              |             | Yes                                                                 |                      | Yes                                                                 |                      | Yes                           |                      | Yes                           |                      | Yes                   |                      | Yes                   |                      | Yes                   |                      |
| 32-Bit CPU timers                                       |                                   | –           | 3                                                                   |                      | 3                                                                   |                      | 3                             |                      | 3                             |                      | 3                     |                      | 3                     |                      | 3                     |                      |
| High-resolution ePWM Channels                           |                                   | 1           | 4 (ePWM1A/2A /3A/4A)                                                |                      | 4 (ePWM1A/2A /3A/4A)                                                |                      | 4 (ePWM1A/2A /3A/4A)          |                      | 4 (ePWM1A/2A /3A/4A)          |                      | –                     |                      | –                     |                      | –                     |                      |
| Comparators w/ Integrated DACs                          |                                   | 0           | 1                                                                   | 2                    | 1                                                                   | 2                    | 1                             | 2                    | 1                             | 2                    | 1                     | 2                    | 1                     | 2                    | 1                     | 2                    |
| Inter-integrated circuit (I2C)                          |                                   | 0           | 1                                                                   |                      | 1                                                                   |                      | 1                             |                      | 1                             |                      | 1                     |                      | 1                     |                      | 1                     |                      |
| Serial Peripheral Interface (SPI)                       |                                   | 1           | 1                                                                   |                      | 1                                                                   |                      | 1                             |                      | 1                             |                      | 1                     |                      | 1                     |                      | 1                     |                      |
| Serial Communications Interface (SCI) (UART Compatible) |                                   | 0           | 1                                                                   |                      | 1                                                                   |                      | 1                             |                      | 1                             |                      | 1                     |                      | 1                     |                      | 1                     |                      |
| I/O pins (shared)                                       | Digital (GPIO)                    | –           | 20                                                                  | 22                   | 20                                                                  | 22                   | 20                            | 22                   | 20                            | 22                   | 20                    | 22                   | 20                    | 22                   | 20                    | 22                   |
|                                                         | Analog (AIO)                      | –           | 6                                                                   |                      | 6                                                                   |                      | 6                             |                      | 6                             |                      | 6                     |                      | 6                     |                      | 6                     |                      |
| External interrupts                                     |                                   | –           | 3                                                                   |                      | 3                                                                   |                      | 3                             |                      | 3                             |                      | 3                     |                      | 3                     |                      | 3                     |                      |
| Supply voltage (nominal)                                |                                   | –           | 3.3 V                                                               |                      | 3.3 V                                                               |                      | 3.3 V                         |                      | 3.3 V                         |                      | 3.3 V                 |                      | 3.3 V                 |                      | 3.3 V                 |                      |
| Temperature options                                     | T: – 40°C to 105°C                | –           | Yes                                                                 | Yes                  | Yes                                                                 | Yes                  | Yes                           | Yes                  | Yes                           | Yes                  | Yes                   | Yes                  | Yes                   | Yes                  | Yes                   | Yes                  |
|                                                         | S: – 40°C to 125°C                | –           | Yes                                                                 | Yes                  | Yes                                                                 | Yes                  | Yes                           | Yes                  | Yes                           | Yes                  | Yes                   | Yes                  | Yes                   | Yes                  | Yes                   | Yes                  |
|                                                         | Q: – 40°C to 125°C <sup>(3)</sup> | –           | Yes                                                                 | Yes                  | Yes                                                                 | Yes                  | Yes                           | Yes                  | Yes                           | Yes                  | –                     | –                    | –                     | –                    | –                     | –                    |

- (1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. These device-specific differences are listed in the [C2000 Real-Time Control Peripherals Reference Guide](#) and in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).
- (2) TMS320F28027F and TMS320F28026F are InstaSPIN-FOC™-enabled MCUs. For more information, see [节 11.3](#) for a list of InstaSPIN Technical Reference Manuals.
- (3) The letter Q refers to AEC Q100 qualification for automotive applications.

## 6.1 Related Products

For information about similar products, see the following links:

### [TMS320F2802x Microcontrollers](#)

The F2802x series offers the lowest pin-count and Flash memory size options. [InstaSPIN-FOC™](#) versions are available.

### [TMS320F2803x Microcontrollers](#)

The F2803x series increases the pin-count and memory size options. The F2803x series also introduces the parallel control law accelerator (CLA) option.

### [TMS320F2805x Microcontrollers](#)

The F2805x series is similar to the F2803x series but adds on-chip programmable gain amplifiers (PGAs). InstaSPIN-FOC and [InstaSPIN-MOTION™](#) versions are available.

### [TMS320F2806x Microcontrollers](#)

The F2806x series is the first to include a floating-point unit (FPU). The F2806x series also increases the pin-count, memory size options, and the quantity of peripherals. InstaSPIN-FOC™ and InstaSPIN-MOTION™ versions are available.

### [TMS320F2807x Microcontrollers](#)

The F2807x series offers the most performance, largest pin counts, flash memory sizes, and peripheral options. The F2807x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

### [TMS320F28004x Microcontrollers](#)

The F28004x series is a reduced version of the F2807x series with the latest generational enhancements. The F28004x series is the best roadmap option for those using the F2806x series. InstaSPIN-FOC and configurable logic block (CLB) versions are available.

## 7 Terminal Configuration and Functions

### 7.1 引脚图

图 7-1 显示了 48 引脚 PT 薄型四方扁平封装 (LQFP) 引脚分配。图 7-2 显示了 38 引脚 DA 薄型小外形尺寸封装 (TSSOP) 引脚分配。

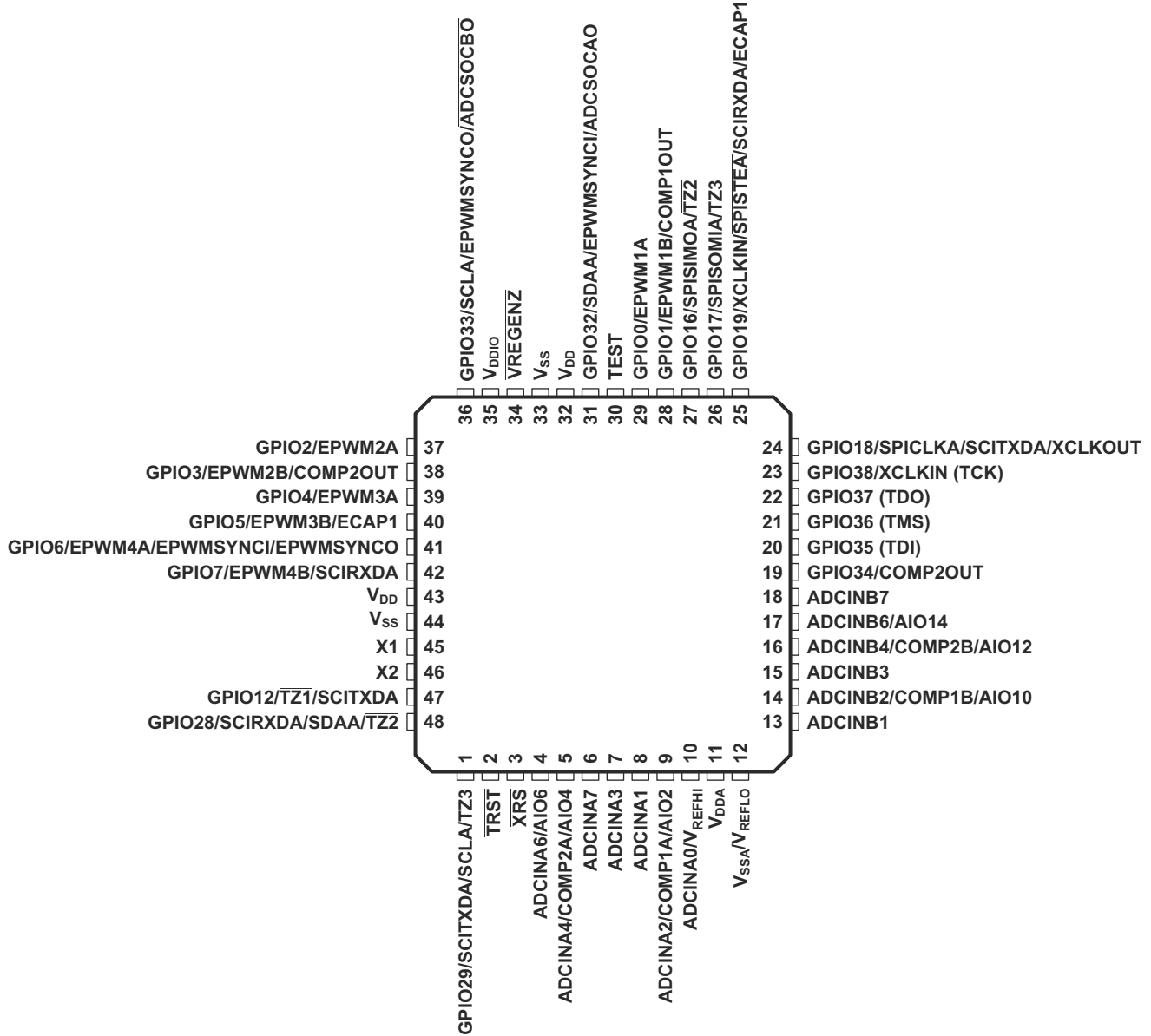


图 7-1. 2802x 48 引脚 PT LQFP (顶视图)



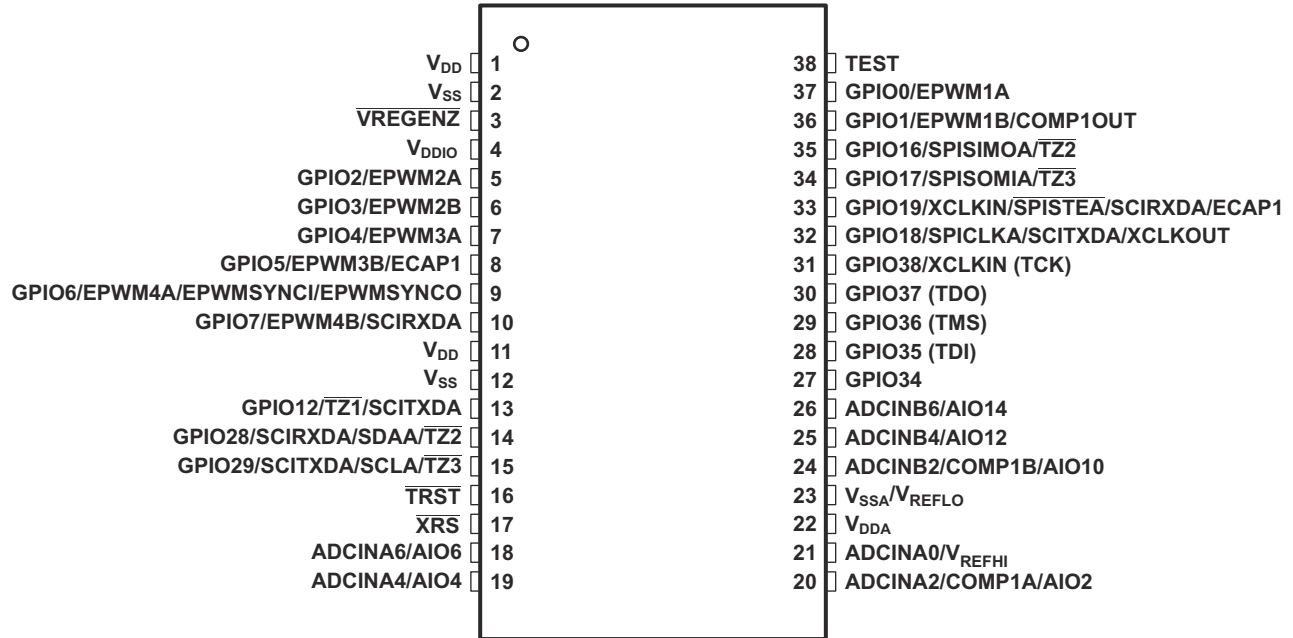


图 7-2. 2802x 38 引脚 DA TSSOP ( 顶视图 )

## 7.2 信号说明

节 7.2.1 对这些信号进行了说明。除 JTAG 引脚以外，除非另有说明，否则 GPIO 功能是复位时的默认功能。它们下面列出的外设信号是供替换的功能。有些外设功能并不在所有器件上提供。有关详细信息，请参阅表 6-1。输入不可承受 5V 电压。所有 GPIO 引脚为 I/O/Z 且有一个内部上拉电阻，在每个引脚上可选择性启用/禁用此电阻。这一特性只适用于 GPIO 引脚。复位时不启用 PWM 引脚上的上拉电阻。复位后启用其他 GPIO 引脚上的上拉电阻。AIO 引脚没有内部上拉电阻。

### 备注

使用片上 VREG 时，GPIO19、GPIO34、GPIO35、GPIO36、GPIO37 和 GPIO38 引脚在上电期间可能有毛刺。这种潜在的毛刺将在读取引导模式引脚之前结束，不会影响引导行为。如果应用不能接受毛刺，可从外部提供 1.8V 电源。或者添加一个与这些引脚串联的限流电阻（例如 470  $\Omega$ ），可考虑使用外部驱动器限制降级到引脚和/或外部电路的可能性。当使用外部 1.8V 电源时，无需电源时序。然而，如果 I/O 引脚的电平转换输出缓冲器中的 3.3V 晶体管在 1.8V 晶体管之前上电，输出缓冲器有可能打开，这会导致上电期间引脚上出现毛刺。为了避免这种情况，V<sub>DD</sub> 引脚应早于 V<sub>DDIO</sub> 引脚或与之同时上电，确保 V<sub>DD</sub> 引脚在 V<sub>DDIO</sub> 引脚达到 0.7V 之前达到 0.7V。

### 7.2.1 信号说明

| 终端                |            |            | I/O/Z | 说明                                                                                                                                                                                                                                                                                                       |
|-------------------|------------|------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 名称 <sup>(1)</sup> | PT<br>引脚编号 | DA<br>引脚编号 |       |                                                                                                                                                                                                                                                                                                          |
| JTAG              |            |            |       |                                                                                                                                                                                                                                                                                                          |
| TRST              | 2          | 16         | I     | 具有内部下拉电阻的 JTAG 测试复位。驱动为高电平时， $\overline{\text{TRST}}$ 交由扫描系统控制器件的运行。如果此信号未连接或驱动为低电平，则器件将在功能模式下工作，测试复位信号将被忽略。<br><b>注意：</b> $\overline{\text{TRST}}$ 是高电平有效的测试引脚，在器件正常工作期间必须始终保持低电平。此引脚上需要一个外部上拉电阻。此电阻的值应该基于设计适用的调试器 Pod 的驱动强度。一个 2.2k $\Omega$ 电阻器一般可提供足够的保护。由于这是特定于应用的，所以 TI 建议验证每个目标板是否能正常运行调试器和应用。(↓) |
| TCK               | 参阅 GPIO38  |            | I     | 参阅 GPIO38。带有内部上拉电阻的 JTAG 测试时钟 (↑)                                                                                                                                                                                                                                                                        |
| TMS               | 参阅 GPIO36  |            | I     | 参阅 GPIO36。带有内部上拉电阻的 JTAG 测试模式选择 (TMS)。此串行控制输入在 TCK 上升沿输入到 TAP 控制器。(↑)                                                                                                                                                                                                                                    |
| TDI               | 参阅 GPIO35  |            | I     | 参阅 GPIO35。带有内部上拉电阻的 JTAG 测试数据输入 (TDI)。TDI 在 TCK 的上升沿输入到选择的寄存器 (指令或数据)。(↑)                                                                                                                                                                                                                                |
| TDO               | 参阅 GPIO37  |            | O/Z   | 参阅 GPIO37。JTAG 扫描输出，测试数据输出 (TDO)。所选寄存器 (指令或数据) 的内容在 TCK 下降沿从 TDO 移出。<br>(8mA 驱动)                                                                                                                                                                                                                         |
| 闪存                |            |            |       |                                                                                                                                                                                                                                                                                                          |
| TEST              | 30         | 38         | I/O   | 测试引脚。为 TI 预留。必须保持未连接状态。                                                                                                                                                                                                                                                                                  |

| 终端                        |                    |            | I/O/Z    | 说明                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------------|--------------------|------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 名称 <sup>(1)</sup>         | PT<br>引脚编号         | DA<br>引脚编号 |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 时钟                        |                    |            |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| XCLKOUT                   | 参阅 GPIO18          |            | O/Z      | 参阅 GPIO18。源自 SYSCLKOUT 的输出时钟。XCLKOUT 频率要么与 SYSCLKOUT 的频率相同，要么是后者的一半或四分之一。这通过 XCLK 寄存器中的位 1:0 (XCLKOUTDIV) 控制。复位时，XCLKOUT = SYSCLKOUT/4。通过将 XCLKOUTDIV 设定为 3，可关闭 XCLKOUT 信号。GPIO18 的多路复用器控制也必须设定为 XCLKOUT，才能使此信号传播到引脚。                                                                                                                                                                                                                                         |
| XCLKIN                    | 参阅 GPIO19 和 GPIO38 |            | I        | 参阅 GPIO19 和 GPIO38。外部振荡器输入。时钟的引脚源由 XCLK 寄存器内的 XCLKINSEL 位控制，默认选择 GPIO38。此引脚馈送来自外部 3.3V 振荡器的时钟。在这种情况下，X1 引脚（如果可用）必须连接至 GND，而且必须通过 CLKCTL 寄存器内的 14 位禁用片上晶体振荡器。如果使用晶振/谐振器，必须通过 CLKCTL 寄存器内的 13 位禁用 XCLKIN 路径。<br><b>注意：</b> 使用 GPIO38/TCK/XCLKIN 引脚提供外部时钟以使器件正常工作的设计可能需要集成一些挂钩，以便在使用 JTAG 连接器调试期间禁用此路径。这是为了防止 JTAG 调试会话期间活动的 TCK 信号相互竞争。此时可使用零引脚内部振荡器为器件计时。                                                                                                      |
| X1                        | 45                 | -          | I        | 1.8V 片上晶体振荡器输入。要使用此振荡器，必须在 X1 和 X2 之间连接一个石英晶振或陶瓷谐振器。在这种情况下，必须通过 CLKCTL 寄存器内的 13 位禁用 XCLKIN 路径。如果此引脚未使用，必须连接至 GND。(I)                                                                                                                                                                                                                                                                                                                                          |
| X2                        | 46                 | -          | O        | 片上晶体振荡器输出。必须在 X1 和 X2 之间连接一个石英晶振或陶瓷谐振器。如果 X2 未使用，必须保持未连接状态。(O)                                                                                                                                                                                                                                                                                                                                                                                                |
| 复位                        |                    |            |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| XRS                       | 3                  | 17         | I/OD     | 器件复位（进）和看门狗复位（出）。这些器件具有内置上电复位 (POR) 电路和欠压复位 (BOR) 电路。在上电或欠压情况下，此引脚由器件驱动为低电平。外部电路也可能驱动此引脚使器件复位生效。发生看门狗复位时，此引脚也由 MCU 驱动为低电平。在看门狗复位期间，XRS 引脚在 512 个 OSCCLK 周期的看门狗复位持续时间内被驱动为低电平。应在 XRS 和 VDDIO 之间放置一个值为 2.2kΩ 至 10kΩ 的电阻器。如果在 XRS 和 VSS 之间放置一个电容器进行噪声滤除，则该电容器的值应为 100nF 或更小。当看门狗复位生效时，这些值将能让看门狗在 512 个 OSCCLK 周期内正确地将 XRS 引脚驱动至 VOL。任何源头的器件复位都会导致器件终止执行。程序计数器指向位置 0x3F FFC0 包含的地址。当复位失效时，从程序计数器指定的位置开始执行。此引脚的输出缓冲器是一个有内部上拉电阻的开漏器件。(†) 如果此引脚由外部器件驱动，则应使用开漏器件进行驱动。 |
| ADC、比较器、模拟 I/O            |                    |            |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| ADCINA7                   | 6                  | -          | I        | ADC 组 A，通道 7 输入                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| ADCINA6<br>AIO6           | 4                  | 18         | I<br>I/O | ADC 组 A，通道 6 输入<br>数字 AIO 6                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| ADCINA4<br>COMP2A<br>AIO4 | 5                  | 19         | I<br>I/O | ADC 组 A，通道 4 输入<br>比较器输入 2A（只在 48 引脚器件内可用）<br>数字 AIO 4                                                                                                                                                                                                                                                                                                                                                                                                        |
| ADCINA3                   | 7                  | -          | I        | ADC 组 A，通道 3 输入                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| ADCINA2<br>COMP1A<br>AIO2 | 9                  | 20         | I<br>I/O | ADC 组 A，通道 2 输入<br>比较器输入 1A<br>数字 AIO 2                                                                                                                                                                                                                                                                                                                                                                                                                       |
| ADCINA1                   | 8                  | -          | I        | ADC 组 A，通道 1 输入                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| ADCINA0<br>VREFHI         | 10                 | 21         | I<br>I   | ADC 组 A，通道 0 输入<br>ADC 外部基准高 - 仅在 ADC 外部基准模式下使用。参阅节 9.9.1.1，ADC。                                                                                                                                                                                                                                                                                                                                                                                              |
| ADCINB7                   | 18                 | -          | I        | ADC 组 B，通道 7 输入                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| ADCINB6<br>AIO14          | 17                 | 26         | I<br>I/O | ADC 组 B，通道 6 输入<br>数字 AIO 14                                                                                                                                                                                                                                                                                                                                                                                                                                  |

| 终端                        |            |            | I/O/Z | 说明                                                                                                 |
|---------------------------|------------|------------|-------|----------------------------------------------------------------------------------------------------|
| 名称 <sup>(1)</sup>         | PT<br>引脚编号 | DA<br>引脚编号 |       |                                                                                                    |
| ADCINB4                   | 16         | 25         | I     | ADC 组 B，通道 4 输入                                                                                    |
| COMP2B                    |            |            | I     | 比较器输入 2B ( 只在 48 引脚器件内可用 )                                                                         |
| AIO12                     |            |            | I/O   | 数字 AIO 12                                                                                          |
| ADCINB3                   | 15         | -          | I     | ADC 组 B，通道 3 输入                                                                                    |
| ADCINB2                   | 14         | 24         | I     | ADC 组 B，通道 2 输入                                                                                    |
| COMP1B                    |            |            | I     | 比较器输入 1B                                                                                           |
| AIO10                     |            |            | I/O   | 数字 AIO 10                                                                                          |
| ADCINB1                   | 13         | -          | I     | ADC 组 B，通道 1 输入                                                                                    |
| CPU 和 I/O 电源              |            |            |       |                                                                                                    |
| V <sub>DDA</sub>          | 11         | 22         |       | 模拟电源引脚。在此引脚附近连接一个 2.2 μF 电容器 ( 典型值 )。                                                              |
| V <sub>SSA</sub>          | 12         | 23         | I     | 模拟接地引脚                                                                                             |
| V <sub>REFLO</sub>        |            |            |       | ADC 外部基准低 ( 始终接地 )                                                                                 |
| V <sub>DD</sub>           | 32         | 1          |       | CPU 和逻辑数字电源引脚。使用内部 VREG 时，在每个 V <sub>DD</sub> 引脚和接地之间放置一个 1.2μF 电容器。可使用值较高的电容器。                    |
|                           | 43         | 11         |       |                                                                                                    |
| V <sub>DDIO</sub>         | 35         | 4          |       | 数字 I/O 缓冲器和闪存电源引脚。启用 VREG 时使用单电源。在此引脚上放置一个去耦电容器。确切值应由系统电压调节解决方案决定。                                 |
| V <sub>SS</sub>           | 33         | 2          |       | 数字接地引脚                                                                                             |
|                           | 44         | 12         |       |                                                                                                    |
| 稳压器控制信号                   |            |            |       |                                                                                                    |
| V <sub>REGENZ</sub>       | 34         | 3          | I     | 具有内部下拉电阻的内部稳压器 (VREG) 使能。直接连接到 VSS ( 低 ) 以启用内部 1.8V VREG。直接连接到 VDDIO ( 高 ) 以禁用 VREG 并使用外部 1.8V 电源。 |
| GPIO 和外设信号 <sup>(2)</sup> |            |            |       |                                                                                                    |
| GPIO0                     | 29         | 37         | I/O/Z | 通用输入/输出 0                                                                                          |
| EPWM1A                    |            |            | O     | 增强型 PWM1 输出 A 和 HRPWM 通道                                                                           |
| -                         |            |            | -     | -                                                                                                  |
| -                         |            |            | -     | -                                                                                                  |
| GPIO1                     | 28         | 36         | I/O/Z | 通用输入/输出 1                                                                                          |
| EPWM1B                    |            |            | O     | 增强型 PWM1 输出 B                                                                                      |
| -                         |            |            | -     | -                                                                                                  |
| COMP1OUT                  |            |            | O     | 比较器 1 的直接输出                                                                                        |
| GPIO2                     | 37         | 5          | I/O/Z | 通用输入/输出 2                                                                                          |
| EPWM2A                    |            |            | O     | 增强型 PWM2 输出 A 和 HRPWM 通道                                                                           |
| -                         |            |            | -     | -                                                                                                  |
| -                         |            |            | -     | -                                                                                                  |
| GPIO3                     | 38         | 6          | I/O/Z | 通用输入/输出 3                                                                                          |
| EPWM2B                    |            |            | O     | 增强型 PWM2 输出 B                                                                                      |
| -                         |            |            | -     | -                                                                                                  |
| COMP2OUT                  |            |            | O     | 比较器 2 的直接输出 ( 只在 48 引脚器件内可用 )                                                                      |
| GPIO4                     | 39         | 7          | I/O/Z | 通用输入/输出 4                                                                                          |
| EPWM3A                    |            |            | O     | 增强型 PWM3 输出 A 和 HRPWM 通道                                                                           |
| -                         |            |            | -     | -                                                                                                  |
| -                         |            |            | -     | -                                                                                                  |

| 终端                                                         |            |            | I/O/Z                             | 说明                                                                                                                                                                                                                                                         |
|------------------------------------------------------------|------------|------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 名称 <sup>(1)</sup>                                          | PT<br>引脚编号 | DA<br>引脚编号 |                                   |                                                                                                                                                                                                                                                            |
| <b>GPIO5</b><br>EPWM3B<br>-<br>ECAP1                       | 40         | 8          | I/O/Z<br>O<br><br>I/O             | 通用输入/输出 5<br>增强型 PWM3 输出 B<br>-<br>增强型捕捉输入/输出 1                                                                                                                                                                                                            |
| <b>GPIO6</b><br>EPWM4A<br>EPWMSYNCl<br>EPWMSYNCO           | 41         | 9          | I/O/Z<br>O<br>I<br>O              | 通用输入/输出 6<br>增强型 PWM4 输出 A 和 HRPWM 通道<br>外部 ePWM 同步脉冲输入<br>外部 ePWM 同步脉冲输出                                                                                                                                                                                  |
| <b>GPIO7</b><br>EPWM4B<br>SCIRXDA<br>-                     | 42         | 10         | I/O/Z<br>O<br>I<br>-              | 通用输入/输出 7<br>增强型 PWM4 输出 B<br>SCI-A 接收数据<br>-                                                                                                                                                                                                              |
| <b>GPIO12</b><br>TZ1<br>SCITXDA<br>-                       | 47         | 13         | I/O/Z<br>I<br>O<br>-              | 通用输入/输出 12<br>跳闸区输入 1<br>SCI-A 发送数据<br>-                                                                                                                                                                                                                   |
| <b>GPIO16</b><br>SPISIMOA<br>-<br>TZ2                      | 27         | 35         | I/O/Z<br>I/O<br><br>I             | 通用输入/输出 16<br>SPI 从器件输入, 主器件输出<br>-<br>跳闸区输入 2                                                                                                                                                                                                             |
| <b>GPIO17</b><br>SPISOMIA<br>-<br>TZ3                      | 26         | 34         | I/O/Z<br>I/O<br><br>I             | 通用输入/输出 17<br>SPI-A 从器件输出, 主器件输入<br>-<br>跳闸区输入 3                                                                                                                                                                                                           |
| <b>GPIO18</b><br>SPICLKA<br>SCITXDA<br>XCLKOUT             | 24         | 32         | I/O/Z<br>I/O<br>O<br>O/Z          | 通用输入/输出 18<br>SPI-A 时钟输入/输出<br>SCI-A 发送<br>源自 SYSCLKOUT 的输出时钟。XCLKOUT 频率要么与 SYSCLKOUT 的频率相同, 要么是后者的一半或四分之一。这通过 XCLK 寄存器中的位 1:0 (XCLKOUTDIV) 控制。复位时, XCLKOUT = SYSCLKOUT/4。通过将 XCLKOUTDIV 设定为 3, 可关闭 XCLKOUT 信号。GPIO18 的多路复用器控制也必须设定为 XCLKOUT, 才能使此信号传播到引脚。 |
| <b>GPIO19</b><br>XCLKIN<br><br>SPISTEA<br>SCIRXDA<br>ECAP1 | 25         | 33         | I/O/Z<br>I<br><br>I/O<br>I<br>I/O | 通用输入/输出 19<br>外部振荡器输入。此引脚到时钟块的路径不受此引脚的多路复用器功能控制。如果此路径用于其他外设功能, 必须注意不要启用此路径来计时。<br>SPI-A 从器件发送使能输入/输出<br>SCI-A 接收<br>增强型捕捉输入/输出 1                                                                                                                           |
| <b>GPIO28</b><br>SCIRXDA<br>SDAA<br>TZ2                    | 48         | 14         | I/O/Z<br>I<br>I/OD<br>I           | 通用输入/输出 28<br>SCI 接收数据<br>I2C 数据开漏双向端口<br>跳闸区输入 2                                                                                                                                                                                                          |

| 终端                                             |            |            | I/O/Z                   | 说明                                                                                                 |
|------------------------------------------------|------------|------------|-------------------------|----------------------------------------------------------------------------------------------------|
| 名称 <sup>(1)</sup>                              | PT<br>引脚编号 | DA<br>引脚编号 |                         |                                                                                                    |
| <b>GPIO29</b><br>SCITXDA<br>SCLA<br>TZ3        | 1          | 15         | I/O/Z<br>O<br>I/OD<br>I | 通用输入/输出 29。<br>SCI 发送数据<br>I2C 时钟开漏双向端口<br>跳闸区输入 3                                                 |
| <b>GPIO32</b><br>SDAA<br>EPWMSYNCl<br>ADCSOCAO | 31         | -          | I/O/Z<br>I/OD<br>I<br>O | 通用输入/输出 32<br>I2C 数据开漏双向端口<br>增强型 PWM 外部同步脉冲输入<br>ADC 转换启动 A                                       |
| <b>GPIO33</b><br>SCLA<br>EPWMSYNCO<br>ADCSOCBO | 36         | -          | I/O/Z<br>I/OD<br>O<br>O | 通用输入/输出 33<br>I2C 时钟开漏双向端口<br>增强型 PWM 外部同步脉冲输入<br>ADC 转换启动 B                                       |
| <b>GPIO34</b><br>COMP2OUT<br>-<br>-            | 19         | 27         | I/O/Z<br>O              | 通用输入/输出 34<br>比较器 2 的直接输出。在 DA 封装中，COMP2OUT 信号不可用。<br>-<br>-                                       |
| GPIO35<br>TDI                                  | 20         | 28         | I/O/Z<br>I              | 通用输入/输出 35<br>带有内部上拉电阻的 JTAG 测试数据输入 (TDI)。TDI 在 TCK 的上升沿输入到选择的寄存器 (指令或数据)                          |
| GPIO36<br>TMS                                  | 21         | 29         | I/O/Z<br>I              | 通用输入/输出 36<br>带有内部上拉电阻的 JTAG 测试模式选择 (TMS)。此串行控制输入在 TCK 上升沿输入到 TAP 控制器。                             |
| GPIO37<br>TDO                                  | 22         | 30         | I/O/Z<br>O/Z            | 通用输入/输出 37<br>JTAG 扫描输出，测试数据输出 (TDO)。所选寄存器 (指令或数据) 的内容在 TCK 下降沿从 TDO 移出 (8mA 驱动)                   |
| GPIO38<br>TCK<br>XCLKIN                        | 23         | 31         | I/O/Z<br>I<br>I         | 通用输入/输出 38<br>带有内部上拉电阻的 JTAG 测试时钟<br>外部振荡器输入。此引脚到时钟块的路径不受此引脚的多路复用器功能控制。如果此路径用于其他功能，必须注意不要启用此路径来计时。 |

(1) I = 输入, O = 输出, Z = 高阻抗, OD = 开漏, ↑ = 上拉, ↓ = 下拉

(2) GPIO 功能 (以粗斜体显示) 在复位时为默认值。它们下面列出的外设信号是供替换的功能。对于 GPIO 功能多路复用的 JTAG 引脚, 输入到 GPIO 块的路径始终有效。根据 TRST 信号条件, 启用/禁用从 GPIO 块输出的路径和从一个引脚到 JTAG 块的路径。有关详细信息, 请参阅 [TMS320F2802x](#)、[TMS320F2802xx](#) [技术参考手册](#) 中的“系统控制”一章。

## 8 规格

### 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                                     |                                                                                                                                                               | MIN   | MAX | UNIT |
|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|------|
| Supply voltage                      | V <sub>DDIO</sub> (I/O and Flash) with respect to V <sub>SS</sub>                                                                                             | - 0.3 | 4.6 | V    |
|                                     | V <sub>DD</sub> with respect to V <sub>SS</sub>                                                                                                               | - 0.3 | 2.5 |      |
| Analog voltage                      | V <sub>DDA</sub> with respect to V <sub>SSA</sub>                                                                                                             | - 0.3 | 4.6 | V    |
| Input voltage                       | V <sub>IN</sub> (3.3 V)                                                                                                                                       | - 0.3 | 4.6 | V    |
|                                     | V <sub>IN</sub> (X1)                                                                                                                                          | - 0.3 | 2.5 |      |
| Output voltage                      | V <sub>O</sub>                                                                                                                                                | - 0.3 | 4.6 | V    |
| Input clamp current                 | Digital/analog input (per pin), I <sub>IK</sub><br>(V <sub>IN</sub> < V <sub>SS</sub> or V <sub>IN</sub> > V <sub>DDIO</sub> ) <sup>(3)</sup>                 | - 20  | 20  | mA   |
|                                     | Analog input (per pin), I <sub>IKANALOG</sub><br>(V <sub>IN</sub> < V <sub>SSA</sub> or V <sub>IN</sub> > V <sub>DDA</sub> )                                  | - 20  | 20  |      |
|                                     | Total for all inputs, I <sub>IKTOTAL</sub><br>(V <sub>IN</sub> < V <sub>SS</sub> /V <sub>SSA</sub> or V <sub>IN</sub> > V <sub>DDIO</sub> /V <sub>DDA</sub> ) | - 20  | 20  |      |
| Output clamp current                | I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DDIO</sub> )                                                                                   | - 20  | 20  | mA   |
| Junction temperature <sup>(4)</sup> | T <sub>J</sub>                                                                                                                                                | - 40  | 150 | °C   |
| Storage temperature <sup>(4)</sup>  | T <sub>stg</sub>                                                                                                                                              | - 65  | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 8.4 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V<sub>SS</sub>, unless otherwise noted.
- (3) Continuous clamp current per pin is  $\pm 2$  mA. Do not operate in this condition continuously as V<sub>DDIO</sub>/V<sub>DDA</sub> voltage may internally rise and impact other electrical specifications.
- (4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see [Semiconductor and IC Package Thermal Metrics](#); [Calculating Useful Lifetimes of Embedded Processors](#); and [Calculating FIT for a Mission Profile](#).

### 8.2 ESD 等级 - 汽车

|                                                                                                                   |                                              |                                          | 值     | 单位 |
|-------------------------------------------------------------------------------------------------------------------|----------------------------------------------|------------------------------------------|-------|----|
| 采用 48 引脚 PT 封装的 TMS320F28027-Q1、TMS320F28027F-Q1、TMS320F28026-Q1、TMS320F28026F-Q1、TMS320F28023-Q1、TMS320F28022-Q  |                                              |                                          |       |    |
| V <sub>(ESD)</sub> 静电放电                                                                                           | 人体放电模型 (HBM), 符合 AEC Q100-002 <sup>(1)</sup> | 所有引脚                                     | ±2000 | V  |
|                                                                                                                   | 充电器件模型 (CDM), 符合 AEC Q100-011                | 除边角引脚以外的所有引脚                             | ±500  |    |
|                                                                                                                   |                                              | 48 引脚 PT 上的转角引脚 : 1、12、13、24、25、36、37、48 | ±750  |    |
| 采用 38 引脚 DA 封装的 TMS320F28027-Q1、TMS320F28027F-Q1、TMS320F28026-Q1、TMS320F28026F-Q1、TMS320F28023-Q1、TMS320F28022-Q1 |                                              |                                          |       |    |
| V <sub>(ESD)</sub> 静电放电                                                                                           | 人体放电模型 (HBM), 符合 AEC Q100-002 <sup>(1)</sup> | 所有引脚                                     | ±2000 | V  |
|                                                                                                                   | 充电器件模型 (CDM), 符合 AEC Q100-011                | 除边角引脚以外的所有引脚                             | ±500  |    |
|                                                                                                                   |                                              | 38 引脚 DA 上的转角引脚 : 1、19、20、38             | ±750  |    |

- (1) AEC Q100-002 指示应当按照 ANSI/ESDA/JEDEC JS-001 规范执行 HBM 应力测试。



### 8.3 ESD 等级 - 商用

|                                                                                                                                                           |                                                                               | 值     | 单位 |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-------|----|
| 采用 48 引脚 PT 封装的 TMS320F28027-Q1、TMS320F28027F-Q1、TMS320F28026-Q1、TMS320F28026F-Q1、TMS320F28023-Q1、TMS320F28022-Q1、TMS320F28021、TMS320F28020、TMS320F280200 |                                                                               |       |    |
| V <sub>(ESD)</sub> 静电放电                                                                                                                                   | 人体放电模型 (HBM), 符合 ANSI/ESDA/JEDEC JS-001 标准 <sup>(1)</sup>                     | ±2000 | V  |
|                                                                                                                                                           | 充电器件模型 (CDM), 符合 JEDEC 规范 JESD22-C101 或 ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±500  |    |
| 采用 38 引脚 DA 封装的 TMS320F28027-Q1、TMS320F28027F-Q1、TMS320F28026-Q1、TMS320F28026F-Q1、TMS320F28023-Q1、TMS320F28022-Q1、TMS320F28021、TMS320F28020、TMS320F280200 |                                                                               |       |    |
| V <sub>(ESD)</sub> 静电放电                                                                                                                                   | 人体放电模型 (HBM), 符合 ANSI/ESDA/JEDEC JS-001 标准 <sup>(1)</sup>                     | ±2000 | V  |
|                                                                                                                                                           | 充电器件模型 (CDM), 符合 JEDEC 规范 JESD22-C101 或 ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±500  |    |

(1) JEDEC 文件 JEP155 规定: 500V HBM 可实现在标准 ESD 控制流程下安全生产。

(2) JEDEC 文档 JEP157 指出: 250V CDM 可实现在标准 ESD 控制流程下安全生产。

### 8.4 建议工作条件

|                                                      |                         | 最小值          | 标称值 | 最大值            | 单位  |
|------------------------------------------------------|-------------------------|--------------|-----|----------------|-----|
| 器件电源电压, I/O, $V_{DDIO}$ <sup>(1)</sup>               |                         | 2.97         | 3.3 | 3.63           | V   |
| 器件电源电压 CPU, $V_{DD}$ ( 当内部 VREG 禁用并且由 1.8V 电源外部供电时 ) |                         | 1.71         | 1.8 | 1.995          | V   |
| 电源接地, $V_{SS}$                                       |                         |              | 0   |                | V   |
| 模拟电源电压, $V_{DDA}$                                    |                         | 2.97         | 3.3 | 3.63           | V   |
| 模拟接地, $V_{SSA}$                                      |                         |              | 0   |                | V   |
| 器件时钟频率 ( 系统时钟 )                                      | 28020、28021、280200      | 2            |     | 40             | MHz |
|                                                      | 28022、28023             | 2            |     | 50             |     |
|                                                      | 28026、28027             | 2            |     | 60             |     |
| 高电平输入电压, $V_{IH}$ (3.3V)                             |                         | 2            |     | $V_{DDIO}+0.3$ | V   |
| 低电平输入电压, $V_{IL}$ (3.3V)                             |                         | $V_{SS}-0.3$ |     | 0.8            | V   |
| 高电平输出源电流, $V_{OH}=V_{OH}$ ( 最小值 ) , $I_{OH}$         | 所有 GPIO/AIO 引脚          |              |     | -4             | mA  |
|                                                      | 组 2 <sup>(2)</sup>      |              |     | -8             | mA  |
| 低电平输出灌电流, $V_{OL}=V_{OL}$ ( 最大值 ) , $I_{OL}$         | 所有 GPIO/AIO 引脚          |              |     | 4              | mA  |
|                                                      | 组 2 <sup>(2)</sup>      |              |     | 8              | mA  |
| 结温, $T_J$ <sup>(3)</sup>                             | T 版本                    | -40          |     | 105            | °C  |
|                                                      | S 版本                    | -40          |     | 125            |     |
|                                                      | Q 版本<br>( AEC Q100 认证 ) | -40          |     | 125            |     |

(1) 如果 BOR 未被使用, 那么  $V_{DDIO}$  可使用一个 ±10% 的容差。有关详细信息, 请参阅 [TMS320F2802x](#)、[TMS320F2802xx MCU 器件勘误表](#)。如果 BOR 被启用,  $V_{DDIO}$  的容差为 ±5%。

(2) 组 2 引脚如下所示: GPIO16、GPIO17、GPIO18、GPIO19、GPIO28、GPIO29、GPIO36、GPIO37

(3)  $T_A$  ( 环境温度 ) 取决于产品 and 应用, 可达到器件的指定  $T_J$  最大值。热性能设计注意事项, 请参阅节 8.8。



## 8.5 功耗摘要

### 8.5.1 TMS320F2802x/F280200 在 40MHz SYSCLKOUT 下的电流消耗

| 模式 <sup>(1)</sup> | 测试条件                                                                                                                                                                                                                  | VREG 启用                          |      |                                 |       | VREG 禁用            |      |                                  |        |                                 |       |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|------|---------------------------------|-------|--------------------|------|----------------------------------|--------|---------------------------------|-------|
|                   |                                                                                                                                                                                                                       | I <sub>DDIO</sub> <sup>(2)</sup> |      | I <sub>DDA</sub> <sup>(3)</sup> |       | I <sub>DD</sub>    |      | I <sub>DDIO</sub> <sup>(2)</sup> |        | I <sub>DDA</sub> <sup>(3)</sup> |       |
|                   |                                                                                                                                                                                                                       | 典型值 <sup>(4)</sup>               | 最大值  | 典型值 <sup>(4)</sup>              | 最大值   | 典型值 <sup>(4)</sup> | 最大值  | 典型值 <sup>(4)</sup>               | 最大值    | 典型值 <sup>(4)</sup>              | 最大值   |
| 工作<br>( 闪存 )      | 启用下列外设时钟 :<br>• ePWM1/2/3/4<br>• eCAP1<br>• SCI-A<br>• SPI-A<br>• ADC<br>• I2C<br>• COMP1/2<br>• CPU Timer0/1/2<br><br>所有 PWM 引脚在 40kHz 下切换。<br>所有 I/O 引脚保持未连接状态。 <sup>(5)</sup><br>代码即将耗尽 1 个等待状态的闪存。<br>XCLKOUT 关闭。 | 70mA                             | 80mA | 13mA                            | 18mA  | 62mA               | 70mA | 15mA                             | 18mA   | 13mA                            | 18mA  |
| 空闲                | 闪存断电。<br>XCLKOUT 关闭。<br>所有外设时钟关闭。                                                                                                                                                                                     | 13mA                             | 16mA | 53 μA                           | 58 μA | 15mA               | 17mA | 120 μA                           | 400 μA | 53 μA                           | 58 μA |
| 待机                | 闪存断电。<br>外设时钟关闭。                                                                                                                                                                                                      | 3mA                              | 6mA  | 10 μA                           | 15 μA | 3mA                | 6mA  | 120 μA                           | 400 μA | 10 μA                           | 15 μA |
| 停机                | 闪存断电。<br>外设时钟关闭。<br>输入时钟禁用。 <sup>(6)</sup>                                                                                                                                                                            | 50 μA                            |      | 10 μA                           | 15 μA | 15 μA              |      | 25 μA                            |        | 10 μA                           | 15 μA |

- (1) 对于 TMS320F280200 器件，从节 8.5.1 中显示的工作模式的 I<sub>DD</sub> ( VREG 禁用 ) / I<sub>DDIO</sub> ( VREG 启用 ) 电流数字中减去 eCAP 的 I<sub>DD</sub> 电流数字 ( 参阅表 8-1 )。
- (2) I<sub>DDIO</sub> 电流取决于 I/O 引脚上的电力负载。
- (3) 要实现空闲、待机、停机模式下的 I<sub>DDA</sub> 电流，必须通过写入 PCLKCR0 寄存器来显式关闭 ADC 模块的时钟。
- (4) 典型值数字适用于室温和标称电压下。
- (5) 在循环中完成以下操作 :
  - 数据持续从 SPI-A 和 SCI-A 端口中发出。
  - 使用硬件乘法器。
  - 复位看门狗。
  - ADC 执行连续转换。
  - COMP1/2 是连续开关电压。
  - 切换 GPIO17。
- (6) 如果使用石英晶振或者陶瓷谐振器作为时钟源，停机模式将关闭片上晶体振荡器。

## 8.5.2 TMS320F2802x 在 50MHz SYSCLKOUT 下的电流消耗

| 模式           | 测试条件                                                                                                                                                                                                                   | VREG 启用                          |      |                                 |            | VREG 禁用         |      |                                  |             |                                 |            |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|------|---------------------------------|------------|-----------------|------|----------------------------------|-------------|---------------------------------|------------|
|              |                                                                                                                                                                                                                        | I <sub>DDIO</sub> <sup>(1)</sup> |      | I <sub>DDA</sub> <sup>(2)</sup> |            | I <sub>DD</sub> |      | I <sub>DDIO</sub> <sup>(1)</sup> |             | I <sub>DDA</sub> <sup>(2)</sup> |            |
|              |                                                                                                                                                                                                                        | 典型值<br>(3)                       | 最大值  | 典型值<br>(3)                      | 最大值        | 典型值<br>(3)      | 最大值  | 典型值<br>(3)                       | 最大值         | 典型值<br>(3)                      | 最大值        |
| 工作<br>( 闪存 ) | 启用下列外设时钟 :<br>• ePWM1/2/3/4<br>• eCAP1<br>• SCI-A<br>• SPI-A<br>• ADC<br>• I2C<br>• COMP1/2<br>• CPU Timer0/1/2<br><br>所有 PWM 引脚在 40kHz 下切换。<br>所有 I/O 引脚保持未连接状态。 <sup>(4)</sup><br>代码即将耗尽有 1 个等待状态的闪存。<br>XCLKOUT 关闭。 | 80mA                             | 90mA | 13mA                            | 18mA       | 71mA            | 80mA | 15mA                             | 18mA        | 13mA                            | 18mA       |
| 空闲           | 闪存断电。<br>XCLKOUT 关闭。<br>所有外设时钟关闭。                                                                                                                                                                                      | 16mA                             | 19mA | 64 $\mu$ A                      | 69 $\mu$ A | 17mA            | 20mA | 120 $\mu$ A                      | 400 $\mu$ A | 64 $\mu$ A                      | 69 $\mu$ A |
| 待机           | 闪存断电。<br>外设时钟关闭。                                                                                                                                                                                                       | 4mA                              | 7mA  | 10 $\mu$ A                      | 15 $\mu$ A | 4mA             | 7mA  | 120 $\mu$ A                      | 400 $\mu$ A | 10 $\mu$ A                      | 15 $\mu$ A |
| 停机           | 闪存断电。<br>外设时钟关闭。<br>输入时钟禁用。 <sup>(5)</sup>                                                                                                                                                                             | 50 $\mu$ A                       |      | 10 $\mu$ A                      | 15 $\mu$ A | 15 $\mu$ A      |      | 25 $\mu$ A                       |             | 10 $\mu$ A                      | 15 $\mu$ A |

- (1) I<sub>DDIO</sub> 电流取决于 I/O 引脚上的电力负载。
- (2) 要实现空闲、待机、停机模式下的 I<sub>DDA</sub> 电流，必须通过写入 PCLKCR0 寄存器来显式关闭 ADC 模块的时钟。
- (3) 典型值数字适用于室温和标称电压下。
- (4) 在循环中完成以下操作 :
  - 数据持续从 SPI-A 和 SCI-A 端口中发出。
  - 使用硬件乘法器。
  - 复位看门狗。
  - ADC 执行连续转换。
  - COMP1/2 是连续开关电压。
  - 切换 GPIO17。
- (5) 如果使用石英晶振或者陶瓷谐振器作为时钟源，停机模式将关闭片上晶体振荡器。

### 8.5.3 TMS320F2802x 在 60MHz SYSCLKOUT 下的电流消耗

| 模式         | 测试条件                                                                                                                                                                                                         | VREG 启用                          |       |                                 |            | VREG 禁用            |      |                                  |             |                                 |            |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|-------|---------------------------------|------------|--------------------|------|----------------------------------|-------------|---------------------------------|------------|
|            |                                                                                                                                                                                                              | I <sub>DDIO</sub> <sup>(1)</sup> |       | I <sub>DDA</sub> <sup>(2)</sup> |            | I <sub>DD</sub>    |      | I <sub>DDIO</sub> <sup>(1)</sup> |             | I <sub>DDA</sub> <sup>(2)</sup> |            |
|            |                                                                                                                                                                                                              | 典型值 <sup>(3)</sup>               | 最大值   | 典型值 <sup>(3)</sup>              | 最大值        | 典型值 <sup>(3)</sup> | 最大值  | 典型值 <sup>(3)</sup>               | 最大值         | 典型值 <sup>(3)</sup>              | 最大值        |
| 工作<br>(闪存) | 启用下列外设时钟：<br>• ePWM1/2/3/4<br>• eCAP1<br>• SCI-A<br>• SPI-A<br>• ADC<br>• I2C<br>• COMP1/2<br>• CPU-TIMER0/1/2<br><br>所有 PWM 引脚在 60kHz 下切换。<br>所有 I/O 引脚保持未连接状态。<br>(4)<br>代码即将耗尽 2 个等待状态的闪存。<br>XCLKOUT 关闭。 | 90mA                             | 100mA | 13mA                            | 18mA       | 80mA               | 90mA | 15mA                             | 18mA        | 13mA                            | 18mA       |
| 空闲         | 闪存断电。<br>XCLKOUT 关闭。<br>所有外设时钟关闭。                                                                                                                                                                            | 18mA                             | 23mA  | 75 $\mu$ A                      | 80 $\mu$ A | 19mA               | 24mA | 120 $\mu$ A                      | 400 $\mu$ A | 75 $\mu$ A                      | 80 $\mu$ A |
| 待机         | 闪存断电。<br>外设时钟关闭。                                                                                                                                                                                             | 4mA                              | 7mA   | 10 $\mu$ A                      | 15 $\mu$ A | 4mA                | 7mA  | 120 $\mu$ A                      | 400 $\mu$ A | 10 $\mu$ A                      | 15 $\mu$ A |
| 停机         | 闪存断电。<br>外设时钟关闭。<br>输入时钟禁用。(5)                                                                                                                                                                               | 50 $\mu$ A                       |       | 10 $\mu$ A                      | 15 $\mu$ A | 15 $\mu$ A         |      | 25 $\mu$ A                       |             | 10 $\mu$ A                      | 15 $\mu$ A |

- (1) I<sub>DDIO</sub> 电流取决于 I/O 引脚上的电力负载。
- (2) 要实现空闲、待机、停机模式下的 I<sub>DDA</sub> 电流，必须通过写入 PCLKCR0 寄存器来显式关闭 ADC 模块的时钟。
- (3) 典型值数字适用于室温和标称电压下。
- (4) 在循环中完成以下操作：
- 数据持续从 SPI-A 和 SCI-A 端口中发出。
  - 使用硬件乘法器。
  - 复位看门狗。
  - ADC 执行连续转换。
  - COMP1/2 是连续开关电压。
  - 切换 GPIO17。
- (5) 如果使用石英晶振或者陶瓷谐振器作为时钟源，停机模式将关闭片上晶体振荡器。

#### 备注

器件中实现的外设 I/O 多路复用可防止同时使用所有可用外设。这是因为多个外设功能可能共享一个 I/O 引脚。然而，可同时打开所有外设的时钟，不过此配置并无用处。如果这么做，器件消耗的电流将大于电流消耗表中指定的数值。

## 8.5.4 Reducing Current Consumption

The 2802x/280200 devices incorporate a method to reduce the device current consumption. Because each peripheral unit has an individual clock-enable bit, significant reduction in current consumption can be achieved by turning off the clock to any peripheral module that is not used in a given application. Furthermore, any one of the three low-power modes could be taken advantage of to reduce the current consumption even further. 表 8-1 indicates the typical reduction in current consumption achieved by turning off the clocks.

**表 8-1. Typical Current Consumption by Various  
Peripherals (at 60 MHz)**

| PERIPHERAL<br>MODULE <sup>(1) (3)</sup> | I <sub>DD</sub> CURRENT<br>REDUCTION (mA) |
|-----------------------------------------|-------------------------------------------|
| ADC                                     | 2 <sup>(2)</sup>                          |
| I2C                                     | 3                                         |
| ePWM                                    | 2                                         |
| eCAP                                    | 2                                         |
| SCI                                     | 2                                         |
| SPI                                     | 2                                         |
| COMP/DAC                                | 1                                         |
| HRPWM                                   | 3                                         |
| CPU-TIMER                               | 1                                         |
| Internal zero-pin oscillator            | 0.5                                       |

- (1) All peripheral clocks (except CPU Timer clocks) are disabled upon reset. Writing to/reading from peripheral registers is possible only after the peripheral clocks are turned on.
- (2) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I<sub>DDA</sub>) as well.
- (3) For peripherals with multiple instances, the current quoted is per module. For example, the 2 mA value quoted for ePWM is for one ePWM module.

### 备注

I<sub>DDIO</sub> current consumption is reduced by 15 mA (typical) when XCLKOUT is turned off.

### 备注

The baseline I<sub>DD</sub> current (current when the core is executing a dummy loop with no peripherals enabled) is 45 mA, typical. To arrive at the I<sub>DD</sub> current for a given application, the current-drawn by the peripherals (enabled by that application) must be added to the baseline I<sub>DD</sub> current.

Following are other methods to reduce power consumption further:

- The flash module may be powered down if code is run off SARAM. This results in a current reduction of 18 mA (typical) in the V<sub>DD</sub> rail and 13 mA (typical) in the V<sub>DDIO</sub> rail.
- Savings in I<sub>DDIO</sub> may be realized by disabling the pullups on pins that assume an output function.
- To realize the lowest V<sub>DDA</sub> current consumption in a low-power mode, see the respective analog chapter of the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#) to ensure each module is powered down as well.

### 8.5.5 流耗图 (VREG 启用)

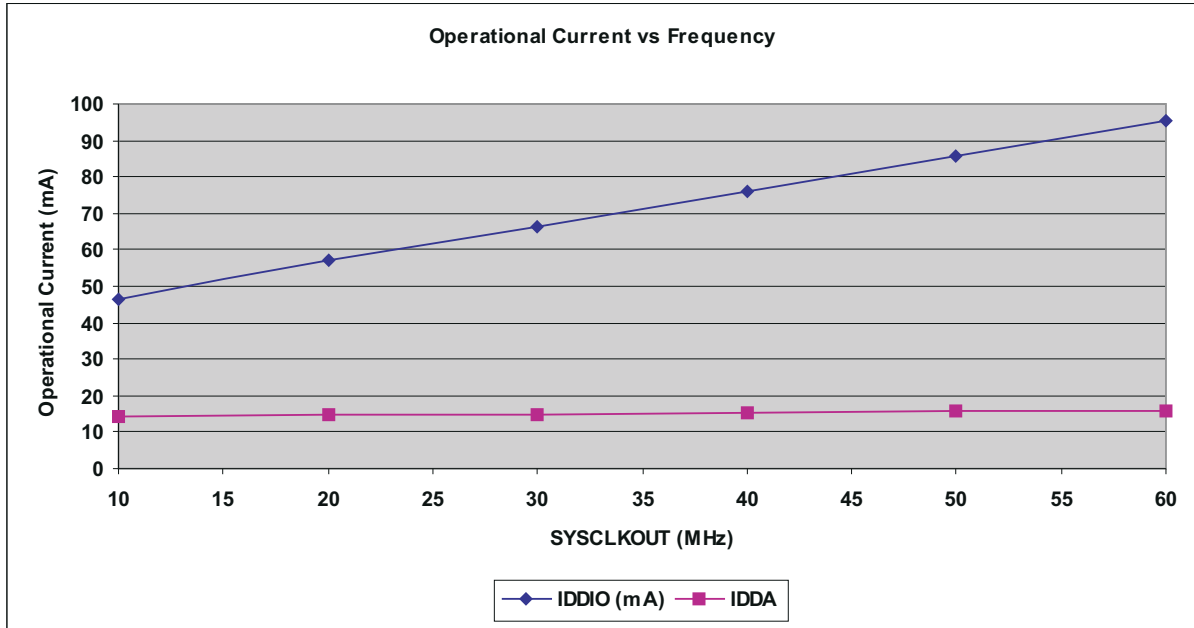


图 8-1. 典型运行电流与频率间的关系 (F2802x/F280200)

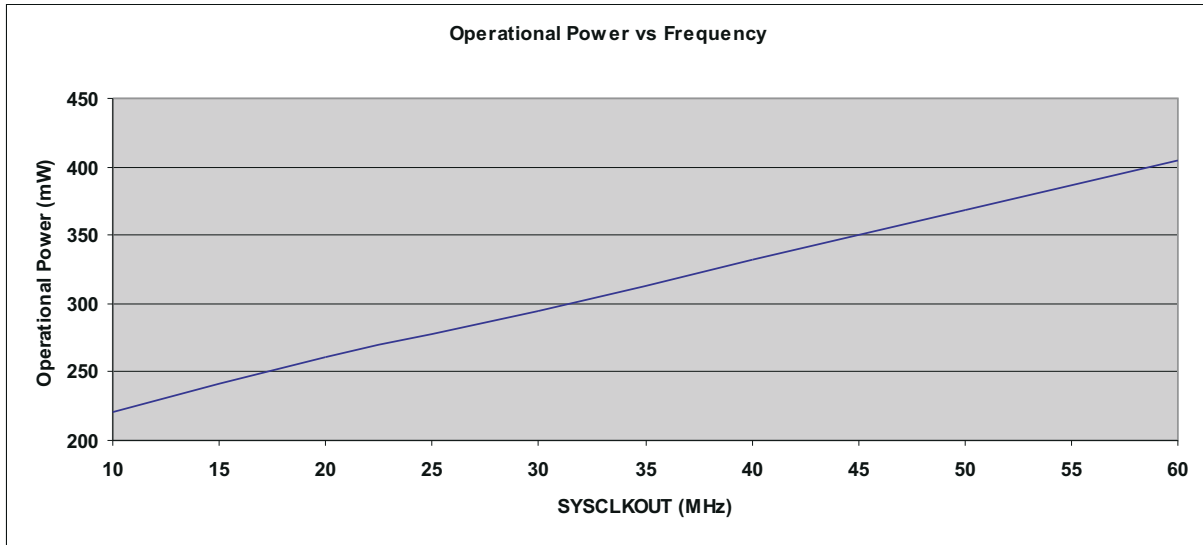


图 8-2. 典型运行功率与频率间的关系 (F2802x/F280200)

### 8.6 电气特性

在推荐的运行条件下 (除非另有说明) <sup>(1)</sup>

| 参数              |                 |                                      | 测试条件                                         |                        | 最小值  | 典型值  | 最大值  | 单位  |
|-----------------|-----------------|--------------------------------------|----------------------------------------------|------------------------|------|------|------|-----|
| V <sub>OH</sub> | 高电平输出电压         | I <sub>OH</sub> =I <sub>OH</sub> 最大值 |                                              | 2.4                    |      |      | V    |     |
|                 |                 | I <sub>OH</sub> =50 μ A              |                                              | V <sub>DDIO</sub> -0.2 |      |      |      |     |
| V <sub>OL</sub> | 低电平输出电压         | I <sub>OL</sub> =I <sub>OL</sub> 最大值 |                                              |                        | 0.4  |      |      | V   |
| I <sub>IL</sub> | 输入电流<br>( 低电平 ) | 启用上拉的引脚                              | V <sub>DDIO</sub> =3.3V， V <sub>IN</sub> =0V | 所有 GPIO                | -80  | -140 | -205 | μ A |
|                 |                 |                                      |                                              | XRS 引脚                 | -225 | -290 | -360 |     |
|                 |                 | 启用下拉的引脚                              | V <sub>DDIO</sub> =3.3V， V <sub>IN</sub> =0V |                        |      | ±2   |      |     |

在推荐的运行条件下 ( 除非另有说明 ) <sup>(1)</sup>

| 参数       |                       |         | 测试条件                                          | 最小值  | 典型值  | 最大值     | 单位      |
|----------|-----------------------|---------|-----------------------------------------------|------|------|---------|---------|
| $I_{IH}$ | 输入电流<br>( 高电平 )       | 启用上拉的引脚 | $V_{DDIO}=3.3V$ , $V_{IN}=V_{DDIO}$           |      |      | $\pm 2$ | $\mu A$ |
|          |                       | 启用下拉的引脚 | $V_{DDIO}=3.3V$ , $V_{IN}=V_{DDIO}$           | 28   | 50   | 80      |         |
| $I_{OZ}$ | 输出电流, 上拉电阻器或者下拉电阻器被禁用 |         | $V_O = V_{DDIO}$ 或 $0V$                       |      |      | $\pm 2$ | $\mu A$ |
| $C_I$    | 输入电容                  |         |                                               |      | 2    |         | pF      |
|          | $V_{DDIO}$ BOR 触发点    |         | 下降的 $V_{DDIO}$                                | 2.42 | 2.65 | 3.135   | V       |
|          | $V_{DDIO}$ BOR 滞后     |         |                                               |      | 35   |         | mV      |
|          | 监视器复位延迟时间             |         | 延迟时间过后, BOR/POR/OVR 事件被移除以释放 $\overline{XRS}$ | 400  |      | 800     | $\mu s$ |
|          | VREG $V_{DD}$ 输出      |         | 内部 VREG 打开                                    |      | 1.9  |         | V       |

(1) 当片上 VREG 被使用时, 它的输出由 POR/BOR 电路监控, 如果内核电压 ( $V_{DD}$ ) 超出范围, 此电路将复位器件。

## 8.7 热阻特性

### 8.7.1 PT 封装

|                              |         | °C/W <sup>(1)</sup> | 气流 (lfm) <sup>(2)</sup> |
|------------------------------|---------|---------------------|-------------------------|
| $R_{\theta JC}$              | 结至外壳热阻  | 13.6                | 不适用                     |
| $R_{\theta JB}$              | 结至电路板热阻 | 30.6                | 不适用                     |
| $R_{\theta JA}$<br>(高 k PCB) | 结至大气热阻  | 64                  | 0                       |
|                              |         | 50.4                | 150                     |
|                              |         | 48.2                | 250                     |
|                              |         | 45                  | 500                     |
| $\Psi_{JT}$                  | 结至封装顶部  | 0.56                | 0                       |
|                              |         | 0.94                | 150                     |
|                              |         | 1.1                 | 250                     |
|                              |         | 1.38                | 500                     |
| $\Psi_{JB}$                  | 结至电路板   | 30.1                | 0                       |
|                              |         | 28.7                | 150                     |
|                              |         | 28.4                | 250                     |
|                              |         | 28                  | 500                     |

(1) 以上值基于 JEDEC 定义的 2S2P 系统 ( 基于 JEDEC 定义的 1S0P 系统的  $\Theta_{JC}$  [ $R_{\theta JC}$ ] 值除外 ) , 将随环境和应用的变化而更改。如需更多信息, 请参阅以下 EIA/JEDEC 标准:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = 线性英尺/分钟

### 8.7.2 DA 封装

|                              |         | °C/W <sup>(1)</sup> | 气流 (lfm) <sup>(2)</sup> |
|------------------------------|---------|---------------------|-------------------------|
| $R_{\theta JC}$              | 结至外壳热阻  | 12.8                | 不适用                     |
| $R_{\theta JB}$              | 结至电路板热阻 | 33                  | 不适用                     |
| $R_{\theta JA}$<br>(高 k PCB) | 结至大气热阻  | 70.1                | 0                       |
|                              |         | 56.4                | 150                     |
|                              |         | 53.9                | 250                     |
|                              |         | 50.2                | 500                     |
| $\Psi_{JT}$                  | 结至封装顶部  | 0.34                | 0                       |
|                              |         | 0.61                | 150                     |
|                              |         | 0.74                | 250                     |
|                              |         | 0.98                | 500                     |
| $\Psi_{JB}$                  | 结至电路板   | 32.5                | 0                       |
|                              |         | 32.1                | 150                     |
|                              |         | 31.7                | 250                     |
|                              |         | 31.1                | 500                     |

(1) 以上值基于 JEDEC 定义的 2S2P 系统 ( 基于 JEDEC 定义的 1S0P 系统的  $\Theta_{JC}$  [ $R_{\theta JC}$ ] 值除外 ) , 将随环境和应用的变化而更改。如需更多信息, 请参阅以下 EIA/JEDEC 标准:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

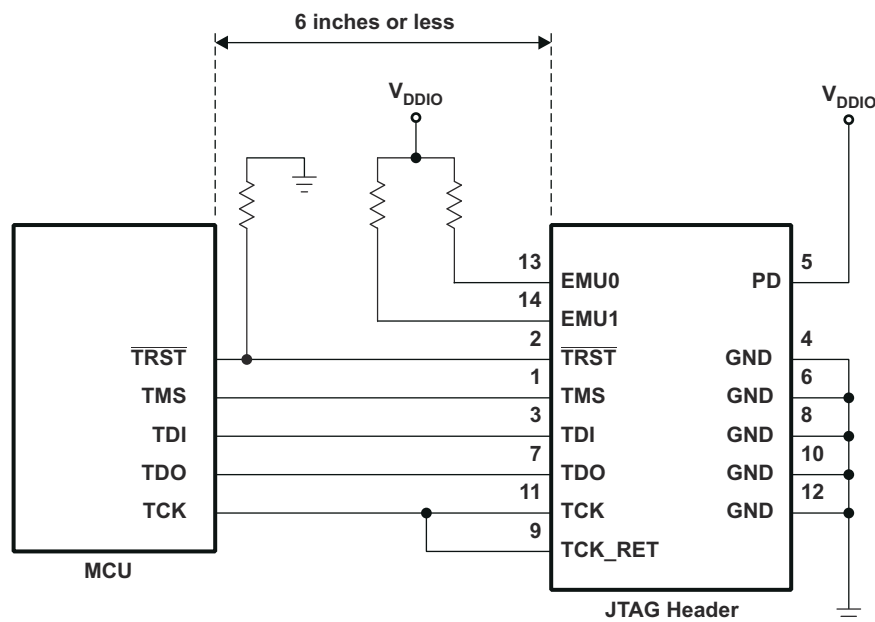
(2) Ifm = 线性英尺/分钟

## 8.8 散热设计注意事项

根据最终应用设计和运行情况， $I_{DD}$  和  $I_{DDIO}$  电流可能有所不同。最终产品中超过建议最大功率损耗的系统可能需要额外的散热增强措施。环境温度 ( $T_A$ ) 因最终应用和产品设计而异。影响可靠性和功能性的关键因素是结温  $T_J$ ，而非环境温度。因此，应该注意将  $T_J$  保持在指定限值内。应该测量  $T_{case}$  以评估运行结温  $T_J$ 。通常在封装顶部表面的中心测量  $T_{case}$ 。热应用报告 [半导体和 IC 封装热指标](#) 可帮助您了解各项热指标和相关定义。

## 8.9 无信号缓冲情况下 MCU 与 JTAG 调试探针的连接

图 8-3 显示了采用单处理器配置时 MCU 和 JTAG 接头之间的连接。如果 JTAG 接头和 MCU 之间的距离大于 6 英寸，那么仿真信号必须被缓冲。如果距离小于 6 英寸，通常无需缓冲。图 8-3 显示了较简单、无缓冲的情况。对于上拉/下拉电阻器的值，请参阅节 7.2，信号说明。



A. 有关 JTAG/GPIO 多路复用的信息，请参阅图 9-39。

图 8-3. 无信号缓冲情况下 MCU 与 JTAG 调试探针的连接

### 备注

2802x 器件无 EMU0/EMU1 引脚。对于具有板载 JTAG 接头的设计，接头上的 EMU0/EMU1 引脚必须通过一个 4.7kΩ (典型值) 电阻连接至  $V_{DDIO}$ 。



## 8.10 参数信息

### 8.10.1 时序参数符号

所用的时序参数符号是按照 JEDEC 标准 100 创建的。为了缩短符号，有些引脚名称和其他相关术语已如下缩写：

| 小写下标及其意义：    | 字母和符号及其意义：     |
|--------------|----------------|
| a 访问时间       | H 高            |
| c 周期时间（周期）   | L 低            |
| d 延迟时间       | V 有效           |
| f 下降时间       | X 未知、改变或者不关心级别 |
| h 保持时间       | Z 高阻抗          |
| r 上升时间       |                |
| su 建立时间      |                |
| t 转换时间       |                |
| v 有效时间       |                |
| w 脉冲持续时间（宽度） |                |

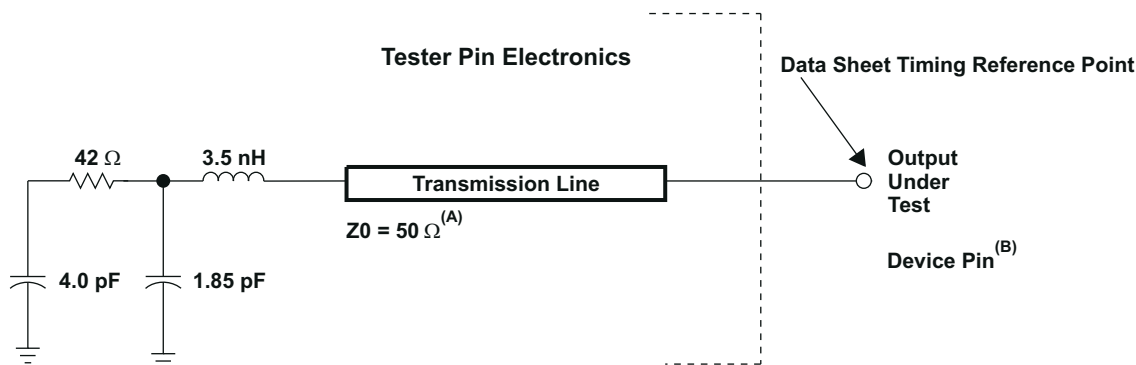
### 8.10.2 定时参数的通用注释

所有 28x 器件的输出信号（包括 XCLKOUT）取自一个内部时钟，这样，对于一个指定半周期的所有输出转换在一个互相之间相对最小转换率时发生。

这个显示在下面时序图中的信号组合也许不一定代表真实的周期。对于真实周期范例，请参见本文档的合适周期说明部分。

## 8.11 测试负载电路

此测试负载电路用于测量本文档中提供的所有开关特性。

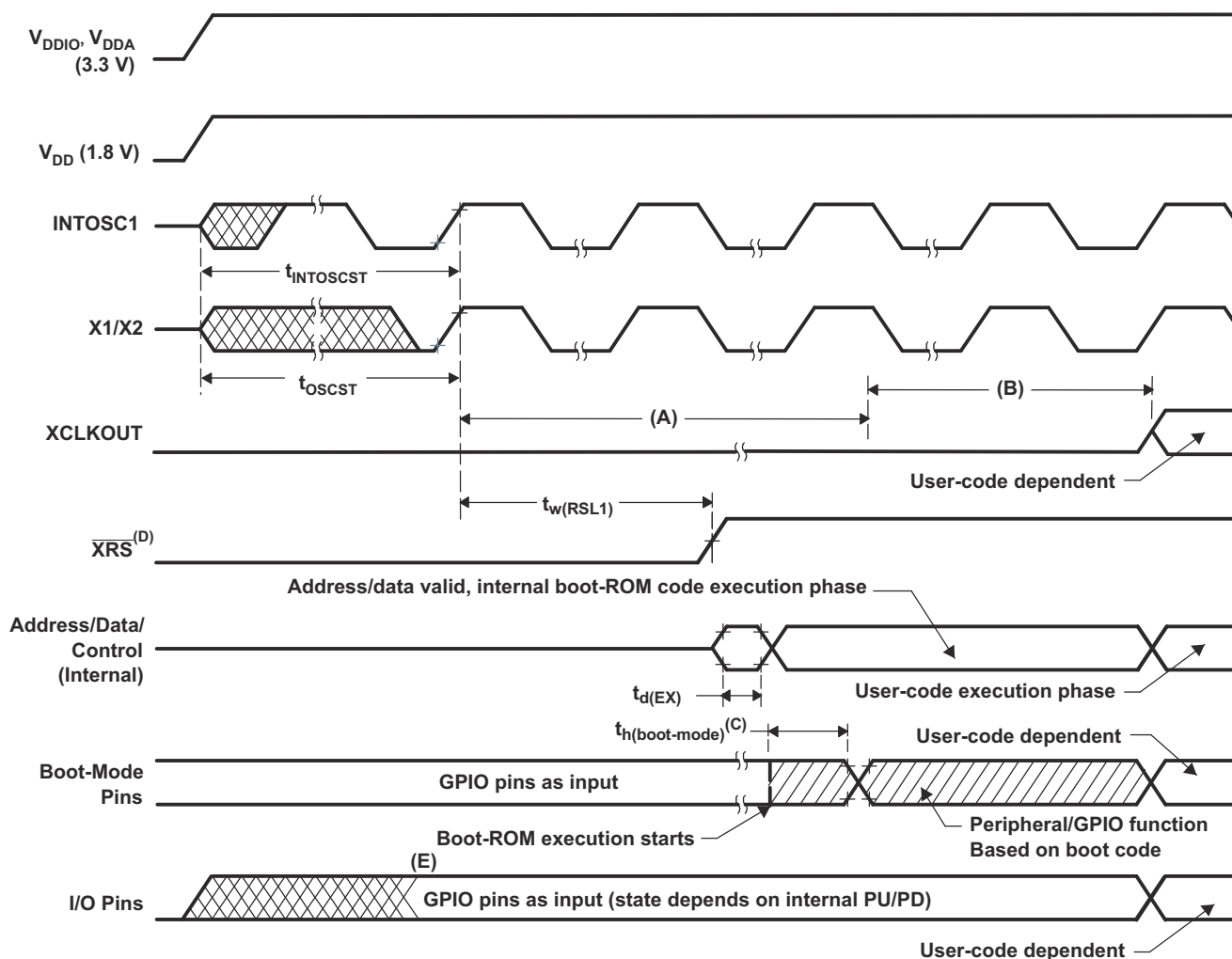


- 此数据表中的输入要求是在器件引脚上以小于每纳秒 4 伏 (4V/ns) 的输入转换率测试得出的。
- 此数据表提供器件引脚上的时序。在分析输出时序时，必须考虑测试仪引脚电子元件及其传输线路影响。可使用具有 2ns 或更长延迟时间的传输线路实现所需的传输线路效果。传输线路只用作负载。无需从数据表时序中增加或者减去传输线路延迟 (2ns 或者更长)。

图 8-4. 3.3V 测试负载电路

## 8.12 电源时序

复位后无需电源时序来确保器件处于正常状态或者防止上电/下电期间的 I/O 上的毛刺脉冲 ( GPIO19、GPIO34 - 38 上没有无毛刺脉冲 I/O )。在器件上电之前, 不应将  $V_{DDIO}$  之上大于二极管压降 (0.7V) 的电压应用于任何数字引脚 (对于模拟引脚, 此值是高于  $V_{DDA}$  0.7V 的电压值)。应用于未加电器件的引脚上的电压会以一种无意的的方式偏置内部 p-n 接头并产生无法预料的结果。



- 上电时, SYSCLKOUT 为 OSCCLK/4。由于 XCLK 寄存器内的 XCLKOUTDIV 位出现复位状态 0, SYSCLKOUT 在出现在 XCLKOUT 上之前会进一步除以 4。这个状态期间, XCLKOUT=OSCCLK/16。
- 引导 ROM 将 DIVSEL 位配置为 /1 运行。在这个状态期间, XCLKOUT=OSCCLK/4。XCLKOUT 只有通过用户代码明确配置, 才会显示在引脚上。
- 复位后, 引导 ROM 代码采样引导模式引脚。基于引导模式引脚的状态, 引导代码向目的内存或者引导代码函数下达分支指令。如果引导 ROM 代码在加电条件后 (在调试器环境中) 执行代码, 引导代码执行时间由当前的 SYSCLKOUT 的速度而定。SYSCLKOUT 将基于用户环境并可在 PLL 启用或者不启用时使用。
- 由于片上加电复位 (POR) 电路, 使用  $\overline{XRS}$  引脚是可选的。
- 当 BOR 被驱动为高电平, 内部上拉/下拉将起作用。

图 8-5. 加电复位

### 8.12.1 复位 ( $\overline{\text{XRS}}$ ) 时序要求

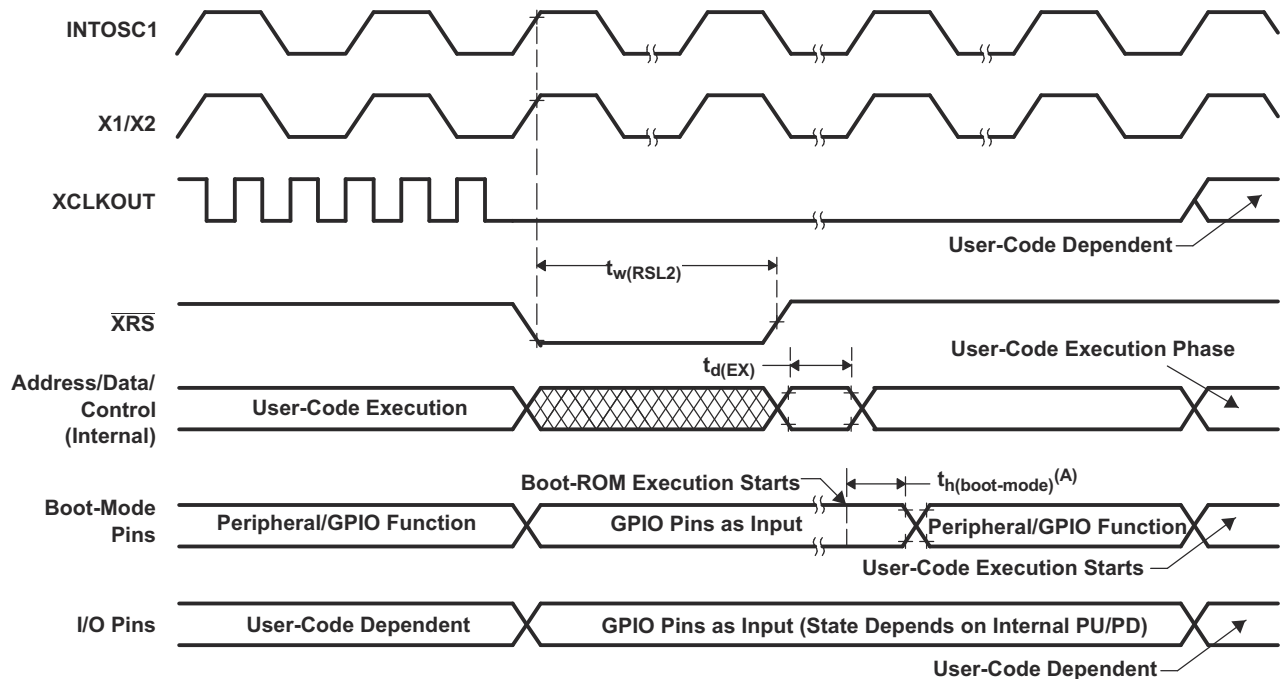
|               |                                            | 最小值  | 最大值             | 单位 |
|---------------|--------------------------------------------|------|-----------------|----|
| $t_h$ (引导模式)  | 引导模式引脚的保持时间                                | 1000 | $t_{c(SCO)}$    | 周期 |
| $t_{w(RSL2)}$ | 脉冲持续时间, 热复位时 $\overline{\text{XRS}}$ 处于低电平 | 32   | $t_{c(OSCCLK)}$ | 周期 |

### 8.12.2 复位 ( $\overline{\text{XRS}}$ ) 开关特性

在推荐的运行条件下 (除非另有说明)

| 参数                       | 测试条件                                        | 最小值 | 典型值 | 最大值             | 单位            |
|--------------------------|---------------------------------------------|-----|-----|-----------------|---------------|
| $t_{w(RSL1)}$            | 脉冲持续时间, $\overline{\text{XRS}}$ 由器件驱动       |     | 600 |                 | $\mu\text{s}$ |
| $t_{w(WDRS)}$            | 脉冲持续时间, 由看门狗生成复位脉冲                          |     | 512 | $t_{c(OSCCLK)}$ | 周期            |
| $t_d(\text{EX})$         | 延迟时间, $\overline{\text{XRS}}$ 高电平后, 地址/数据有效 |     | 32  | $t_{c(OSCCLK)}$ | 周期            |
| $t_{\text{INTOSCST}}$    | 启动时间, 内部零引脚振荡器                              |     | 3   |                 | $\mu\text{s}$ |
| $t_{\text{OSCST}}^{(1)}$ | 片上晶体振荡器启动时间                                 | 1   | 10  |                 | ms            |

(1) 取决于晶体/谐振器和电路板设计。



A. 复位后, 引导 ROM 代码采样引导模式引脚。基于引导模式引脚的状态, 引导代码向目的内存或者引导代码函数下达分支指令。如果引导 ROM 代码在加电条件后 (在调试器环境中) 执行代码, 引导代码执行时间由当前的 SYSCLKOUT 的速度而定。SYSCLKOUT 将基于用户环境并可在 PLL 启用或者不启用时使用。

图 8-6. 热复位

图 8-7 显示了写入 PLLCR 寄存器所产生的效果的一个示例。在第一个阶段， $PLLCR = 0x0004$  且  $SYSCLKOUT = OSCCLK \times 2$ 。然后写入  $0x0008$  到 PLLCR。就在 PLLCR 寄存器被写入后，PLL 锁存阶段开始。在此阶段， $SYSCLKOUT = OSCCLK/2$ 。在 PLL 锁存完成后，SYSCLKOUT 表示新的运行频率， $OSCCLK \times 4$ 。

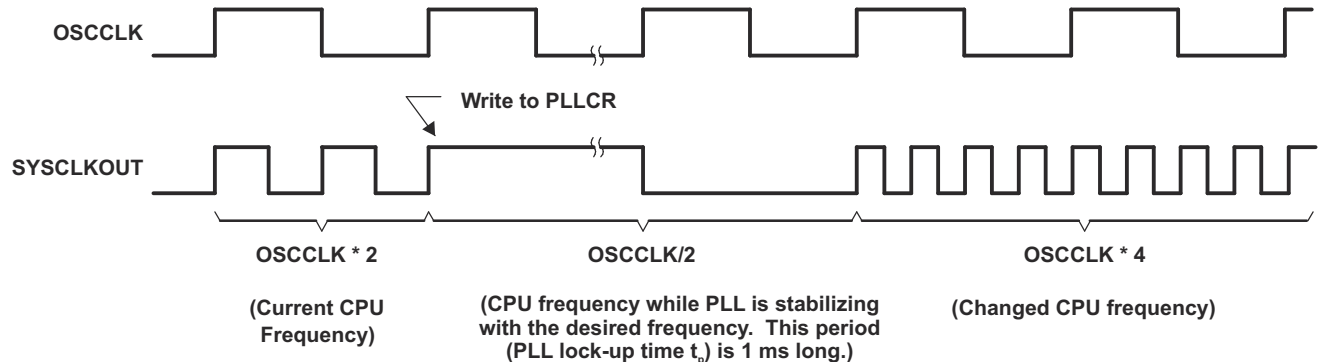


图 8-7. 写入 PLLCR 寄存器所产生的结果的示例

## 8.13 时钟规范

### 8.13.1 器件时钟表

此部分介绍 2802x MCU 上可用的不同时钟选项的定时要求和开关特性。节 8.13.1.1、节 8.13.1.2 和 节 8.13.1.3 列出了不同时钟的周期时间。

#### 8.13.1.1 2802x 时钟表和命名规则 (40MHz 器件)

|                       |                        | 最小值 | 标称值                | 最大值 | 单位  |
|-----------------------|------------------------|-----|--------------------|-----|-----|
| SYSCLKOUT             | $t_{c(SCO)}$ , 周期时间    | 25  |                    | 500 | ns  |
|                       | 频率                     | 2   |                    | 40  | MHz |
| LSPCLK <sup>(1)</sup> | $t_{c(LCO)}$ , 周期时间    | 25  | 100 <sup>(2)</sup> |     | ns  |
|                       | 频率                     |     | 10 <sup>(2)</sup>  | 40  | MHz |
| ADC 时钟                | $t_{c(ADCCLK)}$ , 周期时间 | 25  |                    |     | ns  |
|                       | 频率                     |     |                    | 40  | MHz |

(1) 更低的 LSPCLK 将减少器件功耗。

(2) 如果 SYSCLKOUT=40MHz, 这个值为缺省复位值。

#### 8.13.1.2 2802x 时钟表和命名规则 (50MHz 器件)

|                       |                        | 最小值 | 标称值                 | 最大值 | 单位  |
|-----------------------|------------------------|-----|---------------------|-----|-----|
| SYSCLKOUT             | $t_{c(SCO)}$ , 周期时间    | 20  |                     | 500 | ns  |
|                       | 频率                     | 2   |                     | 50  | MHz |
| LSPCLK <sup>(1)</sup> | $t_{c(LCO)}$ , 周期时间    | 20  | 80 <sup>(2)</sup>   |     | ns  |
|                       | 频率                     |     | 12.5 <sup>(2)</sup> | 50  | MHz |
| ADC 时钟                | $t_{c(ADCCLK)}$ , 周期时间 | 20  |                     |     | ns  |
|                       | 频率                     |     |                     | 50  | MHz |

(1) 更低的 LSPCLK 将减少器件功耗。

(2) 如果 SYSCLKOUT=50MHz, 这个值为缺省复位值。

#### 8.13.1.3 2802x 时钟表和命名规则 (60MHz 器件)

|                       |                        | 最小值   | 标称值                  | 最大值 | 单位  |
|-----------------------|------------------------|-------|----------------------|-----|-----|
| SYSCLKOUT             | $t_{c(SCO)}$ , 周期时间    | 16.67 |                      | 500 | ns  |
|                       | 频率                     | 2     |                      | 60  | MHz |
| LSPCLK <sup>(1)</sup> | $t_{c(LCO)}$ , 周期时间    | 16.67 | 66.67 <sup>(2)</sup> |     | ns  |
|                       | 频率                     |       | 15 <sup>(2)</sup>    | 60  | MHz |
| ADC 时钟                | $t_{c(ADCCLK)}$ , 周期时间 | 16.67 |                      |     | ns  |
|                       | 频率                     |       |                      | 60  | MHz |

(1) 更低的 LSPCLK 将减少器件功耗。

(2) 如果 SYSCLKOUT=60MHz, 这个值为缺省复位值。

#### 8.13.1.4 器件计时要求/特性

|                                     |                          | 最小值   | 标称值 | 最大值  | 单位  |
|-------------------------------------|--------------------------|-------|-----|------|-----|
| 片上振荡器 ( X1/X2 引脚 )<br>( 晶振/谐振器 )    | $t_{c(OSC)}$ , 周期时间      | 50    |     | 200  | ns  |
|                                     | 频率                       | 5     |     | 20   | MHz |
| 外部振荡器/时钟源<br>( XCLKIN 引脚 ) — PLL 启用 | $t_{c(CI)}$ , 周期时间 (C8)  | 33.3  |     | 200  | ns  |
|                                     | 频率                       | 5     |     | 30   | MHz |
| 外部振荡器/时钟源<br>( XCLKIN 引脚 ) — PLL 禁用 | $t_{c(CI)}$ , 周期时间 (C8)  | 33.33 |     | 250  | ns  |
|                                     | 频率                       | 4     |     | 30   | MHz |
| 跛行模式 SYSCLKOUT<br>( /2 启用 )         | 频率范围                     | 1 至 5 |     |      | MHz |
| XCLKOUT                             | $t_{c(XCO)}$ , 周期时间 (C1) | 66.67 |     | 2000 | ns  |
|                                     | 频率                       | 0.5   |     | 15   | MHz |
| PLL 锁定时间 <sup>(1)</sup>             | $t_p$                    |       |     | 1    | ms  |

- (1) PLLLOCKPRD 寄存器必须按照 OSCCLK 周期的数量进行更新。如果内部零引脚振荡器 (10MHz) 被用作时钟源, 那么必须将值 10,000 (最小值) 写入 PLLLOCKPRD 寄存器。

### 8.13.1.5 内部零引脚振荡器 (INTOSC1/INTOSC2) 特性

| 参数                                      |    | 最小值 | 典型值  | 最大值  | 单位     |
|-----------------------------------------|----|-----|------|------|--------|
| 内部零引脚振荡器 1 (INTOSC1) <sup>(1) (2)</sup> | 频率 |     | 10   |      | MHz    |
| 内部零引脚振荡器 2 (INTOSC2) <sup>(1) (2)</sup> | 频率 |     | 10   |      | MHz    |
| 步长尺寸 (粗调)                               |    |     | 55   |      | kHz    |
| 步长尺寸 (微调)                               |    |     | 14   |      | kHz    |
| 温度漂移 <sup>(3)</sup>                     |    |     | 3.03 | 4.85 | kHz/°C |
| 电压 (V <sub>DD</sub> ) 漂移 <sup>(3)</sup> |    |     | 175  |      | Hz/mV  |

(1) 振荡器频率将随温度变化, 请参阅图 8-8。要补偿振荡器温度漂移, 请参阅振荡器补偿指南和 C2000Ware。

(2) 只有当 VREG 被启用时, 才能确保频率范围, VREGENZ=V<sub>SS</sub>。

(3) 内部振荡器的输出频率由温度梯度和电压 (V<sub>DD</sub>) 梯度确定。例如:

- 温度的上升将引起输出频率按照温度系数增加。
- 电压的下降 (V<sub>DD</sub>) 将引起输出频率按照电压系数下降。

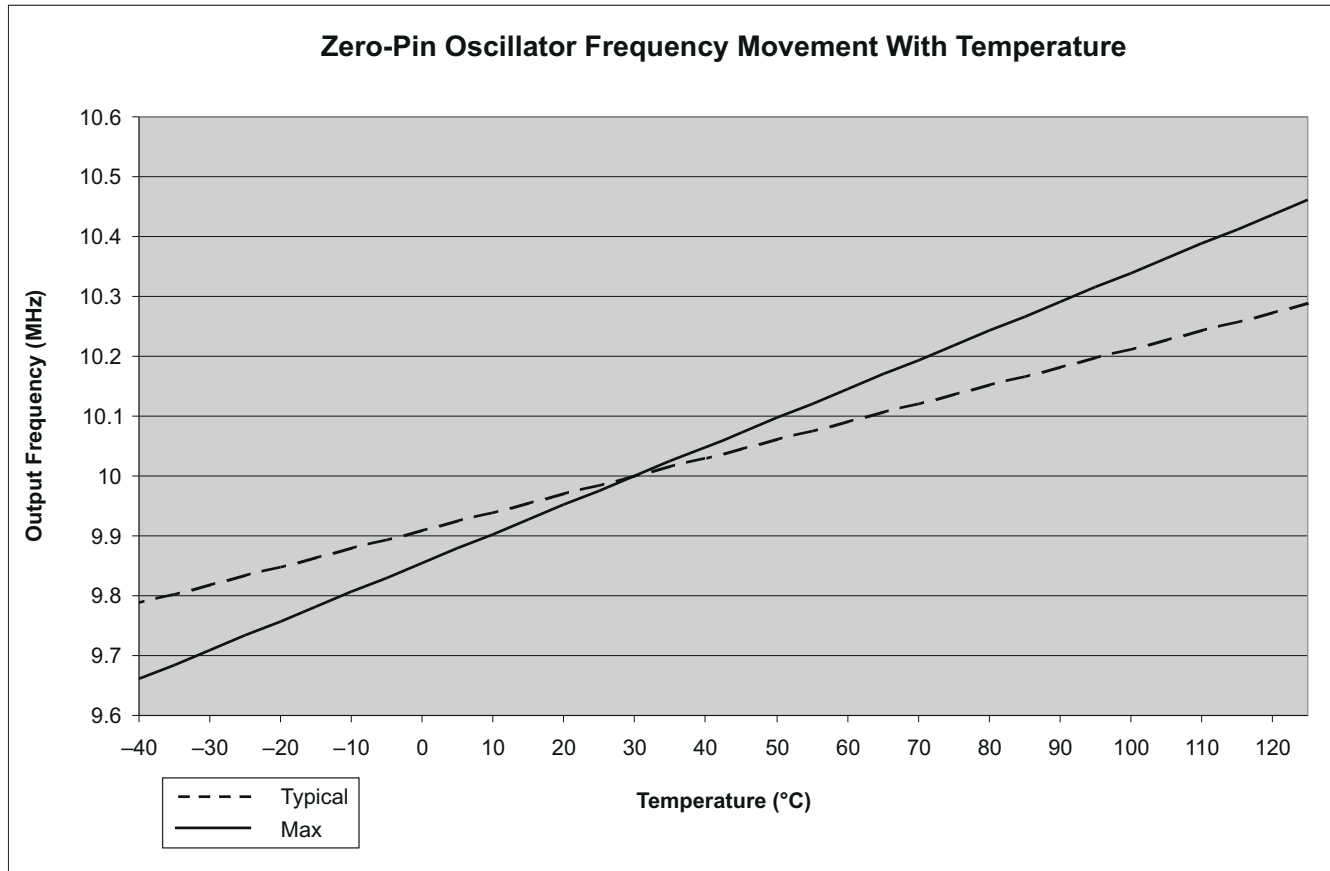


图 8-8. 随温度变化而变化的零引脚振荡器频率

### 8.13.2 时钟要求和特性

#### 8.13.2.1 XCLKIN 定时要求 - PLL 已启用

| 编号  |                                                         | 最小值 | 最大值 | 单位 |
|-----|---------------------------------------------------------|-----|-----|----|
| C9  | $t_{f(CI)}$ 下降时间, XCLKIN                                |     | 6   | ns |
| C10 | $t_{r(CI)}$ 上升时间, XCLKIN                                |     | 6   | ns |
| C11 | $t_{w(CIL)}$ 脉冲持续时间, XCLKIN 低电平为 $t_{c(OSCCLK)}$ 的一个百分比 | 45% | 55% |    |
| C12 | $t_{w(CIH)}$ 脉冲持续时间, XCLKIN 高电平为 $t_{c(OSCCLK)}$ 的一个百分比 | 45% | 55% |    |

#### 8.13.2.2 XCLKIN 时序要求 - PLL 已禁用

| 编号  |                                                         |               | 最小值 | 最大值 | 单位 |
|-----|---------------------------------------------------------|---------------|-----|-----|----|
| C9  | $t_{f(CI)}$ 下降时间, XCLKIN                                | 高达 20MHz      | 6   |     | ns |
|     |                                                         | 20MHz 至 30MHz | 2   |     |    |
| C10 | $t_{r(CI)}$ 上升时间, XCLKIN                                | 高达 20MHz      | 6   |     | ns |
|     |                                                         | 20MHz 至 30MHz | 2   |     |    |
| C11 | $t_{w(CIL)}$ 脉冲持续时间, XCLKIN 低电平为 $t_{c(OSCCLK)}$ 的一个百分比 |               | 45% | 55% |    |
| C12 | $t_{w(CIH)}$ 脉冲持续时间, XCLKIN 高电平为 $t_{c(OSCCLK)}$ 的一个百分比 |               | 45% | 55% |    |

表 9-16 中显示了可能的配置模式。

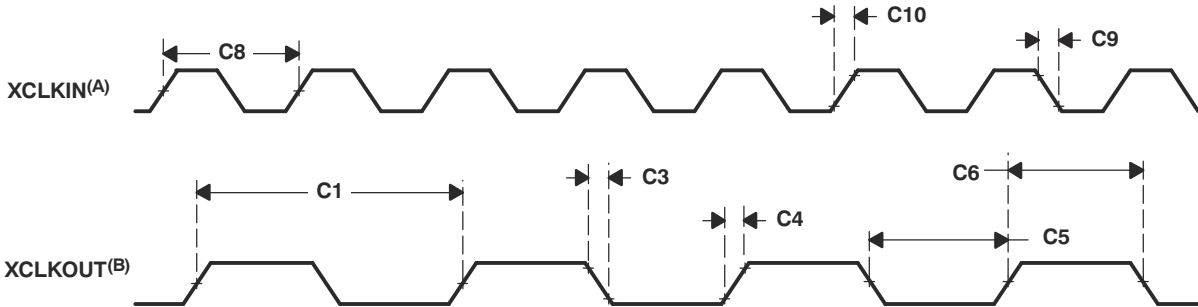
#### 8.13.2.3 XCLKOUT 开关特性 (旁路或启用 PLL)

在推荐的运行条件下 (除非另有说明) <sup>(1)</sup> <sup>(2)</sup>

| 编号 | 参数                                | 最小值   | 最大值   | 单位 |
|----|-----------------------------------|-------|-------|----|
| C3 | $t_{f(XCO)}$ 下降时间, XCLKOUT        |       | 11    | ns |
| C4 | $t_{r(XCO)}$ 上升时间, XCLKOUT        |       | 11    | ns |
| C5 | $t_{w(XCOL)}$ 脉冲持续时间, XCLKOUT 低电平 | H - 2 | H + 2 | ns |
| C6 | $t_{w(XCOH)}$ 脉冲持续时间, XCLKOUT 高电平 | H - 2 | H + 2 | ns |

(1) 这些参数假定有 40pF 负载。

(2)  $H = 0.5t_{c(XCO)}$



A. XCLKIN 与 XCLKOUT 的关系取决于所选择的分频系数。所示波形关系仅用于说明时序参数,可能因实际配置而异。

B. 已配置 XCLKOUT 以反映 SYSCLKOUT。

图 8-9. 时钟时序



## 8.14 闪存定时

### 8.14.1 T 温度材料的闪存/OTP 耐久性

|                               | 温度<br>擦除/编程 <sup>(1)</sup> | 最小值   | 典型值   | 最大值 | 单位 |
|-------------------------------|----------------------------|-------|-------|-----|----|
| $N_f$ 闪存对于阵列的耐受度 (写入/擦除周期)    | 0°C 至 105°C (环境温度)         | 20000 | 50000 |     | 周期 |
| $N_{OTP}$ OTP 对于阵列的耐受度 (写入周期) | 0°C 至 30°C (环境温度)          |       |       | 1   | 写入 |

(1) 所示温度范围之外的写入/擦除操作并未说明, 有可能影响耐受数。

### 8.14.2 S 温度材料的闪存/OTP 耐久性

|                               | 温度<br>擦除/编程 <sup>(1)</sup> | 最小值   | 典型值   | 最大值 | 单位 |
|-------------------------------|----------------------------|-------|-------|-----|----|
| $N_f$ 闪存对于阵列的耐受度 (写入/擦除周期)    | 0°C 至 125°C (环境温度)         | 20000 | 50000 |     | 周期 |
| $N_{OTP}$ OTP 对于阵列的耐受度 (写入周期) | 0°C 至 30°C (环境温度)          |       |       | 1   | 写入 |

(1) 所示温度范围之外的写入/擦除操作并未说明, 有可能影响耐受数。

### 8.14.3 Q 温度材料的闪存/OTP 耐久性

|                               | 温度<br>擦除/编程 <sup>(1)</sup> | 最小值   | 典型值   | 最大值 | 单位 |
|-------------------------------|----------------------------|-------|-------|-----|----|
| $N_f$ 闪存对于阵列的耐受度 (写入/擦除周期)    | -40°C 至 125°C (环境温度)       | 20000 | 50000 |     | 周期 |
| $N_{OTP}$ OTP 对于阵列的耐受度 (写入周期) | -40°C 至 30°C (环境温度)        |       |       | 1   | 写入 |

(1) 所示温度范围之外的写入/擦除操作并未说明, 有可能影响耐受数。

### 8.14.4 60MHz SYSCLKOUT 下的闪存参数

| 参数                                       | 测试条件    | 最小值 | 典型值 | 最大值 | 单位 |
|------------------------------------------|---------|-----|-----|-----|----|
| $I_{DDP}^{(1)}$ 擦除/编程周期内的 $V_{DD}$ 流耗    | VREG 禁用 |     | 80  |     | mA |
| $I_{DDIO}^{(1)}$ 擦除/编程周期内的 $V_{DDIO}$ 流耗 |         |     | 60  |     | mA |
| $I_{DDIO}^{(1)}$ 擦除/编程周期内的 $V_{DDIO}$ 流耗 | VREG 启用 |     | 120 |     | mA |

(1) 室温下包括函数调用开销在内的典型参数, 是在所有外设关闭时的参数。在整个闪存编程过程中保持稳定的电源很重要。可想而知, 闪存编程期间的器件电流消耗可能高于正常工作条件下。如数据表“建议工作条件”中所述, 使用的电源应始终确保  $V_{MIN}$  位于电源轨上。擦除/编程过程中发生任何欠压保护或电源中断, 都可能会损坏密码位置并永久锁定器件。不建议通过 USB 端口为目标板供电 (在闪存编程期间), 因为该端口可能无法响应编程过程中设置的电源需求。

### 8.14.5 50MHz SYSCLKOUT 上的闪存参数 :

| 参数                                       | 测试条件    | 最小值 | 典型值 | 最大值 | 单位 |
|------------------------------------------|---------|-----|-----|-----|----|
| $I_{DDP}^{(1)}$ 擦除/编程周期内的 $V_{DD}$ 流耗    | VREG 禁用 |     | 70  |     | mA |
| $I_{DDIO}^{(1)}$ 擦除/编程周期内的 $V_{DDIO}$ 流耗 |         |     | 60  |     |    |
| $I_{DDIO}^{(1)}$ 擦除/编程周期内的 $V_{DDIO}$ 流耗 | VREG 启用 |     | 110 |     | mA |

(1) 室温下包括函数调用开销在内的典型参数, 是在所有外设关闭时的参数。在整个闪存编程过程中保持稳定的电源很重要。可想而知, 闪存编程期间的器件电流消耗可能高于正常工作条件下。如数据表“建议工作条件”中所述, 使用的电源应始终确保  $V_{MIN}$  位于电源轨上。擦除/编程过程中发生任何欠压保护或电源中断, 都可能会损坏密码位置并永久锁定器件。不建议通过 USB 端口为目标板供电 (在闪存编程期间), 因为该端口可能无法响应编程过程中设置的电源需求。

### 8.14.6 40MHz SYSCLKOUT 上的闪存参数 :

| 参数                                       | 测试条件    | 最小值 | 典型值 | 最大值 | 单位 |
|------------------------------------------|---------|-----|-----|-----|----|
| $I_{DDP}^{(1)}$ 擦除/编程周期内的 $V_{DD}$ 流耗    | VREG 禁用 |     | 60  |     | mA |
| $I_{DDIO}^{(1)}$ 擦除/编程周期内的 $V_{DDIO}$ 流耗 |         |     | 60  |     |    |

| 参数                                       | 测试条件    | 最小值 | 典型值 | 最大值 | 单位 |
|------------------------------------------|---------|-----|-----|-----|----|
| $I_{DDIO}^{(1)}$ 擦除/编程周期内的 $V_{DDIO}$ 流耗 | VREG 启用 |     | 100 |     | mA |

- (1) 室温下包括函数调用开销在内的典型参数，是在所有外设关闭时的参数。在整个闪存编程过程中保持稳定的电源很重要。可想而知，闪存编程期间的器件电流消耗可能高于正常工作条件下。如数据表“建议工作条件”中所述，使用的电源应始终确保  $V_{MIN}$  位于电源轨上。擦除/编程过程中发生任何欠压保护或电源中断，都可能会损坏密码位置并永久锁定器件。不建议通过 USB 端口为目标板供电（在闪存编程期间），因为该端口可能无法响应编程过程中设置的电源需求。

#### 8.14.7 闪存编程/擦除时间

| 参数                  | 测试条件  | 最小值 | 典型值 | 最大值 <sup>(2)</sup> | 单位 |
|---------------------|-------|-----|-----|--------------------|----|
| 编程时间 <sup>(1)</sup> | 8K 扇区 |     | 250 | 2000               | ms |
|                     | 4K 扇区 |     | 125 | 2000               | ms |
|                     | 16 位字 |     | 50  |                    | μs |
| 擦除时间 <sup>(3)</sup> | 8K 扇区 |     | 2   | 12                 | s  |
|                     | 4K 扇区 |     | 2   | 12                 | s  |

- (1) 编程时间是最大器件频率下的值。此表中指示的编程时间仅适用于器件 RAM 中的所有必需代码/数据都可用并准备好进行编程的情况。编程时间包括闪存状态机的开销，但不包括将以下项传输到 RAM 的时间：
- 使用闪存 API 对闪存进行编程的代码
  - 闪存 API 本身
  - 要进行编程的闪存数据
- (2) 所提到的最大闪存参数对应于前 100 个编程和擦除周期。
- (3) 当器件从 TI 出货时，片上闪存存储器处于一个被擦除状态。这样，当首次编辑器件时，在编程前无需擦除闪存存储器。然而，对于所有随后的编程操作，需要执行擦除操作。

#### 8.14.8 闪存 / OTP 访问时序

| 参数                    | 最小值 | 最大值 | 单位 |
|-----------------------|-----|-----|----|
| $t_{a(fp)}$ 页式闪存访问时间  | 40  |     | ns |
| $t_{a(fr)}$ 随机闪存访问时间  | 40  |     | ns |
| $t_{a(OTP)}$ OTP 访问时间 | 60  |     | ns |

#### 8.14.9 Flash Data Retention Duration

| PARAMETER                               | TEST CONDITIONS          | MIN | MAX | UNIT  |
|-----------------------------------------|--------------------------|-----|-----|-------|
| $t_{retention}$ Data retention duration | $T_J = 55^\circ\text{C}$ | 15  |     | years |

表 8-2. Minimum Required Flash/OTP Wait States at Different Frequencies

| SYSCLKOUT<br>(MHz) | SYSCLKOUT<br>(ns) | PAGE<br>WAIT STATE <sup>(1)</sup> | RANDOM<br>WAIT STATE <sup>(1)</sup> | OTP<br>WAIT STATE |
|--------------------|-------------------|-----------------------------------|-------------------------------------|-------------------|
| 60                 | 16.67             | 2                                 | 2                                   | 3                 |
| 55                 | 18.18             | 2                                 | 2                                   | 3                 |
| 50                 | 20                | 1                                 | 1                                   | 2                 |
| 45                 | 22.22             | 1                                 | 1                                   | 2                 |
| 40                 | 25                | 1                                 | 1                                   | 2                 |
| 35                 | 28.57             | 1                                 | 1                                   | 2                 |
| 30                 | 33.33             | 1                                 | 1                                   | 1                 |
| 25                 | 40                | 0                                 | 1                                   | 1                 |

(1) Random wait state must be  $\geq 1$ .

The equations to compute the Flash page wait state and random wait state in 表 8-2 are as follows:

$$\text{Flash Page Wait State} = \left\lceil \left( \frac{t_{a(f.p)}}{t_{c(SCO)}} \right) - 1 \right\rceil \text{ round up to the next highest integer}$$

$$\text{Flash Random Wait State} = \left\lceil \left( \frac{t_{a(f.r)}}{t_{c(SCO)}} \right) - 1 \right\rceil \text{ round up to the next highest integer, or 1, whichever is larger}$$

The equation to compute the OTP wait state in 表 8-2 is as follows:

$$\text{OTP Wait State} = \left\lceil \left( \frac{t_{a(OTP)}}{t_{c(SCO)}} \right) - 1 \right\rceil \text{ round up to the next highest integer, or 1, whichever is larger}$$

## 9 详细说明

### 9.1 Overview

#### 9.1.1 CPU

2802x (C28x) 系列是 TMS320C2000™ 微控制器 (MCU) 平台的成员。基于 C28x 的控制器具有与现有 C28x MCU 一样的 32 位定点架构。它是一款高效的 C/C++ 引擎，不仅支持用户使用高级语言开发控制软件，还支持使用 C/C++ 开发数学算法。此器件在处理 MCU 算术任务时与处理系统控制任务时同样有效，而系统控制任务通常由微控制器器件处理。鉴于此器件具有高效率，无需像很多系统一样使用第二个处理器。利用 32 x 32 位 MAC 64 位处理能力，控制器能够高效地处理更高的数值分辨率问题。添加了带有关键寄存器自动环境保存的快速中断响应，使得一个器件能够用最小的延迟处理很多异步事件。此器件有一个具有流水线式存储器访问的 8 级深受保护流水线。这个流水线式操作使得此器件能够在高速执行而无需求助于昂贵的高速存储器。特别分支超前硬件大大减少了条件不连续而带来的延迟。特别存储条件操作进一步提升了性能。

#### 9.1.2 Memory Bus (Harvard Bus Architecture)

As with many MCU-type devices, multiple buses are used to move data between the memories and peripherals and the CPU. The memory bus architecture contains a program read bus, data read bus, and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write buses consist of 32 address lines and 32 data lines each. The 32-bit-wide data buses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed Harvard Bus, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

|            |                |                                                                          |
|------------|----------------|--------------------------------------------------------------------------|
| — Highest: | Data Writes    | (Simultaneous data and program writes cannot occur on the memory bus.)   |
| —          | Program Writes | (Simultaneous data and program writes cannot occur on the memory bus.)   |
| —          | Data Reads     |                                                                          |
| —          | Program Reads  | (Simultaneous program reads and fetches cannot occur on the memory bus.) |
| — Lowest:  | Fetches        | (Simultaneous program reads and fetches cannot occur on the memory bus.) |

#### 9.1.3 外设总线

为了在多种德州仪器 (TI) MCU 器件系列间实现外设迁移，此器件采用一个针对外设互连的外设总线标准。外设总线桥对各个总线进行多路复用，使处理器内存总线成为包含 16 条地址线和 16 条或 32 条数据线及关联控制信号的单个总线。支持外设总线的三个版本。一个版本只支持 16 位访问 (被称为外设帧 2)。另外版本支持 16 位和 32 位访问 (被称为外设帧 1)。

#### 9.1.4 Real-Time JTAG and Analysis

The devices implement the standard IEEE 1149.1 JTAG <sup>1</sup> interface for in-circuit based debug. Additionally, the devices support real-time mode of operation allowing modification of the contents of memory, peripheral, and register locations while the processor is running and executing code and servicing interrupts. The user can also single step through non-time-critical code while enabling time-critical interrupts to be serviced without interference. The device implements the real-time mode in hardware within the CPU. This is a feature unique to the 28x family of devices, requiring no software monitor. Additionally, special analysis hardware is provided that allows setting of hardware breakpoint or data/address watch-points and generating various user-selectable break events when a match occurs. These devices do not support boundary scan; however, IDCODE and BYPASS features are available if the following considerations are taken into account. The IDCODE does not come by default. The user must go through a sequence of SHIFT IR and SHIFT DR state of JTAG to get the IDCODE. For BYPASS instruction, the first shifted DR value would be 1.

#### 9.1.5 Flash

The F280200 device contains 8K × 16 of embedded flash memory, segregated into two 4K × 16 sectors. The F28021/23/27 devices contain 32K × 16 of embedded flash memory, segregated into four 8K × 16 sectors. The F28020/22/26 devices contain 16K × 16 of embedded flash memory, segregated into four 4K × 16 sectors. All devices also contain a single 1K × 16 of OTP memory at address range 0x3D 7800 to 0x3D 7BFF. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, it can be used to execute code or store data information. Addresses 0x3F 7FF0 to 0x3F 7FF5 are reserved for data variables and should not contain program code.

#### 备注

The Flash and OTP wait states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait-state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

For more information on the Flash options, Flash wait state, and OTP wait-state registers, see the System Control chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).

#### 9.1.6 M0 , M1 SARAM

所有器件包含这两块单周期访问内存，每一个的大小为 1K x 16。复位时，堆栈指针指向块 M1 的开始位置。M0 和 M1 块，与所有其它 C28x 器件上的内存块一样，被映射到程序和数据空间。因此，用户能够使用 M0 和 M1 来执行代码或者用于数据变量。分区在连接器内执行。C28x 器件提供了一个到编程器的统一内存映射。这使得用高级语言编程变得更加容易。

#### 9.1.7 L0 SARAM

此器件包含高达 4K x 16 的单周期访问 RAM。请参考节 9.2 中的器件专用内存映射图表来确定一个指定器件的准确大小。这个块被映射到程序和数据空间。

<sup>1</sup> IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

## 9.1.8 Boot ROM

The Boot ROM is factory-programmed with bootloader software. The Boot ROM uses the boot-mode-select GPIO pins to determine what boot mode to use upon power up. The user can select to boot normally to application code, to download new software from an external connection, or to select boot software that is programmed in the internal Flash/ROM. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math-related algorithms. The boot-ROM content, and hence the checksum value, may vary for different silicon revisions. For details, see the Boot ROM chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).

表 9-1. Boot Mode Selection

| MODE | GPIO37/TDO | GPIO34/COMP2OUT | TRST | MODE                               |
|------|------------|-----------------|------|------------------------------------|
| 3    | 1          | 1               | 0    | GetMode                            |
| 2    | 1          | 0               | 0    | Wait (see 节 9.1.9 for description) |
| 1    | 0          | 1               | 0    | SCI                                |
| 0    | 0          | 0               | 0    | Parallel IO                        |
| EMU  | x          | x               | 1    | Emulation Boot                     |

### 9.1.8.1 仿真引导

连接 JTAG 调试探针时，无法使用 GPIO37/TDO 引脚进行引导模式选择。在这种情况下，引导 ROM 会检测已连接 JTAG 调试探针，并使用 PIE 向量表中的两个保留 SARAM 位置内容来确定引导模式。如果两个位置内的内容均无效，那么使用等待引导选项。可在仿真引导中访问所有引导模式选项。

### 9.1.8.2 GetMode

GetMode 的缺省运行状态选项为引导至闪存。通过在 OTP 中设定两个位置，这个运行状态能够被改变为其它的引导选项。如果两个 OTP 位置的内容均为无效，那么引导至闪存。可以指定以下加载程序之一：SCI、SPI、I2C 或 OTP。

### 9.1.8.3 引导加载器使用的外设引脚

表 9-2 显示了每一个外设引导加载器所使用的 GPIO 引脚。请参阅 GPIO 多路复用器表以检查这些引脚是否与您希望在应用中使用的任一外设冲突。

表 9-2. 外设引导加载器引脚

| 引导加载器 | 外设加载器引脚                                                                        |
|-------|--------------------------------------------------------------------------------|
| SCI   | SCIRXDA (GPIO28)<br>SCITXDA (GPIO29)                                           |
| 并行引导  | 数据 (GPIO[7:0])<br>28x 控制 (GPIO16)<br>主机控制 (GPIO12)                             |
| SPI   | SPISIMOA (GPIO16)<br>SPISOMIA (GPIO17)<br>SPICLKA (GPIO18)<br>SPISTEA (GPIO19) |
| I2C   | SDAA (GPIO32) <sup>(1)</sup><br>SCLA (GPIO33) <sup>(1)</sup>                   |

(1) 在您的器件封装上，GPIO 引脚 32 和 33 也许不可用。在这些器件上，这个引导加载选项不可用。



### 9.1.9 Security

The devices support high levels of security to protect the user firmware from being reverse engineered. The security features a 128-bit password (hardcoded for 16 wait states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents through the JTAG port or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit KEY value that matches the value stored in the password locations within the Flash.

In addition to the CSM, the emulation code security logic (ECSL) has been implemented to prevent unauthorized users from stepping through secure code. Any code or data access to flash, user OTP, or L0 memory while the JTAG debug probe is connected will trip the ECSL and break the debug probe connection. To allow debug of secure code, while maintaining the CSM protection against secure memory reads, the user must write the correct value into the lower 64 bits of the KEY register (KEY0 - KEY3), which matches the value stored in the lower 64 bits of the password locations (PWL0 - PWL3) within the flash. Dummy reads of all 128 bits of the password in the flash must still be performed. If the lower 64 bits of the password locations are all ones (unprogrammed), then the KEY value does not need to match. During debug of secure code, operations like single-stepping is possible. However, the actual contents of the secure memory cannot be seen in the CCS window.

When power is applied to a secure device that is connected to a JTAG debug probe, the CPU will start executing and may execute an instruction that performs an access to a protected area. If this happens, the ECSL will trip and cause the JTAG circuitry to be deactivated. Under this condition, a host (such as a computer running CCS or flash programming software) would not be able to establish connection with the device.

The solution is to use the *Wait* boot option. In this mode, the device loops around a software breakpoint to allow a JTAG debug probe to be connected without tripping security. The user can then exit this mode once the JTAG debug probe is connected by using one of the emulation boot options as described in the Boot ROM chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#). These devices do not support a hardware wait-in-reset mode.

#### 备注

- When the code-security passwords are programmed, all addresses from 0x3F7F80 to 0x3F7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If reprogramming of a secure device via JTAG may be needed in future, it is important to design the board in such a way that the device could be put in Wait boot mode upon power-up (when reprogramming is warranted). Otherwise, ECSL may deactivate the JTAG circuitry and prevent connection to the device, as mentioned earlier. If reconfiguring the device for Wait boot mode in the field is not practical, some mechanism must be implemented in the firmware to detect when a firmware update is warranted. Code could then branch to the desired bootloader in the bootROM. It could also branch to the Wait bootmode, at which point the JTAG debug probe could be connected, device unsecured and programming accomplished through JTAG itself.
- If the code security feature is not used, addresses 0x3F7F80 to 0x3F7FEF may be used for code or data. Addresses 0x3F7FF0 to 0x3F7FF5 are reserved for data and should not contain program code.

The 128-bit password (at 0x3F 7FF8 to 0x3F 7FFF) must not be programmed to zeros. Doing so would permanently lock the device.

## 备注

### Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY (EITHER ROM OR FLASH) AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

### 9.1.10 外设中断扩展 (PIE) 块

PIE 块将许多中断源复用至中断输入的较小的集合中。PIE 块能够支持多达 96 个外设中断。在 F2802x 上，外设使用 96 个可能中断中的 33 个。96 个中断被分成 8 组，每组被提供 12 个 CPU 中断线 (INT1 或者 INT12) 中的 1 个。96 个中断中的每一个中断由其存储在一个可被用户写覆盖的专用 RAM 块中的矢量支持。在处理这个中断时，这个矢量由 CPU 自动抽取。抽取这个矢量以及保存关键 CPU 寄存器将花费 8 个 CPU 时钟周期。因此 CPU 能够对中断事件作出快速响应。可以通过硬件和软件控制中断的优先级。每个中断都可以在 PIE 块内启用/禁用。

### 9.1.11 外部中断 (XINT1-XINT3)

此器件支持 3 个被屏蔽的外部中断 (XINT1-XINT3)。每一个中断可被选择成负边沿、正边沿、或者二者触发并能够被启用/禁用。这些中断还包含一个 16 位自由运行的上数计数器，当检测到一个有效的中断边沿时，该计数器复位为 0。这个计数器可被用于为中断精确计时。没有用于外部引脚的专用引脚。XINT1, XINT2, 和 XINT3 中断可接受来自 GPIO0-GPIO3 引脚的输入。

### 9.1.12 内部零引脚振荡器、振荡器和 PLL

此器件可由两个内部零引脚振荡器、一个外部振荡器或者一个连接至片上振荡器电路 (只适用于 48 引脚器件) 的晶体中的任一个计时。一个提供的 PLL 支持高达 12 个输入时钟缩放比。PLL 比率可用软件中在器件运行时更改，这使得用户需要低功耗运行时能够按比例降低运行频率。请参阅节 8，电气规格，了解时序详细信息。PLL 块可被设定为旁路模式。

### 9.1.13 看门狗

每个器件包含两个看门狗：一个是监视内核的 CPU 看门狗，一个是 NMI 看门狗，后者是时钟丢失检测电路。用户软件必须在特定的时间范围内定期复位 CPU 看门狗计数器；否则，CPU 看门狗将生成对处理器的复位。必要时可禁用 CPU 看门狗。NMI 看门狗仅在发生时钟故障时才起作用，可生成一个中断或者器件复位。

### 9.1.14 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except I2C) can be scaled relative to the CPU clock.



### 9.1.15 Low-power Modes

The devices are full static CMOS devices. Three low-power modes are provided:

|          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDLE:    | Place CPU in low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that must function during IDLE are left operating. An enabled interrupt from an active peripheral or the watchdog timer will wake the processor from IDLE mode.                                                                                                                                                                                                                                                                                                                                           |
| STANDBY: | Turns off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event                                                                                                                                                                                                                                                                                                                                                              |
| HALT:    | This mode basically shuts down the device and places it in the lowest possible power consumption mode. If the internal zero-pin oscillators are used as the clock source, the HALT mode turns them off, by default. To keep these oscillators from shutting down, the INTOSCnHALTI bits in CLKCTL register may be used. The zero-pin oscillators may thus be used to clock the CPU watchdog in this mode. If the on-chip crystal oscillator is used as the clock source, it is shut down in this mode. A reset or an external signal (through a GPIO pin) or the CPU watchdog can wake the device from this mode. |

The CPU clock (OSCCLK) and watchdog clock source should be from the same clock source before attempting to put the device into HALT or STANDBY.

### 9.1.16 外设帧 0, 1, 2 (PFn)

此器件将外设分成 3 个部分。外设映射如下：

|       |        |                            |
|-------|--------|----------------------------|
| PF0 : | PIE :  | PIE 中断启用和控制寄存器加上 PIE 矢量表   |
|       | 闪存 :   | 闪存写入状态寄存器                  |
|       | 定时器 :  | CPU - 定时器 0, 1, 2 寄存器      |
|       | CSM :  | 代码安全模块 KEY 寄存器             |
|       | ADC :  | ADC 结果寄存器                  |
| PF1 : | GPIO : | GPIO MUX 配置和控制寄存器          |
|       | ePWM : | 增强型脉冲宽度调制器模块和寄存器           |
|       | eCAP : | 增强型捕捉模块和寄存器                |
|       | 比较器 :  | 比较器模块 :                    |
| PF2 : | SYS :  | 系统控制寄存器                    |
|       | SCI :  | 串行通信接口 (SCI) 控制和 RX/TX 寄存器 |
|       | SPI :  | 串行端口接口 (SPI) 和 RX/TX 寄存器   |
|       | ADC :  | ADC 状态、控制、和配置寄存器           |
|       | IC2 :  | 集成电路间模块和寄存器                |
|       | XINT : | 外部中断寄存器                    |

### 9.1.17 通用输入/输出 (GPIO) 复用器

大多数的外设信号与通用输入/输出 (GPIO) 信号复用。这使得用户能够在外设信号或者功能不使用时将一个引脚用作 GPIO。复位时，GPIO 引脚被配置为输入。针对 GPIO 模式或者外设信号模式，用户能够独立设定每一个引脚。对于特定的输入，用户也可以选择输入限定周期的数量。这是为了过滤掉有害的噪音毛刺脉冲。GPIO 信号也可被用于使器件脱离特定低功耗模式。

### 9.1.18 32 位 CPU 定时器 (0, 1, 2)

CPU 定时器 0, 1, 和 2 是完全一样的 32 位定时器，这些定时器带有可预先设定的周期和 16 位时钟预分频。此定时器有一个 32 位倒计时寄存器，此寄存器在计数器达到 0 时生成一个中断。这个计数器的减量为被预分频值设置所分频的 CPU 时钟速度的值。当此计数器达到 0 时，它自动重新载入一个 32 位的周期值。

CPU 定时器 0 为通用定时器并被连接至 PIE 块。CPU 定时器 1 为通用定时器并被连接至 CPU 的 INT13。CPU 定时器 2 为 DSP/BIOS 保留。它被连接至 CPU 的 INT14。如果 DSP/BIOS 未被使用，CPU 定时器 2 也可称为通用定时器。

CPU 定时器 2 可由下列任一器件计时：

- SYSCLKOUT (默认)
- 内部零引脚振荡器 1 (INTOSC1)
- 内部零引脚振荡器 2 (INTOSC2)
- 外部时钟源

## 9.1.19 Control Peripherals

The devices support the following peripherals that are used for embedded control and communication:

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ePWM:       | The enhanced PWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism. Some of the PWM pins support the HRPWM high resolution duty and period features. The type 1 module found on 2802x devices also supports increased dead-band resolution, enhanced SOC and interrupt generation, and advanced triggering including trip functions based on comparator outputs. |
| eCAP:       | The enhanced capture peripheral uses a 32-bit time base and registers up to four programmable events in continuous/one-shot capture modes.<br>This peripheral can also be configured to generate an auxiliary PWM signal.                                                                                                                                                                                                                                                      |
| ADC:        | The ADC block is a 12-bit converter. It has up to 13 single-ended channels pinned out, depending on the device. It contains two sample-and-hold units for simultaneous sampling.                                                                                                                                                                                                                                                                                               |
| Comparator: | Each comparator block consists of one analog comparator along with an internal 10-bit reference for supplying one input of the comparator.                                                                                                                                                                                                                                                                                                                                     |

## 9.1.20 串行端口外设

此器件支持下列的串行通信外设：

|      |                                                                                                                                                                                                   |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPI： | SPI 是一个高速同步串行 I/O 端口，此端口允许编程长度（1 至 16 位）的串行位流以可编程的位传输速率移入和移出器件。通常，SPI 用于 MCU 和外部外设或者其他处理器之间的通信。典型应用包括外部 I/O 或者通过诸如移位寄存器、显示驱动器和 ADC 等器件进行外设扩展。多器件通信由 SPI 的主/从操作支持。SPI 包含用于减少中断服务开销的 4 级接收和发送 FIFO。 |
| SCI： | 串行通信接口是一种双线制异步串行端口，通常称为 UART。SCI 包含用于减少中断服务开销的 4 级接收和发送 FIFO。                                                                                                                                     |
| I2C： | 内部集成电路 (I2C) 模块在 MCU 与符合 Philips Semiconductors 内部集成电路总线 (I2C 总线®) 规范版本 2.1 并通过 I2C 总线连接的其他器件之间提供一个接口。该双线串行总线上连接的外部元件可以通过 I2C 模块向 MCU 发送/从 MCU 接收多达 8 位数据。I2C 包含用于减少中断服务开销的 4 级接收和发送 FIFO。        |

## 9.2 Memory Maps

In 图 9-1, 图 9-2, 图 9-3, 图 9-4, and 图 9-5, the following apply:

- Memory blocks are not to scale.
- Peripheral Frame 0, Peripheral Frame 1 and Peripheral Frame 2 memory maps are restricted to data memory only. A user program cannot access these memory maps in program space.
- *Protected* means the order of Write-followed-by-Read operations is preserved rather than the pipeline order.
- Certain memory ranges are EALLOW protected against spurious writes after configuration.
- Locations 0x3D7C80 to 0x3D7CC0 contain the internal oscillator and ADC calibration routines. These locations are not programmable by the user.

|           | Data Space                                                               | Prog Space |
|-----------|--------------------------------------------------------------------------|------------|
| 0x00 0000 | M0 Vector RAM (Enabled if VMAP = 0)                                      |            |
| 0x00 0040 | M0 SARAM (1K × 16, 0-Wait)                                               |            |
| 0x00 0400 | M1 SARAM (1K × 16, 0-Wait)                                               |            |
| 0x00 0800 | Peripheral Frame 0                                                       | Reserved   |
| 0x00 0D00 | PIE Vector - RAM<br>(256 × 16)<br>(Enabled if<br>VMAP = 1,<br>ENPIE = 1) |            |
| 0x00 0E00 | Peripheral Frame 0                                                       |            |
| 0x00 2000 | Reserved                                                                 |            |
| 0x00 6000 | Peripheral Frame 1<br>(4K × 16, Protected)                               | Reserved   |
| 0x00 7000 | Peripheral Frame 2<br>(4K × 16, Protected)                               |            |
| 0x00 8000 | L0 SARAM (4K × 16)<br>(0-Wait, Secure Zone + ECSL, Dual Mapped)          |            |
| 0x00 9000 | Reserved                                                                 |            |
| 0x3D 7800 | User OTP (1K × 16, Secure Zone + ECSL)                                   |            |
| 0x3D 7C00 | Reserved                                                                 |            |
| 0x3D 7C80 | Calibration Data                                                         |            |
| 0x3D 7CC0 | Get_mode function                                                        |            |
| 0x3D 7CE0 | Reserved                                                                 |            |
| 0x3D 7E80 | Calibration Data                                                         |            |
| 0x3D 7EB0 | Reserved                                                                 |            |
| 0x3D 7FFF | PARTID                                                                   |            |
| 0x3D 8000 | Reserved                                                                 |            |
| 0x3F 0000 | FLASH<br>(32K × 16, 4 Sectors, Secure Zone + ECSL)                       |            |
| 0x3F 7FF8 | 128-Bit Password                                                         |            |
| 0x3F 8000 | L0 SARAM (4K × 16)<br>(0-Wait, Secure Zone + ECSL, Dual Mapped)          |            |
| 0x3F 9000 | Reserved                                                                 |            |
| 0x3F E000 | Boot ROM (8K × 16, 0-Wait)                                               |            |
| 0x3F FFC0 | Vector (32 Vectors, Enabled if VMAP = 1)                                 |            |

A. Memory locations 0x3D 7E80 – 0x3D 7EAF are reserved in TMX/TMP silicon.

图 9-1. 28023-Q1/28027-Q1 Memory Map

|           | Data Space                                                               | Prog Space |
|-----------|--------------------------------------------------------------------------|------------|
| 0x00 0000 | <i>M0 Vector RAM (Enabled if VMAP = 0)</i>                               |            |
| 0x00 0040 | M0 SARAM (1K × 16, 0-Wait)                                               |            |
| 0x00 0400 | M1 SARAM (1K × 16, 0-Wait)                                               |            |
| 0x00 0800 | Peripheral Frame 0                                                       | Reserved   |
| 0x00 0D00 | PIE Vector - RAM<br>(256 × 16)<br>(Enabled if<br>VMAP = 1,<br>ENPIE = 1) |            |
| 0x00 0E00 | Peripheral Frame 0                                                       |            |
| 0x00 2000 | Reserved                                                                 |            |
| 0x00 6000 | Peripheral Frame 1<br>(4K × 16, Protected)                               | Reserved   |
| 0x00 7000 | Peripheral Frame 2<br>(4K × 16, Protected)                               |            |
| 0x00 8000 | L0 SARAM (4K × 16)<br>(0-Wait, Secure Zone + ECSL, Dual Mapped)          |            |
| 0x00 9000 | Reserved                                                                 |            |
| 0x3D 7800 | User OTP (1K × 16, Secure Zone + ECSL)                                   |            |
| 0x3D 7C00 | Reserved                                                                 |            |
| 0x3D 7C80 | Calibration Data                                                         |            |
| 0x3D 7CC0 | Get_mode function                                                        |            |
| 0x3D 7CE0 | Reserved                                                                 |            |
| 0x3D 7E80 | Calibration Data                                                         |            |
| 0x3D 7EB0 | Reserved                                                                 |            |
| 0x3D 7FFF | PARTID                                                                   |            |
| 0x3D 8000 | Reserved                                                                 |            |
| 0x3F 4000 | FLASH<br>(16K × 16, 4 Sectors, Secure Zone + ECSL)                       |            |
| 0x3F 7FF8 | 128-Bit Password                                                         |            |
| 0x3F 8000 | L0 SARAM (4K × 16)<br>(0-Wait, Secure Zone + ECSL, Dual Mapped)          |            |
| 0x3F 9000 | Reserved                                                                 |            |
| 0x3F E000 | Boot ROM (8K × 16, 0-Wait)                                               |            |
| 0x3F FFC0 | Vector (32 Vectors, Enabled if VMAP = 1)                                 |            |

A. Memory locations 0x3D 7E80 – 0x3D 7EAF are reserved in TMX/TMP silicon.

**图 9-2. 28022-Q1/28026-Q1 Memory Map**

|           | Data Space                                                               | Prog Space |
|-----------|--------------------------------------------------------------------------|------------|
| 0x00 0000 | M0 Vector RAM (Enabled if VMAP = 0)                                      |            |
| 0x00 0040 | M0 SARAM (1K × 16, 0-Wait)                                               |            |
| 0x00 0400 | M1 SARAM (1K × 16, 0-Wait)                                               |            |
| 0x00 0800 | Peripheral Frame 0                                                       | Reserved   |
| 0x00 0D00 | PIE Vector - RAM<br>(256 × 16)<br>(Enabled if<br>VMAP = 1,<br>ENPIE = 1) |            |
| 0x00 0E00 | Peripheral Frame 0                                                       |            |
| 0x00 2000 | Reserved                                                                 |            |
| 0x00 6000 | Peripheral Frame 1<br>(4K × 16, Protected)                               | Reserved   |
| 0x00 7000 | Peripheral Frame 2<br>(4K × 16, Protected)                               |            |
| 0x00 8000 | L0 SARAM (3K × 16)<br>(0-Wait, Secure Zone + ECSL, Dual Mapped)          |            |
| 0x00 8C00 | Reserved                                                                 |            |
| 0x3D 7800 | User OTP (1K × 16, Secure Zone + ECSL)                                   |            |
| 0x3D 7C00 | Reserved                                                                 |            |
| 0x3D 7C80 | Calibration Data                                                         |            |
| 0x3D 7CC0 | Get_mode function                                                        |            |
| 0x3D 7CE0 | Reserved                                                                 |            |
| 0x3D 7E80 | Calibration Data                                                         |            |
| 0x3D 7EB0 | Reserved                                                                 |            |
| 0x3D 7FFF | PARTID                                                                   |            |
| 0x3D 8000 | Reserved                                                                 |            |
| 0x3F 0000 | FLASH<br>(32K × 16, 4 Sectors, Secure Zone + ECSL)                       |            |
| 0x3F 7FF8 | 128-Bit Password                                                         |            |
| 0x3F 8000 | L0 SARAM (3K × 16)<br>(0-Wait, Secure Zone + ECSL, Dual Mapped)          |            |
| 0x3F 8C00 | Reserved                                                                 |            |
| 0x3F E000 | Boot ROM (8K × 16, 0-Wait)                                               |            |
| 0x3F FFC0 | Vector (32 Vectors, Enabled if VMAP = 1)                                 |            |

A. Memory locations 0x3D 7E80 – 0x3D 7EAF are reserved in TMX/TMP silicon.

**图 9-3. 28021 Memory Map**

|           | Data Space                                                               | Prog Space |
|-----------|--------------------------------------------------------------------------|------------|
| 0x00 0000 | <i>M0 Vector RAM (Enabled if VMAP = 0)</i>                               |            |
| 0x00 0040 | <b>M0 SARAM (1K × 16, 0-Wait)</b>                                        |            |
| 0x00 0400 | <b>M1 SARAM (1K × 16, 0-Wait)</b>                                        |            |
| 0x00 0800 | Peripheral Frame 0                                                       | Reserved   |
| 0x00 0D00 | PIE Vector - RAM<br>(256 × 16)<br>(Enabled if<br>VMAP = 1,<br>ENPIE = 1) |            |
| 0x00 0E00 | Peripheral Frame 0                                                       |            |
| 0x00 2000 | Reserved                                                                 |            |
| 0x00 6000 | Peripheral Frame 1<br>(4K × 16, Protected)                               | Reserved   |
| 0x00 7000 | Peripheral Frame 2<br>(4K × 16, Protected)                               |            |
| 0x00 8000 | <b>L0 SARAM (1K × 16)<br/>(0-Wait, Secure Zone + ECSL, Dual Mapped)</b>  |            |
| 0x00 8400 | Reserved                                                                 |            |
| 0x3D 7800 | <b>User OTP (1K × 16, Secure Zone + ECSL)</b>                            |            |
| 0x3D 7C00 | Reserved                                                                 |            |
| 0x3D 7C80 | Calibration Data                                                         |            |
| 0x3D 7CC0 | Get_mode function                                                        |            |
| 0x3D 7CE0 | Reserved                                                                 |            |
| 0x3D 7E80 | Calibration Data                                                         |            |
| 0x3D 7EB0 | Reserved                                                                 |            |
| 0x3D 7FFF | <b>PARTID</b>                                                            |            |
| 0x3D 8000 | Reserved                                                                 |            |
| 0x3F 4000 | <b>FLASH<br/>(16K × 16, 4 Sectors, Secure Zone + ECSL)</b>               |            |
| 0x3F 7FF8 | <b>128-Bit Password</b>                                                  |            |
| 0x3F 8000 | <b>L0 SARAM (1K × 16)<br/>(0-Wait, Secure Zone + ECSL, Dual Mapped)</b>  |            |
| 0x3F 8400 | Reserved                                                                 |            |
| 0x3F E000 | <b>Boot ROM (8K × 16, 0-Wait)</b>                                        |            |
| 0x3F FFC0 | <i>Vector (32 Vectors, Enabled if VMAP = 1)</i>                          |            |

A. Memory locations 0x3D 7E80 – 0x3D 7EAF are reserved in TMX/TMP silicon.

**图 9-4. 28020 Memory Map**

|           | Data Space                                                               | Prog Space |
|-----------|--------------------------------------------------------------------------|------------|
| 0x00 0000 | M0 Vector RAM (Enabled if VMAP = 0)                                      |            |
| 0x00 0040 | M0 SARAM (1K × 16, 0-Wait)                                               |            |
| 0x00 0400 | M1 SARAM (1K × 16, 0-Wait)                                               |            |
| 0x00 0800 | Peripheral Frame 0                                                       | Reserved   |
| 0x00 0D00 | PIE Vector - RAM<br>(256 × 16)<br>(Enabled if<br>VMAP = 1,<br>ENPIE = 1) |            |
| 0x00 0E00 | Peripheral Frame 0                                                       |            |
| 0x00 2000 | Reserved                                                                 |            |
| 0x00 6000 | Peripheral Frame 1<br>(4K × 16, Protected)                               | Reserved   |
| 0x00 7000 | Peripheral Frame 2<br>(4K × 16, Protected)                               |            |
| 0x00 8000 | L0 SARAM (1K × 16)<br>(0-Wait, Secure Zone + ECSL, Dual Mapped)          |            |
| 0x00 8400 | Reserved                                                                 |            |
| 0x3D 7800 | User OTP (1K × 16, Secure Zone + ECSL)                                   |            |
| 0x3D 7C00 | Reserved                                                                 |            |
| 0x3D 7C80 | Calibration Data                                                         |            |
| 0x3D 7CC0 | Get_mode function                                                        |            |
| 0x3D 7CE0 | Reserved                                                                 |            |
| 0x3D 7E80 | Calibration Data                                                         |            |
| 0x3D 7EB0 | Reserved                                                                 |            |
| 0x3D 7FFF | PARTID                                                                   |            |
| 0x3D 8000 | Reserved                                                                 |            |
| 0x3F 6000 | FLASH<br>(8K × 16, 2 Sectors, Secure Zone + ECSL)                        |            |
| 0x3F 7FF8 | 128-Bit Password                                                         |            |
| 0x3F 8000 | L0 SARAM (1K × 16)<br>(0-Wait, Secure Zone + ECSL, Dual Mapped)          |            |
| 0x3F 8400 | Reserved                                                                 |            |
| 0x3F E000 | Boot ROM (8K × 16, 0-Wait)                                               |            |
| 0x3F FFC0 | Vector (32 Vectors, Enabled if VMAP = 1)                                 |            |

A. Memory locations 0x3D 7E80 – 0x3D 7EAF are reserved in TMX/TMP silicon.

**图 9-5. 280200 Memory Map**



**表 9-3. Addresses of Flash Sectors in F28021/28023-Q1/28027-Q1**

| ADDRESS RANGE          | PROGRAM AND DATA SPACE                                         |
|------------------------|----------------------------------------------------------------|
| 0x3F 0000 to 0x3F 1FFF | Sector D (8K × 16)                                             |
| 0x3F 2000 to 0x3F 3FFF | Sector C (8K × 16)                                             |
| 0x3F 4000 to 0x3F 5FFF | Sector B (8K × 16)                                             |
| 0x3F 6000 to 0x3F 77F7 | Sector A (8K × 16)                                             |
| 0x3F 7F80 to 0x3F 7FF5 | Program to 0x0000 when using the<br>Code Security Module       |
| 0x3F 7FF6 to 0x3F 7FF7 | Boot-to-Flash Entry Point<br>(program branch instruction here) |
| 0x3F 7FF8 to 0x3F 7FFF | Security Password (128-Bit)<br>(Do not program to all zeros)   |

**表 9-4. Addresses of Flash Sectors in F28020/28022-Q1/28026-Q1**

| ADDRESS RANGE          | PROGRAM AND DATA SPACE                                         |
|------------------------|----------------------------------------------------------------|
| 0x3F 4000 to 0x3F 4FFF | Sector D (4K × 16)                                             |
| 0x3F 5000 to 0x3F 5FFF | Sector C (4K × 16)                                             |
| 0x3F 6000 to 0x3F 6FFF | Sector B (4K × 16)                                             |
| 0x3F 7000 to 0x3F 77F7 | Sector A (4K × 16)                                             |
| 0x3F 7F80 to 0x3F 7FF5 | Program to 0x0000 when using the<br>Code Security Module       |
| 0x3F 7FF6 to 0x3F 7FF7 | Boot-to-Flash Entry Point<br>(program branch instruction here) |
| 0x3F 7FF8 to 0x3F 7FFF | Security Password (128-Bit)<br>(Do not program to all zeros)   |

**表 9-5. Addresses of Flash Sectors in F280200**

| ADDRESS RANGE          | PROGRAM AND DATA SPACE                                         |
|------------------------|----------------------------------------------------------------|
| 0x3F 6000 to 0x3F 6FFF | Sector B (4K × 16)                                             |
| 0x3F 7000 to 0x3F 77F7 | Sector A (4K × 16)                                             |
| 0x3F 7F80 to 0x3F 7FF5 | Program to 0x0000 when using the<br>Code Security Module       |
| 0x3F 7FF6 to 0x3F 7FF7 | Boot-to-Flash Entry Point<br>(program branch instruction here) |
| 0x3F 7FF8 to 0x3F 7FFF | Security Password (128-Bit)<br>(Do not program to all zeros)   |

**备注**

- When the code-security passwords are programmed, all addresses from 0x3F 7F80 to 0x3F 7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x3F 7F80 to 0x3F 7FEF may be used for code or data. Addresses 0x3F 7FF0 to 0x3F 7FF5 are reserved for data and should not contain program code.

表 9-6 shows how to handle these memory locations.

**表 9-6. Impact of Using the Code Security Module**

| ADDRESS                | FLASH                 |                           |
|------------------------|-----------------------|---------------------------|
|                        | CODE SECURITY ENABLED | CODE SECURITY DISABLED    |
| 0x3F 7F80 to 0x3F 7FEF | Fill with 0x0000      | Application code and data |
| 0x3F 7FF0 to 0x3F 7FF5 |                       | Reserved for data only    |

Peripheral Frame 1 and Peripheral Frame 2 are grouped together to enable these blocks to be write/read peripheral block protected. The protected mode makes sure that all accesses to these blocks happen as written. Because of the pipeline, a write immediately followed by a read to different memory locations, will appear in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The CPU supports a block protection mode where a region of memory can be protected so that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable and by default, it protects the selected zones.

The wait states for the various spaces in the memory map area are listed in [表 9-7](#).

**表 9-7. Wait States**

| AREA               | WAIT STATES (CPU)                                                       | COMMENTS                                                                                                                                                           |
|--------------------|-------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| M0 and M1 SARAMEs  | 0-wait                                                                  | Fixed                                                                                                                                                              |
| Peripheral Frame 0 | 0-wait                                                                  |                                                                                                                                                                    |
| Peripheral Frame 1 | 0-wait (writes)<br>2-wait (reads)                                       | Cycles can be extended by peripheral generated ready.<br>Back-to-back write operations to Peripheral Frame 1 registers will incur a 1-cycle stall (1-cycle delay). |
| Peripheral Frame 2 | 0-wait (writes)<br>2-wait (reads)                                       | Fixed. Cycles cannot be extended by the peripheral.                                                                                                                |
| L0 SARAME          | 0-wait data and program                                                 | Assumes no CPU conflicts                                                                                                                                           |
| OTP                | Programmable<br>1-wait minimum                                          | Programmed through the Flash registers.<br>1-wait is minimum number of wait states allowed.                                                                        |
| FLASH              | Programmable<br>0-wait Paged min<br>1-wait Random min<br>Random ≥ Paged | Programmed through the Flash registers.                                                                                                                            |
| FLASH Password     | 16-wait fixed                                                           | Wait states of password locations are fixed.                                                                                                                       |
| Boot-ROM           | 0-wait                                                                  |                                                                                                                                                                    |

## 9.3 Register Maps

The devices contain three peripheral register spaces. The spaces are categorized as follows:

- Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See [表 9-8](#).
- Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See [表 9-9](#).
- Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See [表 9-10](#).

**表 9-8. Peripheral Frame 0 Registers**

| NAME <sup>(1)</sup>              | ADDRESS RANGE          | SIZE (×16) | EALLOW PROTECTED <sup>(2)</sup> |
|----------------------------------|------------------------|------------|---------------------------------|
| Device Emulation Registers       | 0x00 0880 to 0x00 0984 | 261        | Yes                             |
| System Power Control Registers   | 0x00 0985 to 0x00 0987 | 3          | Yes                             |
| FLASH Registers <sup>(3)</sup>   | 0x00 0A80 to 0x00 0ADF | 96         | Yes                             |
| Code Security Module Registers   | 0x00 0AE0 to 0x00 0AEF | 16         | Yes                             |
| ADC registers (0 wait read only) | 0x00 0B00 to 0x00 0B0F | 16         | No                              |
| CPU – TIMER0/1/2 Registers       | 0x00 0C00 to 0x00 0C3F | 64         | No                              |
| PIE Registers                    | 0x00 0CE0 to 0x00 0CFF | 32         | No                              |
| PIE Vector Table                 | 0x00 0D00 to 0x00 0DFF | 256        | No                              |

- (1) Registers in Frame 0 support 16-bit and 32-bit accesses.
- (2) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
- (3) The Flash Registers are also protected by the Code Security Module (CSM).

**表 9-9. Peripheral Frame 1 Registers**

| NAME                     | ADDRESS RANGE          | SIZE (×16) | EALLOW PROTECTED    |
|--------------------------|------------------------|------------|---------------------|
| Comparator 1 registers   | 0x00 6400 to 0x00 641F | 32         | <a href="#">(1)</a> |
| Comparator 2 registers   | 0x00 6420 to 0x00 643F | 32         | <a href="#">(1)</a> |
| ePWM1 + HRPWM1 registers | 0x00 6800 to 0x00 683F | 64         | <a href="#">(1)</a> |
| ePWM2 + HRPWM2 registers | 0x00 6840 to 0x00 687F | 64         | <a href="#">(1)</a> |
| ePWM3 + HRPWM3 registers | 0x00 6880 to 0x00 68BF | 64         | <a href="#">(1)</a> |
| ePWM4 + HRPWM4 registers | 0x00 68C0 to 0x00 68FF | 64         | <a href="#">(1)</a> |
| eCAP1 registers          | 0x00 6A00 to 0x00 6A1F | 32         | No                  |
| GPIO registers           | 0x00 6F80 to 0x00 6FFF | 128        | <a href="#">(1)</a> |

- (1) Some registers are EALLOW protected. For more information, see the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).

**表 9-10. Peripheral Frame 2 Registers**

| NAME                             | ADDRESS RANGE          | SIZE (×16) | EALLOW PROTECTED    |
|----------------------------------|------------------------|------------|---------------------|
| System Control Registers         | 0x00 7010 to 0x00 702F | 32         | Yes                 |
| SPI-A Registers                  | 0x00 7040 to 0x00 704F | 16         | No                  |
| SCI-A Registers                  | 0x00 7050 to 0x00 705F | 16         | No                  |
| NMI Watchdog Interrupt Registers | 0x00 7060 to 0x00 706F | 16         | Yes                 |
| External Interrupt Registers     | 0x00 7070 to 0x00 707F | 16         | Yes                 |
| ADC Registers                    | 0x00 7100 to 0x00 717F | 128        | <a href="#">(1)</a> |
| I2C-A Registers                  | 0x00 7900 to 0x00 793F | 64         | <a href="#">(1)</a> |

- (1) Some registers are EALLOW protected. For more information, see the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).

## 9.4 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in [表 9-11](#).

**表 9-11. Device Emulation Registers**

| NAME      | ADDRESS RANGE    | SIZE (x16) | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | EALLOW PROTECTED |
|-----------|------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| DEVICECNF | 0x0880<br>0x0881 | 2          | Device Configuration Register                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Yes              |
| PARTID    | 0x3D 7FFF        | 1          | Part ID Register<br>TMS320F280200PT 0x00C1<br>TMS320F280200DA 0x00C0<br>TMS320F28027PT 0x00CF<br>TMS320F28027DA 0x00CE<br>TMS320F28027FPT 0x00CF<br>TMS320F28027FDA 0x00CE<br>TMS320F28026PT 0x00C7<br>TMS320F28026DA 0x00C6<br>TMS320F28026FPT 0x00C7<br>TMS320F28026FDA 0x00C6<br>TMS320F28023PT 0x00CD<br>TMS320F28023DA 0x00CC<br>TMS320F28022PT 0x00C5<br>TMS320F28022DA 0x00C4<br>TMS320F28021PT 0x00CB<br>TMS320F28021DA 0x00CA<br>TMS320F28020PT 0x00C3<br>TMS320F28020DA 0x00C2 | No               |
| CLASSID   | 0x0882           | 1          | Class ID Register<br>TMS320F280200PT/DA 0x00C7<br>TMS320F28027PT/DA 0x00CF<br>TMS320F28027FPT/DA 0x00CF<br>TMS320F28026PT/DA 0x00C7<br>TMS320F28026FPT/DA 0x00C7<br>TMS320F28023PT/DA 0x00CF<br>TMS320F28022PT/DA 0x00C7<br>TMS320F28021PT/DA 0x00CF<br>TMS320F28020PT/DA 0x00C7                                                                                                                                                                                                         | No               |
| REVID     | 0x0883           | 1          | Revision ID Register<br>0x0000 - Silicon Rev. 0 - TMS<br>0x0001 - Silicon Rev. A - TMS<br>0x0002 - Silicon Rev. B - TMS                                                                                                                                                                                                                                                                                                                                                                  | No               |

## 9.5 VREG/BOR/POR

虽然内核和 I/O 电路运行在两个不同的电压上，这些器件有一个片载电压稳压器 (VREG) 来生成  $V_{DD}$  电压，此电压由  $V_{DDIO}$  电源提供。这在应用板上免除了第二个外部稳压器的成本和空间的需要。此外，在加电和运行模式期间，内部加电复位 (POR) 和欠压复位 (BOR) 电力路监控  $V_{DD}$  和  $V_{DDIO}$  电源轨。

### 9.5.1 片载电压稳压器 (VREG)

一个线性稳压器生成内核电压 ( $V_{DD}$ )，此电压由  $V_{DDIO}$  电源提供。因此，虽然在每一个  $V_{DD}$  引脚上都需要电容器来稳定生成的电压，但是运行此器件并不需要为这些引脚供电。相反地，如果功率或者冗余是应用关心的首要问题，那么可将 VREG 禁用。

#### 9.5.1.1 使用片上 VREG

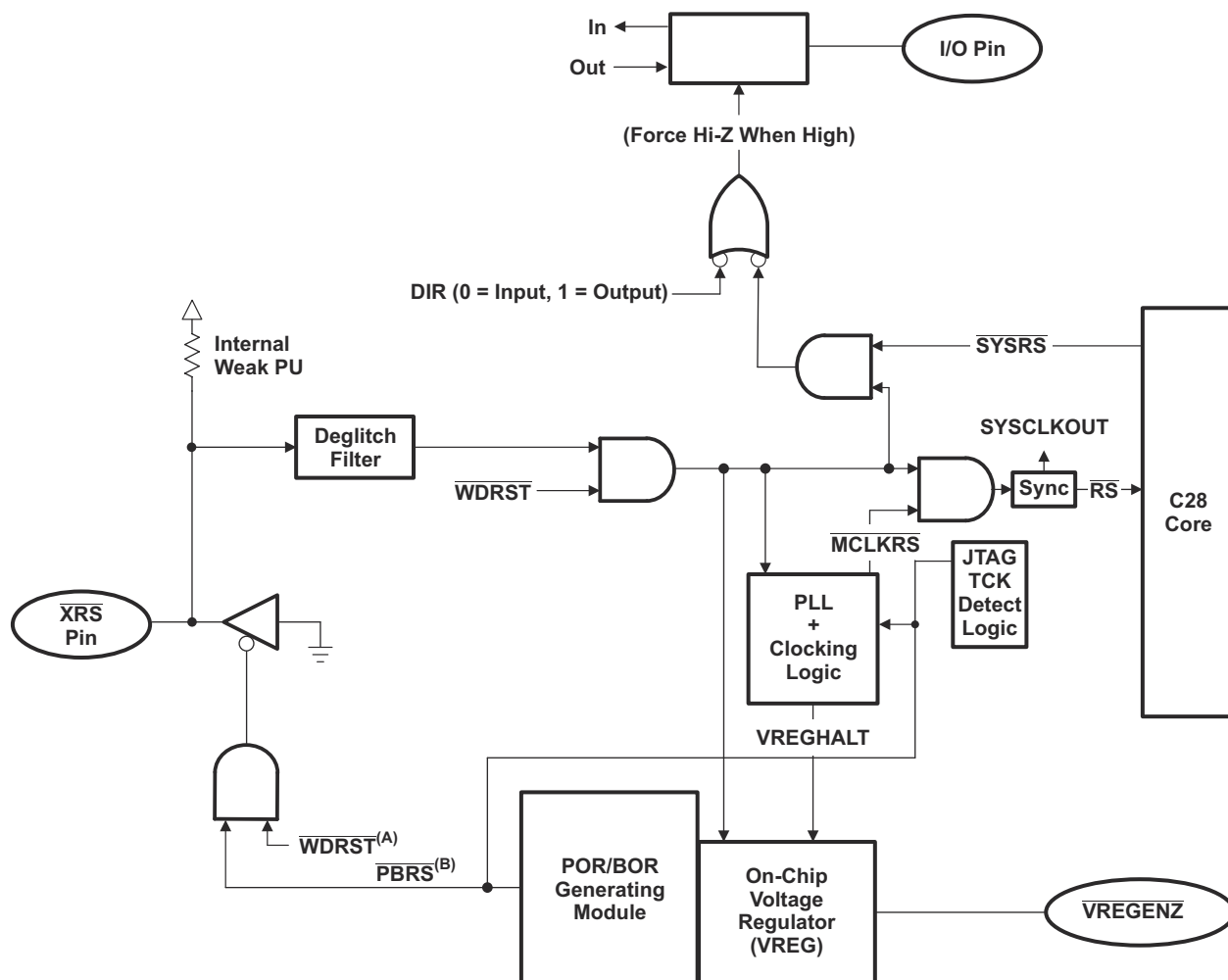
要使用片上 VREG， $\overline{VREGENZ}$  引脚应连接至低电平并且将建议的适当工作电压应用于  $V_{DDIO}$  和  $V_{DDA}$  引脚。在这种情况下，内核逻辑所需的  $V_{DD}$  电压将由 VREG 生成。每个  $V_{DD}$  引脚需要  $1.2\ \mu F$  (最小值) 级别的电容，以正确调节 VREG。这些电容器应尽可能靠近  $V_{DD}$  引脚。不支持使用内部 VREG 驱动外部负载。

#### 9.5.1.2 禁用片载 VREG

为了节约能源，也可禁用片载 VREG 并使用一个效率更高的外部稳压器将内核逻辑电压提供给  $V_{DD}$  引脚。为了启用这个选项， $\overline{VREGNZ}$  引脚必须被接至高电平。

### 9.5.2 On-chip Power-On Reset (POR) and Brown-Out Reset (BOR) Circuit

Two on-chip supervisory circuits, the power-on reset (POR) and the brown-out reset (BOR) remove the burden of monitoring the  $V_{DD}$  and  $V_{DDIO}$  supply rails from the application board. The purpose of the POR is to create a clean reset throughout the device during the entire power-up procedure. The trip point is a looser, lower trip point than the BOR, which watches for dips in the  $V_{DD}$  or  $V_{DDIO}$  rail during device operation. The POR function is present on both  $V_{DD}$  and  $V_{DDIO}$  rails at all times. After initial device power-up, the BOR function is present on  $V_{DDIO}$  at all times, and on  $V_{DD}$  when the internal VREG is enabled ( $\overline{VREGENZ}$  pin is tied low). Both functions tie the  $\overline{XRS}$  pin low when one of the voltages is below their respective trip point.  $V_{DD}$  BOR and overvoltage trip points are outside of the recommended operating voltages. Proper device operation cannot be ensured. If overvoltage or undervoltage conditions affecting the system is a concern for an application, an external voltage supervisor should be added. [Figure 9-6](#) shows the VREG, POR, and BOR. To disable both the  $V_{DD}$  and  $V_{DDIO}$  BOR functions, a bit is provided in the BORCFG register. For details, see the System Control chapter in the [TMS320F2802x TMS320F2802xx Technical Reference Manual](#).



- A. WDRST is the reset signal from the CPU watchdog.
- B. PBR $\overline{S}$  is the reset signal from the POR/BOR module.

### 图 9-6. VREG + POR + BOR + Reset Signal Connectivity

## 9.6 系统控制

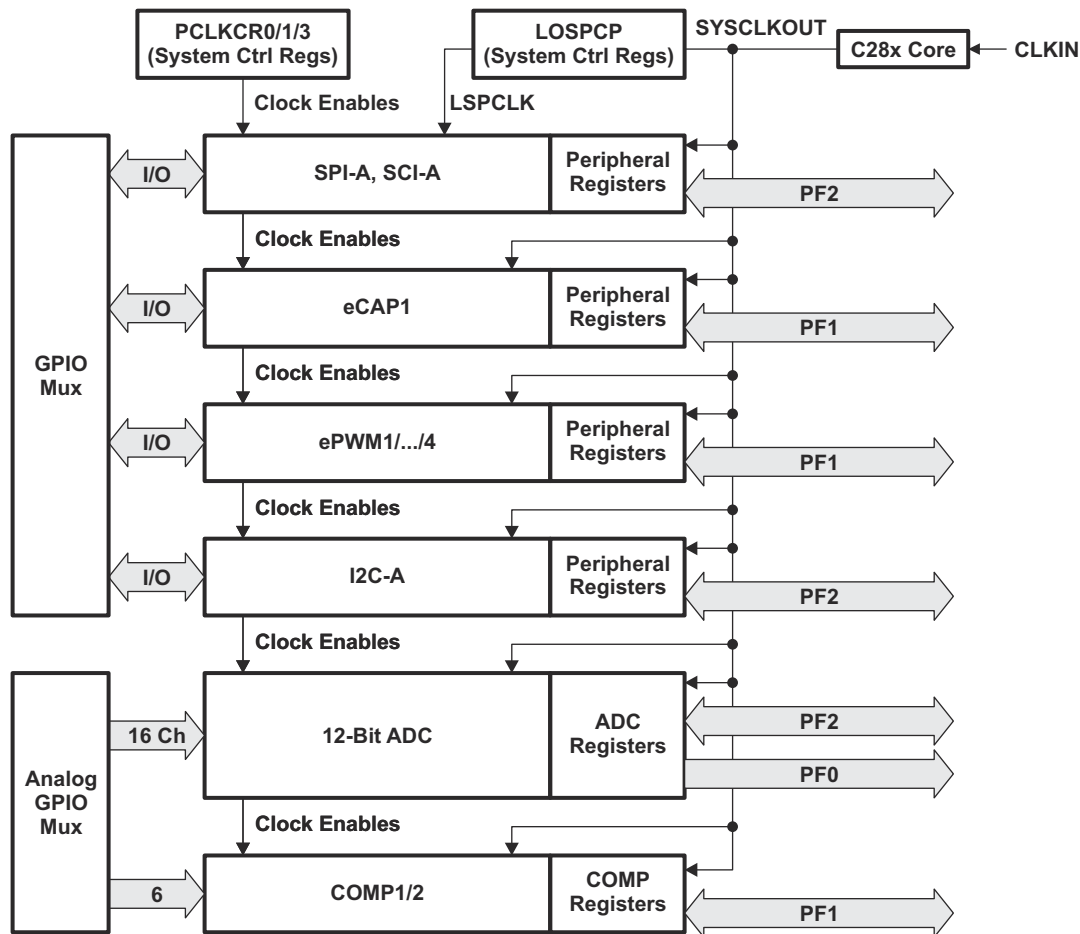
本部分介绍振荡器和时钟机制、看门狗功能以及低功耗模式。

**表 9-12. PLL、时钟、看门狗和低功耗模式寄存器**

| 名称          | 地址        | 大小 (x 16) | 说明 <sup>(1)</sup> |
|-------------|-----------|-----------|-------------------|
| BORCFG      | 0x00 0985 | 1         | BOR 配置寄存器         |
| XCLK        | 0x00 7010 | 1         | XCLKOUT 控制        |
| PLLSTS      | 0x00 7011 | 1         | PLL 状态寄存器         |
| CLKCTL      | 0x00 7012 | 1         | 时钟控制寄存器           |
| PLLLOCKPRD  | 0x00 7013 | 1         | PLL 锁周期           |
| INTOSC1TRIM | 0x00 7014 | 1         | 内部振荡器 1 调整寄存器     |
| INTOSC2TRIM | 0x00 7016 | 1         | 内部振荡器 2 调整寄存器     |
| LOSPCP      | 0x00 701B | 1         | 低速外设时钟预分频器寄存器     |
| PCLKCR0     | 0x00 701C | 1         | 外设时钟控制寄存器 0       |
| PCLKCR1     | 0x00 701D | 1         | 外设时钟控制寄存器 1       |
| LPMCR0      | 0x00 701E | 1         | 低功耗模式控制寄存器 0      |
| PCLKCR3     | 0x00 7020 | 1         | 外设时钟控制寄存器 3       |
| PLLCR       | 0x00 7021 | 1         | PLL 控制寄存器         |
| SCSR        | 0x00 7022 | 1         | 系统控制与状态寄存器        |
| WDCNTR      | 0x00 7023 | 1         | 看门狗计数器寄存器         |
| WDKEY       | 0x00 7025 | 1         | 看门狗复位密钥寄存器        |
| WDCR        | 0x00 7029 | 1         | 看门狗控制寄存器          |

(1) 此表中的所有寄存器都受 EALLOW 保护。

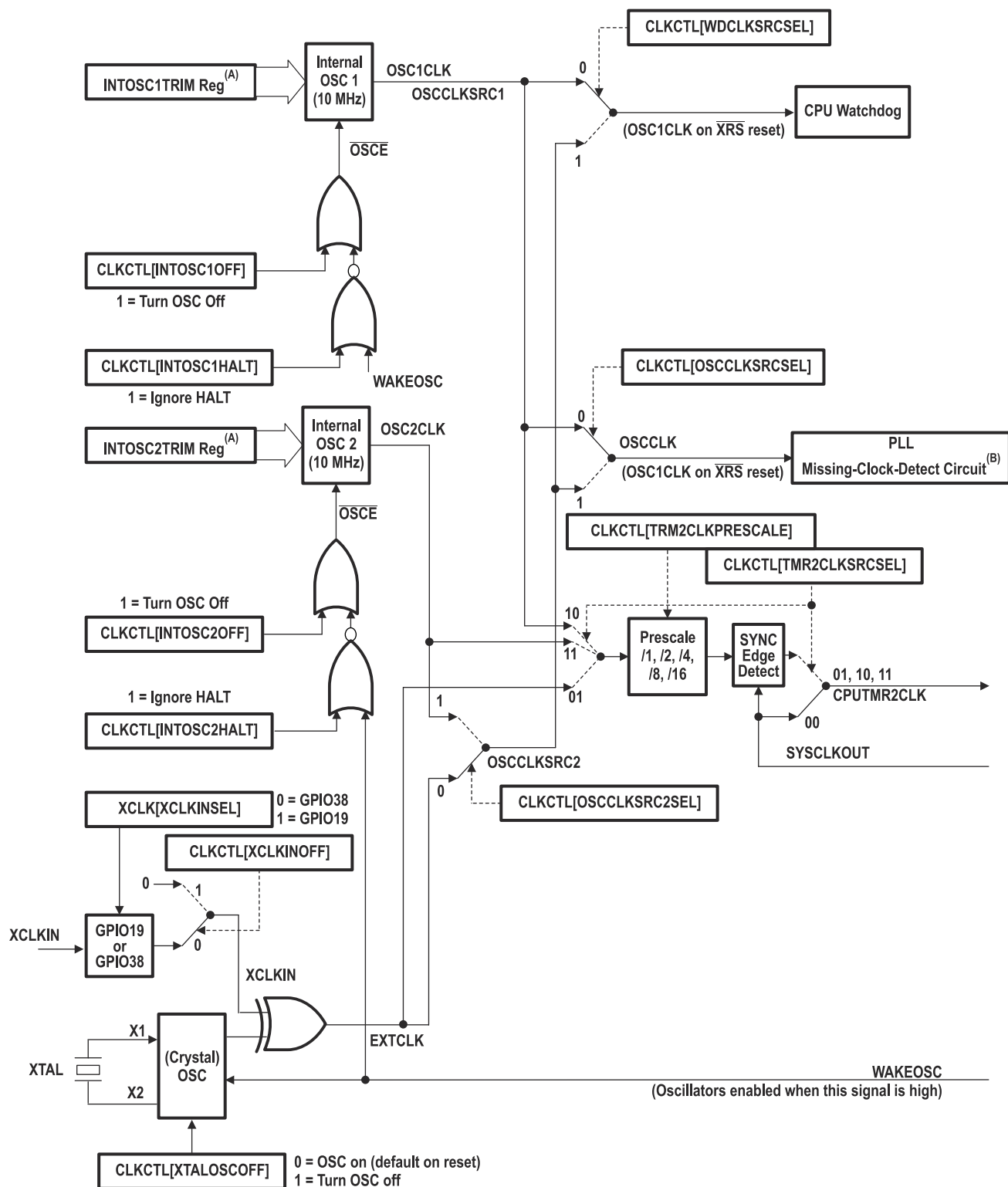
图 9-7 显示了讨论的各种时钟域。图 9-8 显示了能够为器件运行提供时钟的各种时钟源（内部和外部）。



A. CLKIN 为 CPU 提供时钟。它作为 SYSCLKOUT 从 CPU 传出（也就是说，CLKIN 与 SYSCLKOUT 频率相同）。

图 9-7. 时钟和复位域





- A. 从 TI 基于 OTP 的校准功能载入的寄存器。  
B. 请参阅节 9.6.4 了解有关时钟缺失检测的详情。

图 9-8. 时钟树

9.6.1 内部零引脚振荡器

F2802x 器件包含两个独立的内部零引脚振荡器。缺省情况下，两个振荡器在加电时全都打开，此时，内部振荡器 1 是默认时钟源。为了节能，用户可将不使用的振荡器断电。这些振荡器的中心频率由它们各自的振荡器调整寄存器决定，此寄存器在校准例程中被写入作为引导 ROM 执行的一部分。有关这些振荡器的更多信息，请见 节 8，电气规范。

9.6.2 Crystal Oscillator Option

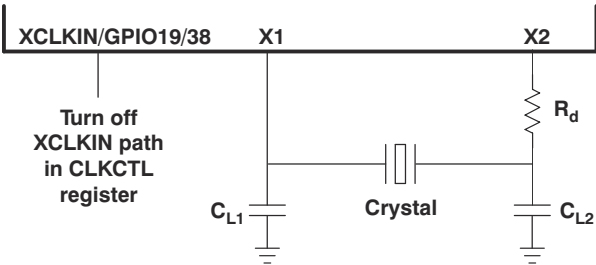
The on-chip crystal oscillator X1 and X2 pins are 1.8-V level signals and must never have 3.3-V level signals applied to them. If a system 3.3-V external oscillator is to be used as a clock source, it should be connected to the XCLKIN pin only. The X1 pin is not intended to be used as a single-ended clock input, it should be used with X2 and a crystal.

The typical specifications for the external quartz crystal (fundamental mode, parallel resonant) are listed in 表 9-13. Furthermore, ESR range = 30 to 150 Ω.

表 9-13. Typical Specifications for External Quartz Crystal<sup>(1)</sup>

| FREQUENCY (MHz) | R <sub>d</sub> (Ω) | C <sub>L1</sub> (pF) | C <sub>L2</sub> (pF) |
|-----------------|--------------------|----------------------|----------------------|
| 5               | 2200               | 18                   | 18                   |
| 10              | 470                | 15                   | 15                   |
| 15              | 0                  | 15                   | 15                   |
| 20              | 0                  | 12                   | 12                   |

(1) C<sub>shunt</sub> should be less than or equal to 5 pF.



A. X1/X2 pins are available in 48-pin package only.

图 9-9. Using the On-chip Crystal Oscillator

备注

- C<sub>L1</sub> and C<sub>L2</sub> are the total capacitance of the circuit board and components excluding the IC and crystal. The value is usually approximately twice the value of the crystal's load capacitance.
- The load capacitance of the crystal is described in the crystal specifications of the manufacturers.
- TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the MCU chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will produce proper start-up and stability over the entire operating range.

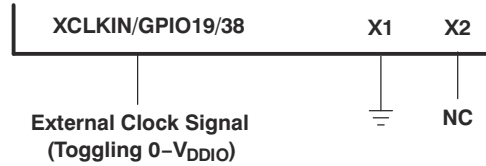


图 9-10. Using a 3.3-V External Oscillator

### 9.6.3 PLL-Based Clock Module

The devices have an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control PLLCR[DIV] to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. It can be re-enabled (if need be) after the PLL module has stabilized, which takes 1 ms. The input clock and PLLCR[DIV] bits should be chosen in such a way that the output frequency of the PLL (VCOCLK) is at least 50 MHz.

表 9-14. PLL Settings

| PLLCR[DIV] VALUE <sup>(2) (3)</sup> | SYSCLKOUT (CLKIN)                      |                    |                    |
|-------------------------------------|----------------------------------------|--------------------|--------------------|
|                                     | PLLSTS[DIVSEL] = 0 or 1 <sup>(1)</sup> | PLLSTS[DIVSEL] = 2 | PLLSTS[DIVSEL] = 3 |
| 0000 (PLL bypass)                   | OSCCLK/4 (Default) <sup>(2)</sup>      | OSCCLK/2           | OSCCLK             |
| 0001                                | (OSCCLK * 1)/4                         | (OSCCLK * 1)/2     | (OSCCLK * 1)/1     |
| 0010                                | (OSCCLK * 2)/4                         | (OSCCLK * 2)/2     | (OSCCLK * 2)/1     |
| 0011                                | (OSCCLK * 3)/4                         | (OSCCLK * 3)/2     | (OSCCLK * 3)/1     |
| 0100                                | (OSCCLK * 4)/4                         | (OSCCLK * 4)/2     | (OSCCLK * 4)/1     |
| 0101                                | (OSCCLK * 5)/4                         | (OSCCLK * 5)/2     | (OSCCLK * 5)/1     |
| 0110                                | (OSCCLK * 6)/4                         | (OSCCLK * 6)/2     | (OSCCLK * 6)/1     |
| 0111                                | (OSCCLK * 7)/4                         | (OSCCLK * 7)/2     | (OSCCLK * 7)/1     |
| 1000                                | (OSCCLK * 8)/4                         | (OSCCLK * 8)/2     | (OSCCLK * 8)/1     |
| 1001                                | (OSCCLK * 9)/4                         | (OSCCLK * 9)/2     | (OSCCLK * 9)/1     |
| 1010                                | (OSCCLK * 10)/4                        | (OSCCLK * 10)/2    | (OSCCLK * 10)/1    |
| 1011                                | (OSCCLK * 11)/4                        | (OSCCLK * 11)/2    | (OSCCLK * 11)/1    |
| 1100                                | (OSCCLK * 12)/4                        | (OSCCLK * 12)/2    | (OSCCLK * 12)/1    |

- (1) By default, PLLSTS[DIVSEL] is configured for /4. (The boot ROM changes this to /1.) PLLSTS[DIVSEL] must be 0 before writing to the PLLCR and should be changed only after PLLSTS[PLLOCKS] = 1.
- (2) The PLL control register (PLLCR) and PLL Status Register (PLLSTS) are reset to their default state by the XRS signal or a watchdog reset only. A reset issued by the debugger or the missing clock detect logic has no effect.
- (3) This register is EALLOW protected. See the System Control chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#) for more information.

表 9-15. CLKIN Divide Options

| PLLSTS [DIVSEL] | CLKIN DIVIDE |
|-----------------|--------------|
| 0               | /4           |
| 1               | /4           |
| 2               | /2           |
| 3               | /1           |

The PLL-based clock module provides four modes of operation:

- **INTOSC1 (Internal Zero-pin Oscillator 1):** This is the on-chip internal oscillator 1. This can provide the clock for the Watchdog block, core and CPU-Timer 2
- **INTOSC2 (Internal Zero-pin Oscillator 2):** This is the on-chip internal oscillator 2. This can provide the clock for the Watchdog block, core and CPU-Timer 2. Both INTOSC1 and INTOSC2 can be independently chosen for the Watchdog block, core and CPU-Timer 2.
- **Crystal/Resonator Operation:** The on-chip (crystal) oscillator enables the use of an external crystal/resonator attached to the device to provide the time base. The crystal/resonator is connected to the X1/X2 pins. Some devices may not have the X1/X2 pins. See 节 7.2.1 for details.
- **External Clock Source Operation:** If the on-chip (crystal) oscillator is not used, this mode allows it to be bypassed. The device clocks are generated from an external clock source input on the XCLKIN pin. The XCLKIN is multiplexed with GPIO19 or GPIO38 pin. The XCLKIN input can be selected as GPIO19 or GPIO38 through the XCLKINSEL bit in XCLK register. The CLKCTL[XCLKINOFF] bit disables this clock input (forced low). If the clock source is not used or the respective pins are used as GPIOs, the user should disable at boot time.

Before changing clock sources, ensure that the target clock is present. If a clock is not present, then that clock source must be disabled (using the CLKCTL register) before switching clocks.

表 9-16. Possible PLL Configuration Modes

| PLL MODE   | REMARKS                                                                                                                                                                                                                                                                                                                                                               | PLLSTS[DIVSEL] | CLKIN AND SYSCLKOUT                          |
|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------------------------------------------|
| PLL Off    | Invoked by the user setting the PLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low-power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN. | 0, 1<br>2<br>3 | OSCCLK/4<br>OSCCLK/2<br>OSCCLK/1             |
| PLL Bypass | PLL Bypass is the default PLL configuration upon power-up or after an external reset (XRS). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL is bypassed but the PLL is not turned off.                                                     | 0, 1<br>2<br>3 | OSCCLK/4<br>OSCCLK/2<br>OSCCLK/1             |
| PLL Enable | Achieved by writing a nonzero value n into the PLLCR register. Upon writing to the PLLCR the device will switch to PLL Bypass mode until the PLL locks.                                                                                                                                                                                                               | 0, 1<br>2<br>3 | OSCCLK * n/4<br>OSCCLK * n/2<br>OSCCLK * n/1 |

#### 9.6.4 输入时钟的损耗 ( NMI 看门狗功能 )

2802x 器件可由两个内部零引脚振荡器 (INTOSC1/INTOSC2) 的其中任一个、片上晶体振荡器、或者一个外部时钟输入提供时钟信号。无论时钟源是什么，在 PLL 启用和 PLL 旁路模式中，如果到 PLL 的输入时钟消失，PLL 将在其输出上发出一个跛行模式时钟。这个跛行模式时钟持续为 CPU 和外设提供一个典型值为 1-5MHz 的时钟。

当跛行模式被激活时，一个被锁存为 NMI 中断的  $\overline{\text{CLOCLFAIL}}$  信号被生成。根据 NMIRESETSEL 位的配置方式，器件复位可能会被立即触发或者 NMI 看门狗计数器溢出时发出复位。除此之外，会设置丢失时钟状态 (MCLKSTS) 位。应用可使用 NMI 中断来检测输入时钟故障并启动所需的校正操作，例如切换到另一个时钟源 (如果有的话) 或者为系统启动一个关断过程。

如果软件对于时钟故障情况没有响应，NMI 看门狗将在一个预编程的时间间隔后触发复位。图 9-11 显示了涉及的中断机制。



2802x 器件上的 CPU 看门狗模块与 281x/280x/283x 器件上所使用的类似。只要 8 位看门狗递增计数器达到了它的最大值，这个模块就生成一个输出脉冲，512 振荡器时钟宽度 (OSCCLK)。为防止这一情况，用户必须禁用计数器，或者软件必须定期向看门狗键值寄存器写入一个 0x55 + 0xAA 序列，用于复位看门狗计数器。图 9-12 显示了看门狗模块内的各种功能块。

备注

备注

在正确 CPU 运行频率绝对关键的应用中应该执行一个机制，通过这个机制，只要输入时钟出现故障，MCU 就被保持在复位状态。例如，只要电容器充满电，一个 R-C 电路可被用于触发 MCU 的  $\overline{\text{XRS}}$  引脚。一个 I/O 引脚可被用于定期为电容器放电以防止其被完全充满。这样一个电路也有助于检测闪存存储器的故障。



**WDINT** 信号支持使用看门狗从空闲/待机模式唤醒。

在空闲模式下， $\overline{\text{WDINT}}$  信号可通过 PIE 对 CPU 生成一个中断，以便使 CPU 退出空闲模式。

在停机模式下，CPU 看门狗可用来通过器件复位唤醒器件。

## 9.7 Low-power Modes Block

表 9-17 summarizes the various modes.

**表 9-17. Low-power Modes**

| MODE                | LPMCR0(1:0) | OSCCLK                                                                                                                     | CLKIN | SYSCLKOUT | EXIT <sup>(1)</sup>                                                                           |
|---------------------|-------------|----------------------------------------------------------------------------------------------------------------------------|-------|-----------|-----------------------------------------------------------------------------------------------|
| IDLE                | 00          | On                                                                                                                         | On    | On        | $\overline{\text{XRS}}$ , CPU watchdog interrupt, any enabled interrupt                       |
| STANDBY             | 01          | On<br>(CPU watchdog still running)                                                                                         | Off   | Off       | $\overline{\text{XRS}}$ , CPU watchdog interrupt, GPIO Port A signal, debugger <sup>(2)</sup> |
| HALT <sup>(3)</sup> | 1X          | Off<br>(on-chip crystal oscillator and PLL turned off, zero-pin oscillator and CPU watchdog state dependent on user code.) | Off   | Off       | $\overline{\text{XRS}}$ , GPIO Port A signal, debugger <sup>(2)</sup> , CPU watchdog          |

- (1) The EXIT column lists which signals or under what conditions the low-power mode is exited. A low signal, on any of the signals, exits the low-power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise, the low-power mode will not be exited and the device will go back into the indicated low-power mode.
- (2) The JTAG port can still function even if the CPU clock (CLKIN) is turned off.
- (3) The WDCLK must be active for the device to go into HALT mode.

The various low-power modes operate as follows:

|               |                                                                                                                                                                                                                                                                                                               |
|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDLE Mode:    | This mode is exited by any enabled interrupt that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.                                                                                                                            |
| STANDBY Mode: | Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signal(s) will wake the device in the GPIOLPMSEL register. The selected signal(s) are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register. |
| HALT Mode:    | CPU watchdog, $\overline{\text{XRS}}$ , and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.                                                                                                                                   |

### 备注

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed. See the System Control chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#) for more details.

## 9.8 Interrupts

图 9-13 shows how the various interrupt sources are multiplexed.

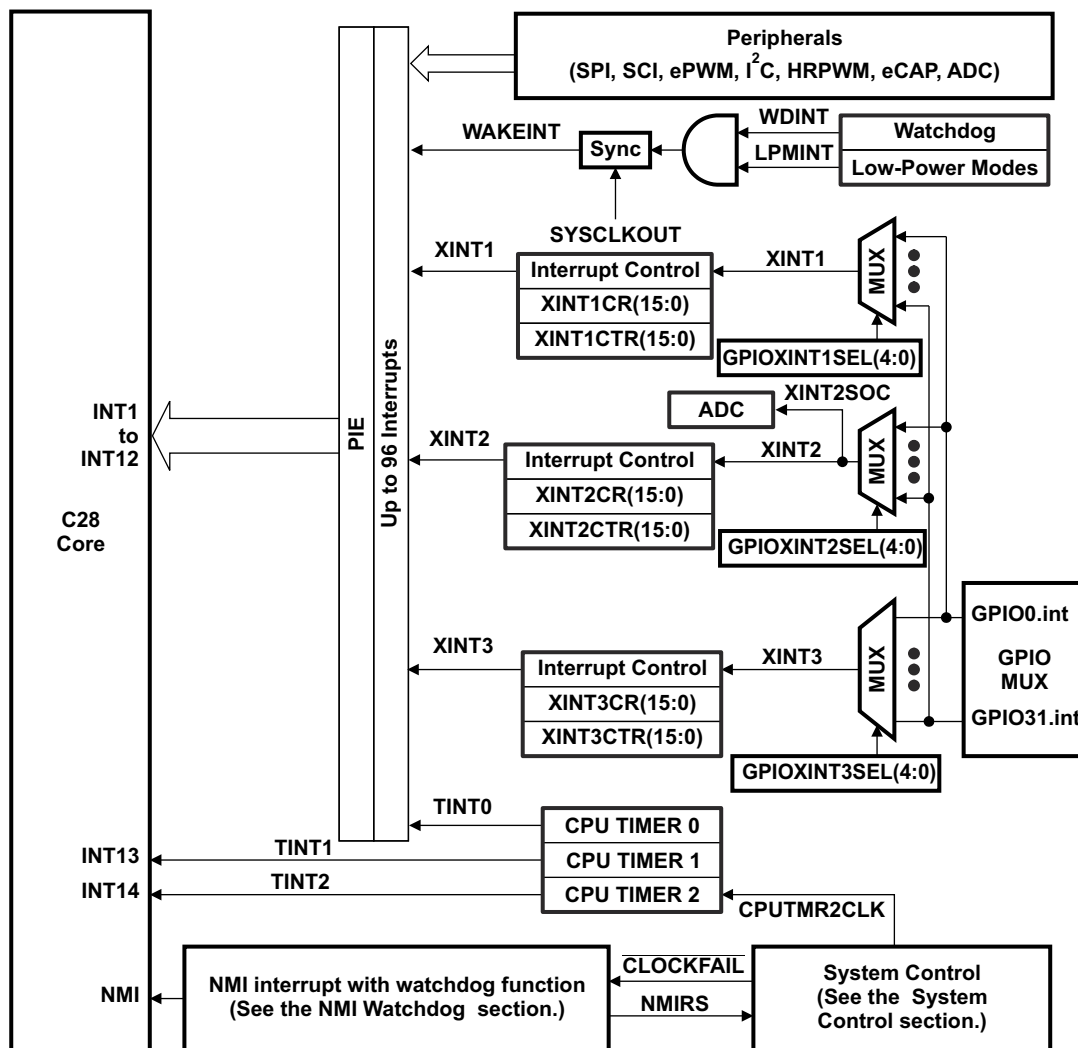


图 9-13. External and PIE Interrupt Sources



Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. 表 9-18 shows the interrupts used by 2802x devices.

The TRAP #VectorNumber instruction transfers program control to the interrupt service routine corresponding to the vector specified. The TRAP #0 instruction attempts to transfer program control to the address pointed to by the reset vector. The PIE vector table does not, however, include a reset vector. Therefore, the TRAP #0 instruction should not be used when the PIE is enabled. Doing so will result in undefined behavior.

When the PIE is enabled, the TRAP #1 to TRAP #12 instructions will transfer program control to the interrupt service routine corresponding to the first vector within the PIE group. For example: the TRAP #1 instruction fetches the vector from INT1.1, the TRAP #2 instruction fetches the vector from INT2.1, and so forth.

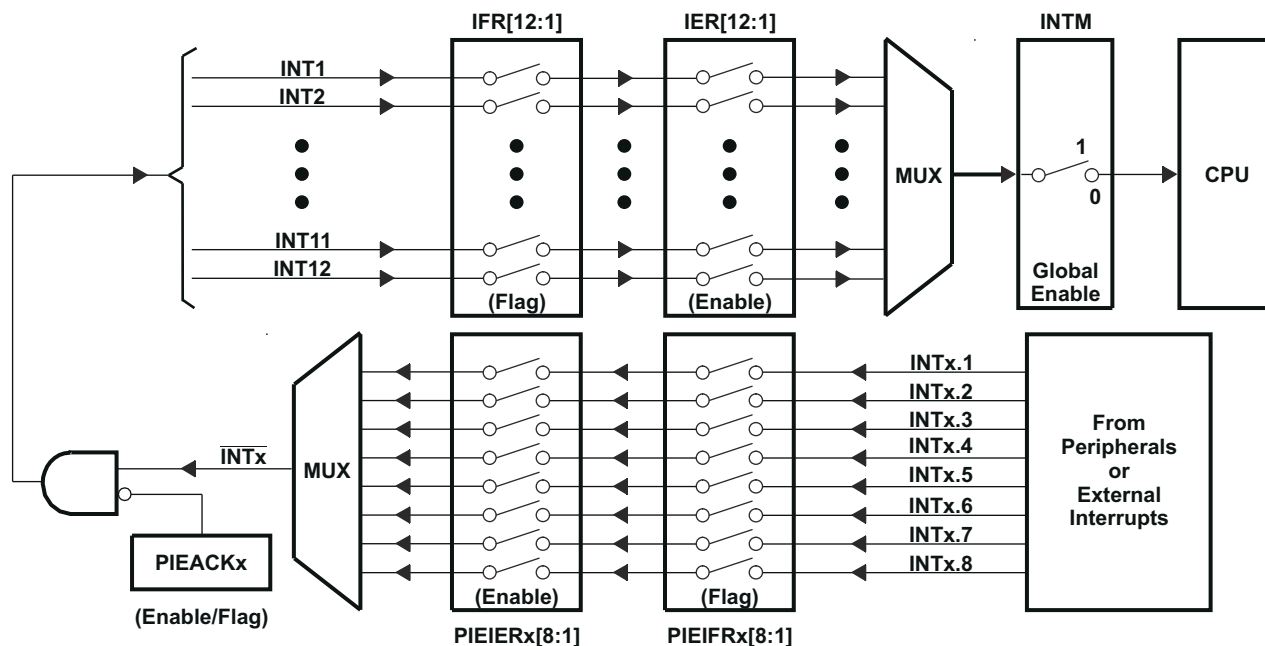


图 9-14. Multiplexing of Interrupts Using the PIE Block

**表 9-18. PIE MUXed Peripheral Interrupt Vector Table**

|         | INTx.8 <sup>(1)</sup>        | INTx.7                      | INTx.6                    | INTx.5                        | INTx.4                          | INTx.3                          | INTx.2                          | INTx.1                          |
|---------|------------------------------|-----------------------------|---------------------------|-------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| INT1.y  | WAKEINT<br>(LPM/WD)<br>0xD4E | TINT0<br>(TIMER 0)<br>0xD4C | ADCINT9<br>(ADC)<br>0xD4A | XINT2<br>Ext. int. 2<br>0xD48 | XINT1<br>Ext. int. 1<br>0xD46   | Reserved<br>-<br>0xD44          | ADCINT2<br>(ADC)<br>0xD42       | ADCINT1<br>(ADC)<br>0xD40       |
| INT2.y  | Reserved<br>-<br>0xD5E       | Reserved<br>-<br>0xD5C      | Reserved<br>-<br>0xD5A    | Reserved<br>-<br>0xD58        | EPWM4_TZINT<br>(ePWM4)<br>0xD56 | EPWM3_TZINT<br>(ePWM3)<br>0xD54 | EPWM2_TZINT<br>(ePWM2)<br>0xD52 | EPWM1_TZINT<br>(ePWM1)<br>0xD50 |
| INT3.y  | Reserved<br>-<br>0xD6E       | Reserved<br>-<br>0xD6C      | Reserved<br>-<br>0xD6A    | Reserved<br>-<br>0xD68        | EPWM4_INT<br>(ePWM4)<br>0xD66   | EPWM3_INT<br>(ePWM3)<br>0xD64   | EPWM2_INT<br>(ePWM2)<br>0xD62   | EPWM1_INT<br>(ePWM1)<br>0xD60   |
| INT4.y  | Reserved<br>-<br>0xD7E       | Reserved<br>-<br>0xD7C      | Reserved<br>-<br>0xD7A    | Reserved<br>-<br>0xD78        | Reserved<br>-<br>0xD76          | Reserved<br>-<br>0xD74          | Reserved<br>-<br>0xD72          | ECAP1_INT<br>(eCAP1)<br>0xD70   |
| INT5.y  | Reserved<br>-<br>0xD8E       | Reserved<br>-<br>0xD8C      | Reserved<br>-<br>0xD8A    | Reserved<br>-<br>0xD88        | Reserved<br>-<br>0xD86          | Reserved<br>-<br>0xD84          | Reserved<br>-<br>0xD82          | Reserved<br>-<br>0xD80          |
| INT6.y  | Reserved<br>-<br>0xD9E       | Reserved<br>-<br>0xD9C      | Reserved<br>-<br>0xD9A    | Reserved<br>-<br>0xD98        | Reserved<br>-<br>0xD96          | Reserved<br>-<br>0xD94          | SPITXINTA<br>(SPI-A)<br>0xD92   | SPIRXINTA<br>(SPI-A)<br>0xD90   |
| INT7.y  | Reserved<br>-<br>0xDAE       | Reserved<br>-<br>0xDAC      | Reserved<br>-<br>0xDAA    | Reserved<br>-<br>0xDA8        | Reserved<br>-<br>0xDA6          | Reserved<br>-<br>0xDA4          | Reserved<br>-<br>0xDA2          | Reserved<br>-<br>0xDA0          |
| INT8.y  | Reserved<br>-<br>0xDBE       | Reserved<br>-<br>0xDBC      | Reserved<br>-<br>0xDBA    | Reserved<br>-<br>0xDB8        | Reserved<br>-<br>0xDB6          | Reserved<br>-<br>0xDB4          | I2CINT2A<br>(I2C-A)<br>0xDB2    | I2CINT1A<br>(I2C-A)<br>0xDB0    |
| INT9.y  | Reserved<br>-<br>0xDCE       | Reserved<br>-<br>0xDCC      | Reserved<br>-<br>0xDCA    | Reserved<br>-<br>0xDC8        | Reserved<br>-<br>0xDC6          | Reserved<br>-<br>0xDC4          | SCITXINTA<br>(SCI-A)<br>0xDC2   | SCIRXINTA<br>(SCI-A)<br>0xDC0   |
| INT10.y | ADCINT8<br>(ADC)<br>0xDDE    | ADCINT7<br>(ADC)<br>0xDDC   | ADCINT6<br>(ADC)<br>0xDDA | ADCINT5<br>(ADC)<br>0xDD8     | ADCINT4<br>(ADC)<br>0xDD6       | ADCINT3<br>(ADC)<br>0xDD4       | ADCINT2<br>(ADC)<br>0xDD2       | ADCINT1<br>(ADC)<br>0xDD0       |
| INT11.y | Reserved<br>-<br>0xDEE       | Reserved<br>-<br>0xDEC      | Reserved<br>-<br>0xDEA    | Reserved<br>-<br>0xDE8        | Reserved<br>-<br>0xDE6          | Reserved<br>-<br>0xDE4          | Reserved<br>-<br>0xDE2          | Reserved<br>-<br>0xDE0          |
| INT12.y | Reserved<br>-<br>0xDFE       | Reserved<br>-<br>0xDFC      | Reserved<br>-<br>0xDFA    | Reserved<br>-<br>0xDF8        | Reserved<br>-<br>0xDF6          | Reserved<br>-<br>0xDF4          | Reserved<br>-<br>0xDF2          | XINT3<br>Ext. Int. 3<br>0xDF0   |

(1) Out of 96 possible interrupts, some interrupts are not used. These interrupts are reserved for future devices. These interrupts can be used as software interrupts if they are enabled at the PIEIFRx level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming in from peripherals may be lost by accidentally clearing their flag while modifying the PIEIFR. To summarize, there are two safe cases when the reserved interrupts could be used as software interrupts:

- No peripheral within the group is asserting interrupts.
- No peripheral interrupts are assigned to the group (for example, PIE groups 5, 7, or 11) .

**表 9-19. PIE Configuration and Control Registers**

| NAME     | ADDRESS            | SIZE (x16) | DESCRIPTION <sup>(1)</sup>       |
|----------|--------------------|------------|----------------------------------|
| PIECTRL  | 0x0CE0             | 1          | PIE, Control Register            |
| PIEACK   | 0x0CE1             | 1          | PIE, Acknowledge Register        |
| PIEIER1  | 0x0CE2             | 1          | PIE, INT1 Group Enable Register  |
| PIEIFR1  | 0x0CE3             | 1          | PIE, INT1 Group Flag Register    |
| PIEIER2  | 0x0CE4             | 1          | PIE, INT2 Group Enable Register  |
| PIEIFR2  | 0x0CE5             | 1          | PIE, INT2 Group Flag Register    |
| PIEIER3  | 0x0CE6             | 1          | PIE, INT3 Group Enable Register  |
| PIEIFR3  | 0x0CE7             | 1          | PIE, INT3 Group Flag Register    |
| PIEIER4  | 0x0CE8             | 1          | PIE, INT4 Group Enable Register  |
| PIEIFR4  | 0x0CE9             | 1          | PIE, INT4 Group Flag Register    |
| PIEIER5  | 0x0CEA             | 1          | PIE, INT5 Group Enable Register  |
| PIEIFR5  | 0x0CEB             | 1          | PIE, INT5 Group Flag Register    |
| PIEIER6  | 0x0CEC             | 1          | PIE, INT6 Group Enable Register  |
| PIEIFR6  | 0x0CED             | 1          | PIE, INT6 Group Flag Register    |
| PIEIER7  | 0x0CEE             | 1          | PIE, INT7 Group Enable Register  |
| PIEIFR7  | 0x0CEF             | 1          | PIE, INT7 Group Flag Register    |
| PIEIER8  | 0x0CF0             | 1          | PIE, INT8 Group Enable Register  |
| PIEIFR8  | 0x0CF1             | 1          | PIE, INT8 Group Flag Register    |
| PIEIER9  | 0x0CF2             | 1          | PIE, INT9 Group Enable Register  |
| PIEIFR9  | 0x0CF3             | 1          | PIE, INT9 Group Flag Register    |
| PIEIER10 | 0x0CF4             | 1          | PIE, INT10 Group Enable Register |
| PIEIFR10 | 0x0CF5             | 1          | PIE, INT10 Group Flag Register   |
| PIEIER11 | 0x0CF6             | 1          | PIE, INT11 Group Enable Register |
| PIEIFR11 | 0x0CF7             | 1          | PIE, INT11 Group Flag Register   |
| PIEIER12 | 0x0CF8             | 1          | PIE, INT12 Group Enable Register |
| PIEIFR12 | 0x0CF9             | 1          | PIE, INT12 Group Flag Register   |
| Reserved | 0x0CFA –<br>0x0CFF | 6          | Reserved                         |

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

## 9.8.1 External Interrupts

表 9-20. External Interrupt Registers

| NAME     | ADDRESS   | SIZE (x16) | DESCRIPTION                  |
|----------|-----------|------------|------------------------------|
| XINT1CR  | 0x00 7070 | 1          | XINT1 configuration register |
| XINT2CR  | 0x00 7071 | 1          | XINT2 configuration register |
| XINT3CR  | 0x00 7072 | 1          | XINT3 configuration register |
| XINT1CTR | 0x00 7078 | 1          | XINT1 counter register       |
| XINT2CTR | 0x00 7079 | 1          | XINT2 counter register       |
| XINT3CTR | 0x00 707A | 1          | XINT3 counter register       |

Each external interrupt can be enabled/disabled or qualified using positive, negative, or both positive and negative edge. For more information, see the System Control chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).

### 9.8.1.1 外部中断电子数据/定时

#### 9.8.1.1.1 External Interrupt Timing Requirements

|                                                                |                | MIN <sup>(1)</sup>          | MAX | UNIT   |
|----------------------------------------------------------------|----------------|-----------------------------|-----|--------|
| $t_{w(INT)}$ <sup>(2)</sup> Pulse duration, INT input low/high | Synchronous    | $1t_{c(SCO)}$               |     | cycles |
|                                                                | With qualifier | $1t_{c(SCO)} + t_{w(IQSW)}$ |     | cycles |

(1) For an explanation of the input qualifier parameters, see [节 9.9.10.1.2.1](#).

(2) This timing is applicable to any GPIO pin configured for ADCSOC functionality.

#### 9.8.1.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                                       | MIN <sup>(1)</sup>           | MAX | UNIT   |
|-----------------------------------------------------------------|------------------------------|-----|--------|
| $t_{d(INT)}$ Delay time, INT low/high to interrupt-vector fetch | $t_{w(IQSW)} + 12t_{c(SCO)}$ |     | cycles |

(1) For an explanation of the input qualifier parameters, see [节 9.9.10.1.2.1](#).

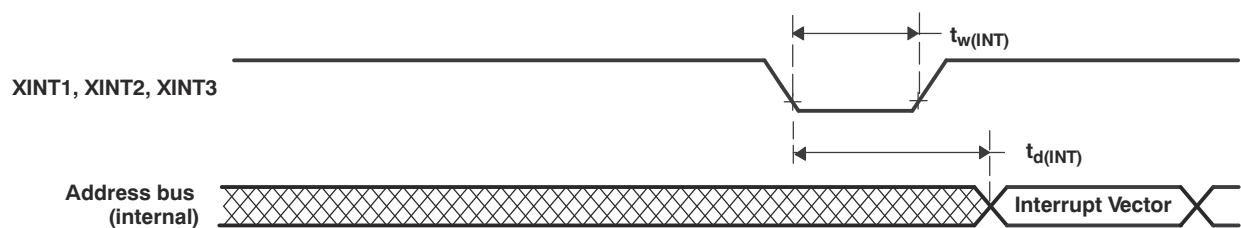


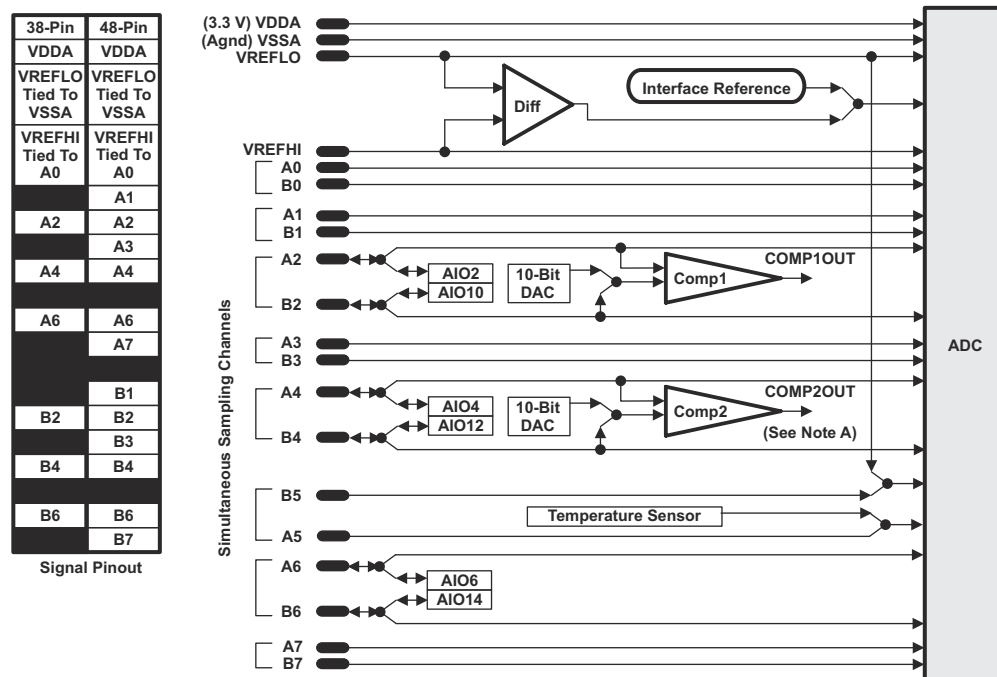
图 9-15. External Interrupt Timing

## 9.9 外设

### 9.9.1 Analog Block

A 12-bit ADC core is implemented that has different timings than the 12-bit ADC used on F280x/F2833x. The ADC wrapper is modified to incorporate the new timings and also other enhancements to improve the timing control of start of conversions. 图 9-16 shows the interaction of the analog module with the rest of the F2802x system.

For more information on the ADC, see the Analog-to-Digital Converter and Comparator chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).



A. Comparator 2 is available only on the 48-pin PT package.

图 9-16. Analog Pin Configurations

### 9.9.1.1 模数转换器 (ADC)

#### 9.9.1.1.1 特性

ADC 的内核包含有一个单一 12 位转换器，此转换器由两个采样保持电路供源。可以对这两个采样保持电路进行同步采样或顺序采样。按顺序，这些电路由总共高达 13 个模拟输入通道供源。此转换器可配置为采用内部带隙基准运行，以便形成基于实际电压的转换，或者采用一对外部电压基准 ( $V_{REFHI}/V_{REFLO}$ ) 运行，形成基于比率的转换。

与之前的 ADC 类型不同，此 ADC 并非基于序列发生器。对于用户来讲，他们可以很容易地从一个单触发来创建一系列的转换。然而，操作的基本原则是以单个转换的配置为中心，被称为 SOC，或者转换启动。

ADC 模块的功能包括：

- 具有内置双采样保持 (S/H) 的 12 位 ADC 内核
- 同步采样模式或顺序采样模式
- 全范围模拟输入：0V 至 3.3V 固定电压，或  $V_{REFHI}/V_{REFLO}$  比率。输入模拟电压的数值源自：
  - 内部基准 ( $V_{REFLO}=V_{SSA}$ 。当使用内部或者外部基准模式时， $V_{REFHI}$  不得超过  $V_{DDA}$ 。)

Digital Value = 0, when input  $\leq 0$  V

Digital Value =  $4096 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{3.3}$  when  $0 \text{ V} < \text{input} < 3.3 \text{ V}$

Digital Value = 4095, when input  $\geq 3.3 \text{ V}$

- 外部基准 ( $V_{REFHI}/V_{REFLO}$  被连接至外部基准。当使用内部或者外部基准模式时， $V_{REFHI}$  不得超过  $V_{DDA}$ 。)

Digital Value = 0, when input  $\leq 0$  V

Digital Value =  $4096 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{V_{REFHI} - V_{REFLO}}$  when  $0 \text{ V} < \text{input} < V_{REFHI}$

Digital Value = 4095, when input  $\geq V_{REFHI}$

- 多达 16 个通道，多路复用输入
- 16 个 SOC，可针对触发、采样窗口和通道进行配置
- 用于存储转换值的 16 个结果寄存器 (可单独寻址)
- 多个触发源
  - S/W - 软件立即启动
  - ePWM 1-4
  - GPIO XINT2
  - CPU 计时器 0/1/2
  - ADCINT1/2
- 9 个灵活的 PIE 中断，可在任一个转换后配置中断请求

表 9-21. ADC 配置和控制寄存器

| 寄存器名称                       | 地址            | 大小<br>(x16) | 受 EALLOW<br>保护 | 说明                           |
|-----------------------------|---------------|-------------|----------------|------------------------------|
| ADCCTL1                     | 0x7100        | 1           | 是              | 控制 1 寄存器                     |
| ADCCTL2                     | 0x7101        | 1           | 是              | 控制 2 寄存器                     |
| ADCINTFLG                   | 0x7104        | 1           | 否              | 中断标志寄存器                      |
| ADCINTFLGCLR                | 0x7105        | 1           | 否              | 中断标志清除寄存器                    |
| ADCINTOVF                   | 0x7106        | 1           | 否              | 中断溢出寄存器                      |
| ADCINTOVFCLR                | 0x7107        | 1           | 否              | 中断溢出清除寄存器                    |
| INTSEL1N2                   | 0x7108        | 1           | 是              | 中断 1 和 2 选择寄存器               |
| INTSEL3N4                   | 0x7109        | 1           | 是              | 中断 3 和 4 选择寄存器               |
| INTSEL5N6                   | 0x710A        | 1           | 是              | 中断 5 和 6 选择寄存器               |
| INTSEL7N8                   | 0x710B        | 1           | 是              | 中断 7 和 8 选择寄存器               |
| INTSEL9N10                  | 0x710C        | 1           | 是              | 中断 9 选择寄存器 ( 被保留的中断 10 选择 )  |
| SOCPRCTL                    | 0x7110        | 1           | 是              | SOC 优先级控制寄存器                 |
| ADCSAMPLEMODE               | 0x7112        | 1           | 是              | 采样模式寄存器                      |
| ADCINTSOCSEL1               | 0x7114        | 1           | 是              | 中断 SOC 选择 1 寄存器 ( 用于 8 个通道 ) |
| ADCINTSOCSEL2               | 0x7115        | 1           | 是              | 中断 SOC 选择 2 寄存器 ( 用于 8 个通道 ) |
| ADCSOFLG1                   | 0x7118        | 1           | 否              | SOC 标志 1 寄存器 ( 用于 16 个通道 )   |
| ADCSOFCRC1                  | 0x711A        | 1           | 否              | SOC 强制 1 寄存器 ( 用于 16 个通道 )   |
| ADCSOCOVF1                  | 0x711C        | 1           | 否              | SOC 溢出 1 寄存器 ( 用于 16 个通道 )   |
| ADCSOCOVFCLR1               | 0x711E        | 1           | 否              | SOC 溢出清除 1 寄存器 ( 用于 16 个通道 ) |
| ADCSOC0CTL 至<br>ADCSOC15CTL | 0x7120-0x712F | 1           | 是              | SOC0 控制寄存器至 SOC15 控制寄存器      |
| ADCREFTIM                   | 0x7140        | 1           | 是              | 基准调整寄存器                      |
| ADCOFFTRIM                  | 0x7141        | 1           | 是              | 偏移调整寄存器                      |
| COMPHYSTCTL                 | 0x714C        | 1           | 是              | 比较器滞后控制寄存器                   |
| ADCREV                      | 0x714F        | 1           | 否              | 修订版本寄存器                      |

表 9-22. ADC 结果寄存器 ( 被映射至 PF0 )

| 寄存器名称                    | 地址            | 大小<br>(x16) | 受 EALLOW<br>保护 | 说明                          |
|--------------------------|---------------|-------------|----------------|-----------------------------|
| ADCRESULT0 至 ADCRESULT15 | 0xB00 至 0xB0F | 1           | 否              | ADC 结果 0 寄存器至 ADC 结果 15 寄存器 |

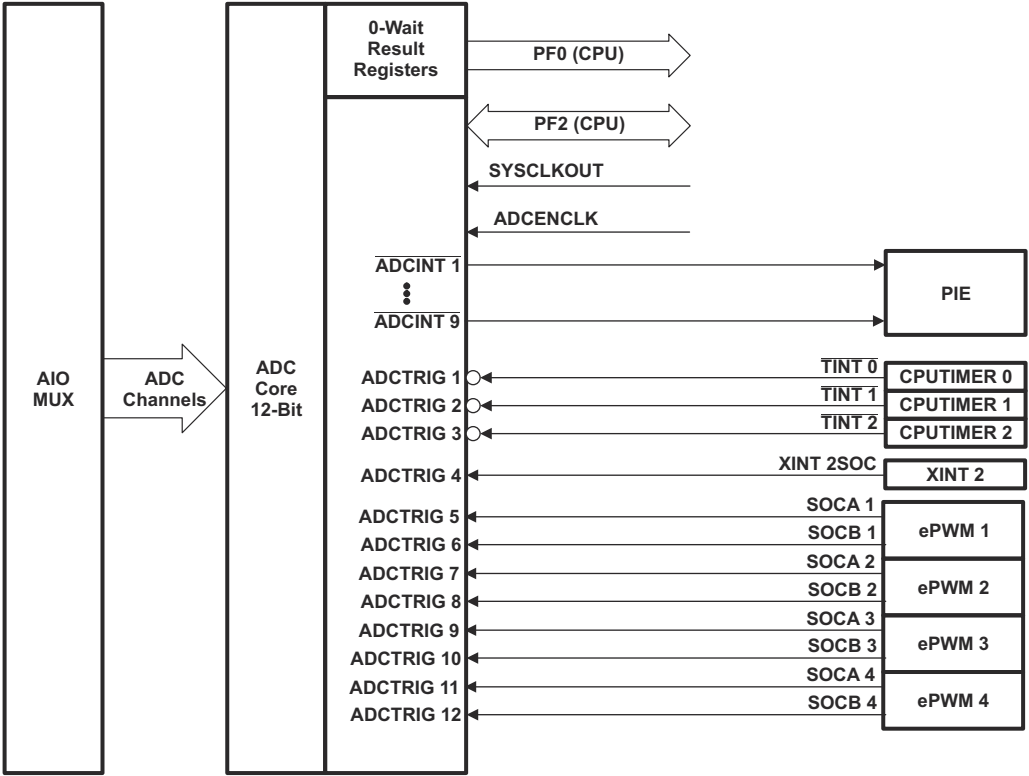


图 9-17. ADC 连接

### 不使用 ADC 时的 ADC 连接

TI 建议即使不使用 ADC，也应保持模拟电源引脚的连接。下面总结了如果 ADC 未在申请中使用，应该如何连接 ADC 引脚：

- $V_{DDA}$  - 连接到  $V_{DDIO}$
- $V_{SSA}$  - 连接到  $V_{SS}$
- $V_{REFLO}$  - 连接到  $V_{SS}$
- $ADCINAn$ ,  $ADCINBn$ ,  $V_{REFHI}$  - 连接到  $V_{SSA}$

当在一个应用中使用 ADC 模块时，未使用的 ADC 输入引脚应被连接至模拟接地 ( $V_{SSA}$ )。

### 备注

与 AIO 功能复用的未使用 ADCIN 引脚不应直接连接到模拟地。它们应该通过一个  $1k\Omega$  电阻器接地。这是为了防止一个错误代码将这些引脚配置为 AIO 输出并将接地的引脚驱动至一个逻辑高电平状态。

当 ADC 未被使用时，为了达到节能的目的，请确保到 ADC 模块的时钟未被打开。



### 9.9.1.1.2 ADC 转换开始电子数据/定时

#### 9.9.1.1.2.1 外部 ADC 转换启动开关特性

在推荐的运行条件下 ( 除非另有说明 )

| 参数                                                    | 最小值            | 最大值 | 单位 |
|-------------------------------------------------------|----------------|-----|----|
| $t_{w(ADCSOCL)}$ 脉冲持续时间, $\overline{ADCSOCxO}$ 低电平的时间 | $32t_{c(HCO)}$ |     | 周期 |

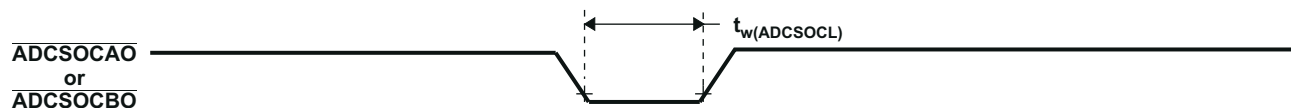


图 9-18.  $\overline{ADCSOCxO}$  或者  $\overline{ADCSOCBO}$  时序

### 9.9.1.1.3 片载模数转换器 (ADC) 电子数据/定时

#### 9.9.1.1.3.1 ADC Electrical Characteristics

| PARAMETER                                                                    |                                                      | MIN                | TYP | MAX | UNIT                 |
|------------------------------------------------------------------------------|------------------------------------------------------|--------------------|-----|-----|----------------------|
| DC SPECIFICATIONS                                                            |                                                      |                    |     |     |                      |
| Resolution                                                                   |                                                      | 12                 |     |     | Bits                 |
| ADC clock                                                                    | 60-MHz device                                        | 0.001              |     |     | 60 MHz               |
| Sample Window                                                                | 28027/26/23/22                                       | 7                  |     |     | ADC<br>Clocks        |
|                                                                              | 28021/20/200                                         | 14                 |     |     |                      |
| ACCURACY                                                                     |                                                      |                    |     |     |                      |
| INL (Integral nonlinearity) at ADC Clock $\leq 30$ MHz <sup>(1)</sup>        |                                                      | - 4                |     |     | 4 LSB                |
| DNL (Differential nonlinearity) at ADC Clock $\leq 30$ MHz, no missing codes |                                                      | - 1                |     |     | 1 LSB                |
| Offset error <sup>(2)</sup>                                                  | Executing Device_Cal function                        | - 20               | 0   | 20  | LSB                  |
|                                                                              | Executing periodic self-recalibration <sup>(3)</sup> | - 4                | 0   | 4   |                      |
| Overall gain error with internal reference                                   |                                                      | - 60               |     |     | 60 LSB               |
| Overall gain error with external reference                                   |                                                      | - 40               |     |     | 40 LSB               |
| Channel-to-channel offset variation                                          |                                                      | - 4                |     |     | 4 LSB                |
| Channel-to-channel gain variation                                            |                                                      | - 4                |     |     | 4 LSB                |
| ADC temperature coefficient with internal reference                          |                                                      | - 50               |     |     | ppm/°C               |
| ADC temperature coefficient with external reference                          |                                                      | - 20               |     |     | ppm/°C               |
| V <sub>REFLO</sub>                                                           |                                                      | - 100              |     |     | μA                   |
| V <sub>REFHI</sub>                                                           |                                                      | 100                |     |     | μA                   |
| ANALOG INPUT                                                                 |                                                      |                    |     |     |                      |
| Analog input voltage with internal reference                                 |                                                      | 0                  |     |     | 3.3 V                |
| Analog input voltage with external reference                                 |                                                      | V <sub>REFLO</sub> |     |     | V <sub>REFHI</sub> V |
| V <sub>REFLO</sub> input voltage <sup>(4)</sup>                              |                                                      | V <sub>SSA</sub>   |     |     | V <sub>SSA</sub> V   |
| V <sub>REFHI</sub> input voltage <sup>(5)</sup>                              | with V <sub>REFLO</sub> = V <sub>SSA</sub>           | 1.98               |     |     | V <sub>DDA</sub> V   |
| Input capacitance                                                            |                                                      | 5                  |     |     | pF                   |
| Input leakage current                                                        |                                                      | ±5                 |     |     | μ A                  |

(1) INL will degrade when the ADC input voltage goes above V<sub>DDA</sub>.

(2) 1 LSB has the weighted value of full-scale range (FSR)/4096. FSR is 3.3 V with internal reference and V<sub>REFHI</sub> - V<sub>REFLO</sub> for external reference.

(3) Periodic self-recalibration will remove system-level and temperature dependencies on the ADC zero offset error. This can be performed as needed in the application without sacrificing an ADC channel by using the procedure listed in the "ADC Zero Offset Calibration" section of the Analog-to-Digital Converter and Comparator chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).

(4) V<sub>REFLO</sub> is always connected to V<sub>SSA</sub>.

(5) V<sub>REFHI</sub> must not exceed V<sub>DDA</sub> when using either internal or external reference modes. Because V<sub>REFHI</sub> is tied to ADCINA0, the input signal on ADCINA0 must not exceed V<sub>DDA</sub>.

#### 9.9.1.1.3.2 ADC 电源模式

| ADC 工作模式      | 条件                                                                              | I <sub>DDA</sub> | 单位 |
|---------------|---------------------------------------------------------------------------------|------------------|----|
| 模式 A - 工作模式   | ADC 时钟启用<br>带隙开启 (ADCBGPWD = 1)<br>基准开启 (ADCREFPWD = 1)<br>ADC 加电 (ADCPWDN = 1) | 13               | mA |
| 模式 B - 快速唤醒模式 | ADC 时钟启用<br>带隙开启 (ADCBGPWD = 1)<br>基准开启 (ADCREFPWD = 1)<br>ADC 加电 (ADCPWDN = 0) | 4                | mA |
| 模式 C - 仅比较器模式 | ADC 时钟启用<br>带隙开启 (ADCBGPWD = 1)<br>基准开启 (ADCREFPWD = 0)<br>ADC 加电 (ADCPWDN = 0) | 1.5              | mA |
| 模式 D - 关闭模式   | ADC 时钟启用<br>带隙开启 (ADCBGPWD = 0)<br>基准开启 (ADCREFPWD = 0)<br>ADC 加电 (ADCPWDN = 0) | 0.075            | mA |

#### 9.9.1.1.3.3 内部温度传感器

##### 9.9.1.1.3.3.1 Temperature Sensor Coefficient

| PARAMETER <sup>(1)</sup> |                                                                                         | MIN | TYP                     | MAX | UNIT   |
|--------------------------|-----------------------------------------------------------------------------------------|-----|-------------------------|-----|--------|
| T <sub>SLOPE</sub>       | Degrees C of temperature movement per measured ADC LSB change of the temperature sensor |     | 0.18 <sup>(3) (2)</sup> |     | °C/LSB |
| T <sub>OFFSET</sub>      | ADC output at 0°C of the temperature sensor                                             |     | 1750                    |     | LSB    |

- (1) The temperature sensor slope and offset are given in terms of ADC LSBs using the internal reference of the ADC. Values must be adjusted accordingly in external reference mode to the external reference voltage.
- (2) Output of the temperature sensor (in terms of LSBs) is sign-consistent with the direction of the temperature movement. Increasing temperatures will give increasing ADC values relative to an initial value; decreasing temperatures will give decreasing ADC values relative to an initial value.
- (3) ADC temperature coefficient is accounted for in this specification

#### 9.9.1.1.3.4 ADC 加电控制位时序

##### 9.9.1.1.3.4.1 ADC 加电延迟

| 参数 <sup>(1)</sup>   |                   | 最小值 | 最大值 | 单位 |
|---------------------|-------------------|-----|-----|----|
| t <sub>d(PWD)</sub> | 加电后, ADC 的延迟时间将稳定 |     | 1   | ms |

- (1) 时序保持与 ADC 模块的兼容性。在首次转换前 t<sub>d(PWD)</sub> ms, 2802x ADC 支持同时驱动所有 3 个位。

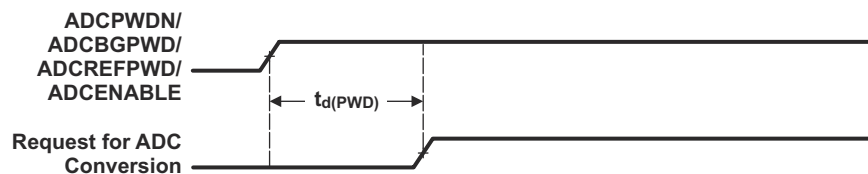
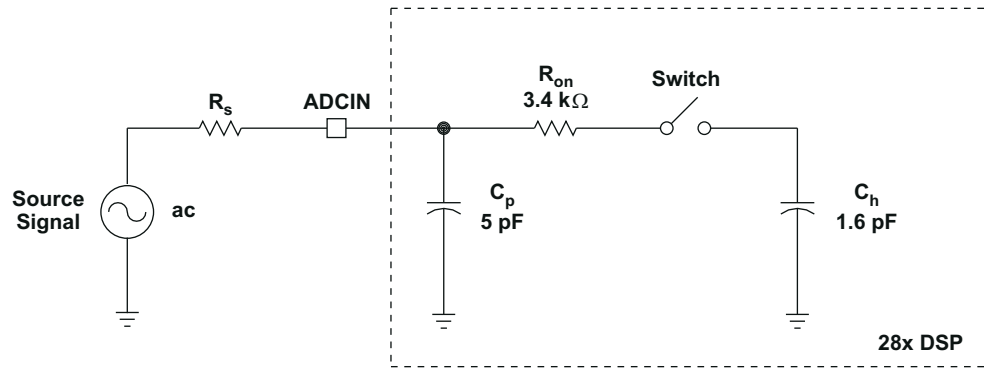


图 9-19. ADC 转换时序



Typical Values of the Input Circuit Components:

Switch Resistance ( $R_{on}$ ): 3.4 kΩ

Sampling Capacitor ( $C_h$ ): 1.6 pF

Parasitic Capacitance ( $C_p$ ): 5 pF

Source Resistance ( $R_s$ ): 50 Ω

图 9-20. ADC 输入阻抗模型

#### 9.9.1.1.3.5 ADC 顺序模式时序和同步模式时序

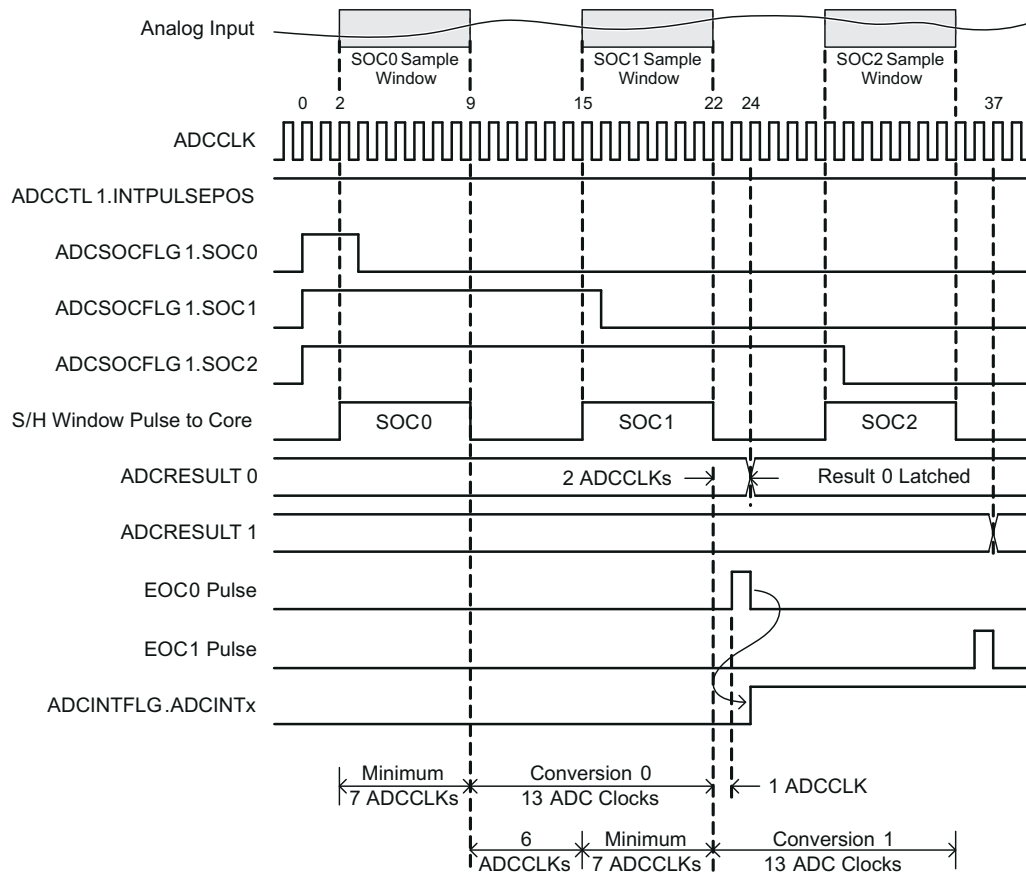


图 9-21. 顺序模式/后期中断脉冲的时序示例

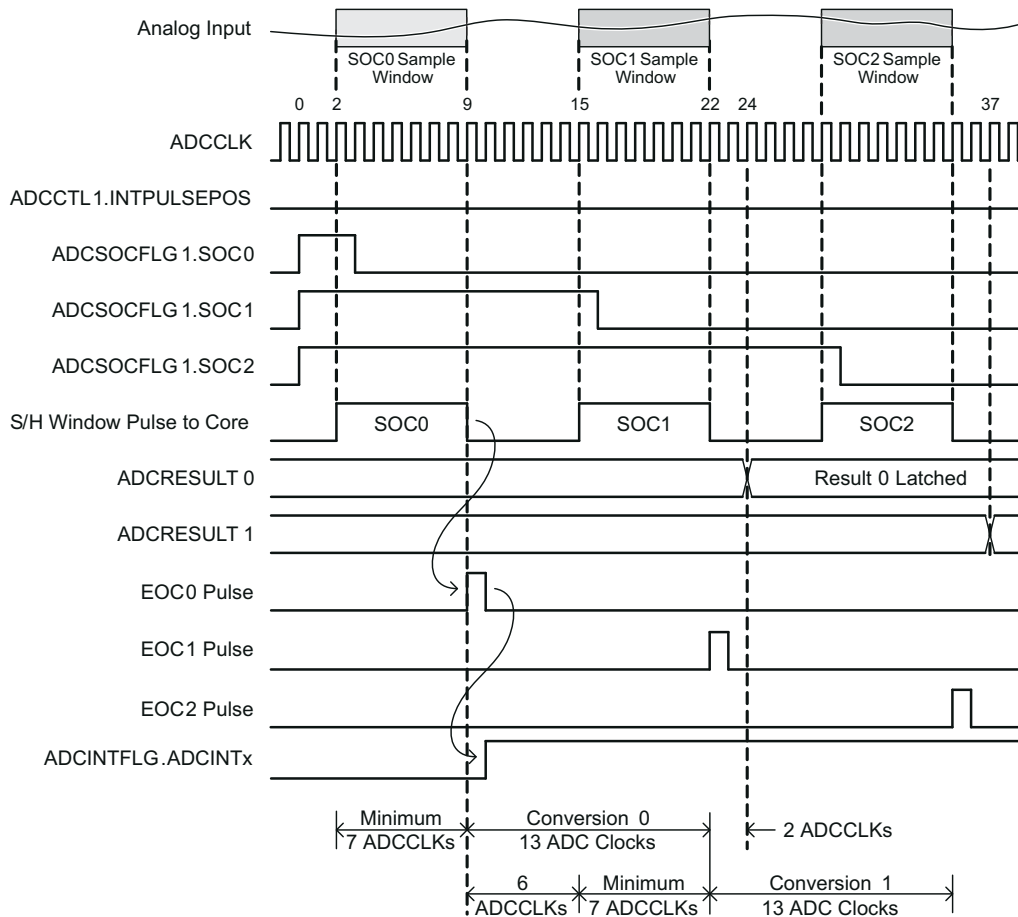


图 9-22. 顺序模式/提前中断脉冲的时序示例

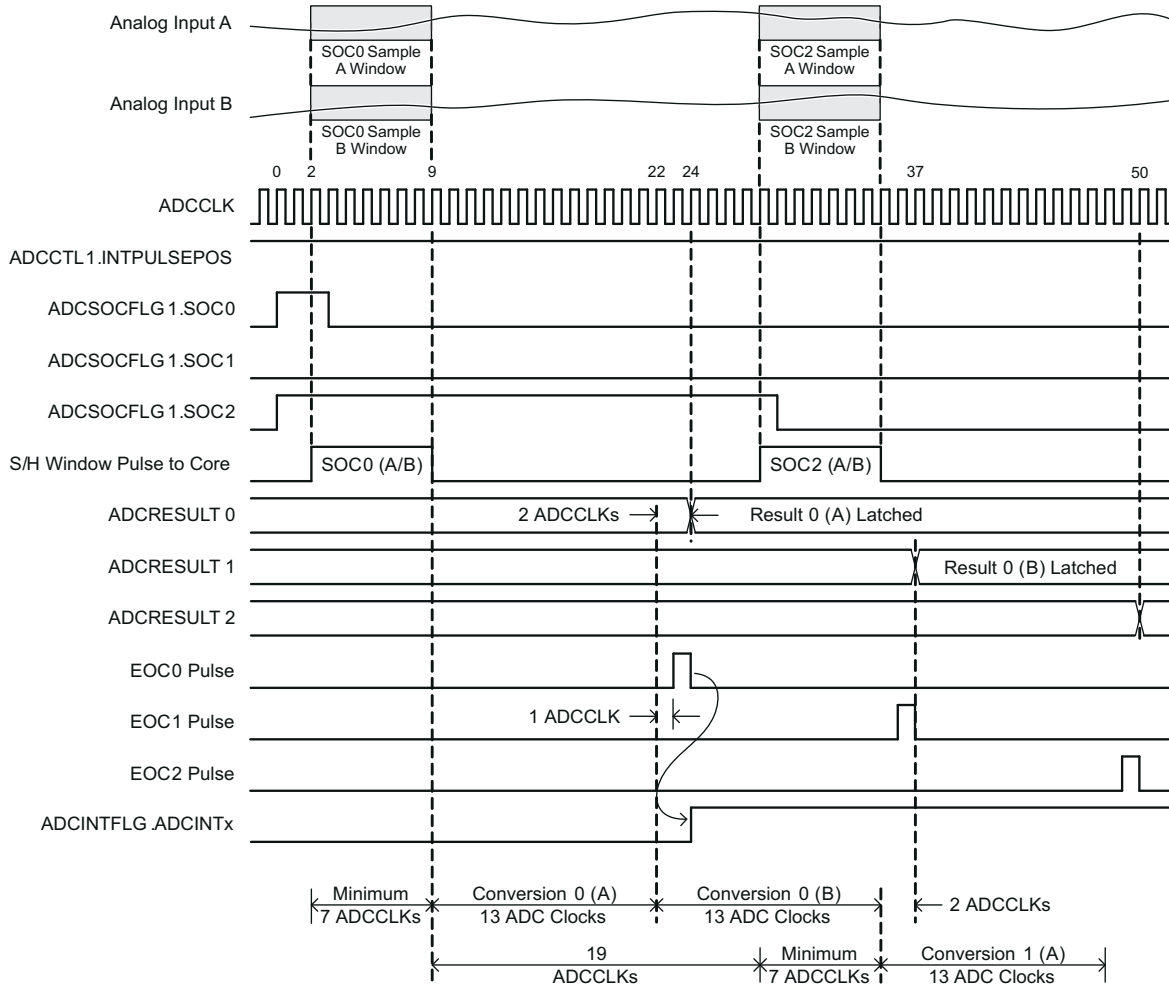


图 9-23. 同步模式/后期中断脉冲的时序示例

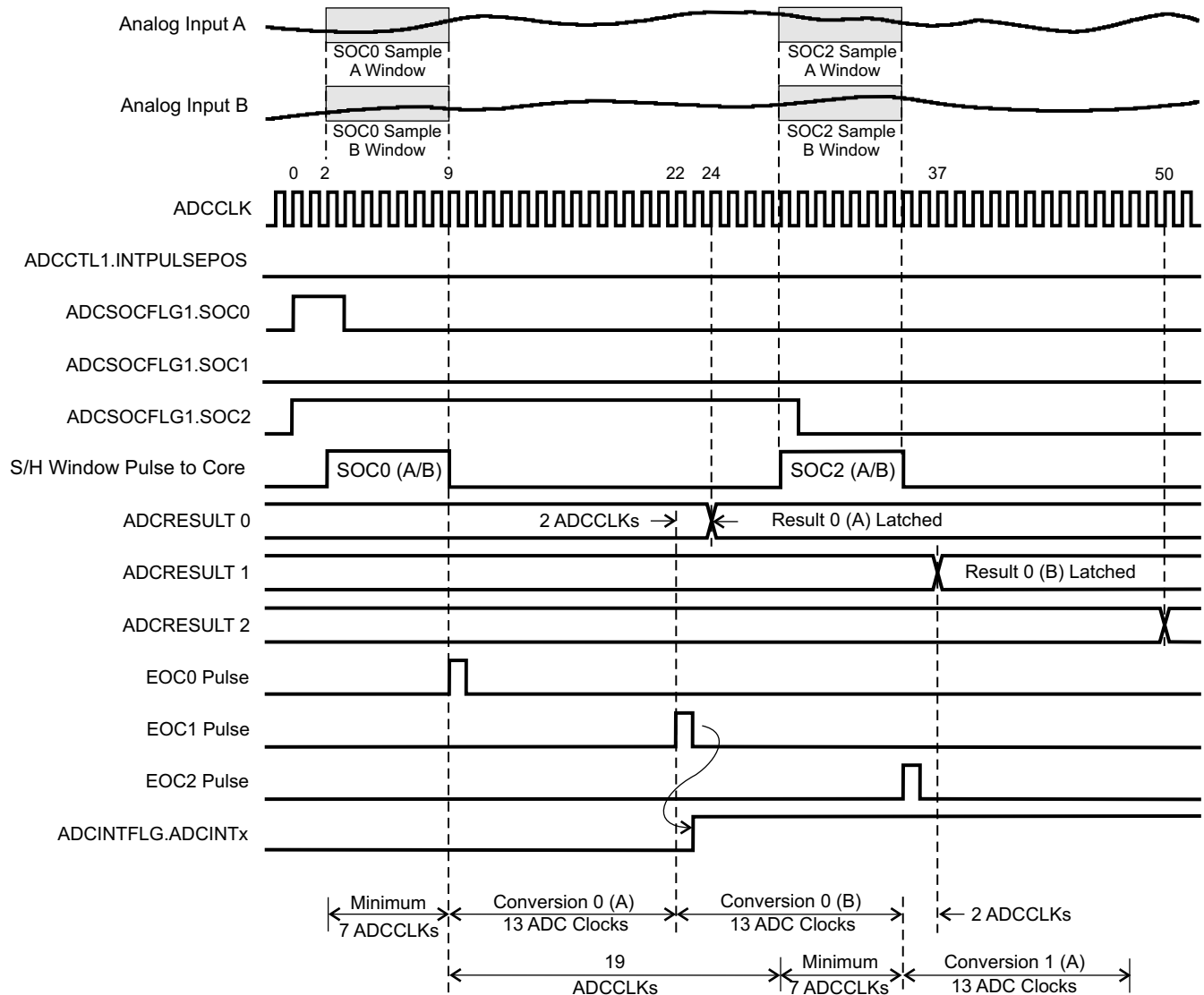


图 9-24. 同步模式/提前中断脉冲的时序示例





### 9.9.1.3 比较器块

图 9-26 显示了比较器，模块与系统其余部分的相互作用。

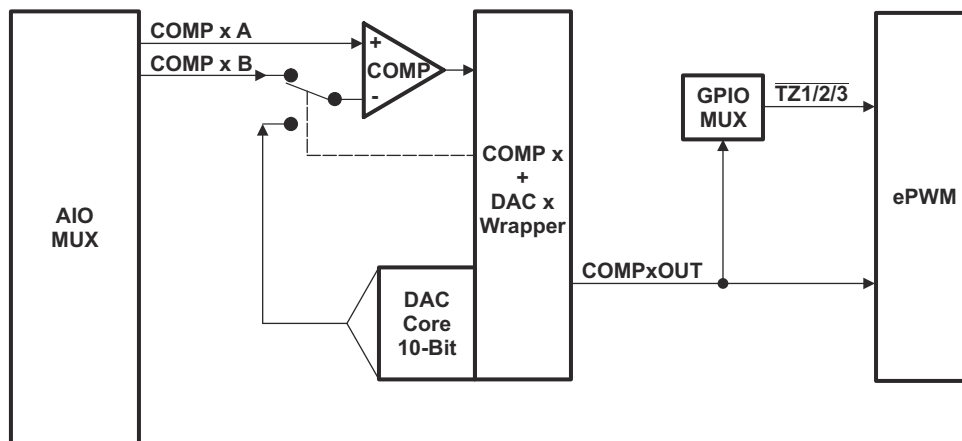


图 9-26. 比较器块图

表 9-23. 比较器控制寄存器

| 寄存器名称             | COMP1<br>地址 | COMP2<br>地址 <sup>(1)</sup> | 大小 (x<br>16) | 受 EALLOW 保<br>护 | 说明                 |
|-------------------|-------------|----------------------------|--------------|-----------------|--------------------|
| COMPCTL           | 0x6400      | 0x6420                     | 1            | 是               | 比较器控制寄存器           |
| COMPSTS           | 0x6402      | 0x6422                     | 1            | 否               | 比较器状态寄存器           |
| DACCTL            | 0x6404      | 0x6424                     | 1            | 是               | DAC 控制寄存器          |
| DACVAL            | 0x6406      | 0x6426                     | 1            | 否               | DAC 值寄存器           |
| RAMPMAXREF_ACTIVE | 0x6408      | 0x6428                     | 1            | 否               | 斜坡发生器最大基准 (有效) 寄存器 |
| RAMPMAXREF_SHDW   | 0x640A      | 0x642A                     | 1            | 否               | 斜坡发生器最大基准 (阴影) 寄存器 |
| RAMPDECVAL_ACTIVE | 0x640C      | 0x642C                     | 1            | 否               | 斜坡发生器减量值 (有效) 寄存器  |
| RAMPDECVAL_SHDW   | 0x640E      | 0x642E                     | 1            | 否               | 斜坡发生器减量值 (阴影) 寄存器  |
| RAMPSTS           | 0x6410      | 0x6430                     | 1            | 否               | 斜坡发生器状态寄存器         |

(1) 比较器 2 只在 48 引脚 PT 封装内可用。

### 9.9.1.3.1 片载比较器 / DAC 电子数据/定时

#### 9.9.1.3.1.1 Electrical Characteristics of the Comparator/DAC

| PARAMETER                                         | MIN                                 | TYP | MAX | UNITS |
|---------------------------------------------------|-------------------------------------|-----|-----|-------|
| Comparator                                        |                                     |     |     |       |
| Comparator Input Range                            | V <sub>SSA</sub> - V <sub>DDA</sub> |     |     | V     |
| Comparator response time to PWM Trip Zone (Async) | 30                                  |     |     | ns    |
| Input Offset                                      | ±5                                  |     |     | mV    |
| Input Hysteresis <sup>(1)</sup>                   | 35                                  |     |     | mV    |
| DAC                                               |                                     |     |     |       |
| DAC Output Range                                  | V <sub>SSA</sub> - V <sub>DDA</sub> |     |     | V     |
| DAC resolution                                    | 10                                  |     |     | bits  |
| DAC settling time                                 | See 图 9-27                          |     |     |       |
| DAC Gain                                          | - 1.5%                              |     |     |       |
| DAC Offset                                        | 10                                  |     |     | mV    |
| Monotonic                                         | Yes                                 |     |     |       |
| INL                                               | ±3                                  |     |     | LSB   |

- (1) Hysteresis on the comparator inputs is achieved with a Schmidt trigger configuration. This results in an effective 100-k $\Omega$  feedback resistance between the output of the comparator and the noninverting input of the comparator. There is an option to disable the hysteresis and, with it, the feedback resistance; see the Analog-to-Digital Converter and Comparator chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#) for more information on this option if needed in your system.

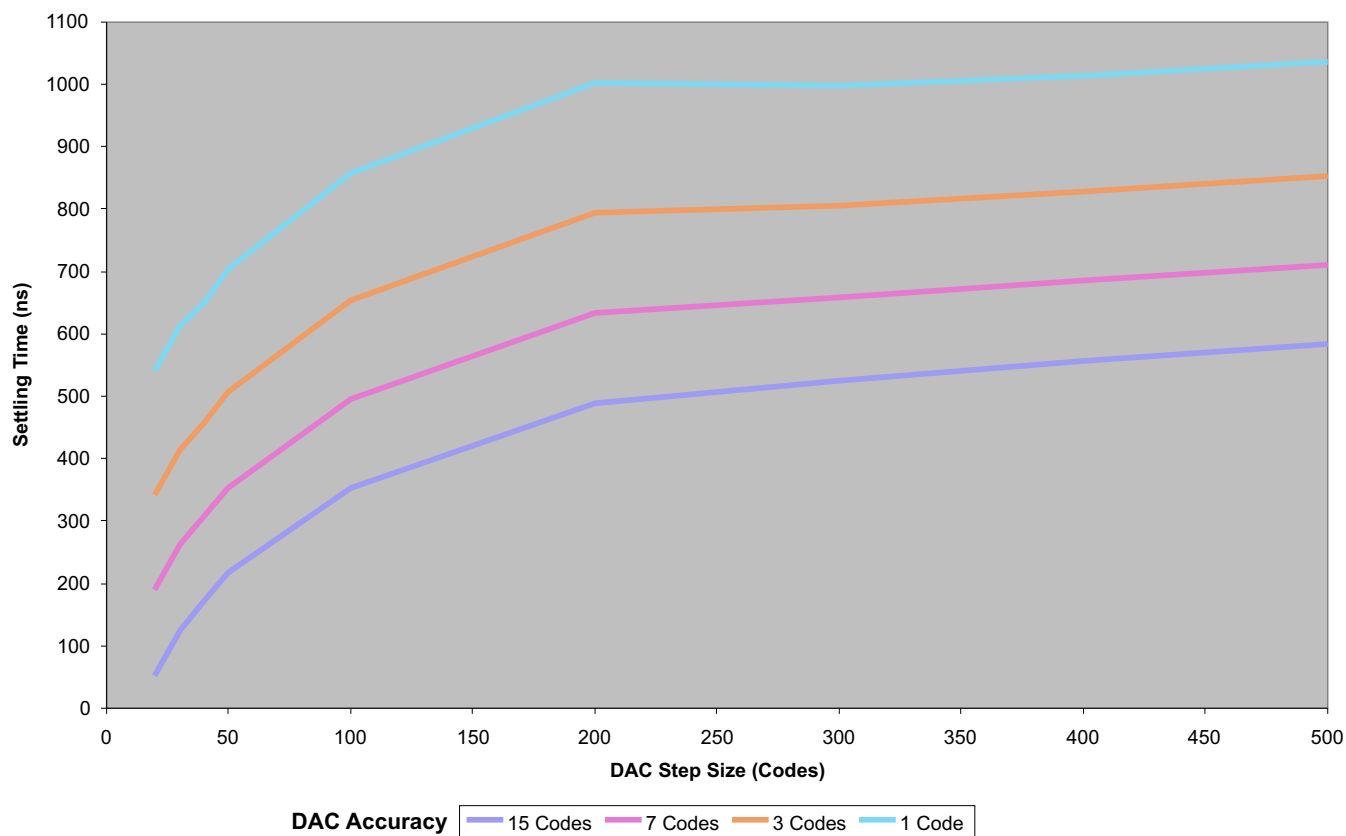


图 9-27. DAC Settling Time

## 9.9.2 详细说明

### 积分非线性

积分非线性是指各个代码与从零到满量程绘制的直线的偏差。在首次代码转换前，作为零点的点出现一半 LSB。满刻度点被定义为超过最后一次代码转换的级别一半 LSB。这个偏离为每一个特定代码的中心到这两个点之间的精确直线的距离。

### 微分非线性

一个理想 ADC 显示分开距离恰好为 1 个 LSB 的代码转换。DNL 是从这个理想值的偏离。一个少于  $\pm 1$  LSB 的微分非线性误差可确保无丢码。

### 零偏移

当模拟输入为零伏时，应当发生主进位转换。零误差被定义为实际转换到那个点的偏离。

### 增益误差

第一个代码转换应该出现在高于负满刻度的一个模拟值一半 LSB 上。最后一次转换应该出现在低于标称满刻度的一个模拟值一倍半 LSB 上。增益误差是首次和末次代码转换间的实际差异以及它们之间的理想差异。

### 信噪比 + 失真 (SINAD)

SINAD 是测得的输入信号的均方根值与所有其它低于那奎斯特频率的频谱分量 (包括谐波但不包括 dc) 的均方根总和的比。SINAD 的值用分贝表示。

### 有效位数 (ENOB)

对于一个正弦波，SINAD 可用位的数量表示。使用下面的公式，
$$N = \frac{(\text{SINAD} - 1.76)}{6.02}$$
有可能获得一个用 N (位的有效数) 表达的性能测量值。因此，对于在给定输入频率上用于正弦波输入的器件的有效位数量可从这个测得的 SINAD 直接计算。

### 总谐波失真 (THD)

THD 是头九个谐波分量的均方根总和与测得的输入信号的均方根值的比并表达为一个百分比或者分贝值。

### 无伪波动态范围 (SFDR)

SFDR 是输入信号均方根振幅与峰值寄生信号间以分贝为单位的差异。

### 9.9.3 Serial Peripheral Interface (SPI) Module

The device includes the four-pin serial peripheral interface (SPI) module. One SPI module (SPI-A) is available. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$ : SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

#### 备注

All four pins can be used as GPIO if the SPI module is not used.

- Two operational modes: master and slave

Baud rate: 125 different programmable rates.

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \quad \text{when SPIBRR} = 3 \text{ to } 127$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{4} \quad \text{when SPIBRR} = 0, 1, 2$$

- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: In control register frame beginning at address 7040h.

#### 备注

All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7 – 0), and the upper byte (15 – 8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 4-level transmit/receive FIFO
- Delayed transmit control
- Bidirectional 3 wire SPI mode support

The SPI port operation is configured and controlled by the registers listed in 表 9-24 .

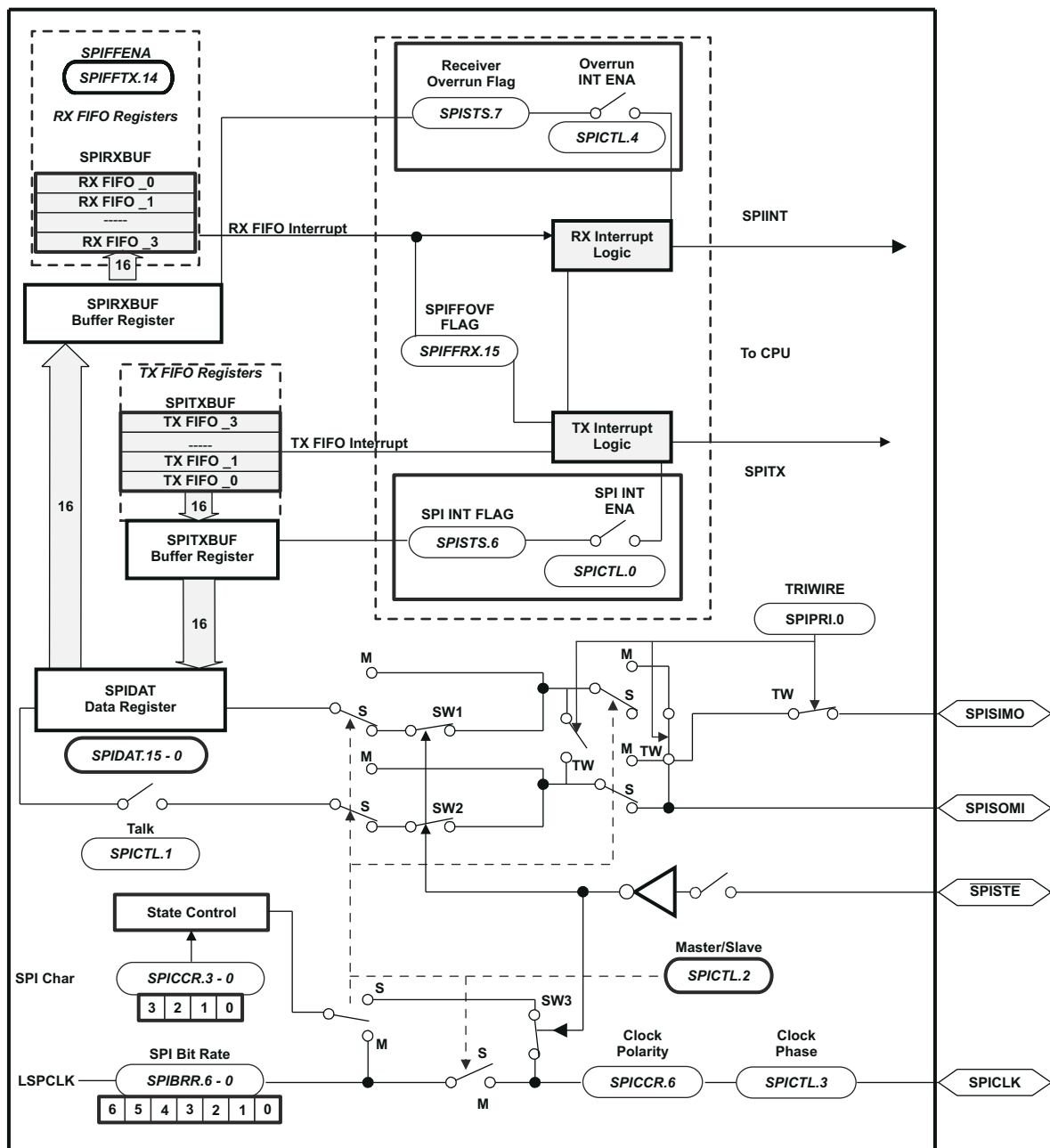
**表 9-24. SPI-A Registers**

| NAME     | ADDRESS | SIZE (x16) | ALLOW PROTECTED | DESCRIPTION <sup>(1)</sup>              |
|----------|---------|------------|-----------------|-----------------------------------------|
| SPICCR   | 0x7040  | 1          | No              | SPI-A Configuration Control Register    |
| SPICTL   | 0x7041  | 1          | No              | SPI-A Operation Control Register        |
| SPISTS   | 0x7042  | 1          | No              | SPI-A Status Register                   |
| SPIBRR   | 0x7044  | 1          | No              | SPI-A Baud Rate Register                |
| SPIRXEMU | 0x7046  | 1          | No              | SPI-A Receive Emulation Buffer Register |
| SPIRXBUF | 0x7047  | 1          | No              | SPI-A Serial Input Buffer Register      |
| SPITXBUF | 0x7048  | 1          | No              | SPI-A Serial Output Buffer Register     |
| SPIDAT   | 0x7049  | 1          | No              | SPI-A Serial Data Register              |
| SPIFFTX  | 0x704A  | 1          | No              | SPI-A FIFO Transmit Register            |
| SPIFFRX  | 0x704B  | 1          | No              | SPI-A FIFO Receive Register             |
| SPIFFCT  | 0x704C  | 1          | No              | SPI-A FIFO Control Register             |
| SPIPRI   | 0x704F  | 1          | No              | SPI-A Priority Control Register         |

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

For more information on the SPI, see the Serial Peripheral Interface (SPI) chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).

图 9-28 is a block diagram of the SPI in slave mode.



A. SPISTE is driven low by the master for a slave device.

图 9-28. SPI Module Block Diagram (Slave Mode)

### 9.9.3.1 SPI 主模式电气数据/时序

节 9.9.3.1.1 列出了主模式时序 ( 时钟相位 = 0 ) , 节 9.9.3.1.2 列出了主模式时序 ( 时钟相位 = 1 ) 。图 9-29 和图 9-30 显示了时序波形。

#### 9.9.3.1.1 SPI Master Mode External Timing (Clock Phase = 0)

| NO. <sup>(1)</sup><br>(2) (3) (4)<br>(5) | PARAMETER                                             | BRR EVEN                                 |                       | BRR ODD                                  |                                          | UNIT |
|------------------------------------------|-------------------------------------------------------|------------------------------------------|-----------------------|------------------------------------------|------------------------------------------|------|
|                                          |                                                       | MIN                                      | MAX                   | MIN                                      | MAX                                      |      |
| 1                                        | $t_{c(SPC)M}$ Cycle time, SPICLK                      | $4t_{c(LSPCLK)}$                         | $128t_{c(LSPCLK)}$    | $5t_{c(LSPCLK)}$                         | $127t_{c(LSPCLK)}$                       | ns   |
| 2                                        | $t_{w(SPC1)M}$ Pulse duration, SPICLK first pulse     | $0.5t_{c(SPC)M} - 10$                    | $0.5t_{c(SPC)M} + 10$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 10$ | ns   |
| 3                                        | $t_{w(SPC2)M}$ Pulse duration, SPICLK second pulse    | $0.5t_{c(SPC)M} - 10$                    | $0.5t_{c(SPC)M} + 10$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 10$ | ns   |
| 4                                        | $t_{d(SIMO)M}$ Delay time, SPICLK to SPISIMO valid    |                                          | 10                    |                                          | 10                                       | ns   |
| 5                                        | $t_{v(SIMO)M}$ Valid time, SPISIMO valid after SPICLK | $0.5t_{c(SPC)M} - 10$                    |                       | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$ |                                          | ns   |
| 8                                        | $t_{su(SOMI)M}$ Setup time, SPISOMI before SPICLK     | 26                                       |                       | 26                                       |                                          | ns   |
| 9                                        | $t_{h(SOMI)M}$ Hold time, SPISOMI valid after SPICLK  | 0                                        |                       | 0                                        |                                          | ns   |
| 23                                       | $t_{d(SPC)M}$ Delay time, SPISTE active to SPICLK     | $1.5t_{c(SPC)M} - 3t_{c(SYSCLOCK)} - 10$ |                       | $1.5t_{c(SPC)M} - 3t_{c(SYSCLOCK)} - 10$ |                                          | ns   |
| 24                                       | $t_{d(STE)M}$ Delay time, SPICLK to SPISTE inactive   | $0.5t_{c(SPC)M} - 10$                    |                       | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$ |                                          | ns   |

- (1) The MASTER / SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
- (2)  $t_{c(SPC)}$  = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
- (3)  $t_{c(LCO)}$  = LSPCLK cycle time
- (4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:  
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX  
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
- (5) The active edge of the SPICLK signal referenced is controlled by the clock polarity bit (SPICCR.6).

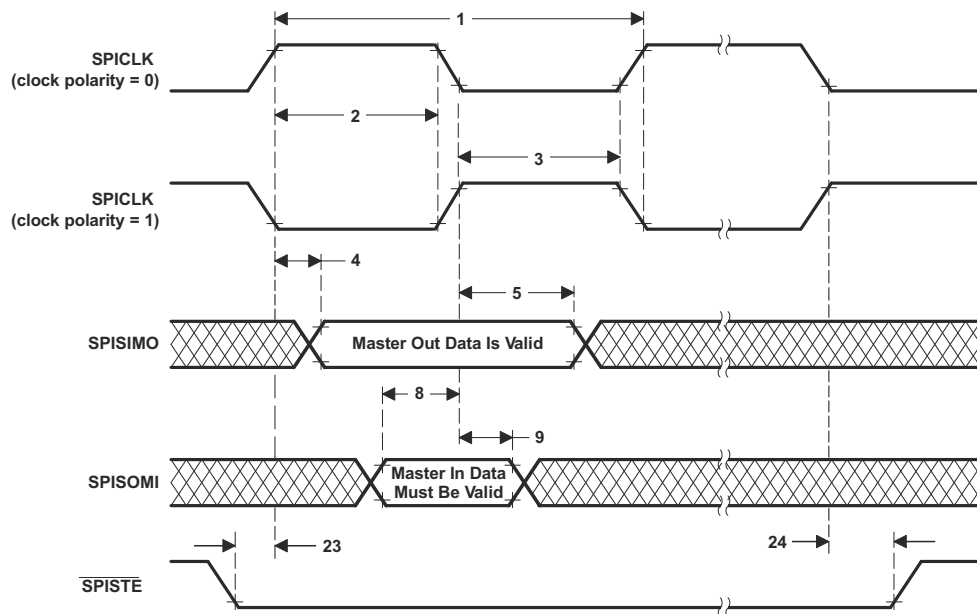


图 9-29. SPI Master Mode External Timing (Clock Phase = 0)



### 9.9.3.1.2 SPI Master Mode External Timing (Clock Phase = 1)

| NO. <sup>(1)</sup><br>(2) (3) (4)<br>(5) | PARAMETER                                                        | BRR EVEN                             |                       | BRR ODD                                  |                                          | UNIT |
|------------------------------------------|------------------------------------------------------------------|--------------------------------------|-----------------------|------------------------------------------|------------------------------------------|------|
|                                          |                                                                  | MIN                                  | MAX                   | MIN                                      | MAX                                      |      |
| 1                                        | $t_{c(SPC)M}$ Cycle time, SPICLK                                 | $4t_{c(LSPCLK)}$                     | $128t_{c(LSPCLK)}$    | $5t_{c(LSPCLK)}$                         | $127t_{c(LSPCLK)}$                       | ns   |
| 2                                        | $t_{w(SPC1)M}$ Pulse duration, SPICLK first pulse                | $0.5t_{c(SPC)M} - 10$                | $0.5t_{c(SPC)M} + 10$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 10$ | ns   |
| 3                                        | $t_{w(SPC2)M}$ Pulse duration, SPICLK second pulse               | $0.5t_{c(SPC)M} - 10$                | $0.5t_{c(SPC)M} + 10$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 10$ | ns   |
| 6                                        | $t_{d(SIMO)M}$ Delay time, SPISIMO valid to SPICLK               | $0.5t_{c(SPC)M} - 10$                |                       | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$ |                                          | ns   |
| 7                                        | $t_{v(SIMO)M}$ Valid time, SPISIMO valid after SPICLK            | $0.5t_{c(SPC)M} - 10$                |                       | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$ |                                          | ns   |
| 10                                       | $t_{su(SOMI)M}$ Setup time, SPISOMI before SPICLK                | 26                                   |                       | 26                                       |                                          | ns   |
| 11                                       | $t_{h(SOMI)M}$ Hold time, SPISOMI valid after SPICLK             | 0                                    |                       | 0                                        |                                          | ns   |
| 23                                       | $t_{d(SPC)M}$ Delay time, $\overline{SPISTE}$ active to SPICLK   | $2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 10$ |                       | $2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 10$     |                                          | ns   |
| 24                                       | $t_{d(STE)M}$ Delay time, SPICLK to $\overline{SPISTE}$ inactive | $0.5t_{c(SPC)} - 10$                 |                       | $0.5t_{c(SPC)} - 0.5t_{c(LSPCLK)} - 10$  |                                          | ns   |

- (1) The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.  
(2)  $t_{c(SPC)} = \text{SPI clock cycle time} = \text{LSPCLK}/4$  or  $\text{LSPCLK}/(\text{SPIBRR} + 1)$   
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:  
Master mode transmit 25 MHz MAX, master mode receive 12.5 MHz MAX  
Slave mode transmit 12.5 MHz MAX, slave mode receive 12.5 MHz MAX.  
(4)  $t_{c(LCO)} = \text{LSPCLK cycle time}$   
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

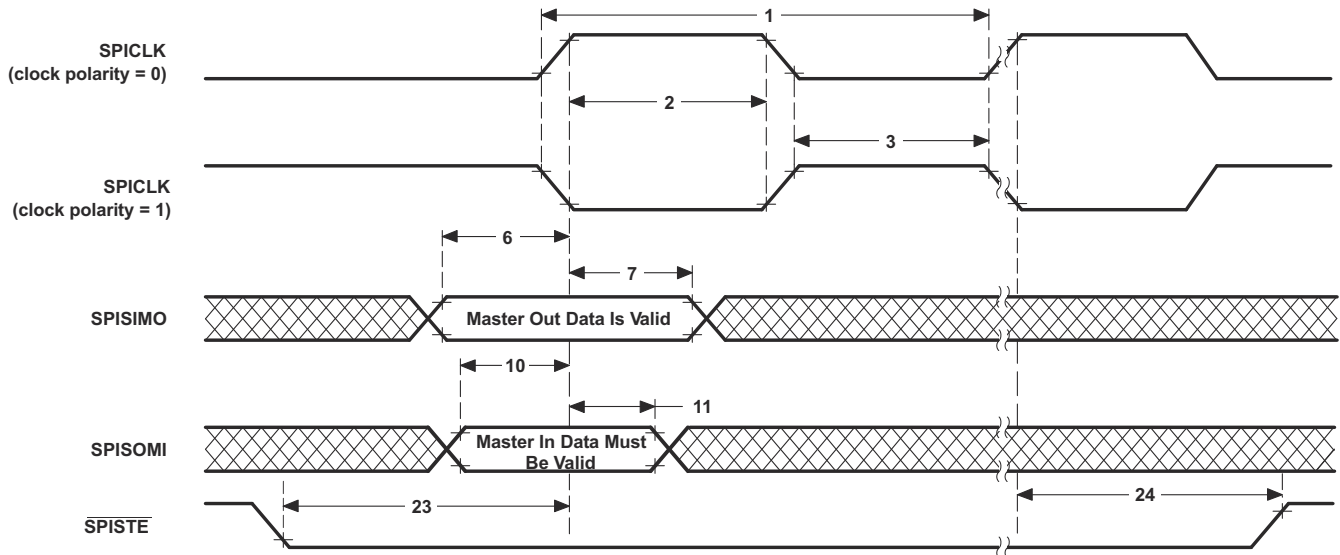


图 9-30. SPI Master Mode External Timing (Clock Phase = 1)

### 9.9.3.2 SPI 从模式电气数据/时序

节 9.9.3.2.1 列出了从模式时序 ( 时钟相位 = 0 ) , 节 9.9.3.2.2 列出了从模式时序 ( 时钟相位 = 1 ) 。图 9-31 和图 9-32 显示了时序波形。

#### 9.9.3.2.1 SPI Slave Mode External Timing (Clock Phase = 0)

### 9.9.3.2.2 SPI Slave Mode External Timing (Clock Phase = 1)

| NO.<br>(1) (2)<br>(3) (4) | PARAMETER                                                           | MIN                  | MAX | UNIT |
|---------------------------|---------------------------------------------------------------------|----------------------|-----|------|
| 12                        | $t_{c(SPC)}S$ Cycle time, SPICLK                                    | $4t_{c(SYSCLK)}$     |     | ns   |
| 13                        | $t_{w(SPC1)}S$ Pulse duration, SPICLK first pulse                   | $2t_{c(SYSCLK)} - 1$ |     | ns   |
| 14                        | $t_{w(SPC2)}S$ Pulse duration, SPICLK second pulse                  | $2t_{c(SYSCLK)} - 1$ |     | ns   |
| 17                        | $t_{d(SOMI)}S$ Delay time, SPICLK to SPISOMI valid                  |                      | 21  | ns   |
| 18                        | $t_{v(SOMI)}S$ Valid time, SPISOMI data valid after SPICLK          | 0                    |     | ns   |
| 21                        | $t_{su(SIMO)}S$ Setup time, SPISIMO valid before SPICLK             | $1.5t_{c(SYSCLK)}$   |     | ns   |
| 22                        | $t_{h(SIMO)}S$ Hold time, SPISIMO data valid after SPICLK           | $1.5t_{c(SYSCLK)}$   |     | ns   |
| 25                        | $t_{su(STE)}S$ Setup time, $\overline{SPISTE}$ active before SPICLK | $1.5t_{c(SYSCLK)}$   |     | ns   |
| 26                        | $t_{h(STE)}S$ Hold time, $\overline{SPISTE}$ inactive after SPICLK  | $1.5t_{c(SYSCLK)}$   |     | ns   |

- (1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
- (2)  $t_{c(SPC)}$  = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
- (3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:  
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX  
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
- (4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

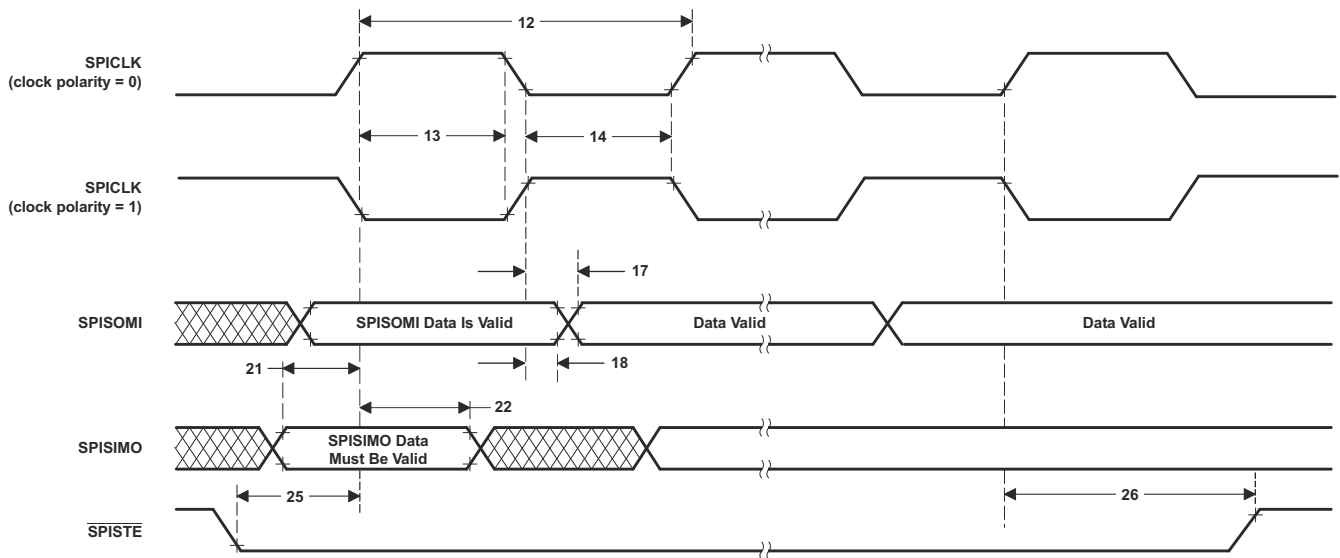


图 9-32. SPI Slave Mode External Timing (Clock Phase = 1)

## 9.9.4 Serial Communications Interface (SCI) Module

The devices include one serial communications interface (SCI) module (SCI-A). The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard nonreturn-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

---

### 备注

Both pins can be used as GPIO if not used for SCI.

---

- Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8} \quad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \quad \text{when BRR} = 0$$

- Data-word format
  - One start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - One or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (nonreturn-to-zero) format

---

### 备注

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7 – 0), and the upper byte (15 – 8) is read as zeros. Writing to the upper byte has no effect.

---

Enhanced features:

- Auto baud-detect hardware logic
- 4-level transmit/receive FIFO

The SCI port operation is configured and controlled by the registers listed in 表 9-25.

**表 9-25. SCI-A Registers**

| NAME <sup>(1)</sup>     | ADDRESS | SIZE (x16) | ALLOW<br>PROTECTED | DESCRIPTION                                  |
|-------------------------|---------|------------|--------------------|----------------------------------------------|
| SCICCR                  | 0x7050  | 1          | No                 | SCI-A Communications Control Register        |
| SCICTL1A                | 0x7051  | 1          | No                 | SCI-A Control Register 1                     |
| SCIHBAUDA               | 0x7052  | 1          | No                 | SCI-A Baud Register, High Bits               |
| SCILBAUDA               | 0x7053  | 1          | No                 | SCI-A Baud Register, Low Bits                |
| SCICTL2A                | 0x7054  | 1          | No                 | SCI-A Control Register 2                     |
| SCIRXSTA                | 0x7055  | 1          | No                 | SCI-A Receive Status Register                |
| SCIRXEMUA               | 0x7056  | 1          | No                 | SCI-A Receive Emulation Data Buffer Register |
| SCIRXBUFA               | 0x7057  | 1          | No                 | SCI-A Receive Data Buffer Register           |
| SCITXBUFA               | 0x7059  | 1          | No                 | SCI-A Transmit Data Buffer Register          |
| SCIFFTXA <sup>(2)</sup> | 0x705A  | 1          | No                 | SCI-A FIFO Transmit Register                 |
| SCIFFRXA <sup>(2)</sup> | 0x705B  | 1          | No                 | SCI-A FIFO Receive Register                  |
| SCIFFCTA <sup>(2)</sup> | 0x705C  | 1          | No                 | SCI-A FIFO Control Register                  |
| SCIPRIA                 | 0x705F  | 1          | No                 | SCI-A Priority Control Register              |

- (1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
- (2) These registers are new registers for the FIFO mode.

For more information on the SCI, see the Serial Communications Interface (SCI) chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).

图 9-33 shows the SCI module block diagram.

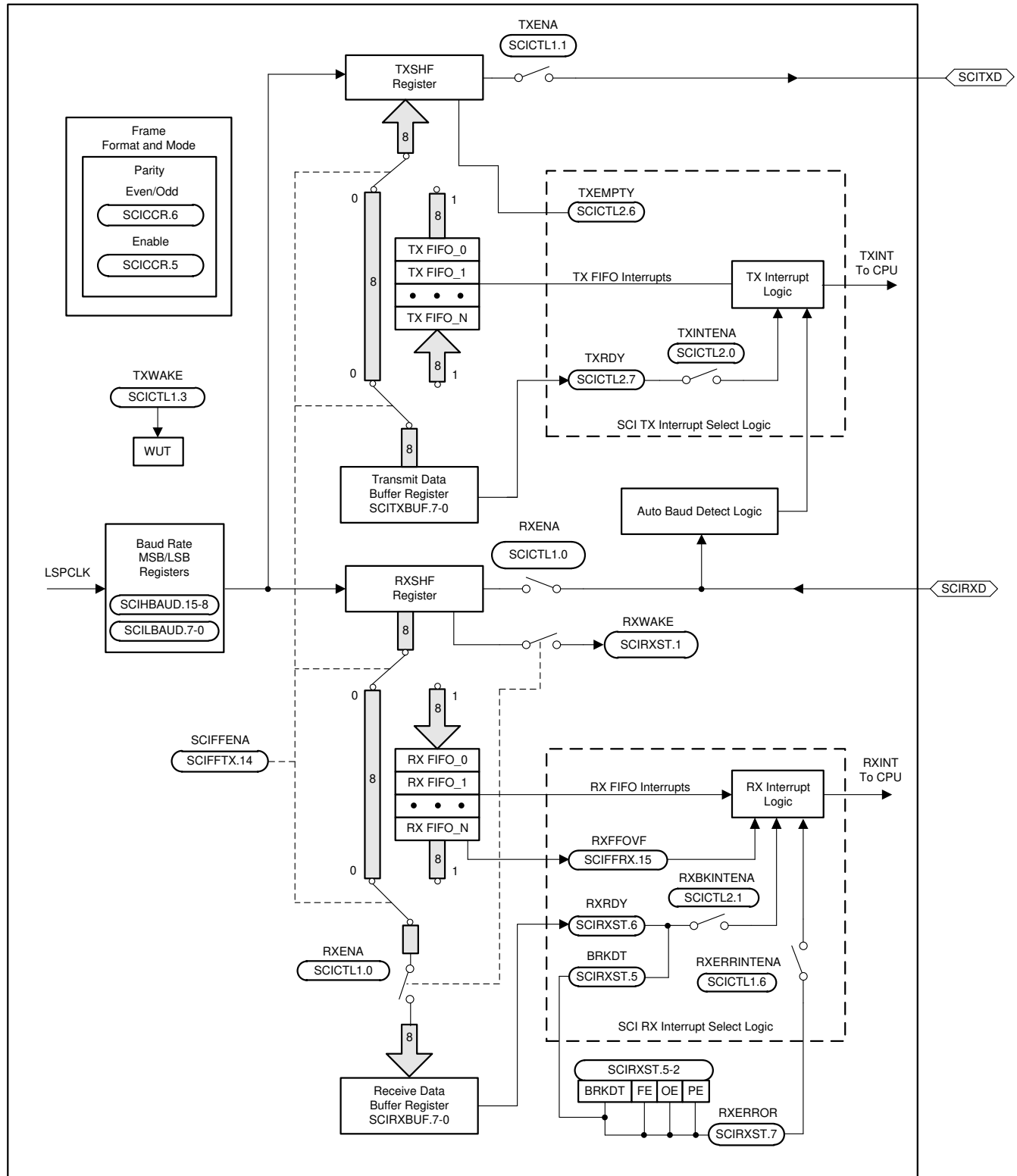


图 9-33. Serial Communications Interface (SCI) Module Block Diagram

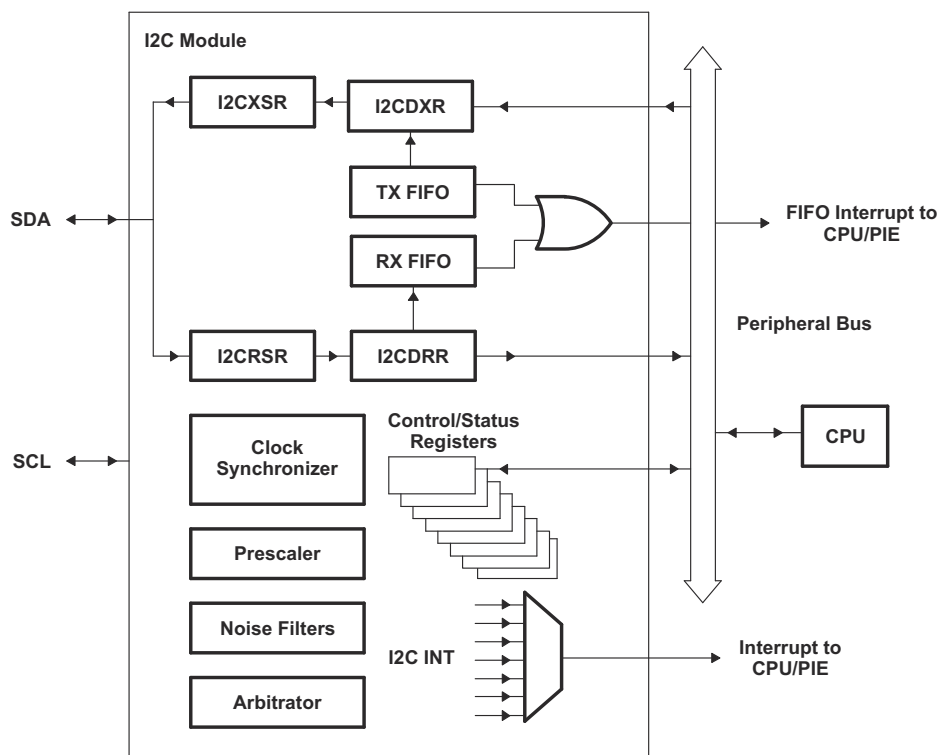
### 9.9.5 Inter-Integrated Circuit (I2C)

The device contains one I2C Serial Port. 图 9-34 shows how the I2C peripheral module interfaces within the device.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I<sup>2</sup>C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (I2C Fast-mode rate)
- One 4-word receive FIFO and one 4-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

For more information on the I2C, see the Inter-Integrated Circuit Module (I2C) chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).



- The I2C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I2C port are also at the SYSCLKOUT rate.
- The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I2C port for low-power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

图 9-34. I2C Peripheral Module Interfaces

The registers in 表 9-26 configure and control the I2C port operation.

表 9-26. I2C-A Registers

| NAME    | ADDRESS | EALLOW<br>PROTECTED | DESCRIPTION                                             |
|---------|---------|---------------------|---------------------------------------------------------|
| I2COAR  | 0x7900  | No                  | I2C own address register                                |
| I2CIER  | 0x7901  | No                  | I2C interrupt enable register                           |
| I2CSTR  | 0x7902  | No                  | I2C status register                                     |
| I2CCLKL | 0x7903  | No                  | I2C clock low-time divider register                     |
| I2CCLKH | 0x7904  | No                  | I2C clock high-time divider register                    |
| I2CCNT  | 0x7905  | No                  | I2C data count register                                 |
| I2CDRR  | 0x7906  | No                  | I2C data receive register                               |
| I2CSAR  | 0x7907  | No                  | I2C slave address register                              |
| I2CDXR  | 0x7908  | No                  | I2C data transmit register                              |
| I2CMODR | 0x7909  | No                  | I2C mode register                                       |
| I2CISRC | 0x790A  | No                  | I2C interrupt source register                           |
| I2CPSC  | 0x790C  | No                  | I2C prescaler register                                  |
| I2CFFTX | 0x7920  | No                  | I2C FIFO transmit register                              |
| I2CFFRX | 0x7921  | No                  | I2C FIFO receive register                               |
| I2CRSR  | -       | No                  | I2C receive shift register (not accessible to the CPU)  |
| I2CXSR  | -       | No                  | I2C transmit shift register (not accessible to the CPU) |



### 9.9.5.1 I2C 电气数据/时序

节 9.9.5.1.1 显示了 I2C 时序要求。节 9.9.5.1.2 显示了 I2C 开关特性。

#### 9.9.5.1.1 I2C 时序要求

|                        |                               |      | 最小值  | 最大值 | 单位      |
|------------------------|-------------------------------|------|------|-----|---------|
| $t_{h(SDA-SCL)START}$  | 保持时间, 启动条件, SDA 下降后 SCL 下降延迟  |      | 0.6  |     | $\mu s$ |
| $t_{su(SCL-SDA)START}$ | 设置时间, 重复启动, SDA 下降延迟之前 SCL 上升 |      | 0.6  |     | $\mu s$ |
| $t_{h(SCL-DAT)}$       | 保持时间, SCL 下降后的数据              |      | 0    |     | $\mu s$ |
| $t_{su(DAT-SCL)}$      | 设置时间, SCL 上升前的数据              |      | 100  |     | ns      |
| $t_r(SDA)$             | 上升时间, SDA                     | 输入容差 | 20   | 300 | ns      |
| $t_r(SCL)$             | 上升时间, SCL                     | 输入容差 | 20   | 300 | ns      |
| $t_f(SDA)$             | 下降时间, SDA                     | 输入容差 | 11.4 | 300 | ns      |
| $t_f(SCL)$             | 下降时间, SCL                     | 输入容差 | 11.4 | 300 | ns      |
| $t_{su(SCL-SDA)STOP}$  | 设置时间, 停止条件, SDA 上升延迟之前 SCL 上升 |      | 0.6  |     | $\mu s$ |

#### 9.9.5.1.2 I2C 开关特性

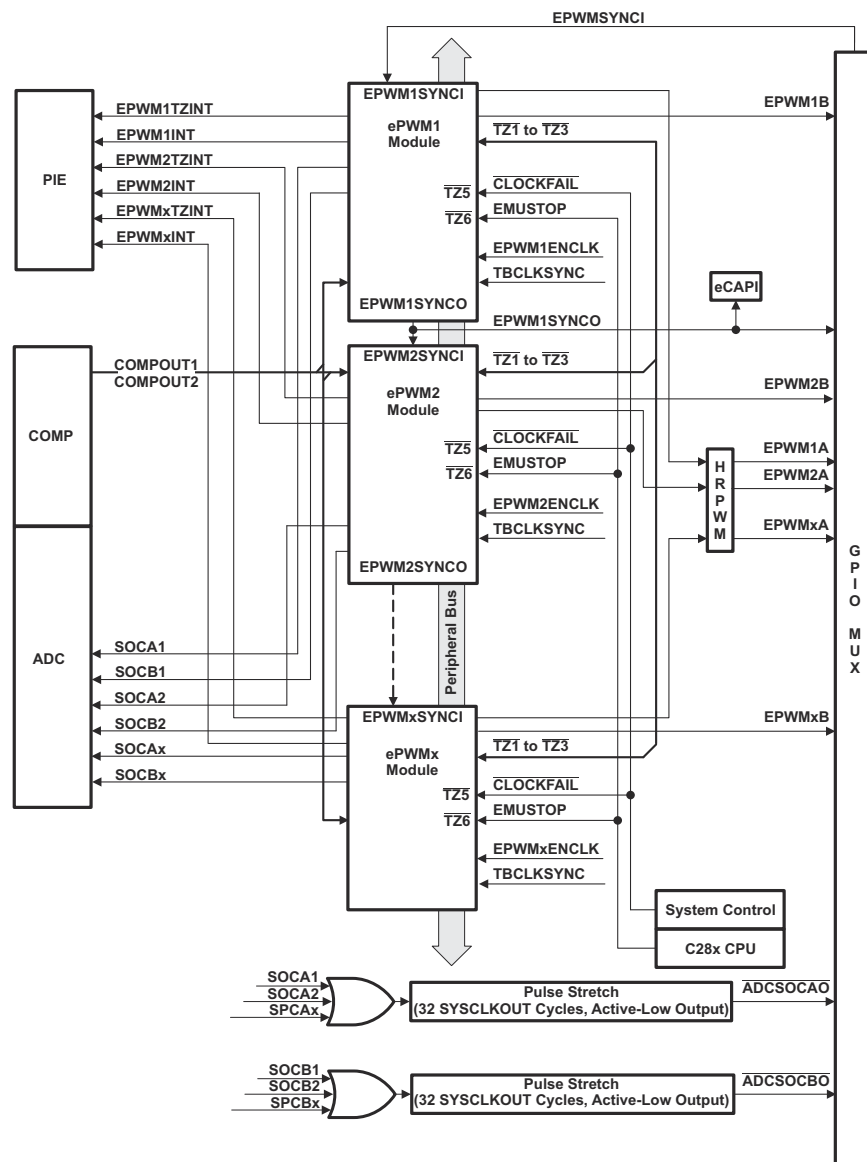
在推荐的运行条件下 ( 除非另有说明 )

| 参数                                                           | 测试条件                                                      | 最小值             | 最大值            | 单位      |
|--------------------------------------------------------------|-----------------------------------------------------------|-----------------|----------------|---------|
| $f_{SCL}$ SCL 时钟频率                                           | I2C 时钟模块频率介于 7MHz 与 12MHz 之间, 并且 I2C 预分频器和时钟分频寄存器进行了适当配置。 |                 | 400            | kHz     |
| $V_{il}$ 低电平输入电压                                             |                                                           |                 | $0.3 V_{DDIO}$ | V       |
| $V_{ih}$ 高电平输入电压                                             |                                                           | $0.7 V_{DDIO}$  |                | V       |
| $V_{hys}$ 输入滞后                                               |                                                           | $0.05 V_{DDIO}$ |                | V       |
| $V_{ol}$ 低电平输出电压                                             | 3mA 灌电流                                                   | 0               | 0.4            | V       |
| $t_{LOW}$ SCL 时钟的低周期                                         | I2C 时钟模块频率介于 7MHz 与 12MHz 之间, 并且 I2C 预分频器和时钟分频寄存器进行了适当配置。 | 1.3             |                | $\mu s$ |
| $t_{HIGH}$ SCL 时钟的高周期                                        | I2C 时钟模块频率介于 7MHz 与 12MHz 之间, 并且 I2C 预分频器和时钟分频寄存器进行了适当配置。 | 0.6             |                | $\mu s$ |
| $I_I$ 输入电压介于 $0.1 V_{DDIO}$ 与 $0.9 V_{DDIO}$ ( 最大值 ) 之间的输入电流 |                                                           | -10             | 10             | $\mu A$ |

### 9.9.6 Enhanced PWM Modules (ePWM1/2/3/4)

The devices contain up to four enhanced PWM Modules (ePWM). 图 9-35 shows a block diagram of multiple ePWM modules. 图 9-36 shows the signal interconnections with the ePWM. For more details, see the Enhanced Pulse Width Modulator (ePWM) chapter in the *TMS320F2802x, TMS320F2802xx Technical Reference Manual*.

表 9-27 shows the complete ePWM register set per module.



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图 9-35. ePWM

**表 9-27. ePWM Control and Status Registers**

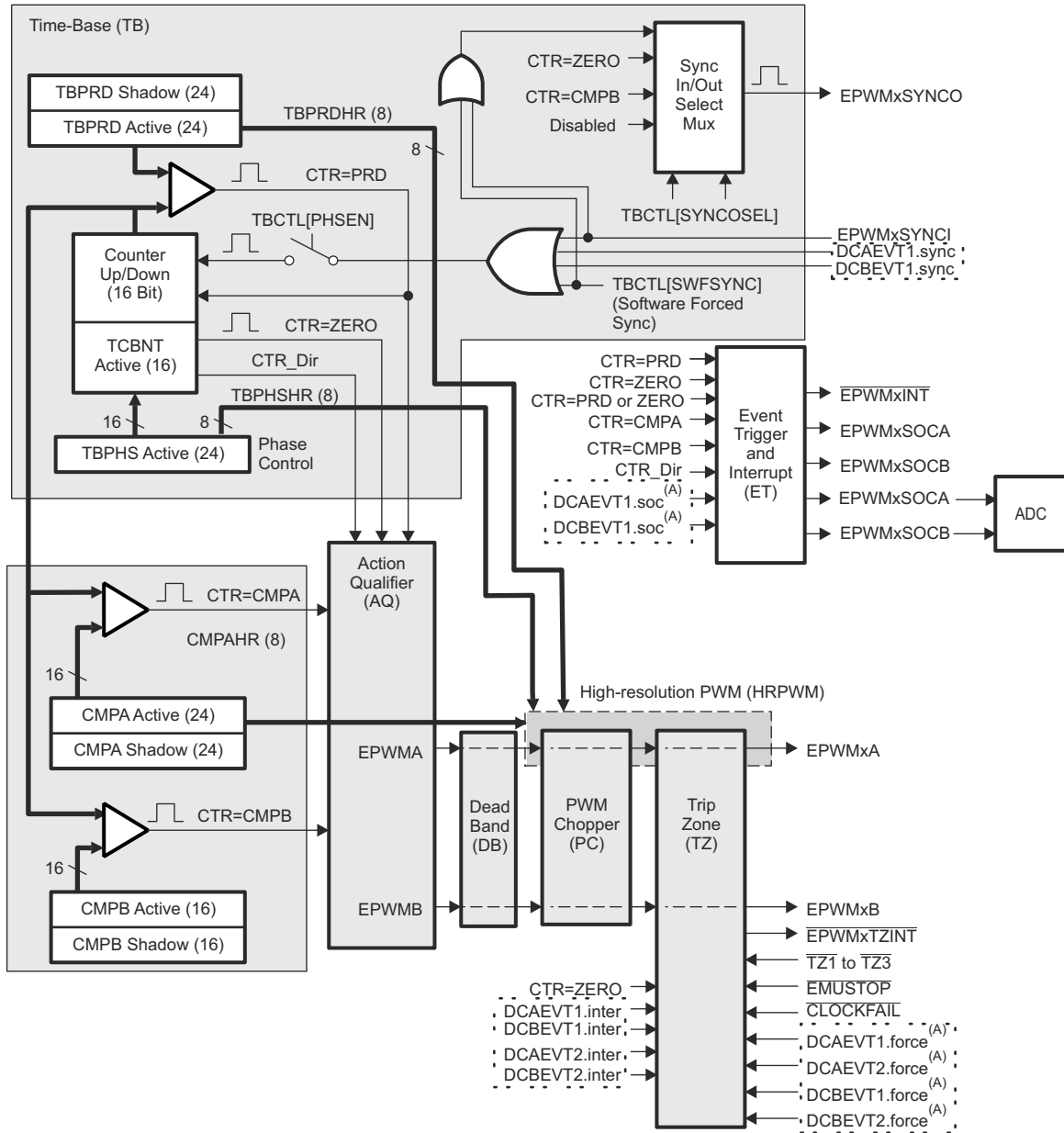
| NAME     | ePWM1  | ePWM2  | ePWM3  | ePWM4  | SIZE (x16) / #SHADOW | DESCRIPTION                                              |
|----------|--------|--------|--------|--------|----------------------|----------------------------------------------------------|
| TBCTL    | 0x6800 | 0x6840 | 0x6880 | 0x68C0 | 1 / 0                | Time Base Control Register                               |
| TBSTS    | 0x6801 | 0x6841 | 0x6881 | 0x68C1 | 1 / 0                | Time Base Status Register                                |
| TBPHSHR  | 0x6802 | 0x6842 | 0x6882 | 0x68C2 | 1 / 0                | Time Base Phase HRPWM Register                           |
| TBPHS    | 0x6803 | 0x6843 | 0x6883 | 0x68C3 | 1 / 0                | Time Base Phase Register                                 |
| TBCTR    | 0x6804 | 0x6844 | 0x6884 | 0x68C4 | 1 / 0                | Time Base Counter Register                               |
| TBPRD    | 0x6805 | 0x6845 | 0x6885 | 0x68C5 | 1 / 1                | Time Base Period Register Set                            |
| TBPRDHR  | 0x6806 | 0x6846 | 0x6886 | 0x68C6 | 1 / 1                | Time Base Period High Resolution Register <sup>(1)</sup> |
| CMPCTL   | 0x6807 | 0x6847 | 0x6887 | 0x68C7 | 1 / 0                | Counter Compare Control Register                         |
| CMPAHR   | 0x6808 | 0x6848 | 0x6888 | 0x68C8 | 1 / 1                | Time Base Compare A HRPWM Register                       |
| CMPA     | 0x6809 | 0x6849 | 0x6889 | 0x68C9 | 1 / 1                | Counter Compare A Register Set                           |
| CMPB     | 0x680A | 0x684A | 0x688A | 0x68CA | 1 / 1                | Counter Compare B Register Set                           |
| AQCTLA   | 0x680B | 0x684B | 0x688B | 0x68CB | 1 / 0                | Action Qualifier Control Register For Output A           |
| AQCTLB   | 0x680C | 0x684C | 0x688C | 0x68CC | 1 / 0                | Action Qualifier Control Register For Output B           |
| AQSFRC   | 0x680D | 0x684D | 0x688D | 0x68CD | 1 / 0                | Action Qualifier Software Force Register                 |
| AQCSFRC  | 0x680E | 0x684E | 0x688E | 0x68CE | 1 / 1                | Action Qualifier Continuous S/W Force Register Set       |
| DBCTL    | 0x680F | 0x684F | 0x688F | 0x68CF | 1 / 1                | Dead-Band Generator Control Register                     |
| DBRED    | 0x6810 | 0x6850 | 0x6890 | 0x68D0 | 1 / 0                | Dead-Band Generator Rising Edge Delay Count Register     |
| DBFED    | 0x6811 | 0x6851 | 0x6891 | 0x68D1 | 1 / 0                | Dead-Band Generator Falling Edge Delay Count Register    |
| TZSEL    | 0x6812 | 0x6852 | 0x6892 | 0x68D2 | 1 / 0                | Trip Zone Select Register <sup>(1)</sup>                 |
| TZDCSEL  | 0x6813 | 0x6853 | 0x6893 | 0x98D3 | 1 / 0                | Trip Zone Digital Compare Register                       |
| TZCTL    | 0x6814 | 0x6854 | 0x6894 | 0x68D4 | 1 / 0                | Trip Zone Control Register <sup>(1)</sup>                |
| TZEINT   | 0x6815 | 0x6855 | 0x6895 | 0x68D5 | 1 / 0                | Trip Zone Enable Interrupt Register <sup>(1)</sup>       |
| TZFLG    | 0x6816 | 0x6856 | 0x6896 | 0x68D6 | 1 / 0                | Trip Zone Flag Register <sup>(1)</sup>                   |
| TZCLR    | 0x6817 | 0x6857 | 0x6897 | 0x68D7 | 1 / 0                | Trip Zone Clear Register <sup>(1)</sup>                  |
| TZFRC    | 0x6818 | 0x6858 | 0x6898 | 0x68D8 | 1 / 0                | Trip Zone Force Register <sup>(1)</sup>                  |
| ETSEL    | 0x6819 | 0x6859 | 0x6899 | 0x68D9 | 1 / 0                | Event Trigger Selection Register                         |
| ETPS     | 0x681A | 0x685A | 0x689A | 0x68DA | 1 / 0                | Event Trigger Prescale Register                          |
| ETFLG    | 0x681B | 0x685B | 0x689B | 0x68DB | 1 / 0                | Event Trigger Flag Register                              |
| ETCLR    | 0x681C | 0x685C | 0x689C | 0x68DC | 1 / 0                | Event Trigger Clear Register                             |
| ETFRC    | 0x681D | 0x685D | 0x689D | 0x68DD | 1 / 0                | Event Trigger Force Register                             |
| PCCTL    | 0x681E | 0x685E | 0x689E | 0x68DE | 1 / 0                | PWM Chopper Control Register                             |
| HRCNFG   | 0x6820 | 0x6860 | 0x68A0 | 0x68E0 | 1 / 0                | HRPWM Configuration Register <sup>(1)</sup>              |
| HRPWR    | 0x6821 | -      | -      | -      | 1 / 0                | HRPWM Power Register                                     |
| HRMSTEP  | 0x6826 | -      | -      | -      | 1 / 0                | HRPWM MEP Step Register                                  |
| HRPCTL   | 0x6828 | 0x6868 | 0x68A8 | 0x68E8 | 1 / 0                | High resolution Period Control Register <sup>(1)</sup>   |
| TBPRDHRM | 0x682A | 0x686A | 0x68AA | 0x68EA | 1 / W <sup>(2)</sup> | Time Base Period HRPWM Register Mirror                   |
| TBPRDM   | 0x682B | 0x686B | 0x68AB | 0x68EB | 1 / W <sup>(2)</sup> | Time Base Period Register Mirror                         |
| CMPAHRM  | 0x682C | 0x686C | 0x68AC | 0x68EC | 1 / W <sup>(2)</sup> | Compare A HRPWM Register Mirror                          |
| CMPAM    | 0x682D | 0x686D | 0x68AD | 0x68ED | 1 / W <sup>(2)</sup> | Compare A Register Mirror                                |
| DCTRISEL | 0x6830 | 0x6870 | 0x68B0 | 0x68F0 | 1 / 0                | Digital Compare Trip Select Register <sup>(1)</sup>      |
| DCACTL   | 0x6831 | 0x6871 | 0x68B1 | 0x68F1 | 1 / 0                | Digital Compare A Control Register <sup>(1)</sup>        |
| DCBCTL   | 0x6832 | 0x6872 | 0x68B2 | 0x68F2 | 1 / 0                | Digital Compare B Control Register <sup>(1)</sup>        |
| DCFCTL   | 0x6833 | 0x6873 | 0x68B3 | 0x68F3 | 1 / 0                | Digital Compare Filter Control Register <sup>(1)</sup>   |

表 9-27. ePWM Control and Status Registers (continued)

| NAME         | ePWM1  | ePWM2  | ePWM3  | ePWM4  | SIZE (x16) /<br>#SHADOW | DESCRIPTION                                             |
|--------------|--------|--------|--------|--------|-------------------------|---------------------------------------------------------|
| DCCAPCT      | 0x6834 | 0x6874 | 0x68B4 | 0x68F4 | 1 / 0                   | Digital Compare Capture Control Register <sup>(1)</sup> |
| DCFOFFSET    | 0x6835 | 0x6875 | 0x68B5 | 0x68F5 | 1 / 1                   | Digital Compare Filter Offset Register                  |
| DCFOFFSETCNT | 0x6836 | 0x6876 | 0x68B6 | 0x68F6 | 1 / 0                   | Digital Compare Filter Offset Counter Register          |
| DCFWINDOW    | 0x6837 | 0x6877 | 0x68B7 | 0x68F7 | 1 / 0                   | Digital Compare Filter Window Register                  |
| DCFWINDOWCNT | 0x6838 | 0x6878 | 0x68B8 | 0x68F8 | 1 / 0                   | Digital Compare Filter Window Counter Register          |
| DCCAP        | 0x6839 | 0x6879 | 0x68B9 | 0x68F9 | 1 / 1                   | Digital Compare Counter Capture Register                |

(1) Registers that are EALLOW protected.

(2) W = Write to shadow register



A. These events are generated by the Type 1 ePWM digital compare (DC) submodule based on the levels of the COMPxOUT and TZ signals.

**图 9-36. ePWM Submodules Showing Critical Internal Signal Interconnections**

### 9.9.6.1 ePWM 电气数据/时序

PWM 是指 ePWM1-4 上的 PWM 输出。节 9.9.6.1.1 显示了 PWM 时序要求和节 9.9.6.1.2，开关特性。

#### 9.9.6.1.1 ePWM Timing Requirements

|                                      |                      | MIN <sup>(1)</sup>          | MAX | UNIT   |
|--------------------------------------|----------------------|-----------------------------|-----|--------|
| $t_{w(SYCN)}$ Sync input pulse width | Asynchronous         | $2t_{c(SCO)}$               |     | cycles |
|                                      | Synchronous          | $2t_{c(SCO)}$               |     | cycles |
|                                      | With input qualifier | $1t_{c(SCO)} + t_{w(IQSW)}$ |     | cycles |

(1) For an explanation of the input qualifier parameters, see 节 9.9.10.1.2.1.

#### 9.9.6.1.2 ePWM 开关特性

在推荐的运行条件下 (除非另有说明)

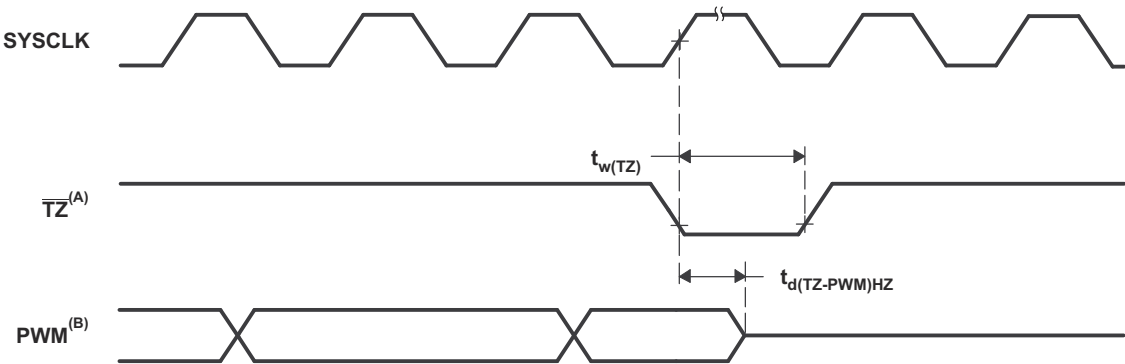
| 参数                                                                 | 测试条件  | 最小值           | 最大值 | 单位 |
|--------------------------------------------------------------------|-------|---------------|-----|----|
| $t_{w(PWM)}$ 脉冲持续时间, PWMx 输出高电平/低电平的时间                             |       | 33.33         |     | ns |
| $t_{w(SYNCOUT)}$ 同步输出脉冲宽度                                          |       | $8t_{c(SCO)}$ |     | 周期 |
| $t_{d(PWM)tza}$ 延迟时间, 跳闸有源输入到 PWM 强制高电平<br>延迟时间, 跳闸有源输入到 PWM 强制低电平 | 无引脚负载 |               | 25  | ns |
| $t_{d(TZ-PWM)HZ}$ 延迟时间, 触发输入有效至 PWM 高阻抗 (Hi-Z) 的时间                 |       |               | 20  | ns |

### 9.9.6.2 触发区输入时序

#### 9.9.6.2.1 Trip-Zone Input Timing Requirements

|                                           |                      | MIN <sup>(1)</sup>            | MAX | UNIT   |
|-------------------------------------------|----------------------|-------------------------------|-----|--------|
| $t_{w(TZ)}$ Pulse duration, TZx input low | Asynchronous         | $2t_{c(TBCLK)}$               |     | cycles |
|                                           | Synchronous          | $2t_{c(TBCLK)}$               |     | cycles |
|                                           | With input qualifier | $2t_{c(TBCLK)} + t_{w(IQSW)}$ |     | cycles |

(1) For an explanation of the input qualifier parameters, see 节 9.9.10.1.2.1.



- A. TZ - TZ1, TZ2, TZ3  
B. PWM refers to all the PWM pins in the device. The state of the PWM pins after TZ is taken high depends on the PWM recovery software.

图 9-37. PWM Hi-Z Characteristics

### 9.9.7 High-Resolution PWM (HRPWM)

This module combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module there is one HR delay line.

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A and Phase registers of the ePWM module.
- HRPWM capabilities, when available on a particular device, are offered only on the A signal path of an ePWM module (that is, on the EPWMxA output). EPWMxB output has conventional PWM capabilities.

#### 备注

The minimum SYSCLKOUT frequency allowed for HRPWM is 50 MHz.

#### 备注

When dual-edge high-resolution is enabled (high-resolution period mode), the PWMxB output is not available for use.

#### 9.9.7.1 HRPWM 电气数据/时序

节 9.9.7.1.1 显示了高分辨率 PWM 的开关特性。

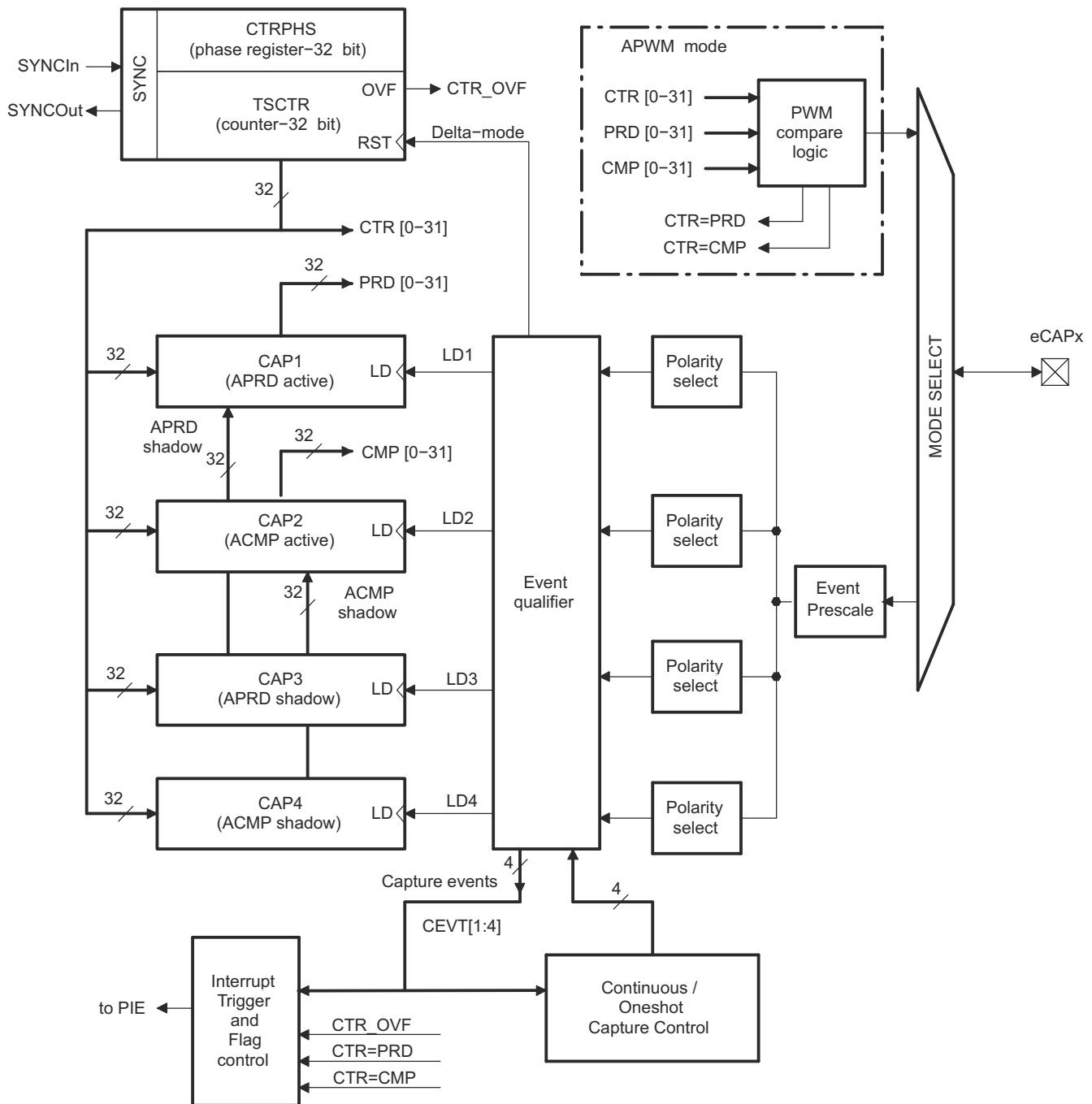
##### 9.9.7.1.1 SYSCLKOUT = 50MHz – 60MHz 下的高分辨率 PWM 特性

| 参数 <sup>(1)</sup>             | 最小值 | 典型值 | 最大值 | 单位 |
|-------------------------------|-----|-----|-----|----|
| 微边沿定位 (MEP) 步长 <sup>(2)</sup> | 150 | 310 |     | ps |

- (1) HRPWM 运行在一个最少 50MHz 的 SYSCLKOUT 频率上。低于 50MHz，在器件过程变化时，MEP 阶跃尺寸有可能下降至低于冷却温度并且高内核电压达到一个要求的值以至于 255 MEP 阶跃将不能跨过整个 SYSCLKOUT 周期。
- (2) 在高温和  $V_{DD}$  上的电压最低时，MEP 步长将达到最大。MEP 步长会随温度升高和电压降低而增加，同时随温度降低和电压升高而减小。  
使用 HRPWM 特性的应用应该使用 MEP 比例因子优化器 (SFO) 估计软件功能。有关在最终应用中使用 SFO 函数的详细信息，请参阅 TI 软件库。SFO 函数有助于在 HRPWM 运行时动态地估计每个 SYSCLKOUT 周期内的 MEP 步数量。

### 9.9.8 Enhanced Capture Module (eCAP1)

The device contains an enhanced capture (eCAP) module. 图 9-38 shows a functional block diagram of a module.



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**图 9-38. eCAP Functional Block Diagram**

The eCAP module is clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1 ENCLK) in the PCLKCR1 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.



表 9-28. eCAP Control and Status Registers

| NAME     | eCAP1            | SIZE (x16) | EALLOW PROTECTED | DESCRIPTION                         |
|----------|------------------|------------|------------------|-------------------------------------|
| TSCTR    | 0x6A00           | 2          |                  | Time-Stamp Counter                  |
| CTPHS    | 0x6A02           | 2          |                  | Counter Phase Offset Value Register |
| CAP1     | 0x6A04           | 2          |                  | Capture 1 Register                  |
| CAP2     | 0x6A06           | 2          |                  | Capture 2 Register                  |
| CAP3     | 0x6A08           | 2          |                  | Capture 3 Register                  |
| CAP4     | 0x6A0A           | 2          |                  | Capture 4 Register                  |
| Reserved | 0x6A0C to 0x6A12 | 8          |                  | Reserved                            |
| ECCTL1   | 0x6A14           | 1          |                  | Capture Control Register 1          |
| ECCTL2   | 0x6A15           | 1          |                  | Capture Control Register 2          |
| ECEINT   | 0x6A16           | 1          |                  | Capture Interrupt Enable Register   |
| ECFLG    | 0x6A17           | 1          |                  | Capture Interrupt Flag Register     |
| ECCLR    | 0x6A18           | 1          |                  | Capture Interrupt Clear Register    |
| ECFRC    | 0x6A19           | 1          |                  | Capture Interrupt Force Register    |
| Reserved | 0x6A1A to 0x6A1F | 6          |                  | Reserved                            |

For more information on the eCAP, see the Enhanced Capture (eCAP) Module chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).

### 9.9.8.1 eCAP 电气数据/时序

节 9.9.8.1.1 显示了 eCAP 时序要求，而节 9.9.8.1.2 显示了 eCAP 开关特性。

#### 9.9.8.1.1 Enhanced Capture (eCAP) Timing Requirement

|              |                      | MIN <sup>(1)</sup>          | MAX | UNIT   |
|--------------|----------------------|-----------------------------|-----|--------|
| $t_{w(CAP)}$ | Asynchronous         | $2t_{c(SCO)}$               |     | cycles |
|              | Synchronous          | $2t_{c(SCO)}$               |     | cycles |
|              | With input qualifier | $1t_{c(SCO)} + t_{w(IQSW)}$ |     | cycles |

(1) For an explanation of the input qualifier parameters, see 节 9.9.10.1.2.1.

#### 9.9.8.1.2 eCAP 开关特性

在推荐的运行条件下 (除非额外注明)

| 参数            | 测试条件                       | 最小值 | 最大值 | 单位 |
|---------------|----------------------------|-----|-----|----|
| $t_{w(APWM)}$ | 脉冲持续时间, APWMx 输出高电平/低电平的时间 | 20  |     | ns |

### 9.9.9 JTAG 端口

在 2802x 器件上，JTAG 端口减少到 5 个引脚 (  $\overline{\text{TRST}}$ 、TCK、TDI、TMS、TDO )。TCK、TDI、TMS 和 TDO 引脚也是 GPIO 引脚。 $\overline{\text{TRST}}$  信号在图 9-39 中为引脚选择 JTAG 或者 GPIO 运行模式。在仿真/调试期间，这些引脚的 GPIO 功能并不可用。如果 GPIO38/TCK/XCLKIN 引脚用于提供外部时钟，则应使用替代时钟源在仿真/调试期间为器件计时，这是因为 TCK 功能需要此引脚。

#### 备注

在 2802x 器件中，JTAG 引脚也可被用作 GPIO 引脚。在电路板设计时应小心以确保连接到这些引脚的电路不会影响 JTAG 引脚功能的仿真能力。要进行成功调试，连接到这些引脚的任何电路不应导致 JTAG 调试探针无法驱动 JTAG 引脚 ( 或无法受其驱动 )。

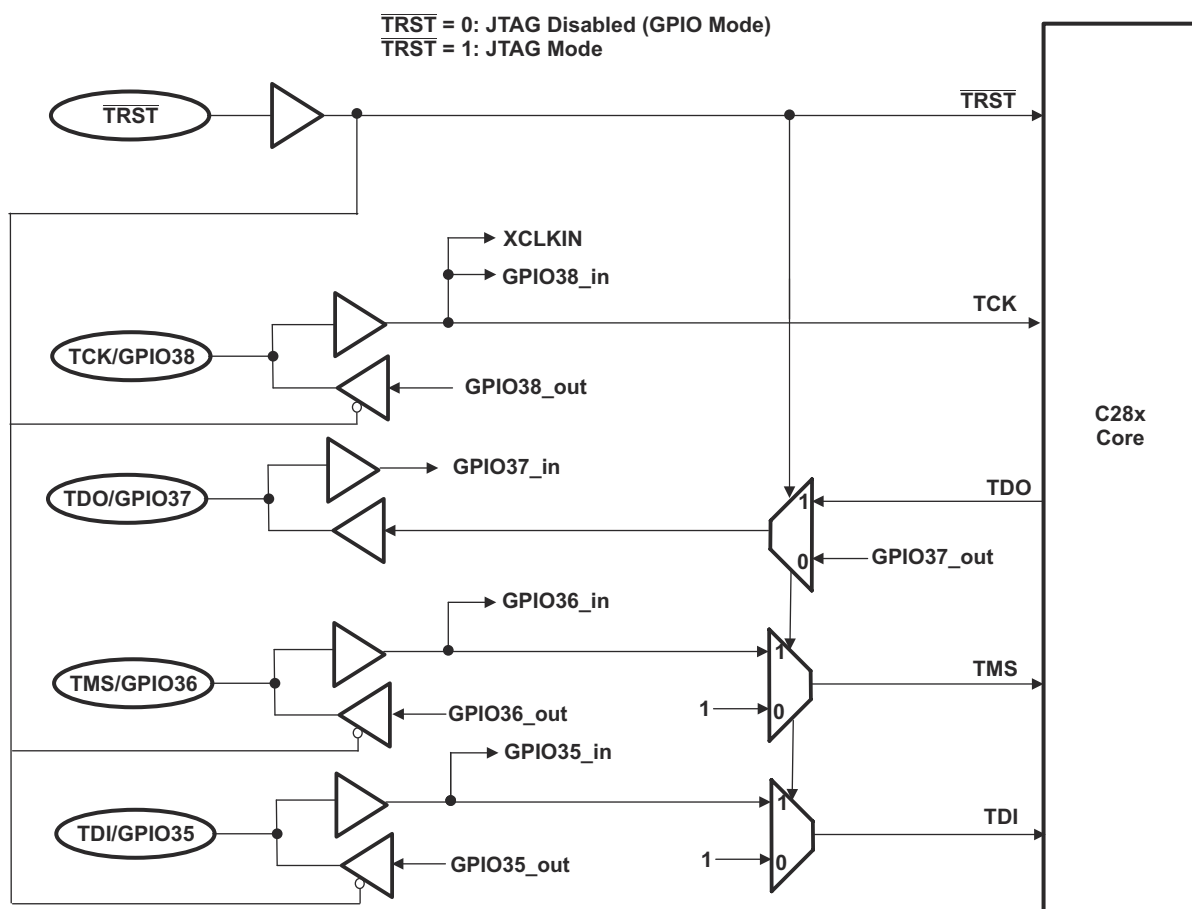


图 9-39. JTAG/GPIO 多路复用

### 9.9.10 General-Purpose Input/Output (GPIO) MUX

The GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging I/O capability.

The device supports 22 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). 表 9-29 shows the GPIO register mapping.

表 9-29. GPIO Registers

| NAME                                                                          | ADDRESS | SIZE (x16) | DESCRIPTION                                       |
|-------------------------------------------------------------------------------|---------|------------|---------------------------------------------------|
| <b>GPIO CONTROL REGISTERS (EALLOW PROTECTED)</b>                              |         |            |                                                   |
| GPACTRL                                                                       | 0x6F80  | 2          | GPIO A Control Register (GPIO0 to 31)             |
| GPAQSEL1                                                                      | 0x6F82  | 2          | GPIO A Qualifier Select 1 Register (GPIO0 to 15)  |
| GPAQSEL2                                                                      | 0x6F84  | 2          | GPIO A Qualifier Select 2 Register (GPIO16 to 31) |
| GPAMUX1                                                                       | 0x6F86  | 2          | GPIO A MUX 1 Register (GPIO0 to 15)               |
| GPAMUX2                                                                       | 0x6F88  | 2          | GPIO A MUX 2 Register (GPIO16 to 31)              |
| GPADIR                                                                        | 0x6F8A  | 2          | GPIO A Direction Register (GPIO0 to 31)           |
| GPAPUD                                                                        | 0x6F8C  | 2          | GPIO A Pullup Disable Register (GPIO0 to 31)      |
| GPBCTRL                                                                       | 0x6F90  | 2          | GPIO B Control Register (GPIO32 to 38)            |
| GPBQSEL1                                                                      | 0x6F92  | 2          | GPIO B Qualifier Select 1 Register (GPIO32 to 38) |
| GPBMUX1                                                                       | 0x6F96  | 2          | GPIO B MUX 1 Register (GPIO32 to 38)              |
| GPBDIR                                                                        | 0x6F9A  | 2          | GPIO B Direction Register (GPIO32 to 38)          |
| GPBPUD                                                                        | 0x6F9C  | 2          | GPIO B Pullup Disable Register (GPIO32 to 38)     |
| AIOMUX1                                                                       | 0x6FB6  | 2          | Analog, I/O mux 1 register (AIO0 to AIO15)        |
| AIODIR                                                                        | 0x6FBA  | 2          | Analog, I/O Direction Register (AIO0 to AIO15)    |
| <b>GPIO DATA REGISTERS (NOT EALLOW PROTECTED)</b>                             |         |            |                                                   |
| GPADAT                                                                        | 0x6FC0  | 2          | GPIO A Data Register (GPIO0 to 31)                |
| GPASET                                                                        | 0x6FC2  | 2          | GPIO A Data Set Register (GPIO0 to 31)            |
| GPACLEAR                                                                      | 0x6FC4  | 2          | GPIO A Data Clear Register (GPIO0 to 31)          |
| GPATOGGLE                                                                     | 0x6FC6  | 2          | GPIO A Data Toggle Register (GPIO0 to 31)         |
| GPBDAT                                                                        | 0x6FC8  | 2          | GPIO B Data Register (GPIO32 to 38)               |
| GPBSET                                                                        | 0x6FCA  | 2          | GPIO B Data Set Register (GPIO32 to 38)           |
| GPBCLEAR                                                                      | 0x6FCC  | 2          | GPIO B Data Clear Register (GPIO32 to 38)         |
| GPBTOGGLE                                                                     | 0x6FCE  | 2          | GPIO B Data Toggle Register (GPIO32 to 38)        |
| AIODAT                                                                        | 0x6FD8  | 2          | Analog I/O Data Register (AIO0 to AIO15)          |
| AIOSET                                                                        | 0x6FDA  | 2          | Analog I/O Data Set Register (AIO0 to AIO15)      |
| AIOCLEAR                                                                      | 0x6FDC  | 2          | Analog I/O Data Clear Register (AIO0 to AIO15)    |
| AIOTOGGLE                                                                     | 0x6FDE  | 2          | Analog I/O Data Toggle Register (AIO0 to AIO15)   |
| <b>GPIO INTERRUPT AND LOW-POWER MODES SELECT REGISTERS (EALLOW PROTECTED)</b> |         |            |                                                   |
| GPIOXINT1SEL                                                                  | 0x6FE0  | 1          | XINT1 GPIO Input Select Register (GPIO0 to 31)    |
| GPIOXINT2SEL                                                                  | 0x6FE1  | 1          | XINT2 GPIO Input Select Register (GPIO0 to 31)    |
| GPIOXINT3SEL                                                                  | 0x6FE2  | 1          | XINT3 GPIO Input Select Register (GPIO0 to 31)    |
| GPIOLPMSSEL                                                                   | 0x6FE8  | 2          | LPM GPIO Select Register (GPIO0 to 31)            |

#### 备注

There is a two-SYSCLKOUT cycle delay from when the write to the GPxMUXn/AIOMUXn and GPxQSELn registers occurs to when the action is valid.

表 9-30. GPIOA MUX

|                                  | DEFAULT AT RESET<br>PRIMARY I/O<br>FUNCTION <sup>(1) (2)</sup> | PERIPHERAL<br>SELECTION 1  | PERIPHERAL<br>SELECTION 2  | PERIPHERAL<br>SELECTION 3   |
|----------------------------------|----------------------------------------------------------------|----------------------------|----------------------------|-----------------------------|
| <b>GPAMUX1 REGISTER<br/>BITS</b> | <b>(GPAMUX1 BITS = 00)</b>                                     | <b>(GPAMUX1 BITS = 01)</b> | <b>(GPAMUX1 BITS = 10)</b> | <b>(GPAMUX1 BITS = 11)</b>  |
| 1-0                              | GPIO0                                                          | EPWM1A (O)                 | Reserved                   | Reserved                    |
| 3-2                              | GPIO1                                                          | EPWM1B (O)                 | Reserved                   | COMP1OUT (O)                |
| 5-4                              | GPIO2                                                          | EPWM2A (O)                 | Reserved                   | Reserved                    |
| 7-6                              | GPIO3                                                          | EPWM2B (O)                 | Reserved                   | COMP2OUT <sup>(3)</sup> (O) |
| 9-8                              | GPIO4                                                          | EPWM3A (O)                 | Reserved                   | Reserved                    |
| 11-10                            | GPIO5                                                          | EPWM3B (O)                 | Reserved                   | ECAP1 (I/O)                 |
| 13-12                            | GPIO6                                                          | EPWM4A (O)                 | EPWMSYNCl (I)              | EPWMSYNCO (O)               |
| 15-14                            | GPIO7                                                          | EPWM4B (O)                 | SCIRXDA (I)                | Reserved                    |
| 17-16                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 19-18                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 21-20                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 23-22                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 25-24                            | GPIO12                                                         | TZ1 (I)                    | SCITXDA (O)                | Reserved                    |
| 27-26                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 29-28                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 31-30                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| <b>GPAMUX2 REGISTER<br/>BITS</b> | <b>(GPAMUX2 BITS = 00)</b>                                     | <b>(GPAMUX2 BITS = 01)</b> | <b>(GPAMUX2 BITS = 10)</b> | <b>(GPAMUX2 BITS = 11)</b>  |
| 1-0                              | GPIO16                                                         | SPISIMOA (I/O)             | Reserved                   | TZ2 (I)                     |
| 3-2                              | GPIO17                                                         | SPISOMIA (I/O)             | Reserved                   | TZ3 (I)                     |
| 5-4                              | GPIO18                                                         | SPICLKA (I/O)              | SCITXDA (O)                | XCLKOUT (O)                 |
| 7-6                              | GPIO19/XCLKIN                                                  | SPISTEA (I/O)              | SCIRXDA (I)                | ECAP1 (I/O)                 |
| 9-8                              | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 11-10                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 13-12                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 15-14                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 17-16                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 19-18                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 21-20                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 23-22                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 25-24                            | GPIO28                                                         | SCIRXDA (I)                | SDAA (I/OD)                | TZ2 (I)                     |
| 27-26                            | GPIO29                                                         | SCITXDA (O)                | SCLA (I/OD)                | TZ3 (I)                     |
| 29-28                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |
| 31-30                            | Reserved                                                       | Reserved                   | Reserved                   | Reserved                    |

(1) The word reserved means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should it be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.

(2) I = Input, O = Output, OD = Open Drain

(3) These functions are not available in the 38-pin package.

**表 9-31. GPIOB MUX**

|                          | DEFAULT AT RESET<br>PRIMARY I/O<br>FUNCTION <sup>(1)</sup> | PERIPHERAL<br>SELECTION 1   | PERIPHERAL<br>SELECTION 2    | PERIPHERAL<br>SELECTION 3    |
|--------------------------|------------------------------------------------------------|-----------------------------|------------------------------|------------------------------|
| GPBMUX1 REGISTER<br>BITS | (GPBMUX1 BITS = 00)                                        | (GPBMUX1 BITS = 01)         | (GPBMUX1 BITS = 10)          | (GPBMUX1 BITS = 11)          |
| 1-0                      | GPIO32 <sup>(2)</sup>                                      | SDAA <sup>(2)</sup> (I/OD)  | EPWMSYNCl <sup>(2)</sup> (I) | ADCSOClAO <sup>(2)</sup> (O) |
| 3-2                      | GPIO33 <sup>(2)</sup>                                      | SCLAl <sup>(2)</sup> (I/OD) | EPWMSYNCO <sup>(2)</sup> (O) | ADCSOClBO <sup>(2)</sup> (O) |
| 5-4                      | GPIO34                                                     | COMP2OUT (O)                | Reserved                     | Reserved                     |
| 7-6                      | GPIO35 (TDI)                                               | Reserved                    | Reserved                     | Reserved                     |
| 9-8                      | GPIO36 (TMS)                                               | Reserved                    | Reserved                     | Reserved                     |
| 11-10                    | GPIO37 (TDO)                                               | Reserved                    | Reserved                     | Reserved                     |
| 13-12                    | GPIO38/XCLKIN (TCK)                                        | Reserved                    | Reserved                     | Reserved                     |
| 15-14                    | Reserved                                                   | Reserved                    | Reserved                     | Reserved                     |
| 17-16                    | Reserved                                                   | Reserved                    | Reserved                     | Reserved                     |
| 19-18                    | Reserved                                                   | Reserved                    | Reserved                     | Reserved                     |
| 21-20                    | Reserved                                                   | Reserved                    | Reserved                     | Reserved                     |
| 23-22                    | Reserved                                                   | Reserved                    | Reserved                     | Reserved                     |
| 25-24                    | Reserved                                                   | Reserved                    | Reserved                     | Reserved                     |
| 27-26                    | Reserved                                                   | Reserved                    | Reserved                     | Reserved                     |
| 29-28                    | Reserved                                                   | Reserved                    | Reserved                     | Reserved                     |
| 31-30                    | Reserved                                                   | Reserved                    | Reserved                     | Reserved                     |

(1) I = Input, O = Output, OD = Open Drain

(2) These pins are not available in the 38-pin package.

**表 9-32. Analog MUX for 48-Pin PT Package**

|                       |                                     | DEFAULT AT RESET <sup>(1)</sup>                      |
|-----------------------|-------------------------------------|------------------------------------------------------|
|                       | AIOx AND PERIPHERAL SELECTION 1     | PERIPHERAL SELECTION 2 AND<br>PERIPHERAL SELECTION 3 |
| AIOMUX1 REGISTER BITS | AIOMUX1 BITS = 0,x                  | AIOMUX1 BITS = 1,x                                   |
| 1-0                   | ADCINA0 (I), V <sub>REFHI</sub> (I) | ADCINA0 (I), V <sub>REFHI</sub> (I)                  |
| 3-2                   | ADCINA1 (I)                         | ADCINA1 (I)                                          |
| 5-4                   | AIO2 (I/O)                          | ADCINA2 (I), COMP1A (I)                              |
| 7-6                   | ADCINA3 (I)                         | ADCINA3 (I)                                          |
| 9-8                   | AIO4 (I/O)                          | ADCINA4 (I), COMP2A (I)                              |
| 11-10                 | –                                   | –                                                    |
| 13-12                 | AIO6 (I/O)                          | ADCINA6 (I)                                          |
| 15-14                 | ADCINA7 (I)                         | ADCINA7 (I)                                          |
| 17-16                 | –                                   | –                                                    |
| 19-18                 | ADCINB1 (I)                         | ADCINB1 (I)                                          |
| 21-20                 | AIO10 (I/O)                         | ADCINB2 (I), COMP1B (I)                              |
| 23-22                 | ADCINB3 (I)                         | ADCINB3 (I)                                          |
| 25-24                 | AIO12 (I/O)                         | ADCINB4 (I), COMP2B (I)                              |
| 27-26                 | –                                   | –                                                    |
| 29-28                 | AIO14 (I/O)                         | ADCINB6 (I)                                          |
| 31-30                 | ADCINB7 (I)                         | ADCINB7 (I)                                          |

(1) I = Input, O = Output

表 9-33. Analog MUX for 38-Pin DA Package

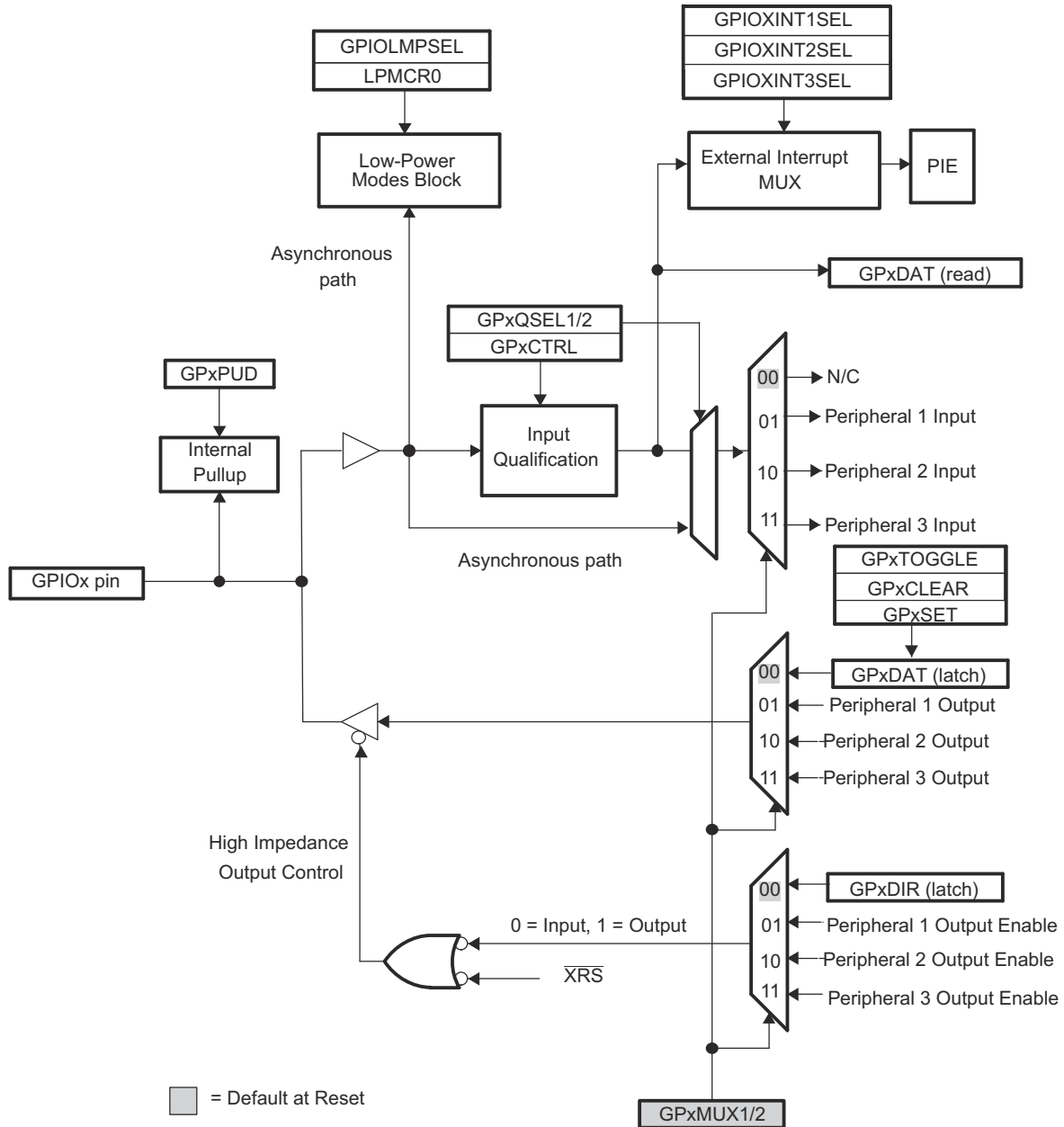
|                       |                                     | DEFAULT AT RESET <sup>(1)</sup>                   |
|-----------------------|-------------------------------------|---------------------------------------------------|
|                       | AIOx AND PERIPHERAL SELECTION 1     | PERIPHERAL SELECTION 2 AND PERIPHERAL SELECTION 3 |
| AIOMUX1 REGISTER BITS | AIOMUX1 BITS = 0,x                  | AIOMUX1 BITS = 1,x                                |
| 1-0                   | ADCINA0 (I), V <sub>REFHI</sub> (I) | ADCINA0 (I), V <sub>REFHI</sub> (I)               |
| 3-2                   | -                                   | -                                                 |
| 5-4                   | AIO2 (I/O)                          | ADCINA2 (I), COMP1A (I)                           |
| 7-6                   | -                                   | -                                                 |
| 9-8                   | AIO4 (I/O)                          | ADCINA4 (I)                                       |
| 11-10                 | -                                   | -                                                 |
| 13-12                 | AIO6 (I/O)                          | ADCINA6 (I)                                       |
| 15-14                 | -                                   | -                                                 |
| 17-16                 | -                                   | -                                                 |
| 19-18                 | -                                   | -                                                 |
| 21-20                 | AIO10 (I/O)                         | ADCINB2 (I), COMP1B (I)                           |
| 23-22                 | -                                   | -                                                 |
| 25-24                 | AIO12 (I/O)                         | ADCINB4 (I)                                       |
| 27-26                 | -                                   | -                                                 |
| 29-28                 | AIO14 (I/O)                         | ADCINB6 (I)                                       |
| 31-30                 | -                                   | -                                                 |

(1) I = Input, O = Output

The user can select the type of input qualification for each GPIO pin through the GPxQSEL1/2 registers from four choices:

- Synchronization To SYSCLKOUT Only (GPxQSEL1/2 = 0, 0): This is the default mode of all GPIO pins at reset and it simply synchronizes the input signal to the system clock (SYSCLKOUT).
- Qualification Using Sampling Window (GPxQSEL1/2 = 0, 1 and 1, 0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.
- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. It specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in 图 9-42 (for 6 sample mode).
- No Synchronization (GPxQSEL1/2 = 1, 1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multilevel multiplexing that is required on the device, there may be cases where a peripheral input signal can be mapped to more than one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.



- A. x stands for the port, either A or B. For example, GPxDIR refers to either the GPADIR and GPBDIR register depending on the particular GPIO pin selected.
- B. GPxDAT latch/read are accessed at the same memory location.
- C. This is a generic GPIO MUX block diagram. Not all options may be applicable for all GPIO pins. For pin-specific variations, see the System Control chapter in the [TMS320F2802x, TMS320F2802xx Technical Reference Manual](#).

**图 9-40. GPIO Multiplexing**

9.9.10.1 GPIO 电气数据/时序

9.9.10.1.1 GPIO - 输出时序

9.9.10.1.1.1 通用输出开关特性

在推荐的运行条件下 ( 除非另有说明 )

| 参数           |                          |         | 最小值 | 最大值               | 单位  |
|--------------|--------------------------|---------|-----|-------------------|-----|
| $t_{r(GPO)}$ | 上升时间, GPIO 从低电平切换至高电平的时间 | 所有 GPIO |     | 13 <sup>(1)</sup> | ns  |
| $t_{f(GPO)}$ | 下降时间, GPIO 从高电平切换至低电平的时间 | 所有 GPIO |     | 13 <sup>(1)</sup> | ns  |
| $t_{fGPO}$   | 切换频率                     |         |     | 15                | MHz |

(1) 上升时间和下降时间随着 I/O 引脚上的电力负荷变化。节 9.9.10.1.1.1 中指定的值适用于一个 I/O 引脚上的 40pF 负载。

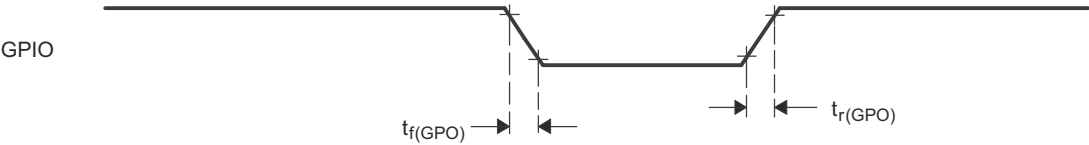


图 9-41. 通用输出定时



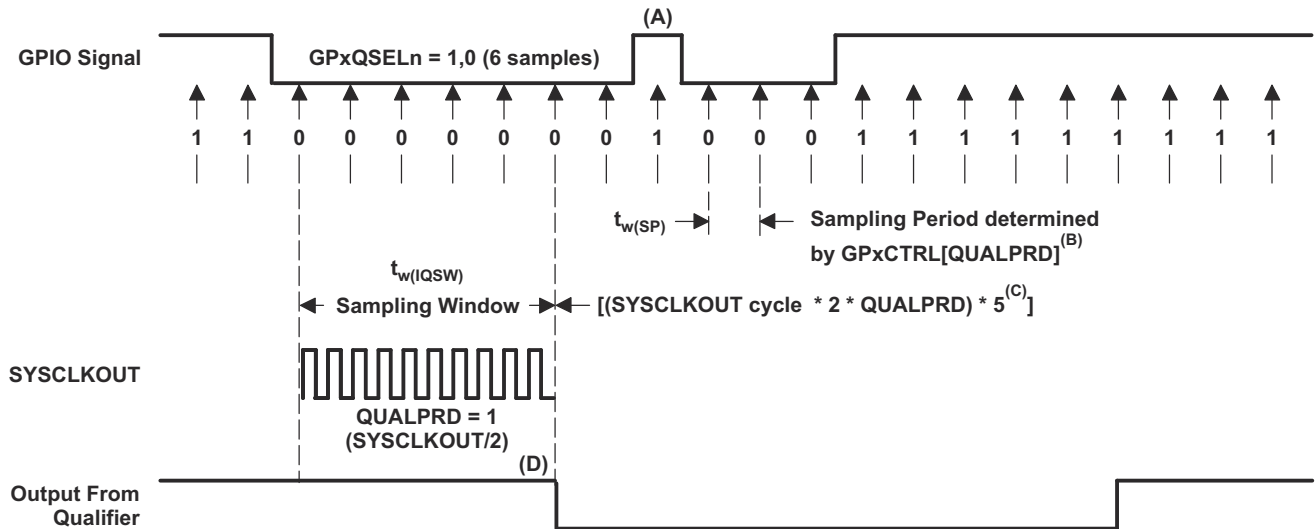
### 9.9.10.1.2 GPIO - 输入时序

#### 9.9.10.1.2.1 通用输入时序要求

|                  |                         | 最小值                                     | 最大值           | 单位 |
|------------------|-------------------------|-----------------------------------------|---------------|----|
| $t_{w(SP)}$      | 采样周期                    | $1t_{c(SCO)}$                           |               | 周期 |
|                  | QUALPRD=0               |                                         |               |    |
|                  | QUALPRD $\neq$ 0        | $2t_{c(SCO)} * QUALPRD$                 |               | 周期 |
| $t_{w(IQSW)}$    | 输入限定器采样窗口               | $t_{w(SP)} * (n^{(1)} - 1)$             |               | 周期 |
| $t_{w(GPI)}$ (2) | 脉冲持续时间, GPIO 低电平/高电平的时间 | 同步模式                                    | $2t_{c(SCO)}$ | 周期 |
|                  | 带输入限定器                  | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SCO)}$ |               | 周期 |

(1) "n" 代表由 GPxQSELn 寄存器定义的限定采样的数量。

(2) 对于  $t_{w(GPI)}$ , 对于一个低电平有效信号, 脉宽在  $V_{IL}$  至  $V_{IL}$  之间进行测量, 而对于一个高电平有效信号脉宽在  $V_{IH}$  至  $V_{IH}$  之间进行测量。



- A. 这个毛刺脉冲将被输入限定器所忽略。QUALPRD 位字段指定了限定采样周期。它可在 00 至 0xFF 间变化。如果 QUALPRD=00, 那么采样周期为 1 个 SYSCLKOUT 周期。对于任何其它的 "n" 值, 限定采样周期为 2n SYSCLKOUT 周期 (也就是说, 在每一个 SYSCLKOUT 周期上, GPIO 引脚将被采样)。
- B. 通过 GPxCTRL 寄存器选择的限定期会应用于 8 个 GPIO 引脚的组。
- C. 此限定块可采样 3 个或者 6 个样本。GPxQSELn 寄存器选择使用的采样模式。
- D. 在所示的示例中, 为了使限定器检测到变化, 输入应该在 10 个 SYSCLKOUT 周期或者更长的时间内保持稳定。换句话说, 输入应该在  $(5 \times QUALPRD \times 2)$  SYSCLKOUT 周期内保持稳定。这将确保发生 5 个用于检测的采样周期。由于外部信号是异步驱动的, 因此一个 13 SYSCLKOUT 宽的脉冲将会确保可靠识别。

图 9-42. 采样模式

### 9.9.10.1.3 针对输入信号的采样窗口宽度

下面的部分总结了不同的输入限定器配置下用于输入信号的采样窗口宽度。

采样频率表明相对于 SYSCLKOUT 的信号采样频率。

如果  $QUALPRD \neq 0$  的话, 采样频率 =  $SYSCLKOUT / (2 \times QUALPRD)$

如果  $QUALPRD = 0$  的话, 采样频率 =  $SYSCLKOUT$

如果  $QUALPRD \neq 0$  的话, 采样周期 =  $SYSCLKOUT$  周期  $\times 2 \times QUALPRD$

在上面的等式中,  $SYSCLKOUT$  周期表明  $SYSCLKOUT$  的时间周期。

如果  $QUALPRD = 0$  的话, 采样周期 =  $SYSCLKOUT$  周期

在指定的采样窗口中, 采取输入信号的 3 个样本或者 6 个样本来确定信号的有效性。这取决于写入  $GPxQSELn$  寄存器的值。

#### 情况 1 :

使用 3 个样本限定

如果  $QUALPRD \neq 0$  的话, 采样窗口宽度 =  $(SYSCLKOUT \text{ 周期} \times 2 \times QUALPRD) \times 2$

如果  $QUALPRD = 0$  的话, 采样窗口宽度 =  $(SYSCLKOUT \text{ 周期}) \times 2$

#### 情况 2 :

使用 6 个样本限定

如果  $QUALPRD \neq 0$  的话, 采样窗口宽度 =  $(SYSCLKOUT \text{ 周期} \times 2 \times QUALPRD) \times 5$

如果  $QUALPRD = 0$  的话, 采样窗口宽度 =  $(SYSCLKOUT \text{ 周期}) \times 5$

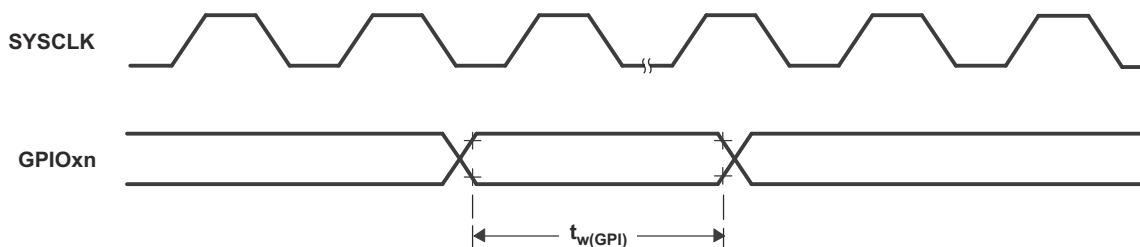


图 9-43. 通用输入时序

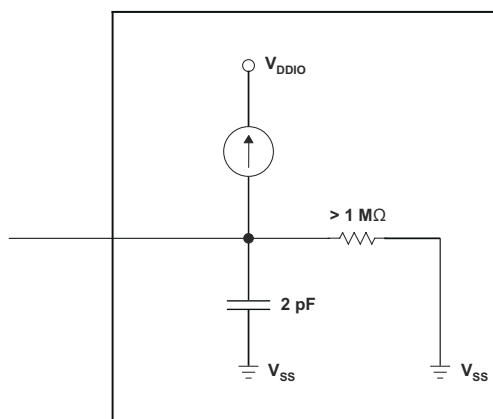


图 9-44. 针对带有内部上拉电阻的 GPIO 引脚的输入电阻模型

#### 9.9.10.1.4 低功耗唤醒时序

节 9.9.10.1.4.1 显示时序要求，节 9.9.10.1.4.2 显示了开关特性，而图 9-45 显示了 IDLE 模式下的时序图

##### 9.9.10.1.4.1 IDLE Mode Timing Requirements

|                   |                                         | MIN <sup>(1)</sup>      | MAX                         | UNIT   |
|-------------------|-----------------------------------------|-------------------------|-----------------------------|--------|
| $t_{w(WAKE-INT)}$ | Pulse duration, external wake-up signal | Without input qualifier | $2t_{c(SCO)}$               | cycles |
|                   |                                         | With input qualifier    | $5t_{c(SCO)} + t_{w(IQSW)}$ |        |

(1) For an explanation of the input qualifier parameters, see 节 9.9.10.1.2.1.

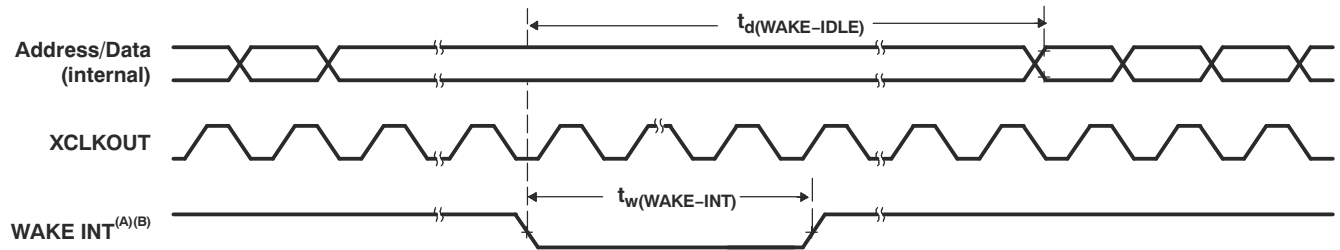
##### 9.9.10.1.4.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

|                    | PARAMETER <sup>(1)</sup>                                                    | TEST CONDITIONS         | MIN | MAX                            | UNIT   |
|--------------------|-----------------------------------------------------------------------------|-------------------------|-----|--------------------------------|--------|
| $t_{d(WAKE-IDLE)}$ | Delay time, external wake signal to program execution resume <sup>(2)</sup> |                         |     |                                | cycles |
|                    | • Wake up from Flash<br>– Flash module in active state                      | Without input qualifier |     | $20t_{c(SCO)}$                 | cycles |
|                    |                                                                             | With input qualifier    |     | $20t_{c(SCO)} + t_{w(IQSW)}$   |        |
|                    | • Wake up from Flash<br>– Flash module in sleep state                       | Without input qualifier |     | $1050t_{c(SCO)}$               | cycles |
|                    |                                                                             | With input qualifier    |     | $1050t_{c(SCO)} + t_{w(IQSW)}$ |        |
|                    | • Wake up from SARAM                                                        | Without input qualifier |     | $20t_{c(SCO)}$                 | cycles |
|                    |                                                                             | With input qualifier    |     | $20t_{c(SCO)} + t_{w(IQSW)}$   |        |

(1) For an explanation of the input qualifier parameters, see 节 9.9.10.1.2.1.

(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.



A. WAKE INT can be any enabled interrupt, WDINT or XRS.

B. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least 4 OSCCLK cycles have elapsed.

图 9-45. IDLE Entry and Exit Timing

#### 9.9.10.1.4.3 待机模式时序要求

|                   |                   | 最小值                  | 最大值                               | 单位 |
|-------------------|-------------------|----------------------|-----------------------------------|----|
| $t_{w(WAKE-INT)}$ | 脉冲持续时间, 外部唤醒信号的时间 | 无输入限定                | $3t_{c(OSCCLK)}$                  | 周期 |
|                   |                   | 带输入限定 <sup>(1)</sup> | $(2 + QUALSTDBY) * t_{c(OSCCLK)}$ |    |

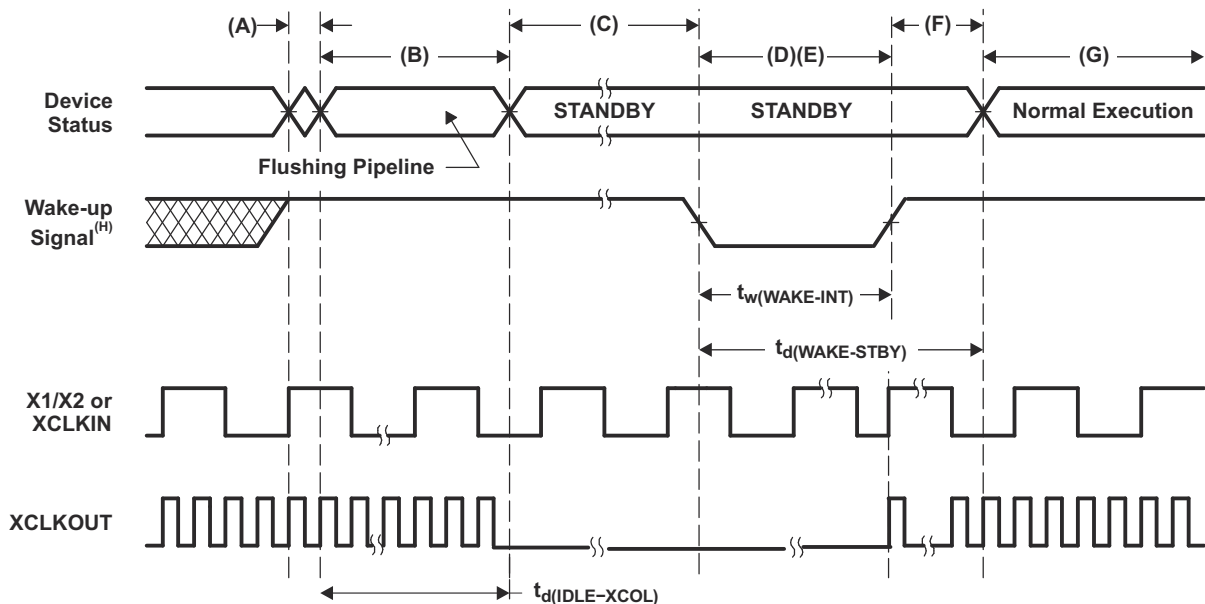
(1) QUALSTDBY 是 LPMCR0 寄存器中的一个 6 位字段。

#### 9.9.10.1.4.4 待机模式开关特性

在推荐的运行条件下 ( 除非另有说明 )

| 参数                 |                                                                                                                                                   | 测试条件   | 最小值            | 最大值                                | 单位 |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------|------------------------------------|----|
| $t_{d(IDLE-XCOL)}$ | 延迟时间, IDLE 指令执行到 XCLKOUT 低电平的时间                                                                                                                   |        | $32t_{c(SCO)}$ | $45t_{c(SCO)}$                     | 周期 |
| $t_{d(WAKE-STBY)}$ | 延迟时间, 外部唤醒信号到程序执行重新开始的时间 <sup>(1)</sup>                                                                                                           |        |                |                                    | 周期 |
|                    | <ul style="list-style-type: none"> <li>从闪存唤醒                             <ul style="list-style-type: none"> <li>激活状态中的闪存模块</li> </ul> </li> </ul> | 无输入限定器 |                | $100t_{c(SCO)}$                    | 周期 |
|                    |                                                                                                                                                   | 带输入限定器 |                | $100t_{c(SCO)} + t_{w(WAKE-INT)}$  |    |
|                    | <ul style="list-style-type: none"> <li>从闪存唤醒                             <ul style="list-style-type: none"> <li>睡眠状态中的闪存模块</li> </ul> </li> </ul> | 无输入限定器 |                | $1125t_{c(SCO)}$                   | 周期 |
|                    |                                                                                                                                                   | 带输入限定器 |                | $1125t_{c(SCO)} + t_{w(WAKE-INT)}$ |    |
|                    | <ul style="list-style-type: none"> <li>从 SARAM 中唤醒</li> </ul>                                                                                     | 无输入限定器 |                | $100t_{c(SCO)}$                    | 周期 |
|                    |                                                                                                                                                   | 带输入限定器 |                | $100t_{c(SCO)} + t_{w(WAKE-INT)}$  |    |

(1) 这个时间是在 IDLE 指令之后立即开始指令执行的时间。ISR ( 由唤醒信号触发 ) 的执行需要额外延迟。



- A. 执行 IDLE 指令将器件置于待机模式。
- B. PLL 块响应待机信号。SYSCLKOUT 在关闭之前保持以下所示数量的周期：
- 当 DIVSEL=00 或 01 时，16 个周期
  - 当 DIVSEL=10 时，32 个周期
  - 当 DIVSEL=11 时，64 个周期
- 此延迟使得 CPU 流水线和其待定操作适当清除。
- C. 外设的时钟关闭。然而，PLL 和看门狗未关闭。此器件现在处于待机模式。
- D. 外部唤醒信号驱动为有效。
- E. 为唤醒器件而馈送给 GPIO 引脚的唤醒信号必须符合最小脉冲宽度要求。此外，此信号不能有毛刺。如果噪声信号馈送到 GPIO 引脚，器件的唤醒行为将是不确定的并且在随后的唤醒脉冲中器件可能不会退出低功耗模式。
- F. 在延迟周期后，退出待机模式。
- G. 正常执行重新开始。器件将响应中断（如果启用）。
- H. 自执行将器件置于低功耗模式（LPM）的 IDLE 指令开始，至少经历 4 个 OSCCLK 周期后才启动唤醒。

**图 9-46. 待机进入和退出时序图**

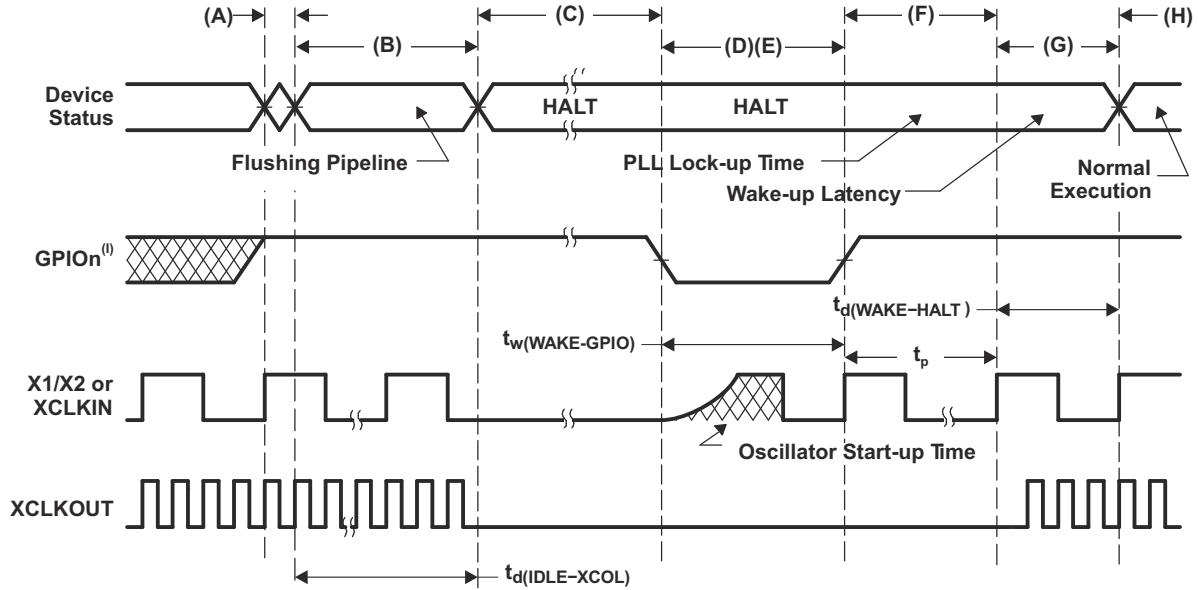
#### 9.9.10.1.4.5 HALT Mode Timing Requirements

|                         |                                     | MIN                                      | MAX | UNIT   |
|-------------------------|-------------------------------------|------------------------------------------|-----|--------|
| $t_w(\text{WAKE-GPIO})$ | Pulse duration, GPIO wake-up signal | $t_{\text{oscst}} + 2t_c(\text{OSCCLK})$ |     | cycles |
| $t_w(\text{WAKE-XRS})$  | Pulse duration, XRS wake-up signal  | $t_{\text{oscst}} + 8t_c(\text{OSCCLK})$ |     | cycles |

#### 9.9.10.1.4.6 停机模式开关特性

在推荐的运行条件下（除非另有说明）

| 参数                      |                                                                                 | 最小值                 | 最大值                   | 单位 |
|-------------------------|---------------------------------------------------------------------------------|---------------------|-----------------------|----|
| $t_d(\text{IDLE-XCOL})$ | 延迟时间，IDLE 指令执行到 XCLKOUT 低电平的时间                                                  | $32t_c(\text{SCO})$ | $45t_c(\text{SCO})$   | 周期 |
| $t_p$                   | PLL 锁存时间                                                                        |                     | 1                     | ms |
| $t_d(\text{WAKE-HALT})$ | 延迟时间，PLL 锁存到程序执行重新开始的时间                                                         |                     |                       |    |
|                         | <ul style="list-style-type: none"> <li>• 从闪存唤醒</li> <li>– 睡眠状态中的闪存模块</li> </ul> |                     | $1125t_c(\text{SCO})$ | 周期 |
|                         | <ul style="list-style-type: none"> <li>• 从 SARAM 中唤醒</li> </ul>                 |                     | $35t_c(\text{SCO})$   | 周期 |



- IDLE 指令被执行以将器件置于停机模式。
- PLL 块响应停机信号。在振荡器被关闭并且到内核的 CLKIN 被停止前 SYSCLKOUT 在下面所示的一定数量的周期内保持：
  - 当 DIVSEL=00 或 01 时，16 个周期
  - 当 DIVSEL=10 时，32 个周期
  - 当 DIVSEL=11 时，64 个周期

此延迟使得 CPU 流水线和其他待定操作适当清除。

- 到外设的时钟被关闭并且 PLL 被关断。如果一个石英晶振或者陶瓷谐振器被用作时钟源，内部振荡器也被关断。器件现在处于停机模式，消耗绝对最小功率。可在停机模式中保持零引脚内部振荡器 (INTOSC1 和 INTOSC2) 以及看门狗可用。可通过对 CLKCTL 寄存器中的适当位进行写入操作来实现此功能。
- 当 GPIO<sub>n</sub> 引脚 (用于使器件脱离停机模式) 被驱动为低电平时，振荡器开启并且振荡器唤醒序列被启动。只有当振荡器稳定时，GPIO 才应被驱动为高电平。这样可在 PLL 锁序列期间提供一个洁净的时钟信号。由于 GPIO 引脚的下降边沿会以异步方式开始唤醒过程，因此在进入停机模式之前和在此模式期间，应该注意保持低噪声环境。
- 为唤醒器件而馈送给 GPIO 引脚的唤醒信号必须符合最小脉冲宽度要求。此外，此信号不能有毛刺。如果噪声信号馈送到 GPIO 引脚，器件的唤醒行为将是不确定的并且在随后的唤醒脉冲中器件可能不会退出低功耗模式。
- 一旦振荡器已经稳定，PLL 锁序列被启动 (耗时 1ms)。
- 当到内核的 CLKIN 被启用时，在一个延迟后，此器件响应此中断 (如果被启用)。现在退出停机模式。
- 正常运行重新开始。
- 自执行将器件置于低功耗模式 (LPM) 的 IDLE 指令开始，至少经历 4 个 OSCCLK 周期后才启动唤醒。

图 9-47. 使用 GPIO<sub>n</sub> 唤醒停机模式

## 10 应用、实施和布局

### 备注

以下部分中的信息不属于 TI 器件规范，TI 不保证其准确性和完整性。TI 客户应负责确定这些元件是否适用于其应用。客户应验证并测试其设计实现，以确认系统功能。

### 10.1 TI 参考设计

TI 参考设计库是一个涵盖模拟、嵌入式处理器和连接的强大参考设计资源库。所有参考设计由 TI 专家构建，旨在帮助您快速开始系统设计，其中包括原理图或方框图、BOM 和设计文件，助您加快产品上市步伐。在[精选 TI 参考设计](#)页面上搜索并下载设计。

#### [具有响应时间小于 1us 的堵转电流限制的 36V/1kW 无刷直流电机驱动器参考设计](#)

此参考设计可用作电池供电式园艺工具和电动工具中无刷电机的功率级，额定功率高达 1kW，使用 10 节锂离子电池，电压范围为 36V 至 42V。设计采用 60V、N 沟道 NexFET™ 技术和 SON5x6 SMD 封装，具有极低的 1.8mΩ 漏源极电阻 (RDS\_ON)，可实现 57mm × 59mm 的小尺寸 PCB。三相栅极驱动器用于驱动三相 MOSFET 电桥，该电桥可在 6V 至 60V 的电压范围内工作，支持可编程栅极电流（最高 2.3A 灌电流/1.7A 拉电流）。C2000 F28027 LaunchPad™ 开发套件 ([LAUNCHXL-F28027](#)) 与此功率级结合使用，并在软件中通过霍尔传感器实现对 BLDC 电机的 120 度梯形控制。栅极驱动器的逐周期电流限制特性将功率级中允许的最大电流限制到安全级别，从而保护电路板免受电机失速期间导致的过流损害。

#### [使用磁通门传感器通过单端信号调节电路进行电流和电压测量](#)

此设计为集成在微控制器中通过磁通门传感器测量电机电流的单端 SAR ADC 提供 4 通道信号调节解决方案。此外还提供带有外部 SAR ADC 的备选测量电路以及高速过流和接地故障检测电路。适当的信号调节可在电机驱动中提高关键电路测量的抗噪性能。此参考设计有助于增加模数转换的有效分辨率，提高电机驱动效率。

## 11 器件和文档支持

### 11.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320 MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS320F28023**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

|            |                                                                                                                                      |
|------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <b>TMX</b> | Experimental device that is not necessarily representative of the final device's electrical specifications                           |
| <b>TMP</b> | Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification |
| <b>TMS</b> | Fully qualified production device                                                                                                    |

Support tool development evolutionary flow:

|             |                                                                                                         |
|-------------|---------------------------------------------------------------------------------------------------------|
| <b>TMDX</b> | Development-support product that has not yet completed Texas Instruments internal qualification testing |
| <b>TMDS</b> | Fully qualified development-support product                                                             |

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:  
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

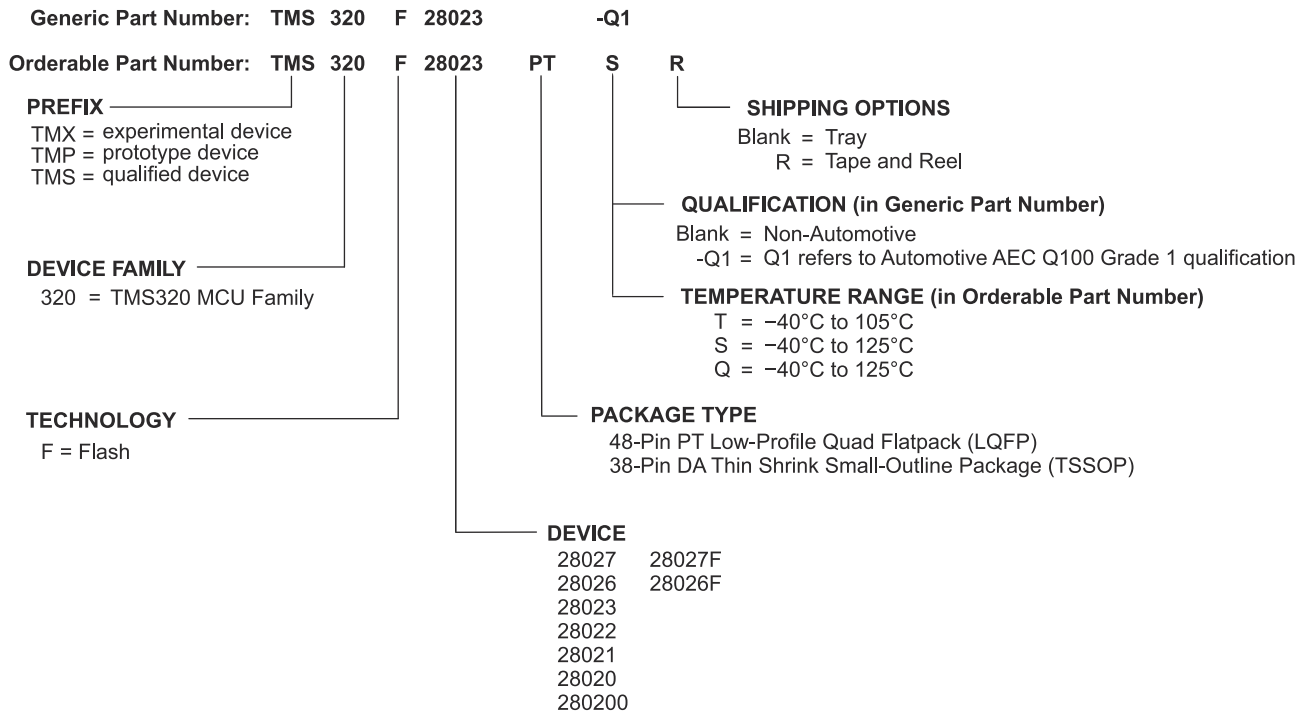
Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PT) and temperature range (for example, S). [图 11-1](#) provides a legend for reading the complete device name for any family member.

For device part numbers and further ordering information, see the TI website ([www.ti.com](http://www.ti.com)) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the [TMS320F2802x, TMS320F2802xx MCUs Silicon Errata](#).





A. For more information on peripheral, temperature, and package availability for a specific device, see [表 6-1](#).

**图 11-1. Device Nomenclature**

## 11.2 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below. To view all available tools and software for C2000™ real-time control MCUs, visit the [C2000 real-time control MCUs – Design & development](#) page.

### Development Tools

#### [Code Composer Studio \(CCS\) Integrated Development Environment \(IDE\) for C2000 Microcontrollers](#)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. CCS comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. CCS combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

#### [C2000 F28027 LaunchPad™ development kit](#)

The C2000 F28027 LaunchPad™ development kit is an inexpensive, modular, and fun evaluation platform, enabling you to dive into real-time, closed-loop control development with Texas Instruments' C2000 32-bit microcontroller family. This platform provides a great starting point for development of many common power electronics applications, including motor control, digital power supplies, solar inverters, digital LED lighting, precision sensing, and more.

To view all available C2000 LaunchPad development kits and BoosterPack™ plug-in modules, visit the [Embedded development hardware kits & boards](#) site.

### Software Tools

[powerSUITE - Digital Power Supply Design Software Tools for C2000™ MCUs](#)

powerSUITE is a suite of digital power supply design software tools for Texas Instruments' C2000 real-time microcontroller (MCU) family. powerSUITE helps power supply engineers drastically reduce development time as they design digitally-controlled power supplies based on C2000 real-time control MCUs.

#### [C2000Ware for C2000 MCUs](#)

C2000Ware for C2000™ microcontrollers is a cohesive set of development software and documentation designed to minimize software development time. From device-specific drivers and libraries to device peripheral examples, C2000Ware provides a solid foundation to begin development and evaluation of your product.

#### [UniFlash Standalone Flash Tool](#)

UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

#### **Models**

Various models are available for download from the product Tools & Software pages. These include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Models section of the Tools & Software page for each device.

#### **Training**

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the [C2000™ real-time control MCUs – Support & training](#) site.

Specific TMS320F2802x hands-on training resources can be found at [C2000™ MCU Device Workshops](#).

#### [InstaSPIN-FOC LaunchPad and BoosterPack](#)

This 6-part series provides information about the C2000 InstaSPIN-FOC Motor Control LaunchPad Development Kit and BoosterPack Plug-in Module.

The InstaSPIN-FOC enabled C2000 F28027 LaunchPad™ development kit is an inexpensive evaluation platform designed to help you leap right into the world of sensorless motor control using the InstaSPIN-FOC solution.

- [Part 1: Introduction and Overview](#)
- [Part 2: Identifying Your Motor](#)
- [Part 3: Zero Speed, Low Speed, & Tuning](#)
- [Part 4: Accelerations & Speed Reversals with Texas Instruments](#)
- [Part 5: High, Higher, Highest Speeds with Texas Instruments](#)
- [BOOSTXL-DRV8301 BoosterPack with Texas Instruments](#)

## 11.3 文档支持

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击右上角的 [通知我进行注册](#)，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

下面列出了介绍处理器、相关外设以及其他配套技术资料的最新文档。

### 勘误

[TMS320F2802x、TMS320F2802xx MCU 器件勘误表](#)介绍了器件上的已知问题并提供了权变措施。

### 技术参考手册

[TMS320F2802x、TMS320F2802xx 技术参考手册](#)详述了器件中每一个外设和子系统的集成、环境、功能说明，以及编程模型。

### InstaSPIN 技术参考手册

[InstaSPIN-FOC™ 和 InstaSPIN-MOTION™ 用户指南](#)介绍了 InstaSPIN-FOC 和 InstaSPIN-MOTION 器件。

[TMS320F28026F、TMS320F28027F InstaSPIN™-FOC 软件技术参考手册](#)介绍了 TMS320F28026F 和 TMS320F28027F InstaSPIN-FOC 软件。

### CPU 用户指南

[TMS320C28x CPU 和指令集参考指南](#)描述了 TMS320C28x 定点数字信号处理器 (DSP) 的中央处理器 (CPU) 和汇编语言指令。此参考指南还介绍了上述 DSP 所提供的仿真特性。

### 外设指南

[C2000 实时控制外设参考指南](#)介绍了 28x 数字信号处理器 (DSP) 的外设参考指南。

### 工具指南

[TMS320C28x 汇编语言工具 v20.2.0.LTS 用户指南](#)介绍了用于 TMS320C28x 器件的汇编语言工具 (用于开发汇编语言代码的汇编器和其他工具)、汇编器指令、宏、通用目标文件格式和符号调试指令。

[TMS320C28x 优化 C/C++ 编译器 v20.2.0.LTS 用户指南](#)介绍了 TMS320C28x C/C++ 编译器。此编译器接受 ANSI 标准 C/C++ 源代码，并为 TMS320C28x 器件生成 TMS320 DSP 汇编语言源代码。

### 应用报告

[半导体封装方法](#)介绍了准备半导体器件以发货给最终用户时所用的封装方法。

[计算嵌入式处理器的有效使用寿命](#)介绍了如何计算 TI 嵌入式处理器 (EP) 在电子系统中运行时的有效使用寿命。本文档的目标读者为希望确定 TI EP 的可靠性是否符合终端系统可靠性要求的总工程师。

[半导体和 IC 封装热指标](#)介绍了以前和更新的热指标，并将它们应用于系统级结温估算。

[计算任务剖面的 FIT](#)说明了如何使用 TI 的可靠性降额工具计算系统任务剖面在加电条件下的元件级 FIT。

[振荡器补偿指南](#)介绍了一种为内部振荡器补偿温度引起的频率漂移的工厂方法。

[IBIS \(I/O 缓冲器信息规范\) 建模简介](#)讨论了 IBIS 的各个方面，包括其历史、优势、兼容性、模型生成流程、输入/输出结构建模中的数据要求以及未来趋势。

[C2000™ 微控制器串行闪存编程](#)讨论了如何使用闪存内核和 ROM 加载程序对器件进行串行编程。

## 11.4 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

## 11.5 商标

InstaSPIN-FOC™, TMS320C2000™, NexFET™, LaunchPad™, TMS320™, BoosterPack™, InstaSPIN-MOTION™, and TI E2E™ are trademarks of Texas Instruments.

I2C 总线® is a registered trademark of NXP B.V. Corporation.

所有商标均为其各自所有者的财产。

## 11.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序, 可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级, 大至整个器件故障。精密的集成电路可能更容易受到损坏, 这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.7 术语表

**TI 术语表**      本术语表列出并解释了术语、首字母缩略词和定义。

## 12 机械、封装和可订购信息

### 12.1 封装信息

下述页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的基于浏览器的版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier      | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)            |
|----------------------------------|---------------|----------------------|-----------------|----------------------------|-------------|--------------------------------------|-----------------------------------|--------------|--------------------------------|
| <a href="#">TMS320F280200DAS</a> | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F280200DAS<br>S320             |
| TMS320F280200DAS.A               | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F280200DAS<br>S320             |
| TMS320F280200DAS.B               | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F280200DAS<br>S320             |
| <a href="#">TMS320F280200DAT</a> | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | F280200DAT<br>S320             |
| TMS320F280200DAT.A               | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F280200DAT<br>S320             |
| TMS320F280200DAT.B               | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F280200DAT<br>S320             |
| <a href="#">TMS320F280200PTT</a> | Active        | Production           | LQFP (PT)   48  | 250   JEDEC<br>TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | (S320, S320 980)<br>F280200PTT |
| TMS320F280200PTT.A               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC<br>TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F280200PTT |
| TMS320F280200PTT.B               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC<br>TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F280200PTT |
| <a href="#">TMS320F28020DAS</a>  | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28020DAS<br>S320              |
| TMS320F28020DAS.A                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28020DAS<br>S320              |
| TMS320F28020DAS.B                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28020DAS<br>S320              |
| <a href="#">TMS320F28020DAT</a>  | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | F28020DAT<br>S320              |
| TMS320F28020DAT.A                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28020DAT<br>S320              |
| TMS320F28020DAT.B                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28020DAT<br>S320              |
| <a href="#">TMS320F28020PTS</a>  | Active        | Production           | LQFP (PT)   48  | 250   JEDEC<br>TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28020PTS  |

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|---------------------------------|---------------|----------------------|-----------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| TMS320F28020PTS.A               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28020PTS |
| TMS320F28020PTS.B               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28020PTS |
| <a href="#">TMS320F28020PTT</a> | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | (S320, S320 980)<br>F28020PTT |
| TMS320F28020PTT.A               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28020PTT |
| TMS320F28020PTT.B               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28020PTT |
| <a href="#">TMS320F28021DAS</a> | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28021DAS<br>S320             |
| TMS320F28021DAS.A               | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28021DAS<br>S320             |
| TMS320F28021DAS.B               | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28021DAS<br>S320             |
| <a href="#">TMS320F28021DAT</a> | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | F28021DAT<br>S320             |
| TMS320F28021DAT.A               | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28021DAT<br>S320             |
| TMS320F28021DAT.B               | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28021DAT<br>S320             |
| <a href="#">TMS320F28021PTS</a> | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28021PTS |
| TMS320F28021PTS.A               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28021PTS |
| TMS320F28021PTS.B               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28021PTS |
| <a href="#">TMS320F28021PTT</a> | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | (S320, S320 980)<br>F28021PTT |
| TMS320F28021PTT.A               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28021PTT |
| TMS320F28021PTT.B               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28021PTT |

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier      | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|----------------------------------|---------------|----------------------|-----------------|----------------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| <a href="#">TMS320F28022DAQ</a>  | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAQ<br>S320             |
| TMS320F28022DAQ.A                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAQ<br>S320             |
| TMS320F28022DAQ.B                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAQ<br>S320             |
| <a href="#">TMS320F28022DAQR</a> | Active        | Production           | TSSOP (DA)   38 | 2000   LARGE T&R           | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAQ<br>S320             |
| TMS320F28022DAQR.A               | Active        | Production           | TSSOP (DA)   38 | 2000   LARGE T&R           | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAQ<br>S320             |
| TMS320F28022DAQR.B               | Active        | Production           | TSSOP (DA)   38 | 2000   LARGE T&R           | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAQ<br>S320             |
| <a href="#">TMS320F28022DAS</a>  | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAS<br>S320             |
| TMS320F28022DAS.A                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAS<br>S320             |
| TMS320F28022DAS.B                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAS<br>S320             |
| <a href="#">TMS320F28022DAT</a>  | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | F28022DAT<br>S320             |
| TMS320F28022DAT.A                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAT<br>S320             |
| TMS320F28022DAT.B                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE                  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28022DAT<br>S320             |
| <a href="#">TMS320F28022PTQ</a>  | Active        | Production           | LQFP (PT)   48  | 250   JEDEC<br>TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28022PTQ |
| TMS320F28022PTQ.A                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC<br>TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28022PTQ |
| TMS320F28022PTQ.B                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC<br>TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28022PTQ |
| <a href="#">TMS320F28022PTS</a>  | Active        | Production           | LQFP (PT)   48  | 250   JEDEC<br>TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28022PTS |
| TMS320F28022PTS.A                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC<br>TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28022PTS |



| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)        |
|---------------------------------|---------------|----------------------|-----------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------|
| TMS320F28022PTS.B               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28022PTS |
| <a href="#">TMS320F28022PTT</a> | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | Call TI   Nipdau                     | Level-2-260C-1 YEAR               | -40 to 105   | S320 980 F28022PTT         |
| TMS320F28022PTT.A               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | Call TI                              | Level-2-260C-1 YEAR               | -40 to 125   | S320 980 F28022PTT         |
| TMS320F28022PTT.B               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | Call TI                              | Level-2-260C-1 YEAR               | -40 to 125   | S320 980 F28022PTT         |
| <a href="#">TMS320F28023DAS</a> | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28023DAS S320             |
| TMS320F28023DAS.A               | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28023DAS S320             |
| TMS320F28023DAS.B               | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28023DAS S320             |
| <a href="#">TMS320F28023DAT</a> | Active        | Production           | TSSOP (DA)   38 | 40   JEDEC TRAY (5+1)   | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | F28023DAT S320             |
| TMS320F28023DAT.A               | Active        | Production           | TSSOP (DA)   38 | 40   JEDEC TRAY (5+1)   | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28023DAT S320             |
| TMS320F28023DAT.B               | Active        | Production           | TSSOP (DA)   38 | 40   JEDEC TRAY (5+1)   | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28023DAT S320             |
| <a href="#">TMS320F28023PTQ</a> | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | Call TI   Nipdau                     | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28023PTQ |
| TMS320F28023PTQ.A               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | Call TI                              | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28023PTQ |
| TMS320F28023PTQ.B               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | Call TI                              | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28023PTQ |
| <a href="#">TMS320F28023PTS</a> | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28023PTS |
| TMS320F28023PTS.A               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28023PTS |
| TMS320F28023PTS.B               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28023PTS |
| <a href="#">TMS320F28023PTT</a> | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | (S320, S320 980) F28023PTT |

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|----------------------------------|---------------|----------------------|-----------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| TMS320F28023PTT.A                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28023PTT |
| TMS320F28023PTT.B                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28023PTT |
| <a href="#">TMS320F28026DAS</a>  | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28026DAS<br>S320             |
| TMS320F28026DAS.A                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28026DAS<br>S320             |
| TMS320F28026DAS.B                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28026DAS<br>S320             |
| <a href="#">TMS320F28026DAT</a>  | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | F28026DAT<br>S320             |
| TMS320F28026DAT.A                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28026DAT<br>S320             |
| TMS320F28026DAT.B                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28026DAT<br>S320             |
| <a href="#">TMS320F28026FPTT</a> | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | S320 980<br>F28026FPTT        |
| TMS320F28026FPTT.A               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | S320 980<br>F28026FPTT        |
| TMS320F28026FPTT.B               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | S320 980<br>F28026FPTT        |
| <a href="#">TMS320F28026PTQ</a>  | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | Call TI   Nipdau                     | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28026PTQ |
| TMS320F28026PTQ.A                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | Call TI                              | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28026PTQ |
| TMS320F28026PTQ.B                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | Call TI                              | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28026PTQ |
| <a href="#">TMS320F28026PTS</a>  | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28026PTS |
| TMS320F28026PTS.A                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28026PTS |
| TMS320F28026PTS.B                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28026PTS |

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|----------------------------------|---------------|----------------------|-----------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| <a href="#">TMS320F28026PTT</a>  | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | (S320, S320 980)<br>F28026PTT |
| TMS320F28026PTT.A                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28026PTT |
| TMS320F28026PTT.B                | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28026PTT |
| <a href="#">TMS320F28027DAS</a>  | Active        | Production           | TSSOP (DA)   38 | 40   JEDEC TRAY (5+1)   | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28027DAS<br>S320             |
| TMS320F28027DAS.A                | Active        | Production           | TSSOP (DA)   38 | 40   JEDEC TRAY (5+1)   | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28027DAS<br>S320             |
| TMS320F28027DAS.B                | Active        | Production           | TSSOP (DA)   38 | 40   JEDEC TRAY (5+1)   | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28027DAS<br>S320             |
| <a href="#">TMS320F28027DASR</a> | Active        | Production           | TSSOP (DA)   38 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28027DAS<br>S320             |
| TMS320F28027DASR.A               | Active        | Production           | TSSOP (DA)   38 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28027DAS<br>S320             |
| TMS320F28027DASR.B               | Active        | Production           | TSSOP (DA)   38 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28027DAS<br>S320             |
| <a href="#">TMS320F28027DAT</a>  | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | F28027DAT<br>S320             |
| TMS320F28027DAT.A                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28027DAT<br>S320             |
| TMS320F28027DAT.B                | Active        | Production           | TSSOP (DA)   38 | 40   TUBE               | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28027DAT<br>S320             |
| <a href="#">TMS320F28027DATR</a> | Active        | Production           | TSSOP (DA)   38 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | F28027DAT<br>S320             |
| TMS320F28027DATR.A               | Active        | Production           | TSSOP (DA)   38 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28027DAT<br>S320             |
| TMS320F28027DATR.B               | Active        | Production           | TSSOP (DA)   38 | 2000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | F28027DAT<br>S320             |
| <a href="#">TMS320F28027FPTQ</a> | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320<br>F28027FPTQ            |
| TMS320F28027FPTQ.A               | Active        | Production           | LQFP (PT)   48  | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320<br>F28027FPTQ            |

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|-----------------------------------|---------------|----------------------|----------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| TMS320F28027FPTQ.B                | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320<br>F28027FPTQ            |
| <a href="#">TMS320F28027FPTT</a>  | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | S320 980<br>F28027FPTT        |
| TMS320F28027FPTT.A                | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | S320 980<br>F28027FPTT        |
| TMS320F28027FPTT.B                | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | S320 980<br>F28027FPTT        |
| <a href="#">TMS320F28027FPTTR</a> | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | S320 980<br>F28027FPTT        |
| TMS320F28027FPTTR.A               | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | S320 980<br>F28027FPTT        |
| TMS320F28027FPTTR.B               | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | S320 980<br>F28027FPTT        |
| <a href="#">TMS320F28027PTQ</a>   | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28027PTQ |
| TMS320F28027PTQ.A                 | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28027PTQ |
| TMS320F28027PTQ.B                 | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28027PTQ |
| <a href="#">TMS320F28027PTQR</a>  | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320<br>F28027PTQ             |
| TMS320F28027PTQR.A                | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320<br>F28027PTQ             |
| TMS320F28027PTQR.B                | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320<br>F28027PTQ             |
| <a href="#">TMS320F28027PTR</a>   | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | S320<br>F28027PTT             |
| TMS320F28027PTR.A                 | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320<br>F28027PTT             |
| TMS320F28027PTR.B                 | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R        | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320<br>F28027PTT             |
| <a href="#">TMS320F28027PTS</a>   | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980)<br>F28027PTS |

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier   | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)        |
|---------------------------------|---------------|----------------------|----------------|-------------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------|
| TMS320F28027PTS.A               | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28027PTS |
| TMS320F28027PTS.B               | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28027PTS |
| TMS320F28027PTSG4               | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320 F28027PTS             |
| TMS320F28027PTSG4.A             | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320 F28027PTS             |
| TMS320F28027PTSG4.B             | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320 F28027PTS             |
| <a href="#">TMS320F28027PTT</a> | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 105   | (S320, S320 980) F28027PTT |
| TMS320F28027PTT.A               | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28027PTT |
| TMS320F28027PTT.B               | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | (S320, S320 980) F28027PTT |
| TMS320F28027PTTG4               | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320 F28027PTT             |
| TMS320F28027PTTG4.A             | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320 F28027PTT             |
| TMS320F28027PTTG4.B             | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (5+1)  | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | S320 F28027PTT             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TMS320F28022, TMS320F28022-Q1, TMS320F28023, TMS320F28023-Q1, TMS320F28026, TMS320F28026-Q1, TMS320F28027, TMS320F28027-Q1, TMS320F28027F, TMS320F28027F-Q1 :**

- Catalog : [TMS320F28022](#), [TMS320F28023](#), [TMS320F28026](#), [TMS320F28027](#), [TMS320F28027F](#)
- Automotive : [TMS320F28022-Q1](#), [TMS320F28023-Q1](#), [TMS320F28026-Q1](#), [TMS320F28027-Q1](#), [TMS320F28027F-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

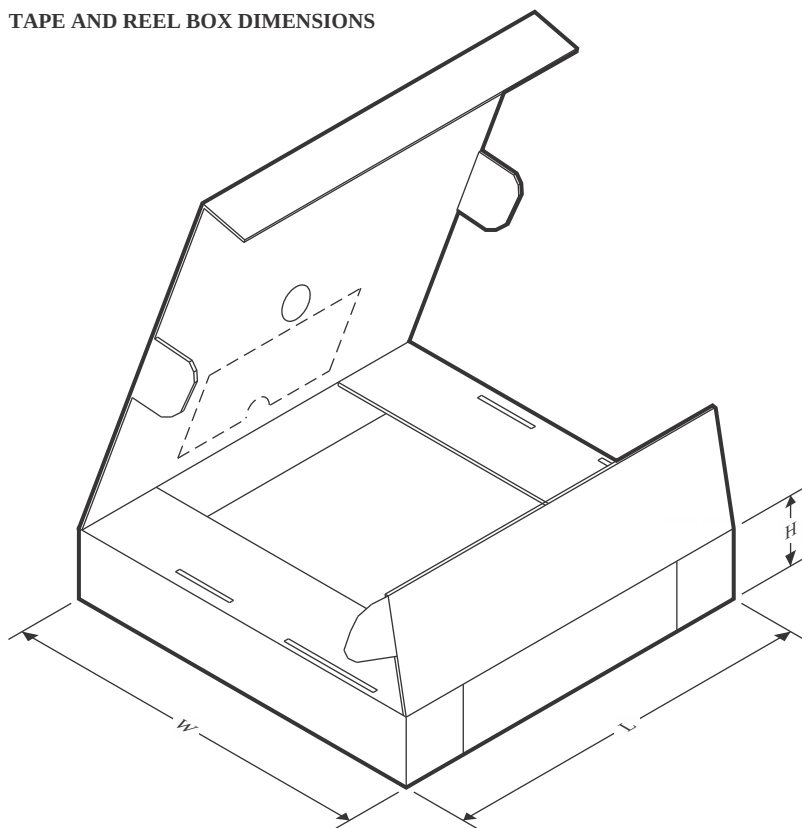
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TMS320F28022DAQR | TSSOP        | DA              | 38   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| TMS320F28027DASR | TSSOP        | DA              | 38   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| TMS320F28027DATR | TSSOP        | DA              | 38   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| TMS320F28027PTR  | LQFP         | PT              | 48   | 1000 | 330.0              | 16.4               | 9.6     | 9.6     | 1.9     | 12.0    | 16.0   | Q2            |

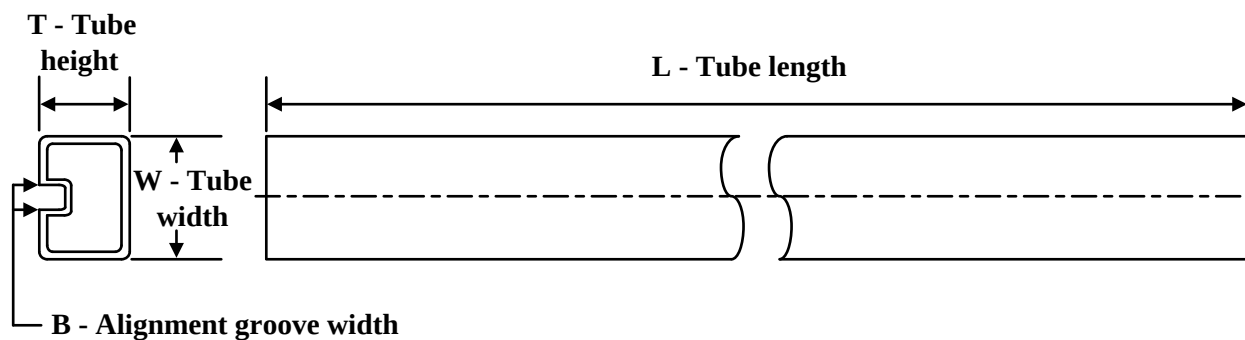
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TMS320F28022DAQR | TSSOP        | DA              | 38   | 2000 | 350.0       | 350.0      | 43.0        |
| TMS320F28027DASR | TSSOP        | DA              | 38   | 2000 | 350.0       | 350.0      | 43.0        |
| TMS320F28027DATR | TSSOP        | DA              | 38   | 2000 | 350.0       | 350.0      | 43.0        |
| TMS320F28027PTR  | LQFP         | PT              | 48   | 1000 | 350.0       | 350.0      | 43.0        |



**TUBE**


\*All dimensions are nominal

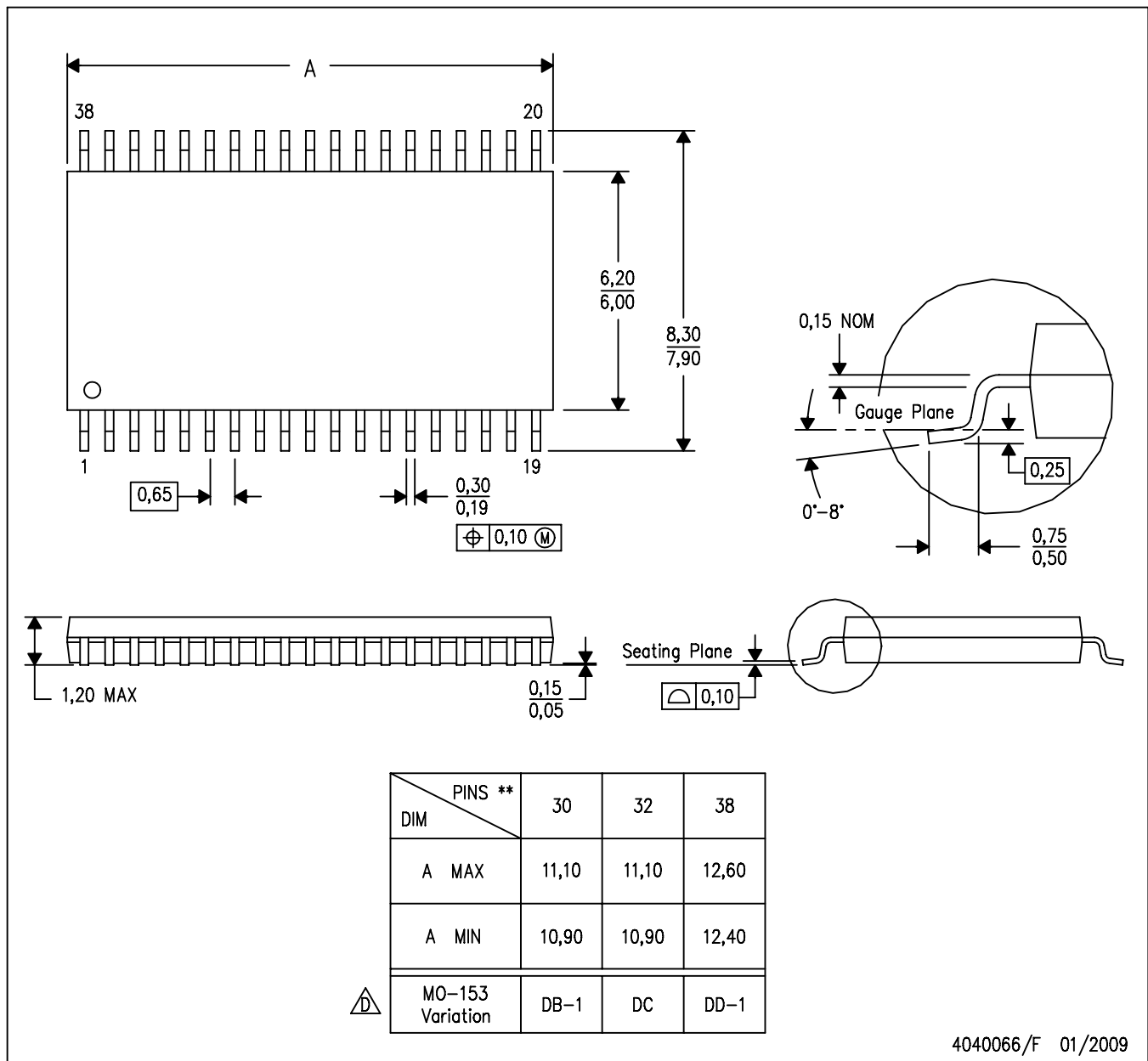
| Device             | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TMS320F280200DAS   | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F280200DAS.A | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F280200DAS.B | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F280200DAT   | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F280200DAT.A | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F280200DAT.B | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28020DAS    | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28020DAS.A  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28020DAS.B  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28020DAT    | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28020DAT.A  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28020DAT.B  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28021DAS    | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28021DAS.A  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28021DAS.B  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28021DAT    | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28021DAT.A  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28021DAT.B  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28022DAQ    | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28022DAQ.A  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28022DAQ.B  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28022DAS    | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28022DAS.A  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28022DAS.B  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28022DAT    | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28022DAT.A  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28022DAT.B  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28023DAS    | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28023DAS.A  | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |

| Device            | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TMS320F28023DAS.B | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28023DAT   | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28023DAT.A | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28023DAT.B | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28026DAS   | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28026DAS.A | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28026DAS.B | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28026DAT   | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28026DAT.A | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28026DAT.B | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28027DAS   | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28027DAS.A | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28027DAS.B | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28027DAT   | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28027DAT.A | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |
| TMS320F28027DAT.B | DA           | TSSOP        | 38   | 40  | 530    | 11.89  | 3600   | 4.9    |

DA (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

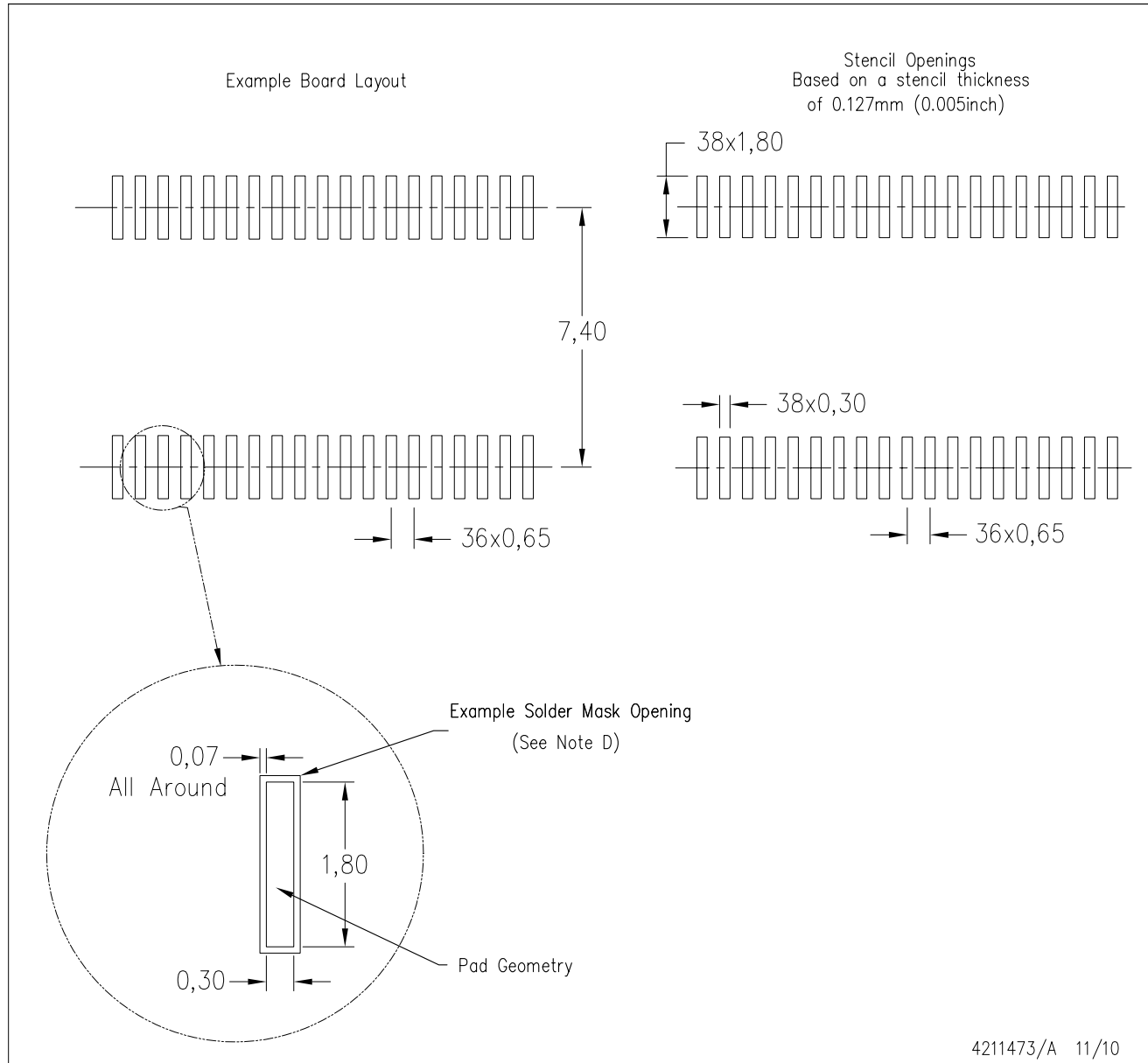
38 PIN SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-153, except 30 pin body length.

DA (R-PDSO-G38)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - D. Contact the board fabrication site for recommended soldermask tolerances.



**LQFP - 1.6 mm max height**

Technical drawing of a square electronic component, likely a microchip, showing dimensions and feature callouts.

**Top View Dimensions:**

- Overall width: 9.2
- Overall height: 9.2
- Distance from top edge to center of top pins: 8.8
- Distance from left edge to center of left pins: 7.2
- Distance from right edge to center of right pins: 6.8
- Distance from bottom edge to center of bottom pins: 7.2
- Distance from left edge to center of left pins: 6.8

**Pin Dimensions:**

- Pin pitch: 0.5
- Pin width: 0.17
- Pin height: 0.27
- Pin length: 44X
- Pin spacing: 4X 5.5

**Feature Callouts:**

- SEE DETAIL A:** Points to a circular feature on the top surface.
- 1.6 MAX:** Dimension for the circular feature.
- SEATING PLANE:** Dimension for the bottom surface.
- 0.1 C:** Dimension for the bottom surface.
- 0.08 M C A B:** Dimension for the bottom surface.
- 0.25 GAGE PLANE:** Dimension for the bottom surface.
- 0.75 0.45:** Dimension for the bottom surface.
- 1.45 1.35:** Dimension for the bottom surface.
- 0.05 MIN:** Dimension for the bottom surface.
- 0° - 7°:** Angle for the bottom surface.

**DETAIL A:** A circular feature on the top surface, likely a mounting hole or a test point.

NOTES:

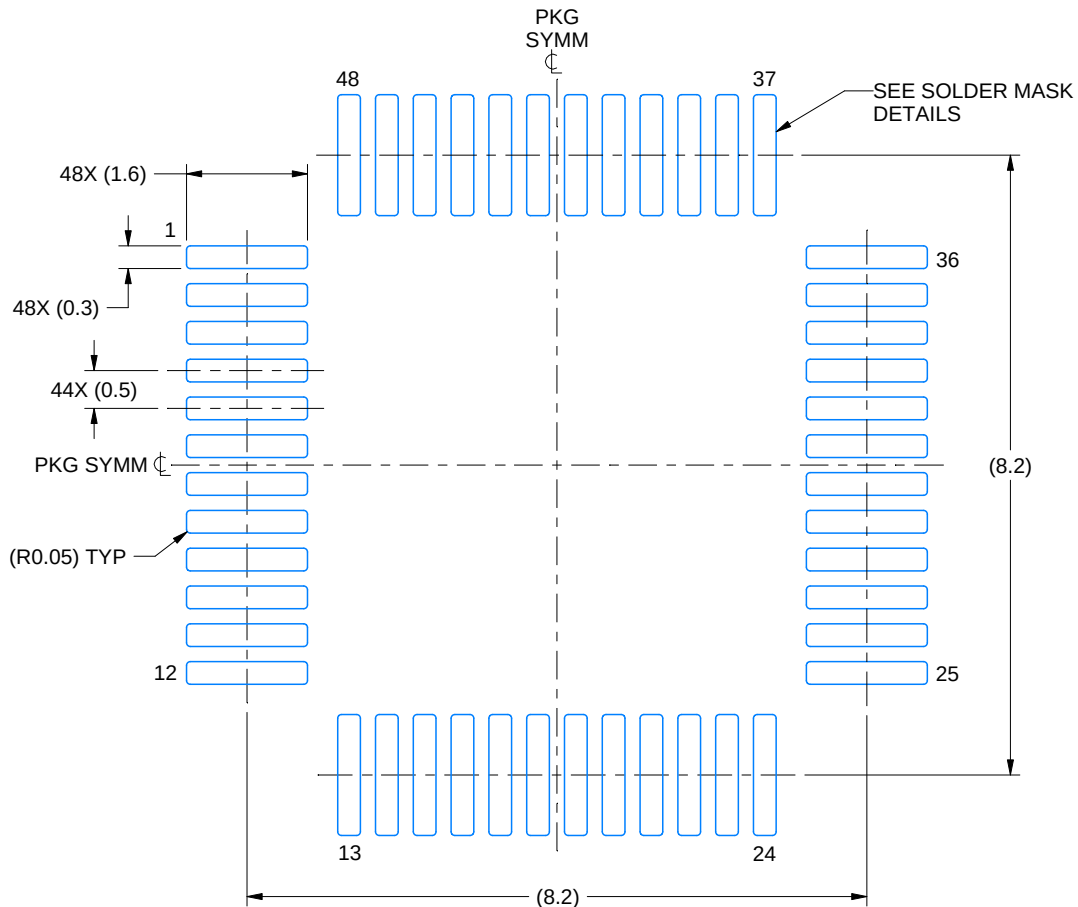
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads connected to the die pads.

# EXAMPLE BOARD LAYOUT

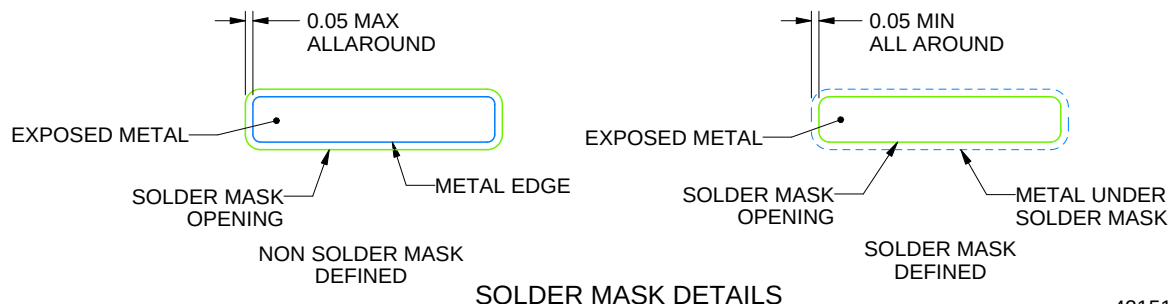
PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE 10.000



4215159/B 11/2023

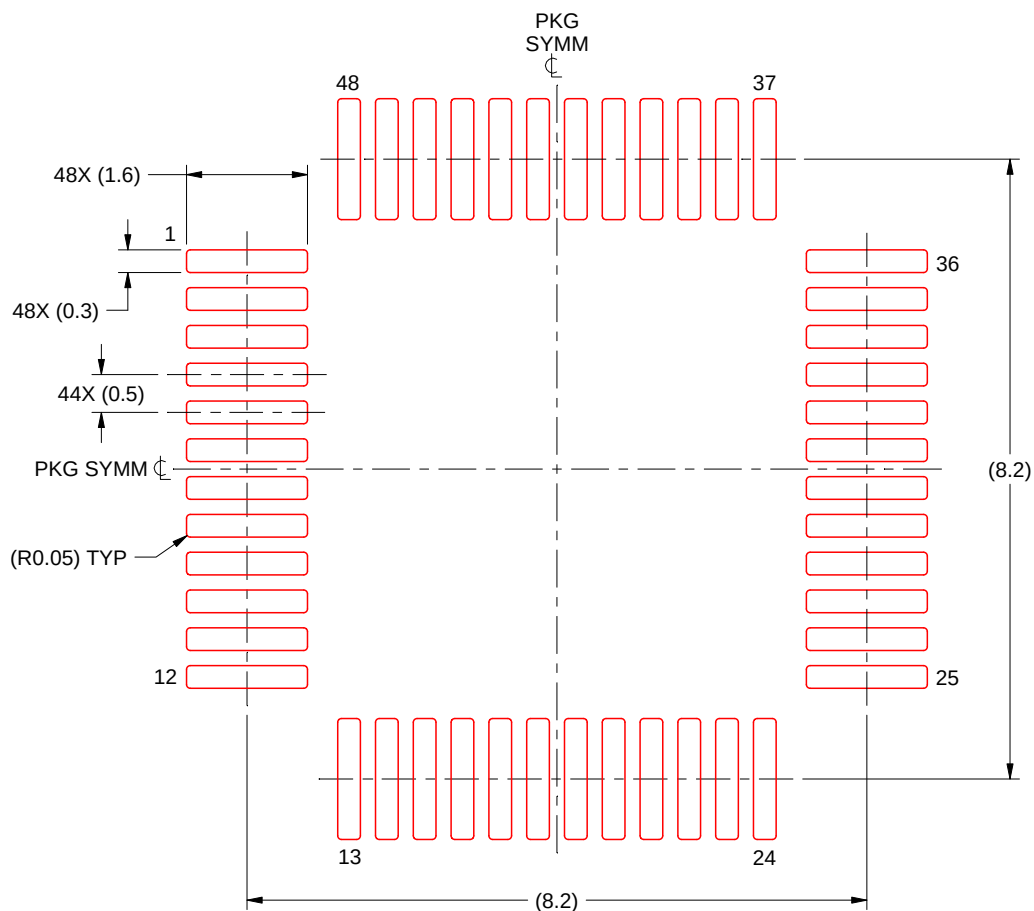
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PT0048A

**LQFP - 1.6 mm max height**

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月