TLV906xS 适用于成本敏感型系统的 10MHz、RRIO、CMOS 运算放大器

1 特性

- 轨到轨输入和输出
- 低输入失调电压：±0.3mV
- 单位增益带宽：10MHz
- 低宽带噪声：10nV/ √Hz
- 低输入偏置电流：0.5pA
- 低静态电流：538µA
- 单位增益稳定
- 内置 RFI 和 EMI 滤波器
- 可在电源电压低至 1.8V 的情况下运行
- 由于具有电阻式开环输出阻抗，因此在较高的电容性负载下更易稳定
- 关断版本：TLV906xS
- 工作温度范围：-40°C 至 125°C

2 应用

- 电动自行车
- 烟雾探测器
- HVAC：暖通空调
- 电机控制：交流感应
- 冰箱
- 可穿戴设备
- 笔记本电脑
- 洗衣机
- 传感器信号调节
- 电源模块
- 条形码扫描仪
- 有源滤波器
- 低侧电流检测

3 说明

TLV9061（单通道）、TLV9062（双通道）和 TLV9064（四通道）是低压、1.8V 至 5.5V、运算放大器，具有轨到轨输入和输出摆幅能力。

这些器件具有高成本效益，适用于需要低压运行、小型封装和高容性负载驱动能力的应用。

虽然 TLV906x 的容性负载驱动能力为 100pF，但电阻式开环输出阻抗便于在更高的容性负载下更轻松地实现稳定。此类运算放大器专为低工作电压（1.8V 至 5.5V）而设计，性能规格类似于 OPAx316 和 TLVx316 器件。

TLV906xS 器件具有关断模式，允许放大器切换至典型电流消耗低于 1µA 的待机模式。

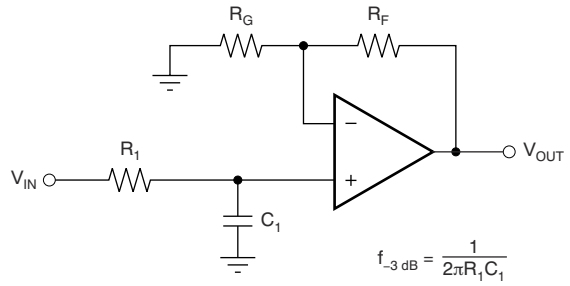
TLV906xS 系列有助于简化系统设计，因为该系列具有稳定的单位增益，集成了 RFI 和 EMI 抑制滤波器，而且在过驱条件下不会出现相位反转。

除了业内通用封装（如 SOIC、MSOP、SOT-23 和 TSSOP），还针对所有通道类型（单通道、双通道和四通道）提供了*微型*封装（如 X2SON 和 X2QFN）。

器件信息

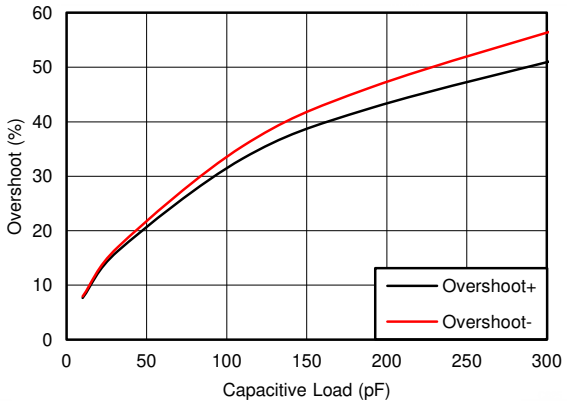
器件型号(3)	封装(1)	本体尺寸（标称值）(4)
TLV9061	DBV（SOT-23，5）	2.90mm × 1.60mm
	DCK（SC70，5）	2.00mm × 1.25mm
	DRL（SOT-553，5）(2)	1.60mm × 1.20mm
	DPW（X2SON，5）	0.80mm × 0.80mm
TLV9061S	DBV（SOT-23，6）	2.90mm × 1.60mm
	DRY（USON，6）	1.45mm × 1.00mm
TLV9062	D（SOIC，8）	4.90mm × 3.90mm
	PW（TSSOP，8）	3.00mm × 4.40mm
	DGK（VSSOP，8）	3.00mm × 3.00mm
	DDF（SOT-23，8）	2.90mm × 1.60mm
	DSG（WSON，8）	2.00mm × 2.00mm
TLV9062S	DGS（VSSOP，10）	3.00mm × 3.00mm
	RUG（X2QFN，10）	2.00mm × 1.50mm
	YCK（DSBGA，9）	1.00mm x 1.00mm
TLV9064	D（SOIC，14）	8.65mm × 3.90mm
	PW（TSSOP，14）	5.00mm × 4.40mm
	RTE（WQFN，16）	3.00mm × 3.00mm
	RUC（X2QFN，14）	2.00mm × 2.00mm
TLV9064S	RTE（WQFN，16）	3.00mm × 3.00mm

(1) 有关所有可用封装，请参阅节 10。
(2) 封装仅为预发布状态。
(3) 请参阅*器件比较*。
(4) 本体尺寸（长 × 宽）为标称值，不包括引脚。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

单极低通滤波器



小信号过冲与负载电容间的关系

内容

器件比较表

器件	通道数量	封装引线														
		SOIC D	USON DRY	SOT-23 DBV	SC-70 DCK	VSSOP DGK	VSSOP DGS	DSBGA YCK	X2SON DPW	SOT-553 DRL	WSON DSG	TSSOP PW	SOT-23 DDF	WQFN RTE	X2QFN RUC	X2QFN RUG
TLV9061	1	8	—	5	5	—	—	—	5	5	—	—	—	—	—	—
TLV9061S		—	6	6	—	—	—	—	—	—	—	—	—	—	—	—
TLV9062	2	8	—	—	—	8	10	—	—	—	8	8	8	—	—	—
TLV9062S		—	—	—	—	—	10	9	—	—	—	—	—	—	—	10
TLV9064	4	14	—	—	—	—	—	—	—	—	—	14	—	16	14	—
TLV9064S		—	—	—	—	—	—	—	—	—	—	—	—	16	—	—

4 引脚配置和功能

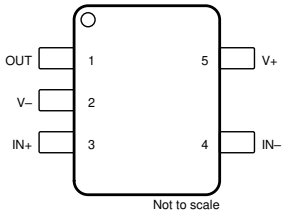


图 4-1. TLV9061 DBV 或 DRL 封装，5 引脚 SOT-23 或 SOT-553（顶视图）

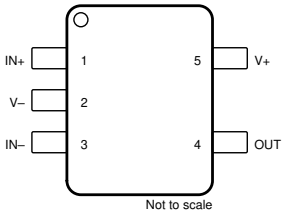


图 4-2. TLV9061 DCK 封装，5 引脚 SC70（顶视图）

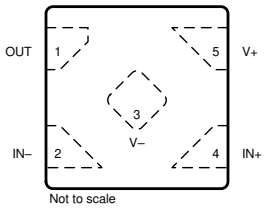


图 4-3. TLV9061 DPW 封装，5 引脚 X2SON（顶视图）

表 4-1. 引脚功能：TLV9061

引脚				类型(1)	说明
名称	SOT-23、SOT-553	SC70	X2SON		
IN –	4	3	2	I	反相输入
IN+	3	1	4	I	同相输入
OUT	1	4	1	O	输出
V –	2	2	3	I 或 —	负（低）电源或接地（对于单电源供电）
V+	5	5	5	I	正（高）电源

(1) I = 输入，O = 输出

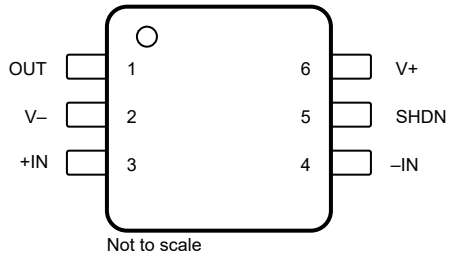


图 4-4. TLV9061S DBV 封装，6 引脚 SOT-23（顶视图）

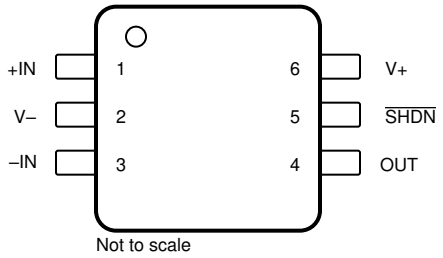


图 4-5. TLV9061S DRY 封装，6 引脚 USON（顶视图）

表 4-2. 引脚功能：TLV9061S

引脚			类型(1)	说明
名称	SOT-23	USON		
IN –	4	3	I	反相输入
IN+	3	1	I	同相输入
OUT	1	4	O	输出
$\overline{SHDN}$	5	5	I	关断：低电平 = 禁用放大器，高电平 = 启用放大器。有关更多信息，请参阅*关断功能*。
V –	2	2	I 或 —	负（低）电源或接地（对于单电源供电）
V+	6	6	I	正（高）电源

(1) I = 输入，O = 输出

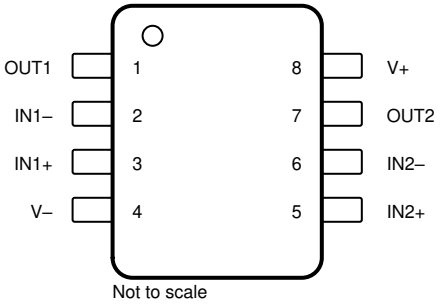
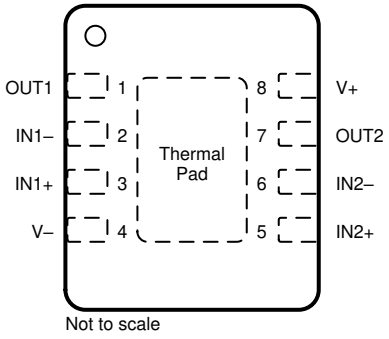


图 4-6. TLV9062 D，DGK、PW、DDF 封装 8 引脚 SOIC、VSSOP、TSSOP、SOT-23 顶视图



A. 将散热焊盘连接至 V –

图 4-7. TLV9062 DSG 封装，8 引脚 WSON（带有外露散热焊盘）（顶视图）

表 4-3. 引脚功能：TLV9062

引脚		类型(1)	说明
名称	编号		
IN1 –	2	I	反相输入，通道 1
IN1+	3	I	同相输入，通道 1
IN2 –	6	I	反相输入，通道 2
IN2+	5	I	同相输入，通道 2
OUT1	1	O	输出，通道 1
OUT2	7	O	输出，通道 2
V –	4	—	负（最低）电源或接地（对于单电源供电）

表 4-3. 引脚功能：TLV9062（续）

引脚		类型(1)	说明
名称	编号		
V+	8	—	正（最高）电源

(1) I = 输入，O = 输出

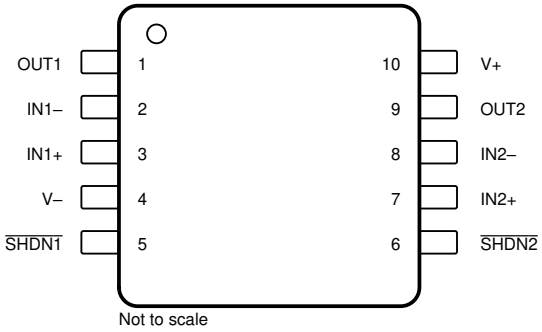


图 4-8. TLV9062S DGS 封装，10 引脚 VSSOP（顶视图）

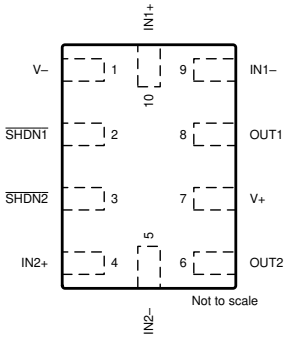


图 4-9. TLV9062S RUG 封装，10 引脚 X2QFN（顶视图）

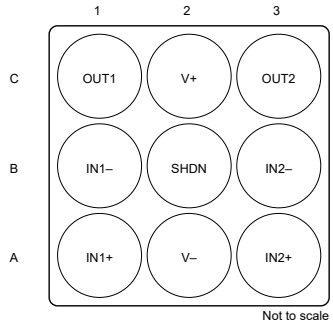


图 4-10. TLV9062S YCK 封装
9 引脚 DSBGA (WCSP)
底视图

表 4-4. 引脚功能：TLV9062S

引脚				I/O	说明
名称	VSSOP	X2QFN	DSBGA (WCSP)		
IN1 –	2	9	B1	I	反相输入，通道 1
IN1+	3	10	A1	I	同相输入，通道 1
IN2 –	8	5	B3	I	反相输入，通道 2
IN2+	7	4	A3	I	同相输入，通道 2
OUT1	1	8	C1	O	输出，通道 1
OUT2	9	6	C3	O	输出，通道 2
$\overline{\text{SHDN1}}$	5	2	—	I	关断：低 = 禁用放大器，高 = 启用放大器，通道 1。有关更多信息，请参阅*关断功能*。
$\overline{\text{SHDN2}}$	6	3	—	I	关断：低 = 禁用放大器，高 = 启用放大器，通道 1。有关更多信息，请参阅*关断功能*。

表 4-4. 引脚功能：TLV9062S（续）

引脚				I/O	说明
名称	VSSOP	X2QFN	DSBGA (WCSP)		
$\overline{SHDN}$	—	—	B2		关断：低 = 禁用两个放大器，高 = 启用两个放大器
V –	4	1	A2	I 或 —	负（低）电源或接地（对于单电源供电）
V+	10	7	C2	I	正（高）电源

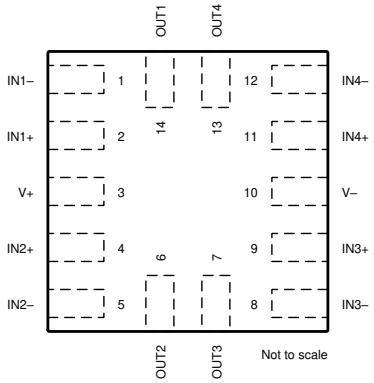
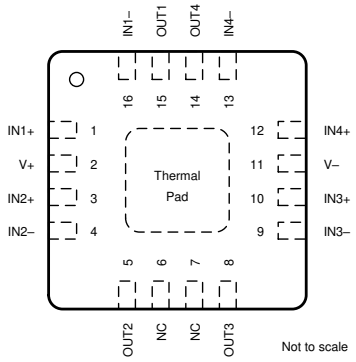


图 4-11. TLV9064 RUC 封装， 14 引脚 X2QFN （顶视图）



A. 将散热焊盘连接至 V –

图 4-12. TLV9064 RTE 封装， 16 引脚 WQFN（带有外露散热焊盘）（顶视图）

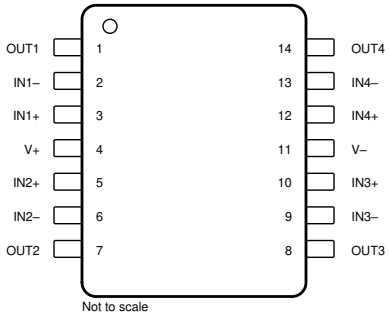
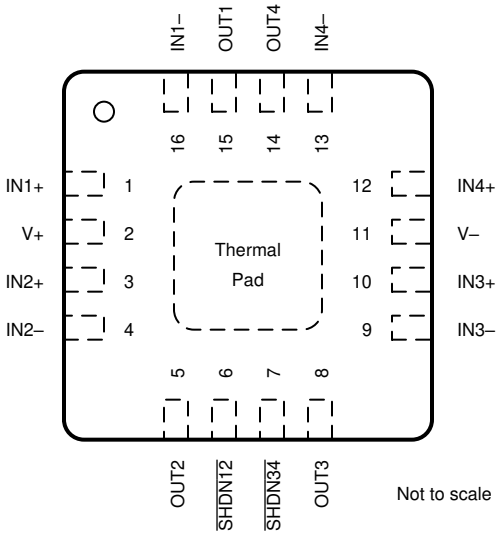


图 4-13. TLV9064 D 或 PW 封装； 14 引脚 SOIC 或 TSSOP （顶视图）

表 4-5. 引脚功能：TLV9064

引脚				类型(1)	说明
名称	SOIC、TSSOP	WQFN	X2QFN		
IN1 –	2	16	1	I	反相输入，通道 1
IN1+	3	1	2	I	同相输入，通道 1
IN2 –	6	4	5	I	反相输入，通道 2
IN2+	5	3	4	I	同相输入，通道 2
IN3 –	9	9	8	I	反相输入，通道 3
IN3+	10	10	9	I	同相输入，通道 3
IN4 –	13	13	12	I	反相输入，通道 4
IN4+	12	12	11	I	同相输入，通道 4
NC	—	6、7	—	—	无内部连接
OUT1	1	15	14	O	输出，通道 1
OUT2	7	5	6	O	输出，通道 2
OUT3	8	8	7	O	输出，通道 3
OUT4	14	14	13	O	输出，通道 4
V –	11	11	10	I 或 —	负（低）电源或接地（对于单电源供电）
V+	4	2	3	I	正（高）电源

(1) I = 输入，O = 输出



A. 将散热焊盘连接至 V –

图 4-14. TLV9064S RTE 封装， 16 引脚 WQFN（带有外露散热焊盘）（顶视图）

表 4-6. 引脚功能：TLV9064S

引脚		类型(1)	说明
名称	编号		
IN1 –	16	I	反相输入，通道 1
IN1+	1	I	同相输入，通道 1
IN2 –	4	I	反相输入，通道 2
IN2+	3	I	同相输入，通道 2
IN3 –	9	I	反相输入，通道 3
IN3+	10	I	同相输入，通道 3
IN4 –	13	I	反相输入，通道 4
IN4+	12	I	同相输入，通道 4
OUT1	15	O	输出，通道 1
OUT2	5	O	输出，通道 2
OUT3	8	O	输出，通道 3
OUT4	14	O	输出，通道 4
$\overline{\text{SHDN12}}$	6	I	关断：低电平 = 禁用放大器，高电平 = 启用放大器。通道 1。有关更多信息，请参阅*关断功能*。
$\overline{\text{SHDN34}}$	7	I	关断：低电平 = 禁用放大器，高电平 = 启用放大器。通道 1。有关更多信息，请参阅*关断功能*。
V –	11	I 或 —	负（低）电源或接地（对于单电源供电）
V+	2	I	正（高）电源

(1) I = 输入，O = 输出

5 规格

5.1 绝对最大额定值

在工作环境温度范围内（除非另外注明）(1)

			最小值	最大值	单位
电源电压 [(V+) – (V–)]			0	6	V
信号输入引脚	电压(2)	共模	(V–) – 0.5	(V+) + 0.5	V
		差分		(V+) – (V–) + 0.2	V
	电流(2)		-10	10	mA
输出短路(3)			持续		mA
温度	额定温度，T_A		-40	125	°C
	结温，T_J			150	
	贮存温度，T_{stg}		-65	150	

(1) 应力超出*绝对最大额定值*下面列出的值可能会对器件造成永久损坏。这些仅为应力等级，并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 输入引脚被二极管钳制至电源轨。对于摆幅能超过电源轨 0.5V 的输入信号，应将其电流限制在 10mA 或者更低。
(3) 接地短路，每个封装对应一个放大器。

5.2 ESD 等级

		值	单位
TLV9061 封装			
$V_{(ESD)}$ 静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±2500	V
	充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1500	
所有其他封装			
$V_{(ESD)}$ 静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±4000	V
	充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1500	

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

在工作环境温度范围内测得（除非另有说明）

		最小值	最大值	单位
V_S	电源电压 (V_S = [V+] – [V–])	1.8	5.5	V
V_I	输入电压范围	(V–) – 0.1	(V+) + 0.1	V
V_O	输出电压范围	V–	V+	V
V_{SHDN_IH}	关断引脚上的高电平输入电压（放大器为启用状态）	1.1	V+	V
V_{SHDN_IL}	关断引脚上的低电平输入电压（放大器为禁用状态）	V–	0.2	V
T_A	额定温度	-40	125	°C

5.4 热性能信息：TLV9061

热性能指标(1)		TLV9061			单位
		DBV (SOT-23)	DCK (SC70)	DPW (X2SON)	
		5 引脚	5 引脚	5 引脚	
$R_{\theta JA}$	结至环境热阻	221.7	263.3	467	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	144.7	75.5	211.6	°C/W
$R_{\theta JB}$	结至电路板热阻	49.7	51	332.2	°C/W
ψ_{JT}	结至顶部特征参数	26.1	1	29.3	°C/W
ψ_{JB}	结至电路板特征参数	49	50.3	330.6	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	125	°C/W

(1) 有关新旧热性能指标的更多信息，请参阅*半导体和 IC 封装热指标*。

5.5 热性能信息：TLV9061S

热性能指标(1)		TLV9061S		单位
		DBV (SOT-23)	DRY (USON)	
		6 引脚	6 引脚	
$R_{\theta JA}$	结至环境热阻	216.5	待定	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	155.1	待定	°C/W
$R_{\theta JB}$	结至电路板热阻	96.2	待定	°C/W
ψ_{JT}	结至顶部特征参数	80.3	待定	°C/W
ψ_{JB}	结至电路板特征参数	95.9	待定	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*。

5.6 热性能信息：TLV9062

热性能指标(1)		TLV9062					单位
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	DDF (SOT-23)	
		8 引脚	8 引脚	8 引脚	8 引脚	8 引脚	
$R_{\theta JA}$	结至环境热阻	157.6	201.2	94.4	205.1	184.4	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	104.6	85.7	116.5	93.7	112.8	°C/W
$R_{\theta JB}$	结至电路板热阻	99.7	122.9	61.3	135.7	99.9	°C/W
ψ_{JT}	结至顶部特征参数	55.6	21.2	13	25.0	18.7	°C/W
ψ_{JB}	结至电路板特征参数	99.2	121.4	61.7	134.0	99.3	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	34.4	不适用	不适用	°C/W

(1) 有关新旧热性能指标的更多信息，请参阅*半导体和 IC 封装热指标*。

5.7 热性能信息：TLV9062S

热指标(1)		TLV9002S			单位
		YCK (DSBGA)	RUG (X2QFN)	DGS (VSSOP)	
		9 引脚	10 引脚	10 引脚	
$R_{\theta JA}$	结至环境热阻	129.8	197.2	170.4	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	0.9	93.3	84.9	°C/W
$R_{\theta JB}$	结至电路板热阻	37.5	123.8	113.5	°C/W
Ψ_{JT}	结至顶部特征参数	0.5	3.7	16.4	°C/W
Ψ_{JB}	结至电路板特征参数	37.1	120.2	112.3	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	不适用	°C/W

(1) 有关新旧热指标的更多信息，请参阅半导体和 IC 封装热指标应用报告。

5.8 热性能信息：TLV9064

热性能指标(1)		TLV9064				单位
		PW (TSSOP)	D (SOIC)	RTE (WQFN)	RUC (X2QFN)	
		14 引脚	14 引脚	16 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	135.8	106.9	65.1	205.5	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	64	64	67.9	72.5	°C/W
$R_{\theta JB}$	结至电路板热阻	79	63	40.4	150.2	°C/W
ψ_{JT}	结至顶部特征参数	15.7	25.9	5.5	3.0	°C/W
ψ_{JB}	结至电路板特征参数	78.4	62.7	40.2	149.6	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	23.8	不适用	°C/W

(1) 有关新旧热性能指标的更多信息，请参阅*半导体和 IC 封装热指标*。

5.9 热性能信息：TLV9064S

热性能指标(1)		TLV9064S	单位
		RTE (WQFN)	
		16 引脚	
$R_{\theta JA}$	结至环境热阻	65.1	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	67.9	°C/W
$R_{\theta JB}$	结至电路板热阻	40.4	°C/W
ψ_{JT}	结至顶部特征参数	5.5	°C/W
ψ_{JB}	结至电路板特征参数	40.2	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	23.8	°C/W

(1) 有关新旧热性能指标的更多信息，请参阅*半导体和 IC 封装热指标*。

5.10 电气特性

在 V_S（总电源电压）= (V+) – (V–) = 1.8V 至 5.5V、T_A = 25°C、R_L = 10kΩ（连接至 V_S/2）、V_{CM} = V_S/2 且 V_{OUT} = V_S/2 条件下（除非另有说明）

参数		测试条件	最小值	典型值	最大值	单位
失调电压						
V_{OS}	输入失调电压	V_S = 5V		±0.3	±1.6	mV
		V_S = 5V，T_A = –40°C 至 125°C			±2	
dV_{OS}/dT	漂移	V_S = 5V，T_A = –40°C 至 125°C		±0.53		µV/°C
PSRR	电源抑制比	V_S = 1.8V – 5.5V，V_{CM} = (V–)		±7	±80	µV/V
	通道分离，直流	直流时		100		dB
输入电压范围						
V_{CM}	共模电压范围	V_S = 1.8V 至 5.5V	(V–) – 0.1		(V+) + 0.1	V
CMRR	共模抑制比	V_S = 5.5V，(V–) – 0.1V < V_{CM} < (V+) – 1.4V，T_A = –40°C 至 125°C	80	103		dB
		V_S = 5.5V，V_{CM} = –0.1V 至 5.6V，T_A = –40°C 至 125°C	57	87		
		V_S = 1.8V，(V–) – 0.1V < V_{CM} < (V+) – 1.4V，T_A = –40°C 至 125°C		88		
		V_S = 1.8V，V_{CM} = –0.1V 至 1.9V，T_A = –40°C 至 125°C		81		
输入偏置电流						
I_B	输入偏置电流			±0.5		pA
I_{OS}	输入失调电流			±0.05		pA
噪声						
E_n	输入电压噪声（峰峰值）	V_S = 5V，f = 0.1Hz 至 10Hz		4.77		μV_{PP}
e_n	输入电压噪声密度	V_S = 5V，f = 10kHz		10		nV/√Hz
		V_S = 5V，f = 1kHz		16		
i_n	输入电流噪声密度	f = 1kHz		23		fA/√Hz
输入电容						
C_{ID}	差分			2		pF
C_{IC}	共模			4		pF
开环增益						
A_{OL}	开环电压增益	V_S = 1.8V，(V–) + 0.04V < V_O < (V+) – 0.04V，R_L = 10kΩ		100		dB
		V_S = 5.5V，(V–) + 0.05V < V_O < (V+) – 0.05V，R_L = 10kΩ	104	130		
		V_S = 1.8V，(V–) + 0.06V < V_O < (V+) – 0.06V，R_L = 2kΩ		100		
		V_S = 5.5V，(V–) + 0.15V < V_O < (V+) – 0.15V，R_L = 2kΩ		130		
频率响应						
GBP	增益带宽积	V_S = 5V，G = +1		10		MHz
Φ_m	相位裕度	V_S = 5V，G = +1		55		°
SR	压摆率	V_S = 5V，G = +1		6.5		V/µs
t_S	建立时间	精度达到 0.1%，V_S = 5V，2V 阶跃，G = +1，C_L = 100pF		0.5		µs
		精度达到 0.01%，V_S = 5V，2V 阶跃，G = +1，C_L = 100pF		1		
t_{OR}	过载恢复时间	V_S = 5V，V_{IN} × 增益 > V_S		0.2		µs
THD + N	总谐波失真 + 噪声(1)	V_S = 5.5V，V_{CM} = 2.5V，V_O = 1V_{RMS}，G = +1，f = 1kHz		0.0008%		
输出						

5.10 电气特性（续）

在 V_S（总电源电压）= (V+) – (V–) = 1.8V 至 5.5V、T_A = 25°C、R_L = 10kΩ（连接至 V_S/2）、V_{CM} = V_S/2 且 V_{OUT} = V_S/2 条件下（除非另有说明）

参数		测试条件	最小值	典型值	最大值	单位
V_O	相对于电源轨的电压输出摆幅	V_S = 5.5V，R_L = 10kΩ			20	mV
		V_S = 5.5V，R_L = 2kΩ			60	
I_{SC}	短路电流	V_S = 5V		±50		mA
Z_O	开环输出阻抗	V_S = 5V，f = 10MHz		100		Ω
电源						
I_Q	每个放大器的静态电流	V_S = 5.5V，I_O = 0mA		538	750	μA
		V_S = 5.5V，I_O = 0mA，T_A = -40°C 至 125°C			800	
关断						
I_{QSD}	每个放大器的静态电流	V_S = 1.8V 至 5.5V，所有放大器都被禁用，$\overline{SHDN}$ = 低电平		0.5	1.5	μA
Z_{SHDN}	关断时的输出阻抗	V_S = 1.8V 至 5.5V，放大器被禁用		10 ‖ 8		GΩ ‖ pF
$V_{SHDN\_THR\_HI}$	高电平电压关断阈值（放大器为启用状态）	V_S = 1.8V 至 5.5V		(V–) + 0.9V	(V–) + 1.1V	V
$V_{SDHN\_THR\_LO}$	低电平电压关断阈值（放大器为禁用状态）	V_S = 1.8V 至 5.5V	(V–) + 0.2V	(V–) + 0.7V		V
t_{ON}	放大器启用时间（关断）(2)	V_S = 1.8V 至 5.5V，完全关断；G = 1，V_{OUT} = 0.9 × V_S/2，R_L 连接到 V–		10		μs
t_{OFF}	放大器禁用时间(2)	V_S = 1.8V 至 5.5V，G = 1，V_{OUT} = 0.1 × V_S /2，R_L 连接到 V–		0.6		μs
	$\overline{SHDN}$ 引脚输入偏置电流（每个引脚）	V_S = 1.8V 至 5.5V，V+ ≥ $\overline{SHDN}$ ≥ (V+) – 0.8V		130		pA
		V_S = 1.8V 至 5.5V，V– ≤ $\overline{SHDN}$ ≤ V– + 0.8V		40		

(1) 三阶滤波器；-3dB 时的带宽 = 80kHz。
(2) 禁用时间 (t_{OFF}) 和启用时间 (t_{ON}) 是指施加给 $\overline{SHDN}$ 引脚的信号为 50% 时到输出电压达到 10%（禁用）或 90%（启用）电平时之间的间隔。

5.11 典型特性

T_A = 25°C，V_S = 5.5V，R_L = 10kΩ（连接至 V_S/2），V_{CM} = V_S/2 且 V_{OUT} = V_S/2（除非另有说明）

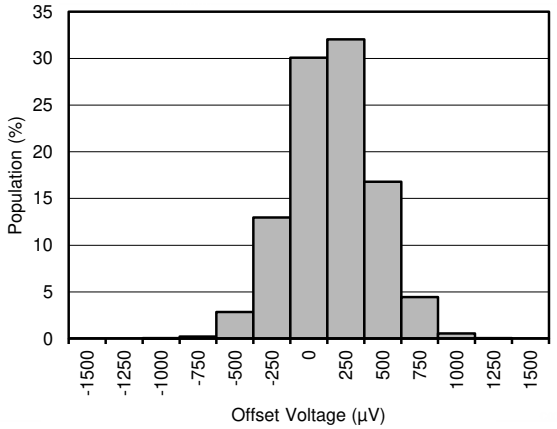
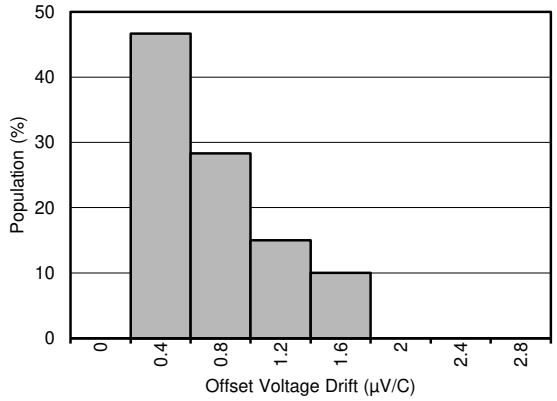


图 5-1. 失调电压产生分布



T_A = -40°C 至 125°C

图 5-2. 失调电压漂移分布

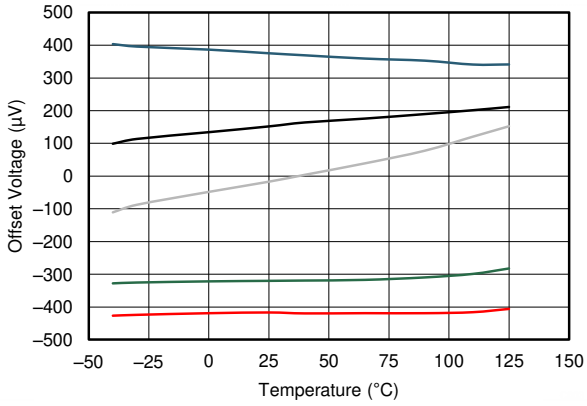
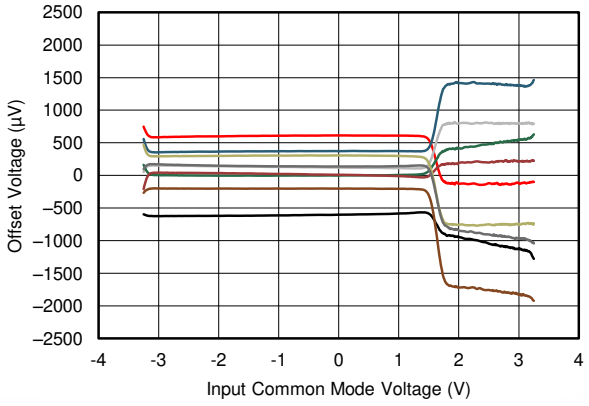
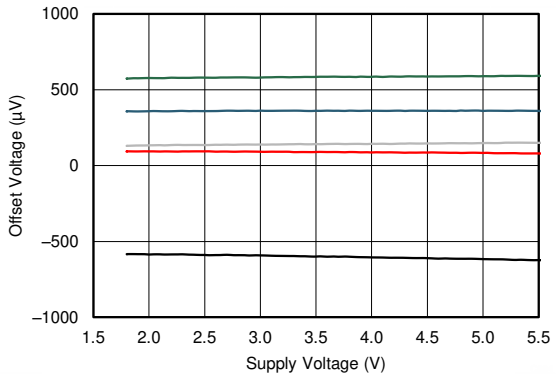


图 5-3. 失调电压与温度间的关系



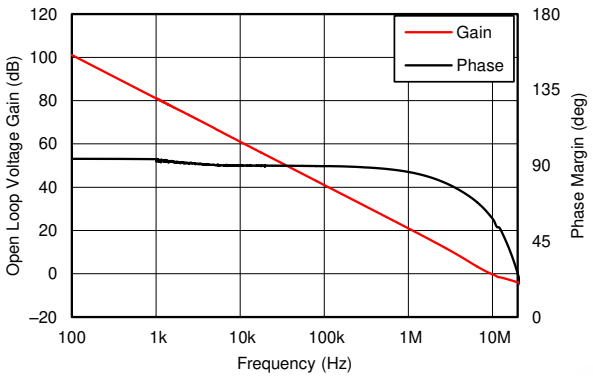
V+ = 2.75V　　V– = –2.75V

图 5-4. 失调电压与共模电压间的关系



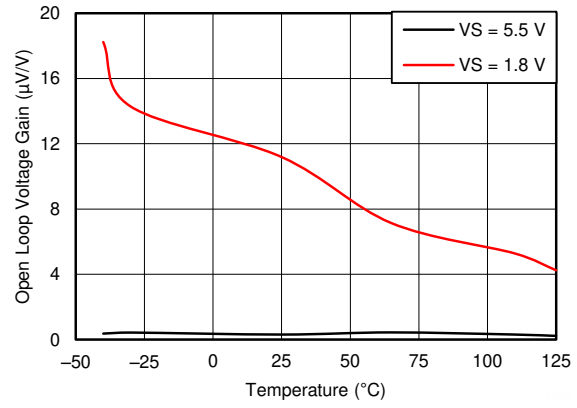
V_S = 1.8V 至 5.5V

图 5-5. 失调电压与电源间的关系



C_L = 10pF

图 5-6. 开环增益和相位与频率间的关系



R_L = 2kΩ

图 5-7. 开环增益与温度间的关系

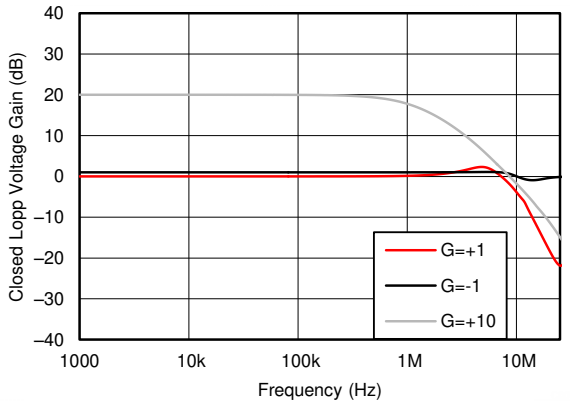


图 5-8. 闭环增益与频率间的关系

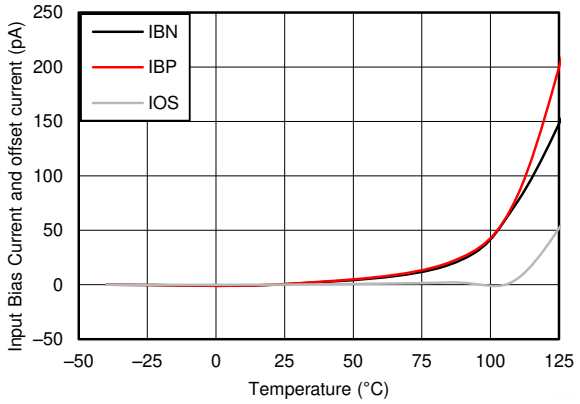
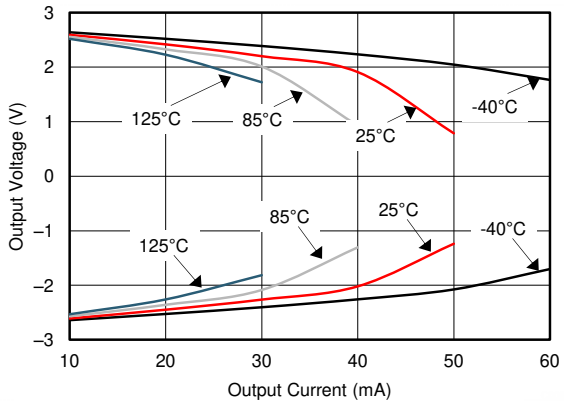


图 5-9. 输入偏置电流与温度间的关系



V+ = 2.75V　　V – = – 2.75V

图 5-10. 输出电压摆幅与输出电流间的关系

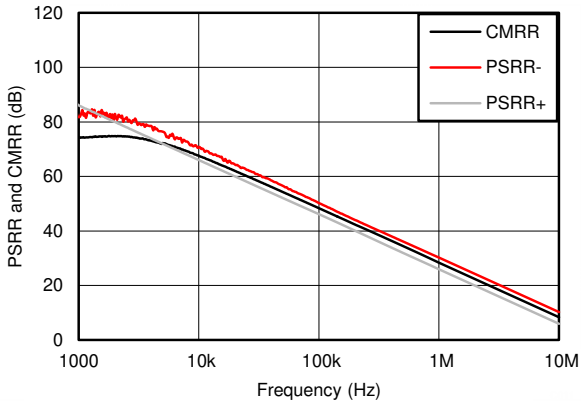
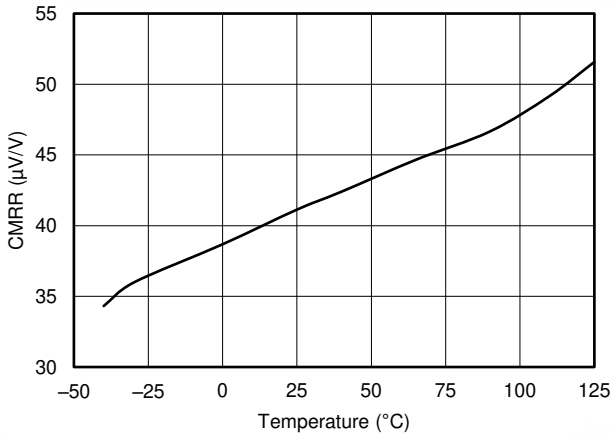
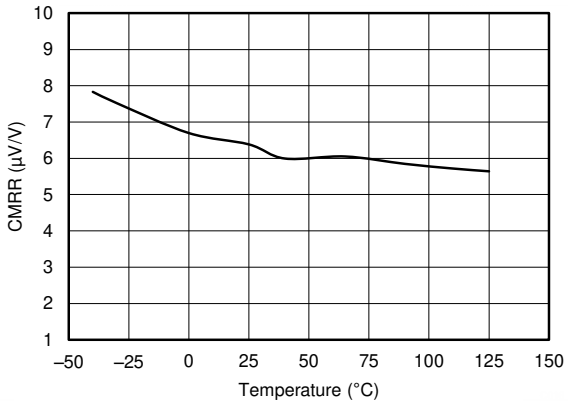


图 5-11. CMRR 和 PSRR 与频率间的关系（以输入为参考）



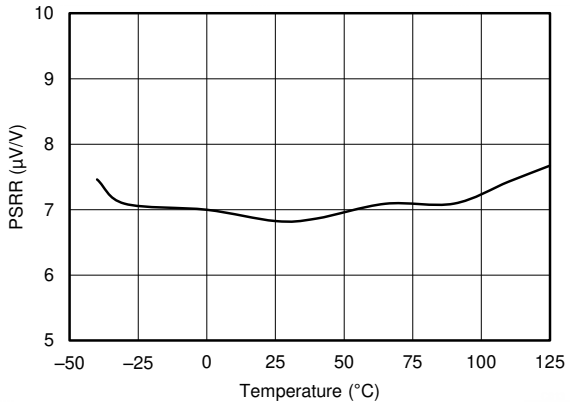
V_S = 5.5V　　V_{CM} = -0.1V 至 5.6V　　T_A= – 40°C 至 125°C
R_L = 10kΩ

图 5-12. CMRR 与温度间的关系



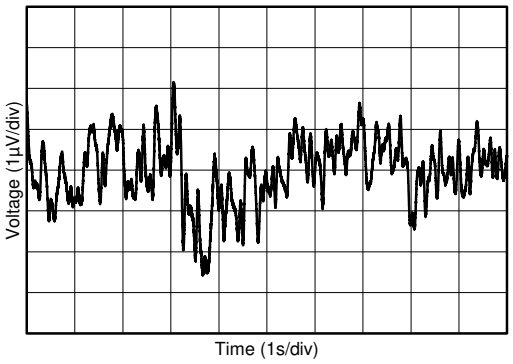
V_{CM} = (V–) – 0.1V 至 (V+) – 1.4V
T_A= –40°C 至 125°C R_L = 10kΩ V_S = 5.5V

图 5-13. CMRR 与温度间的关系



V_S = 1.8V 至 5.5V

图 5-14. PSRR 与温度间的关系



V_S = 1.8V 至 5.5V

图 5-15. 0.1Hz 至 10Hz 输入电压噪声

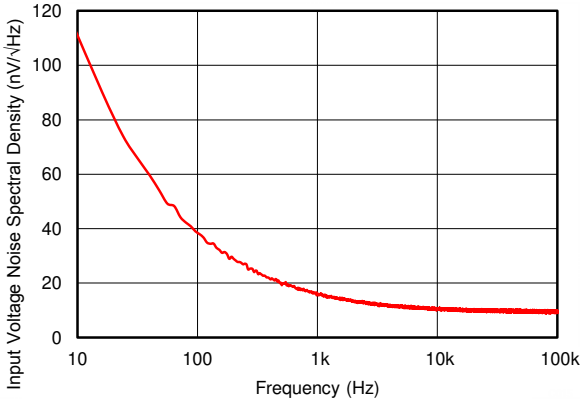
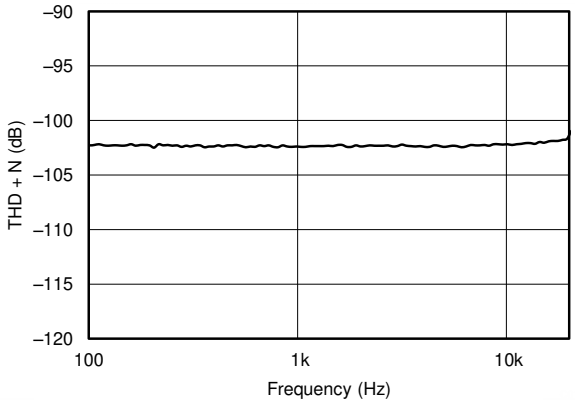
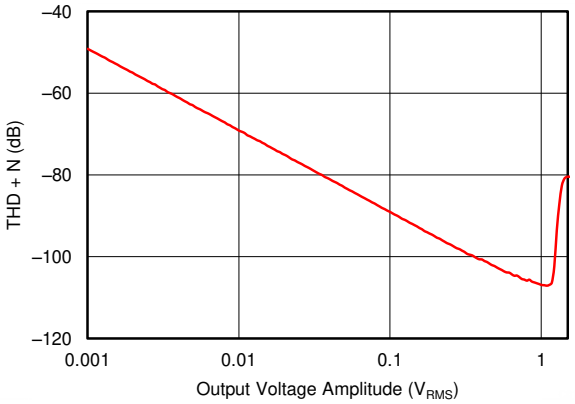


图 5-16. 输入电压噪声频谱密度与频率间的关系



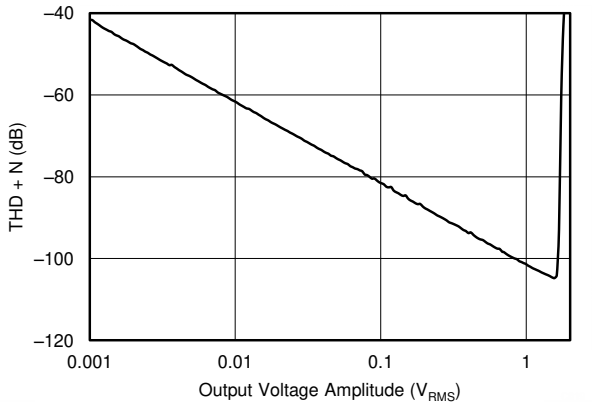
V_S = 5.5V V_{CM} = 2.5V R_L = 2kΩ
V_{OUT} = 0.5V_{RMS} BW = 80kHz G = +1

图 5-17. THD+N 与频率间的关系



V_S = 5.5V R_L = 2kΩ G = +1
V_{CM} = 2.5V BW = 80kHz f = 1kHz

图 5-18. THD + N 与幅度间的关系



V_S = 5.5V V_{CM} = 2.5V R_L = 2kΩ
G = -1 BW = 80kHz f = 1kHz

图 5-19. THD + N 与幅度间的关系

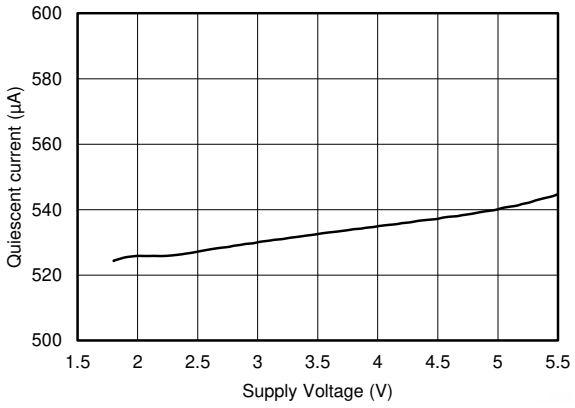


图 5-20. 静态电流与电源电压间的关系

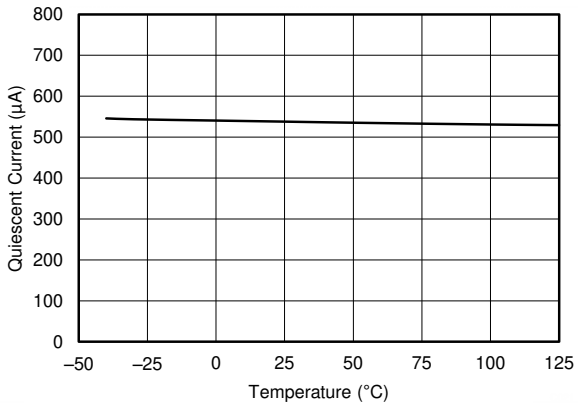


图 5-21. 静态电流与温度间的关系

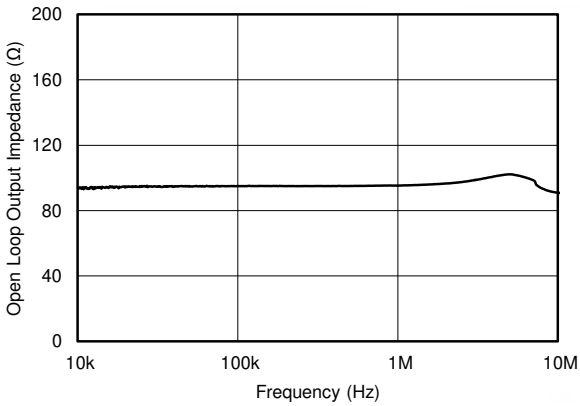
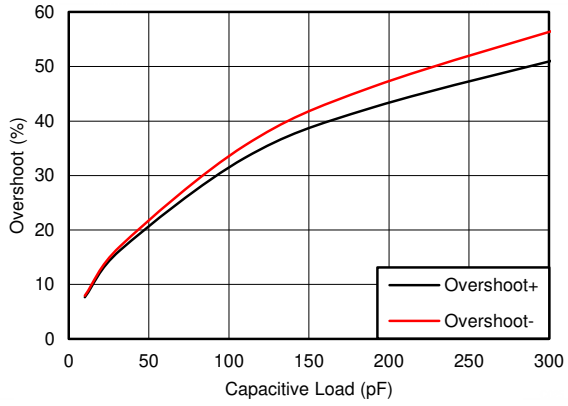
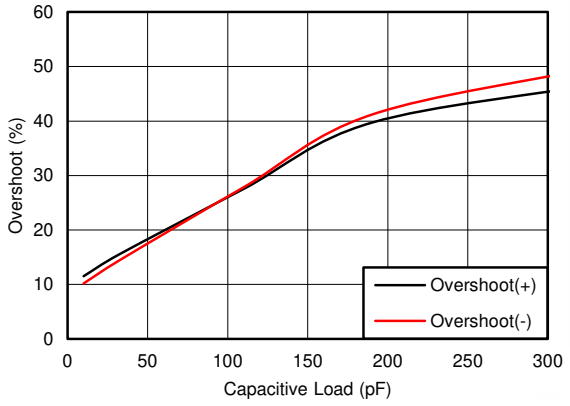


图 5-22. 开环输出阻抗与频率间的关系



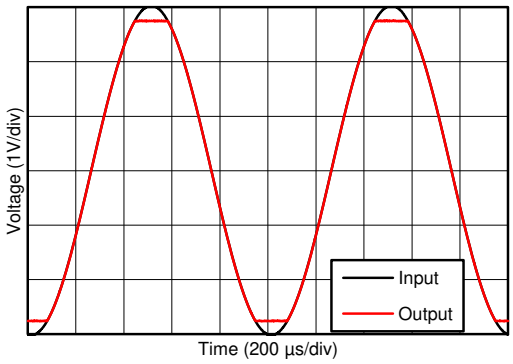
V+ = 2.75V V – = – 2.75V G = +1V/V
V_{OUT} 阶跃 = 100mV_{p-p} R_L = 10kΩ

图 5-23. 小信号过冲与负载电容间的关系



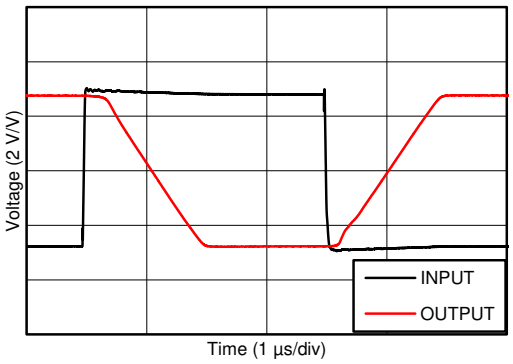
V+ = 2.75V V – = – 2.75V G = -1V/V
V_{OUT} 阶跃 = 100mV_{p-p} R_L = 10kΩ

图 5-24. 小信号过冲与负载电容间的关系



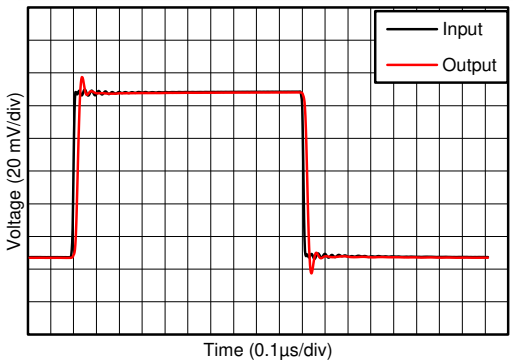
V+ = 2.75V V – = –2.75V

图 5-25. 无相位反转



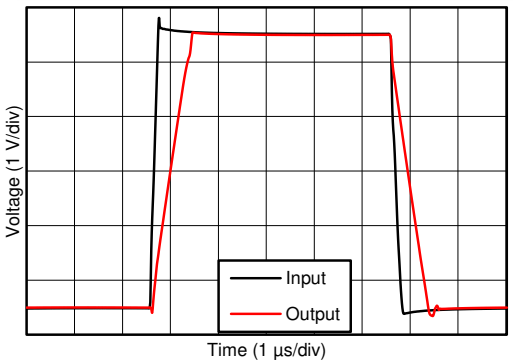
V+ = 2.75V V – = –2.75V G = -10V/V

图 5-26. 过载恢复



V+ = 2.75V V – = –2.75V G = 1V/V

图 5-27. 小信号阶跃响应



V+ = 2.75V V – = –2.75V C_L = 100pF
G = 1V/V

图 5-28. 大信号阶跃响应

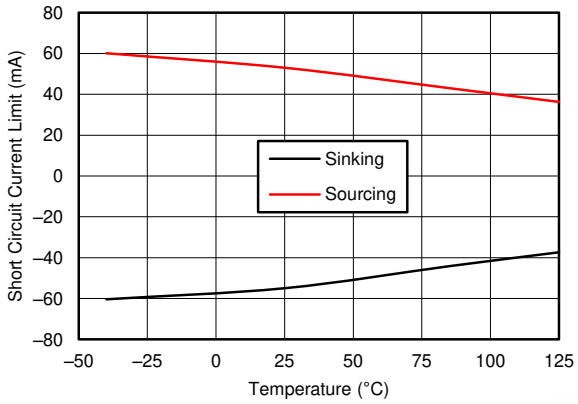
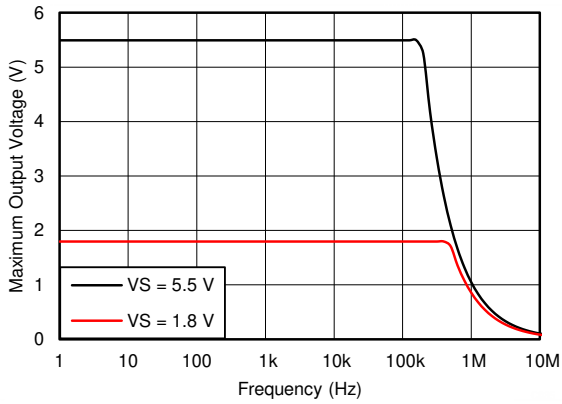
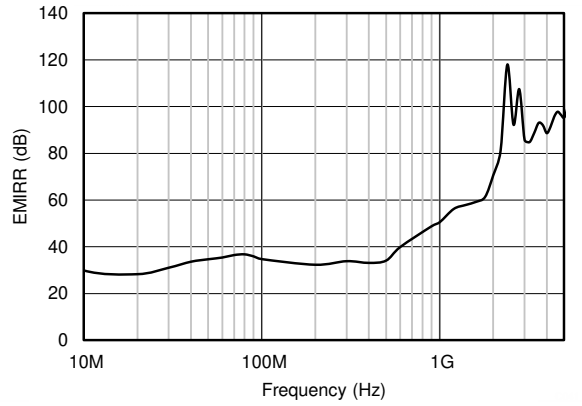


图 5-29. 短路电流与温度间的关系



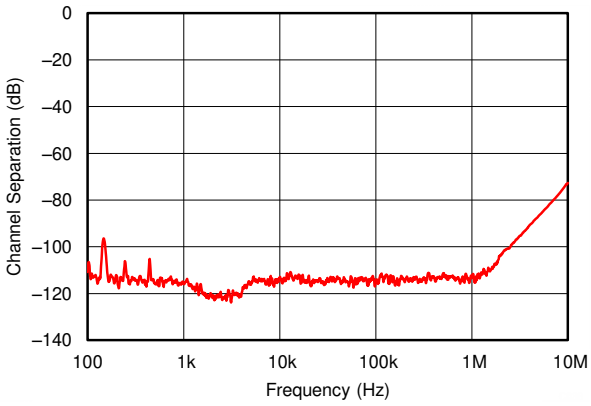
R_L = 10kΩ C_L = 10pF

图 5-30. 最大输出电压与频率和电源电压间的关系



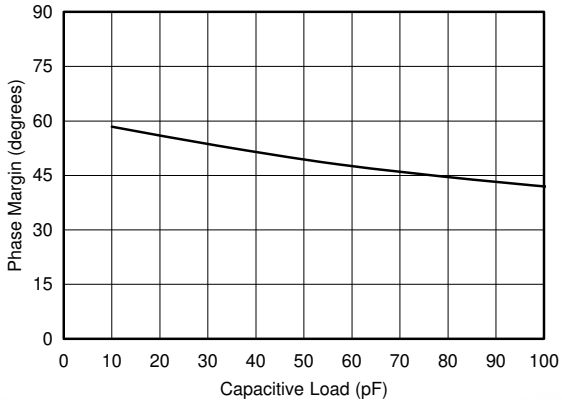
P_{RF} = – 10dBm

图 5-31. 以同相输入为基准的电磁干扰抑制比 (EMIRR+) 与频率间的关系



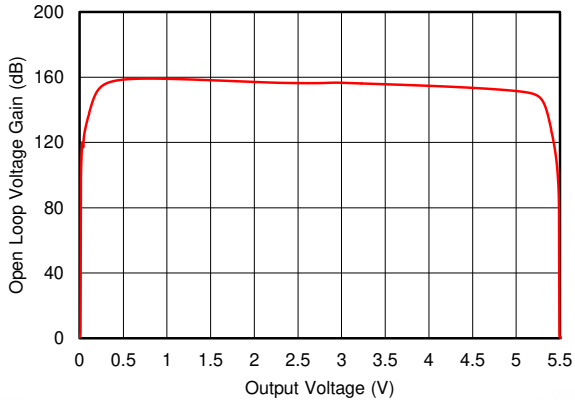
V+ = 2.75V V – = – 2.75V

图 5-32. 通道隔离与频率间的关系



V_S = 5.5V

图 5-33. 相位裕度与容性负载间的关系



V_S = 5.5V

图 5-34. 开环电压增益与输出电压间的关系

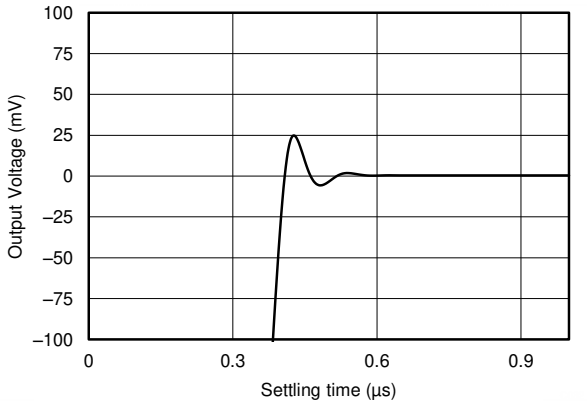


图 5-35. 大信号建立时间（正）

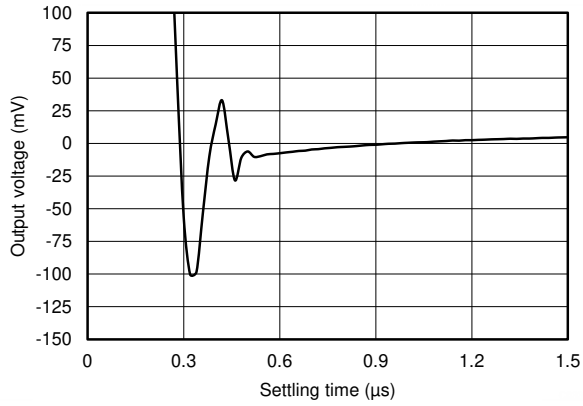


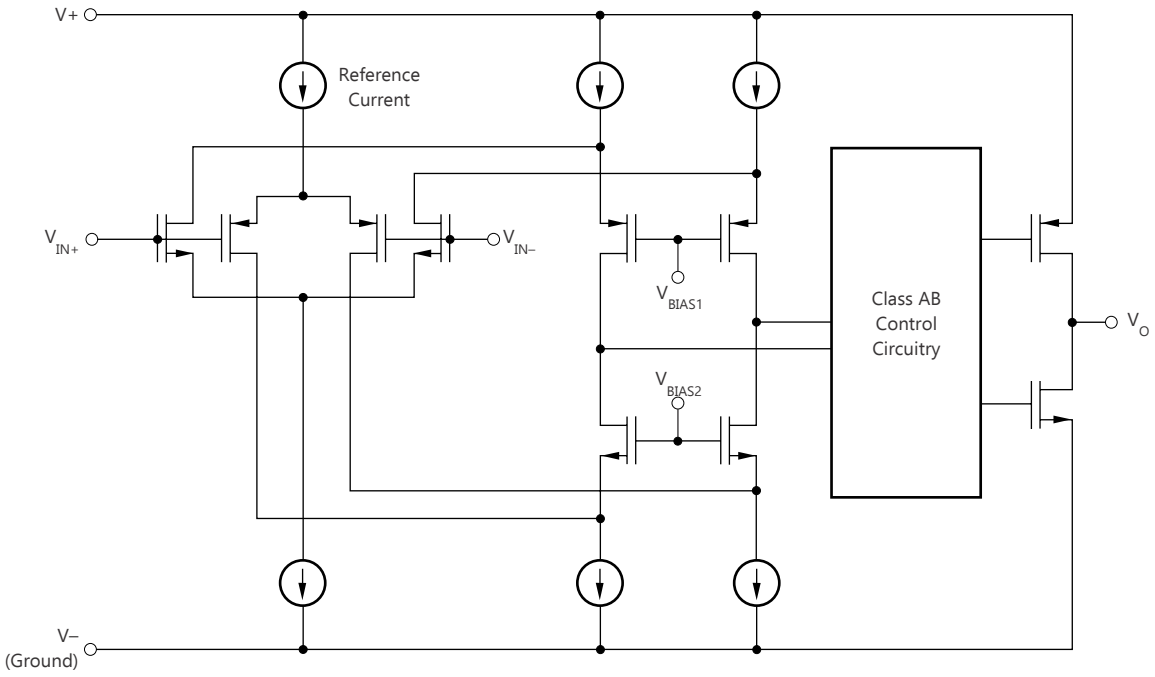
图 5-36. 大信号建立时间（负）

6 详细说明

6.1 概述

TLV906x 器件是低功耗、轨到轨输入和输出运算放大器系列。这些器件的工作电压范围为 1.8V 至 5.5V，具有单位增益稳定特性，并且适用于各种通用应用。输入共模电压范围包括两个电源轨，并支持将 TLV906x 系列器件用于几乎任何单电源应用。轨到轨输入和输出摆幅可大幅扩大动态范围（尤其在低电源电压应用中）。高带宽使该系列能够驱动模数转换器 (ADC) 的采样保持电路。

6.2 功能方框图



6.3 特性说明

6.3.1 轨到轨输入

TLV906x 系列的输入共模电压范围相对于电源轨向外扩展了 100mV，从而支持 1.8V 至 5.5V 的完整电源电压范围。此性能由一个互补输入级实现：一个 N 沟道输入差分对和一个与之并联的 P 沟道差分对，如*功能方框图* 所示。N 沟道对对于靠近正电源轨的输入电压有效，通常比正电源高 (V+) – 1.4V 至 200mV，而 P 沟道对针对低于负电源轨 200mV 至大约 (V+) – 1.4V 间的输入打开。有一个小转换区域，通常介于 (V+) – 1.2V 至 (V+) – 1V 之间，在这个区间内两个对都打开。此 200mV 转换区域可能会随工艺不同而发生变化，最高可达 200mV。因此，此转换区域 (两个级都打开) 在低端上的范围介于 (V+) – 1.4V 至 (V+) – 1.2V 之间，而在高端上的范围高达 (V+) – 1V 至 (V+) – 0.8V。在此转换区域内，与器件在该区域外运行相比，PSRR、CMRR、失调电压、温漂和 THD 等性能可能会下降。

6.3.2 轨到轨输出

TLV906x 系列器件是一种低功耗、低电压运算放大器，可提供强大的输出驱动能力。一个具有共源晶体管的 AB 类输出级可实现完全的轨到轨输出摆幅功能。对于 10kΩ 的阻性负载，无论施加的电源电压是多少，输出摆幅都在两个电源轨的 15mV 范围内。不同的负载情况会改变放大器在靠近电源轨范围内摆动的能力。

6.3.3 EMI 抑制

TLV906x 通过集成电磁干扰 (EMI) 滤波降低无线通信设备、混合使用模拟信号链和数字元件的高密度电路板等干扰源产生的 EMI 效应。利用电路设计技术可以提高 EMI 抗扰度；TLV906x 从这些设计改进中受益。德州仪器 (TI) 已经开发出在 10MHz 至 6GHz 扩展宽频谱范围内准确测量和量化运算放大器抗扰度的功能。图 6-1 展示了对 TLV906x 执行此测试的结果。表 6-1 列出了在实际应用中 TLV906x 在常见特定频率下的 EMIRR IN+ 值。有关详细信息，请参阅*运算放大器的 EMI 抑制比 应用手册*。

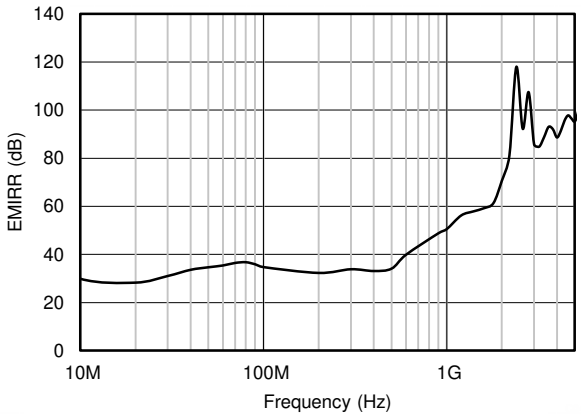


图 6-1. EMIRR 测试

表 6-1. TLV906x 在目标频率下的 EMIRR IN+

频率	应用或分配	EMIRR IN+
400MHz	移动无线广播、移动卫星、太空操作、气象、雷达、超高频 (UHF) 应用	59.5dB
900MHz	全球移动通信系统 (GSM) 应用、无线电通信、导航、GPS (最高可达 1.6GHz) 、GSM、航空移动通信及 UHF 应用	68.9dB
1.8GHz	GSM 应用、个人移动通信、宽带、卫星和 L 波段 (1GHz 至 2GHz)	77.8dB
2.4GHz	802.11b、802.11g、802.11n、Bluetooth®、个人移动通信、工业、科学和医疗 (ISM) 无线频段、业余无线电通信和卫星、S 波段 (2GHz 至 4GHz)	78.0dB
3.6GHz	无线电定位、航空通信和导航、卫星、移动通信、S 波段	88.8dB
5GHz	802.11a、802.11n、航空通信和导航、移动通信、太空和卫星运行、C 波段 (4GHz 至 8GHz)	87.6dB

6.3.4 过载恢复

过载恢复定义为运算放大器输出从饱和状态恢复到线性状态所需的时间。当输出电压由于高输入电压或高增益而超过额定工作电压时，运算放大器的输出器件进入饱和区。器件进入饱和区后，输出器件中的电荷载体需要时间回到线性状态。当电荷载体回到线性状态时，器件开始以指定的压摆率进行转换。因此，传播延迟（过载情况下）等于过载恢复时间与转换时间之和。TLV906x 系列的过载恢复时间约为 200ns。

6.3.5 关断功能

TLV906xS 器件具有 $\overline{\text{SHDN}}$ 引脚，可禁用运算放大器，将其置于低功耗待机模式。在该模式下，运算放大器消耗的电流通常低于 1μA。$\overline{\text{SHDN}}$ 引脚为低电平有效，这意味着当 $\overline{\text{SHDN}}$ 引脚的输入为有效的逻辑低电平时，则启用关断模式。

$\overline{\text{SHDN}}$ 引脚以运算放大器的负电源电压为基准。关断特性的阈值在 800mV（典型值）左右，且不随电源电压的变化而变化。开关阈值中包含了迟滞，以确保顺畅的开关特性。为了确保最佳的关断行为，应通过有效逻辑信号驱动 $\overline{\text{SHDN}}$ 引脚。有效逻辑低电平是指介于 V– 和 V– + 0.2V 之间的电压。有效逻辑高电平是指介于 V– + 1.2V 和 V+ 之间的电压。关断引脚必须连接到有效的高电压或低电压或者被驱动，而不是处于开路状态。 ***没有*** 用于启用放大器的内部上拉电阻。

$\overline{\text{SHDN}}$ 引脚为高阻抗 CMOS 输入。双通道运算放大器版本是独立控制的，而四通道运算放大器版本是采用逻辑输入成对控制的。对于电池供电的应用，这种特性可用于大幅降低平均电流并延长电池使用寿命。所有通道全部关断时，启用时间为 10μs；禁用时间为 6μs。禁用时，输出呈现高阻抗状态。该架构允许将 TLV906xS 作为门控放大器（或将器件输出复用到公共模拟输出总线上）。关断时间 (t_{OFF}) 取决于负载条件，并随负载电阻的增加而增加。为了确保在特定的关断时间内关断（禁用），指定的 10kΩ 负载需加载到中间电源 (V_S/2)。如果在没有负载的情况下使用 TLV906xS，则所需的关断时间会显著增加。

6.4 器件功能模式

TLV906x 系列可在 1.8V (±0.9V) 和 5.5V (±2.75V) 的电源电压范围内正常工作。TLV906xS 器件具有关断模式，在关断引脚上施加有效逻辑低电平时会关断。

7 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 应用信息

TLV906x 系列具有 10MHz 带宽和 6.5V/µs 压摆率，且每个通道仅消耗 538µA 的电源电流，从而在功耗超低的情况下提供良好的交流性能。对于直流应用，该系列在 10kHz 下具有 10nV/√Hz 的超低输入噪声电压，并且具有低输入偏置电流和 0.3mV 的典型输入失调电压，从而提供良好的性能。

7.2 典型应用

7.2.1 典型的低侧电流检测应用

图 7-1 显示了低侧电流感应应用中配置的 TLV906x。

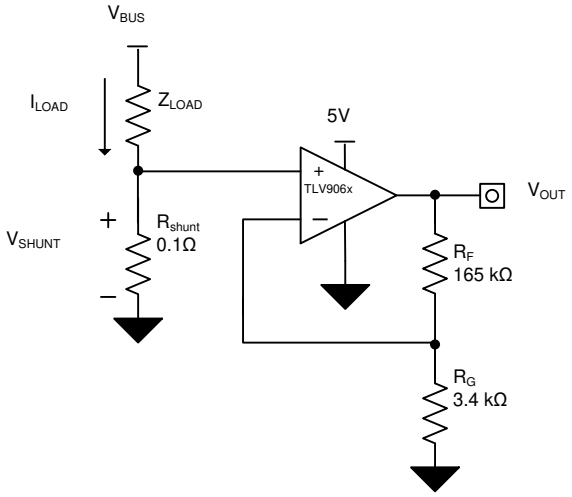


图 7-1. 低侧电流检测应用中的 TLV906x

7.2.2 设计要求

此设计的设计要求如下：

- 负载电流：0A 至 1A
- 输出电压：4.95V
- 最大分流电压：100mV

7.2.3 详细设计过程

方程式 1 提供了图 7-1 中的电路传递函数。

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times GAIN \quad (1)$$

负载电流 (I_{LOAD}) 在分流电阻器 (R_{SHUNT}) 上产生压降。负载电流设置为 0A 至 1A。为了在最大负载电流下保持分流电压低于 100mV，使用方程式 2 定义了最大分流电阻。

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

根据方程式 2 可知，R_{SHUNT} 等于 100mΩ。I_{LOAD} 和 R_{SHUNT} 产生的压降由 TLV906x 放大，从而产生约 0V 至 4.95V 的输出电压。方程式 3 可计算 TLV906x 生成必要输出电压所需的增益。

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

根据方程式 3 计算出的所需增益等于 49.5V/V，通过 R_F 和 R_G 电阻器进行设置。方程式 4 可确定 R_F 和 R_G 电阻器的大小，从而将 TLV906x 的增益设置为 49.5V/V。

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

选择 R_F 为 165kΩ 以及 R_G 为 3.4kΩ 可提供等于约 49.5V/V 的组合。图 7-2 展示了图 7-1 中所示电路测得的传递函数。请注意，增益只是反馈和增益电阻器的函数。通过改变电阻器的比率来调整该增益，实际电阻器阻值由设计人员希望建立的阻抗水平决定。阻抗水平决定了电流损耗、杂散电容的影响以及其他一些行为。并不存在适用于每个系统的最佳阻抗选择，您必须选择适合您的系统参数的阻抗。

7.2.4 应用曲线

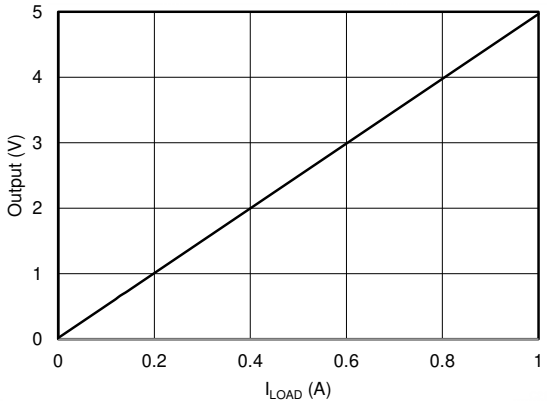


图 7-2. 低侧电流检测传递函数

7.3 电源相关建议

TLV906x 系列的额定工作范围为 1.8V 至 5.5V（±0.9V 至 ±2.75V）；多种规格适用于 –40°C 至 125°C 的温度范围。*典型特性* 部分介绍了可能会随工作电压或温度而显著变化的参数。

小心

电源电压大于 6V 会对器件造成永久损坏；请参阅*绝对最大额定值* 表。

将 0.1µF 旁路电容器置于电源引脚附近，以减少来自高噪声电源或高阻抗电源的耦合误差。有关旁路电容器位置的更多详细信息，请参阅*布局*部分。

7.3.1 输入和 ESD 保护

TLV906x 系列器件在所有引脚上均整合了内部 ESD 保护电路。对于输入和输出引脚，这种保护主要包括输入和电源引脚之间连接的导流二极管。只要电流如*绝对最大额定值*表中所示不超过 10mA，这些 ESD 保护二极管就可以提供电路内输入过驱保护。图 7-3 展示了如何通过将串联输入电阻器添加到被驱动的输入端来限制输入电流。添加的电阻器会增加放大器输入端的热噪声，在对噪声敏感的应用中，该值必须保持在最低。

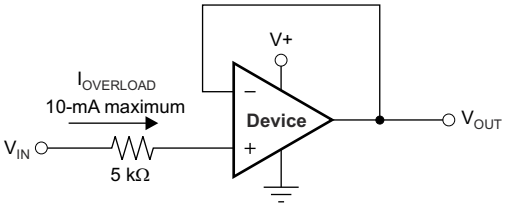


图 7-3. 输入电流保护

7.4 布局

7.4.1 布局指南

为了使器件具有出色的运行性能，请使用良好的印刷电路板 (PCB) 布局实践，包括：

- 噪声可以通过整个电路的电源引脚和运算放大器本身的电源引脚传入模拟电路。旁路电容用于通过为局部模拟电路提供低阻抗电源，以降低耦合噪声。
  - 在每个电源引脚和接地端之间连接低等效串联电阻 (ESR) 0.1µF 陶瓷旁路电容器，并尽量靠近器件放置。从 V+ 到接地端的单个旁路电容器足以满足单电源应用的需求。
- 将电路中的模拟部分和数字部分单独接地是最简单、最有效的噪声抑制方法之一。多层 PCB 上的一层或多层通常专门用于作为接地平面。接地层有助于散热和降低电磁干扰 (EMI) 噪声拾取。请小心地对数字接地和模拟接地进行物理隔离，同时应注意接地电流。有关更多详细信息，请参阅*电路板布局布线技巧*。
- 为了减少寄生耦合，应让输入布线尽可能远离电源或输出布线。如果这些走线不能保持分开，则以 90 度角穿过敏感走线比平行于噪声走线来排布走线要好得多。
- 外部元件应尽量靠近器件放置。如图 7-5 所示，使 R_F 和 R_G 接近反相输入可最大限度地减小反相输入端的寄生电容。
- 尽可能缩短输入布线的长度。切记，输入布线是电路中最敏感的部分。
- 考虑在关键布线周围设定驱动型低阻抗保护环。这样可显著减少附近布线在不同电势下产生的漏电流。
- 为获得卓越性能，建议在组装 PCB 板后进行清洁。
- 任何精密集成电路都可能因湿气渗入塑料封装中而出现性能变化。在执行任何 PCB 水清洁流程之后，建议将 PCB 组件烘干，以去除清洁时渗入器件封装中的水分。大多数情形下，清洗后在 85°C 下低温烘干 30 分钟即可。

7.4.2 布局示例

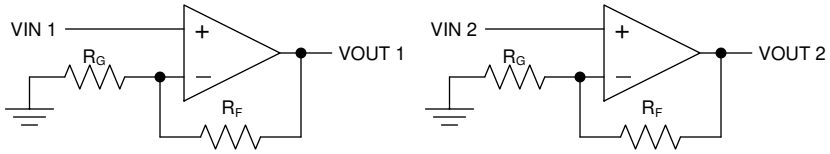


图 7-4. 布局示例的原理图表示

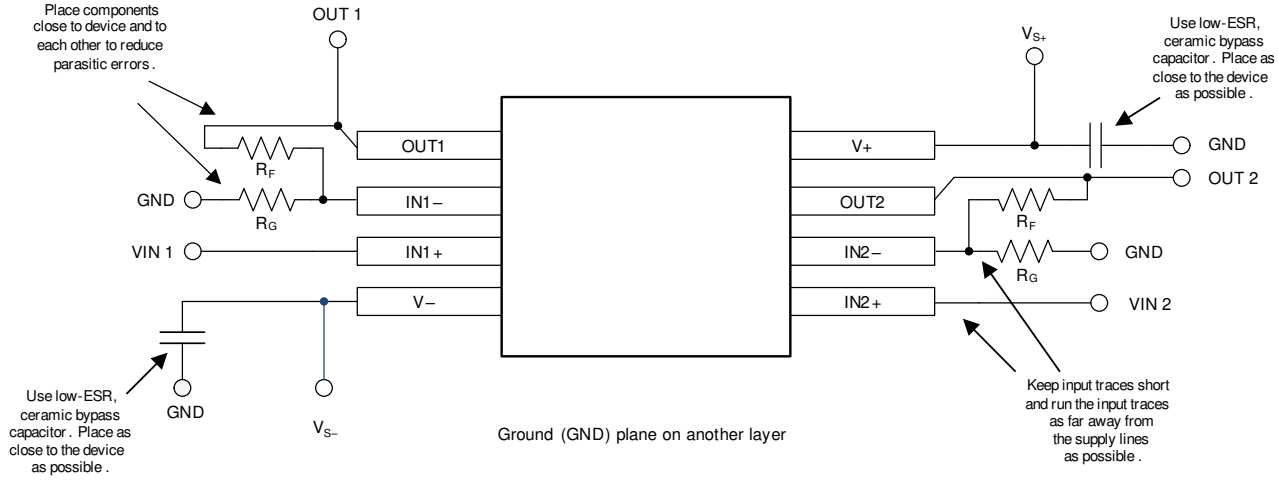


图 7-5. 布局示例

8 器件和文档支持

8.1 文档支持

8.1.1 相关文档

请参阅以下相关文档：

- 德州仪器 (TI)，*电路板布局技巧*
- 德州仪器 (TI)，*运算放大器的 EMI 抑制比* 应用手册
- 德州仪器 (TI)，*QFN/SON PCB 连接* 应用手册
- 德州仪器 (TI)，*Quad Flatpack No-Lead 逻辑封装* 应用手册
- 德州仪器 (TI)，*单端输入至差分输出转换电路* 设计指南
- 德州仪器 (TI)，*TLVx313 适用于成本敏感型系统的低功耗、轨到轨输入/输出、500µV 典型失调电压、1MHz 运算放大器* 数据表
- 德州仪器 (TI)，*TLVx314 3MHz、低功耗、内置 EMI 滤波器、RRIO、运算放大器* 数据表

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 商标

TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision L (September 2024) to Revision M (December 2024)	Page
• 更改了 TLV9061S DBV (SOT-23) 引脚排列图以与*引脚功能* 表相匹配	4

Changes from Revision K (July 2024) to Revision L (September 2024)	Page
• 删除了*器件信息* 表中 TLV9062S（YCK，DSBGA）封装的预发布说明	1

Changes from Revision J (September 2019) to Revision K (July 2024) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1
- 更新了*器件信息*表.....1
- 在*器件信息*表中新增了 TLV9062S（YCK，DSBGA）封装的封装预发布说明.....1
- 向*器件比较*表添加了 YCK 封装.....3
- 向*引脚配置和功能*部分添加了 TLV9062S YCK (DSBGA) 引脚排列图.....4

Changes from Revision I (May 2019) to Revision J (September 2019) **Page**

- 删除了整个数据表中的 TLV9062IDDFR（SOT-23，8）封装预发布说明.....1
- 向*器件比较*表添加了业界通用封装名称.....3
- 向具有散热焊盘的封装添加了说明，指明散热焊盘需要连接到 V–.....4
- 在 $\overline{\text{SHDN}}$ 引脚功能行中添加了指向*关断功能*部分的链接.....4
- 向*特性说明*部分中添加了 *EMI 抑制*部分.....22
- 更改了*关断功能*部分，以添加更多阐述.....23

Changes from Revision H (April 2019) to Revision I (May 2019) **Page**

- 添加了 DDF (SOT-23) 热性能信息以替换 TBD.....11

Changes from Revision G (December 2018) to Revision H (April 2019) **Page**

- 向*器件信息*表中添加了（SOT-23，8）信息.....1
- 向*器件比较*表添加了 DDF 封装列.....3
- 向*引脚功能*添加了 DDF (SOT-23) 封装.....4
- 向以下部分添加了 DDF (SOT-23) 封装：*热性能信息*.....11

Changes from Revision F (September 2018) to Revision G (December 2018) **Page**

- 将 TLV9064 RUC 封装名称从（WQFN，14）更改为（X2QFN，14）（在*器件信息*表中）.....1
- 向以下部分添加了 RUC (X2QFN) 封装引脚排列信息：“引脚功能：TLV9064”表.....4
- 向*引脚配置和功能*部分中添加了 TLV9064 RUC (X2QFN) 引脚排列图.....4
- 向以下部分添加了 RUC (X2QFN) 封装：热性能信息 TLV9064 表.....12

Changes from Revision E (July 2018) to Revision F (September 2018) **Page**

- 删除了数据表标题中的关断器件型号.....1
- 删除了 TLV9062 *器件信息*表中的（X2QFN，10）封装.....1
- 向“说明”部分添加了对关断器件型号的引用.....1
- 将整个数据表中的 TLV906xS 系列更改为 TLV906xS 系列.....1
- 向“器件比较”表添加了关断器件.....3
- 更改了所有引脚排列图的引脚名称以反映更新的命名规则.....4
- 添加了“TLV9061S 热性能信息”表.....11
- 添加了“TLV9064S 热性能信息”表.....12
- 删除了部分关断放大器启用时间.....13
- 在“典型应用”部分中添加了有关为电流检测应用选择电阻器的阐述.....25
- 更改了“布局指南”中第三个要点的措辞.....27

Changes from Revision D (June 2018) to Revision E (July 2018) **Page**

- 向*器件信息*表添加了 TLV9061S 器件 1
- 向*器件信息*表添加了 TLV9064S 器件 1
- 向*器件比较*表添加了 RUC 和 RUG 封装 3
- 向*引脚配置和功能*部分中添加了 TLV9061S DBV (SOT-23) 引脚排列图 4
- 向以下部分添加了 TLV9061S DBV (SOT-23) 封装引脚排列信息：*引脚功能：TLV9061S* 表 4
- 向*引脚配置和功能*部分中添加了 TLV9062S RUG (VSSOP) 封装引脚排列图 4
- 向以下部分添加了 TLV9064 RTE 引脚排列信息：*引脚功能：TLV9064* 表 4
- 向*引脚配置和功能*部分添加了 TLV9064S RTE (WQFN) 引脚排列图 4
- 向以下部分添加了 TLV9062S RUG (VSSOP) 封装引脚排列信息：*引脚功能：TLV9062S* 表 4
- 向*引脚配置和功能*部分添加了 TLV9064 RTE (WQFN) 引脚排列图 4

Changes from Revision C (March 2018) to Revision D (June 2018) **Page**

- 向文档标题中的“TLV906x”添加了“关断”英文的首字母 (S) 作为后缀 1
- 向*特性*列表添加了“关断版本”要点 1
- 向*器件信息*表添加了 TLV9062S 器件 1
- 向*说明（续）*部分添加了“关断”文本 1
- 在*绝对最大额定值*表添加了 (V_S = [V+] – [V–]) 电源电压参数 10
- 向*建议运行条件*表添加了“输入电压范围”和“输出电压范围”参数和值 10
- 向*建议运行条件*表添加了关断引脚的建议运行条件 10
- 在*建议运行条件*表中将 T_A 符号添加至“额定温度”参数 10
- 添加了*热信息：TLV9062S* 热性能表数据 12
- 向*电气特性：V_S（总电源电压）= (V+) – (V–) = 1.8V 至 5.5V* 表中添加了“关断”部分 13
- 添加了*关断功能*部分 23

Changes from Revision B (October 2017) to Revision C (March 2018) **Page**

- 将器件状态从“量产数据/混合状态”更改为“量产数据” 1
- 删除了*器件信息*表中 TLV9061（DPW，X2SON）封装的预发布说明 1
- 删除了 TLV9061 DPW (X2SON) 封装引脚排列图中的封装预发布说明 4
- 更改了 *ESD 额定值*表的格式以显示所有封装所对应的不同结果 10
- 在以下部分中删除了 DPW (X2SON) 封装的预发布说明：*热性能信息：TLV9061*）表 11
- 在以下部分中删除了 DPW (X2SON) 封装中的封装预发布说明：*热性能信息：TLV9061* 表 11

Changes from Revision A (June 2017) to Revision B (October 2017) **Page**

- 向*引脚配置和功能*部分添加了 8 引脚 PW 封装 4
- 向*热性能信息*表添加了 DSG (WSON) 封装 11
- 向 TLV9062 *热性能信息*表添加了 PW (TSSOP) 封装 11
- 将最大输入失调电压值从 ±1.6mV 更改为 2mV 13
- 将最大输入失调电压值从 ±1.5mV 更改为 ±1.6mV 13
- 将最小共模抑制比输入电压范围从 86dB 更改为 80dB 13
- 将典型输入电流噪声密度值从 10 更改为 23fA/$\sqrt{\text{Hz}}$ 13
- 将 THD + N 测试条件从 V_S = 5V 更改为 V_S = 5.5V 13
- 向*电气特性*表中的 THD + N 参数添加了 V_{CM} = 2.5V 测试条件 13
- 添加了 25mV 至 60mV 的最大输出电压摆幅值 13

- 将最大输出电压摆幅值从 15mV 更改为 20mV 13

Changes from Revision * (March 2017) to Revision A (June 2017) **Page**

- 将器件状态从“预告信息”更改为“量产数据” 1

10 机械、封装和可订购信息

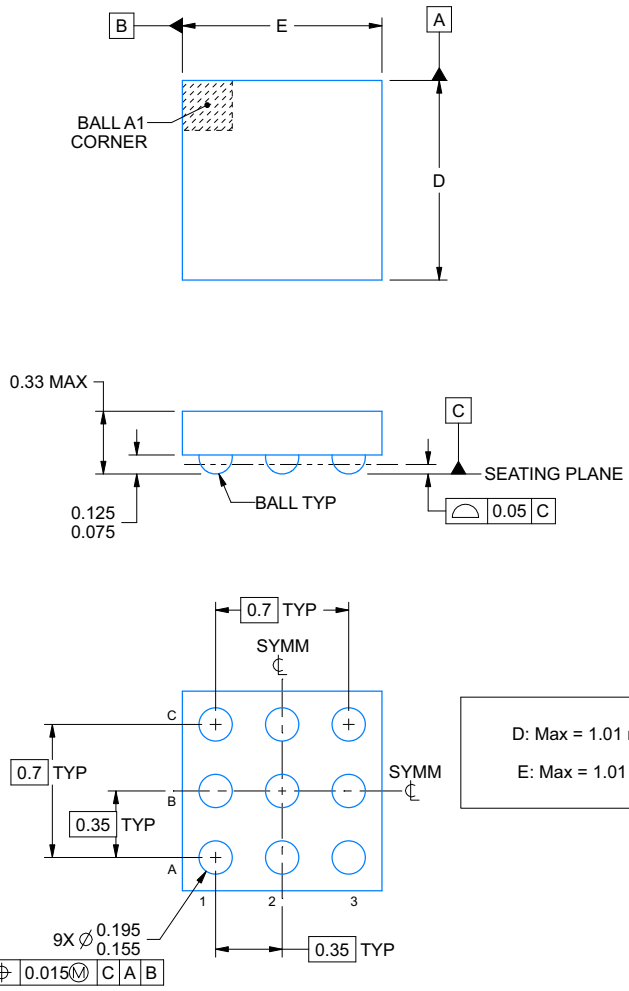
以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

PACKAGE OUTLINE

YCK0009-C01

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

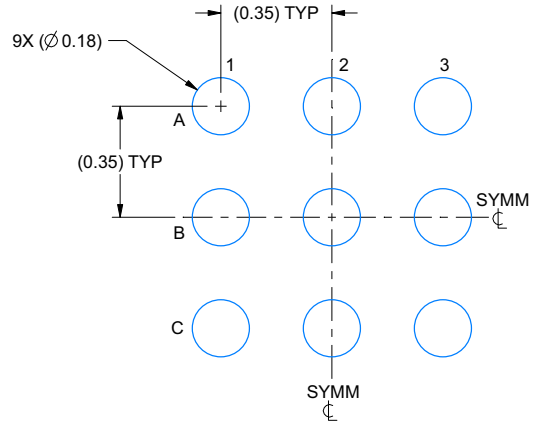
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

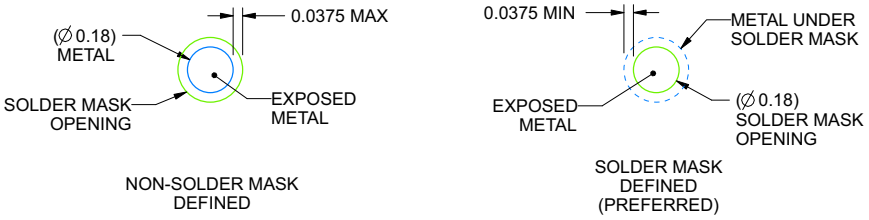
YCK0009-C01

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

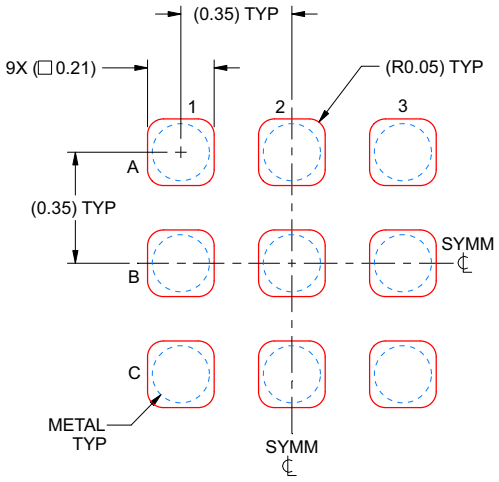
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCK0009-C01

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9061IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1OAF
TLV9061IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OAF
TLV9061IDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OAF
TLV9061IDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OAF
TLV9061IDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1CA
TLV9061IDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1CA
TLV9061IDPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(C, CG)
TLV9061IDPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(C, CG)
TLV9061SIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1OEF
TLV9061SIDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OEF
TLV9061SIDBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OEF
TLV9061SIDBVRG4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OEF
TLV9062IDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062
TLV9062IDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062
TLV9062IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	T062
TLV9062IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T062
TLV9062IDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062
TLV9062IDGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062
TLV9062IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T062
TLV9062IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T062
TLV9062IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9062
TLV9062IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9062
TLV9062IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9062
TLV9062IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9062
TLV9062IDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062
TLV9062IDSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062
TLV9062IDSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062
TLV9062IDSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9062IDSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062
TLV9062IDSGT.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062
TLV9062IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TL9062
TLV9062IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TL9062
TLV9062SIDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1TDX
TLV9062SIDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1TDX
TLV9062SIRUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	EOF
TLV9062SIRUGR.A	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	EOF
TLV9062SIYCKR	Active	Production	DSBGA (YCK) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EH
TLV9062SIYCKR.A	Active	Production	DSBGA (YCK) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EH
TLV9064IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9064D
TLV9064IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9064D
TLV9064IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TLV9064
TLV9064IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9064
TLV9064IPWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TLV9064
TLV9064IPWT.A	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TLV9064
TLV9064IRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9064
TLV9064IRTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9064
TLV9064IRUCR	Active	Production	QFN (RUC) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1DD
TLV9064IRUCR.A	Active	Production	QFN (RUC) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1DD
TLV9064IRUCRG4	Active	Production	QFN (RUC) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1DD
TLV9064IRUCRG4.A	Active	Production	QFN (RUC) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1DD
TLV9064SIRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9064S
TLV9064SIRTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9064S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV9061, TLV9062, TLV9064 :

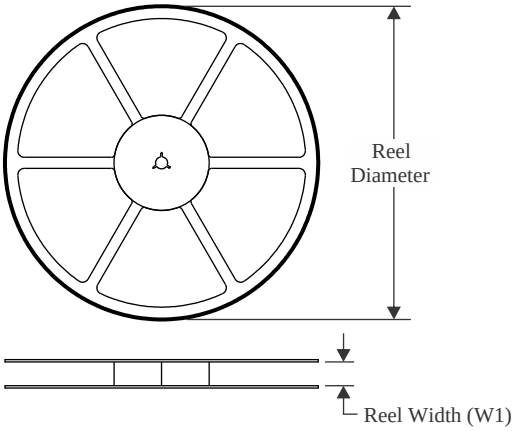
- Automotive : TLV9061-Q1, TLV9062-Q1, TLV9064-Q1

NOTE: Qualified Version Definitions:

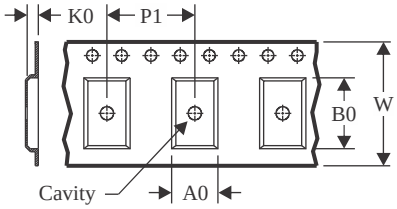
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

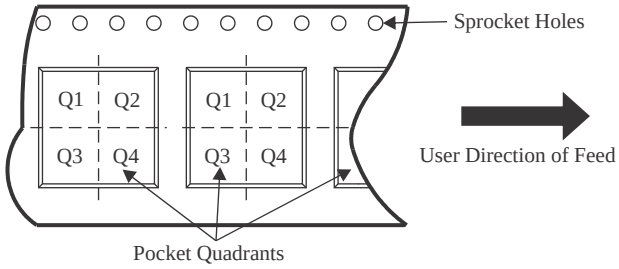


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

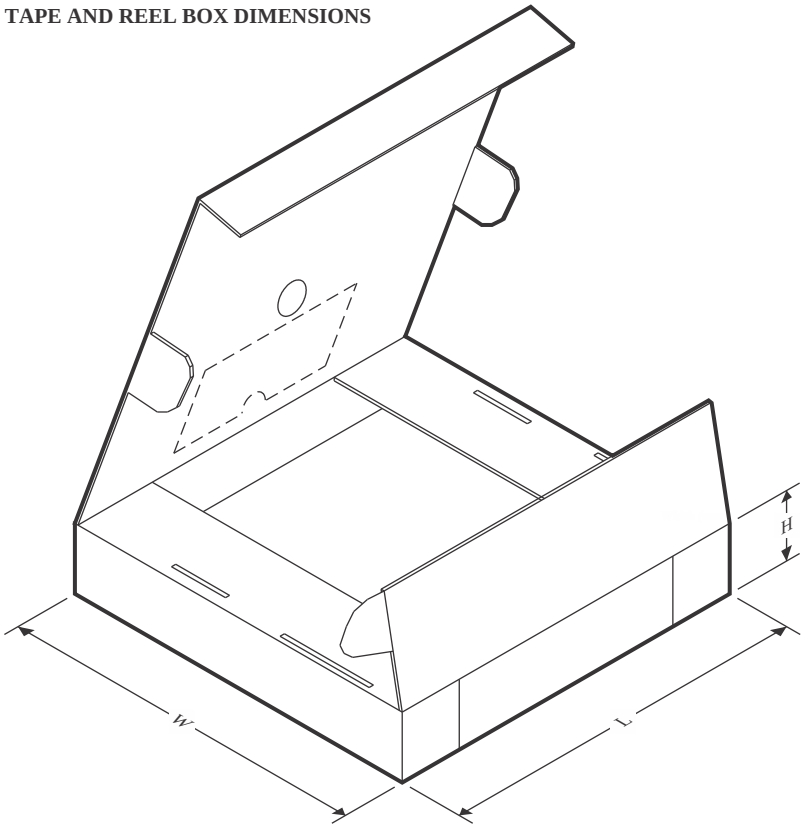


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9061IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061IDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061IDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061IDCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TLV9061IDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV9061IDPWR	X2SON	DPW	5	3000	180.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9061SIDBVR	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061SIDBVRG4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9062IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9062IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9062IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDGKT	VSSOP	DGK	8	250	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9062IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9062SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9062SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
TLV9062SIYCKR	DSBGA	YCK	9	3000	180.0	8.4	1.1	1.1	0.4	2.0	8.0	Q1
TLV9064IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9064IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9064IPWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9064IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV9064IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
TLV9064IRUCRG4	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
TLV9064SIRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

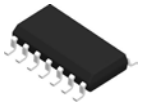
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9061IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061IDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061IDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061IDCKR	SC70	DCK	5	3000	208.0	191.0	35.0
TLV9061IDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV9061IDPWR	X2SON	DPW	5	3000	210.0	185.0	35.0
TLV9061SIDBVR	SOT-23	DBV	6	3000	208.0	191.0	35.0
TLV9061SIDBVRG4	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9062IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9062IDGKR	VSSOP	DGK	8	2500	356.0	356.0	36.0
TLV9062IDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV9062IDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
TLV9062IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV9062IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLV9062IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9062IDSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9062IDSGT	WSON	DSG	8	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9062IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLV9062SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TLV9062SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
TLV9062SIYCKR	DSBGA	YCK	9	3000	182.0	182.0	20.0
TLV9064IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV9064IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV9064IPWT	TSSOP	PW	14	250	353.0	353.0	32.0
TLV9064IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TLV9064IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9064IRUCRG4	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9064SIRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

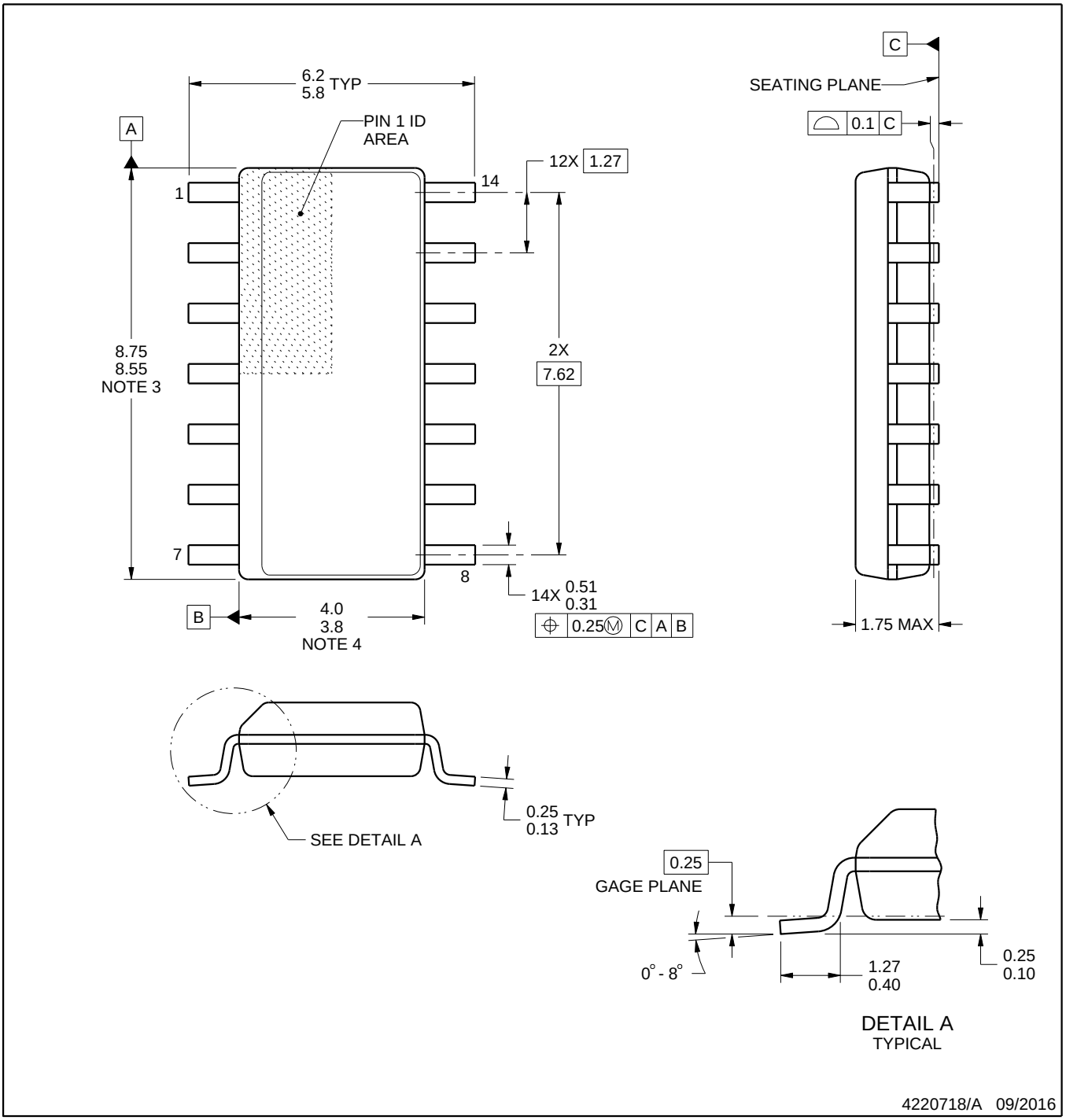


PACKAGE OUTLINE

D0014A

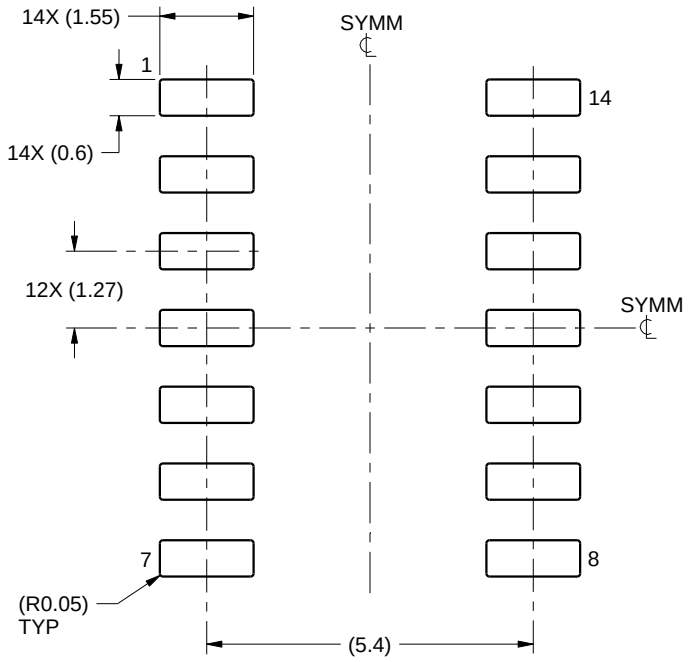
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

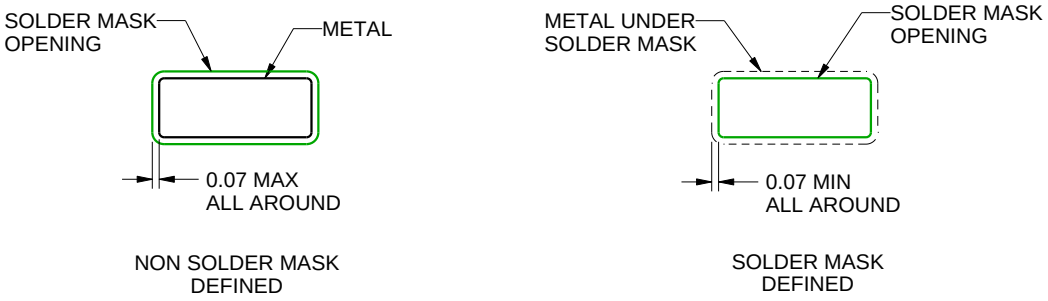


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

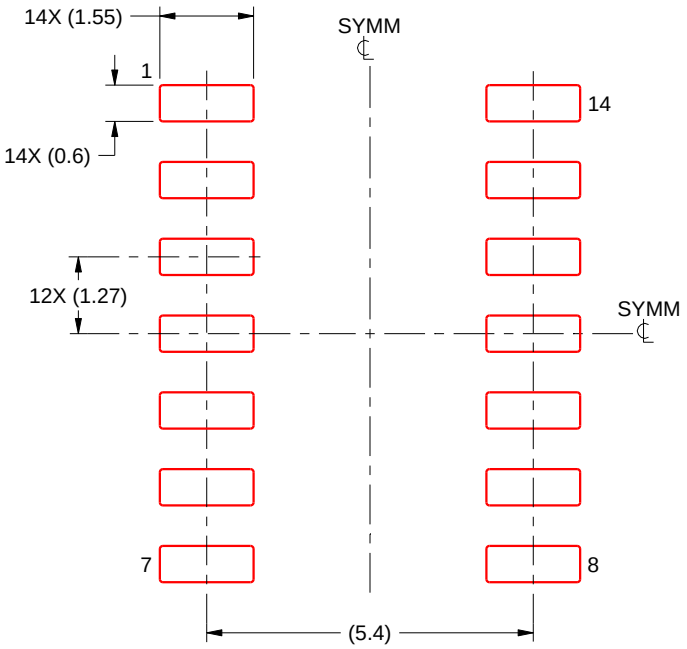
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

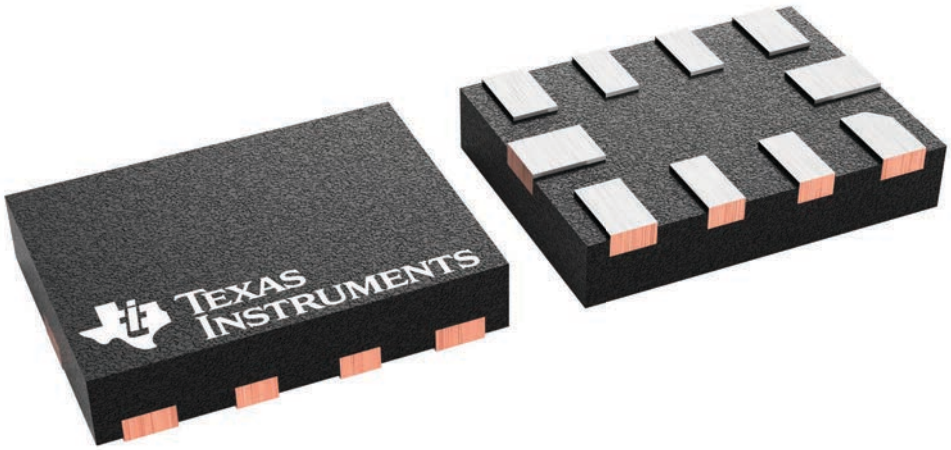
RUG 10

X2QFN - 0.4 mm max height

1.5 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



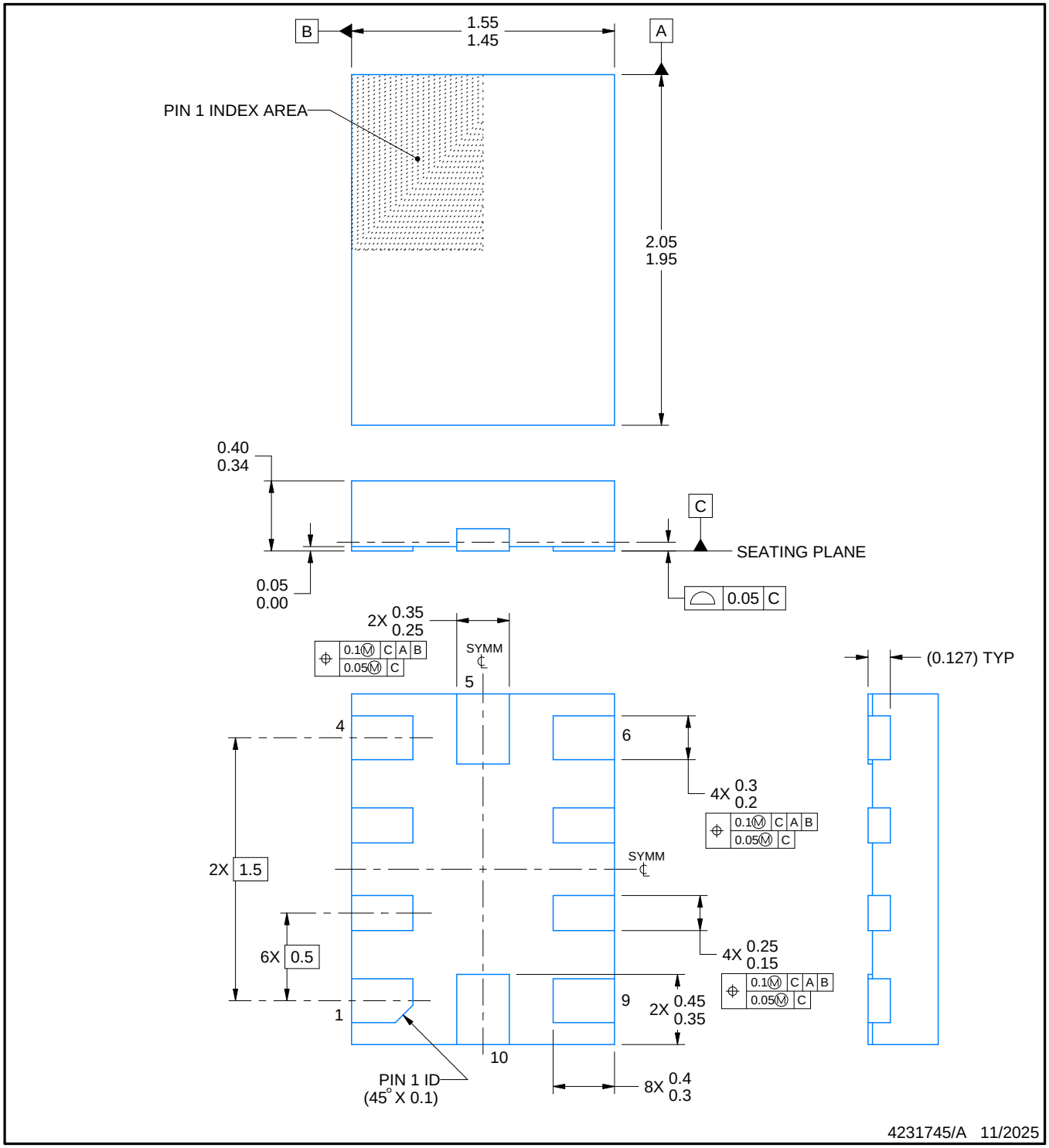
4231768/A

RUG0010A

PACKAGE OUTLINE

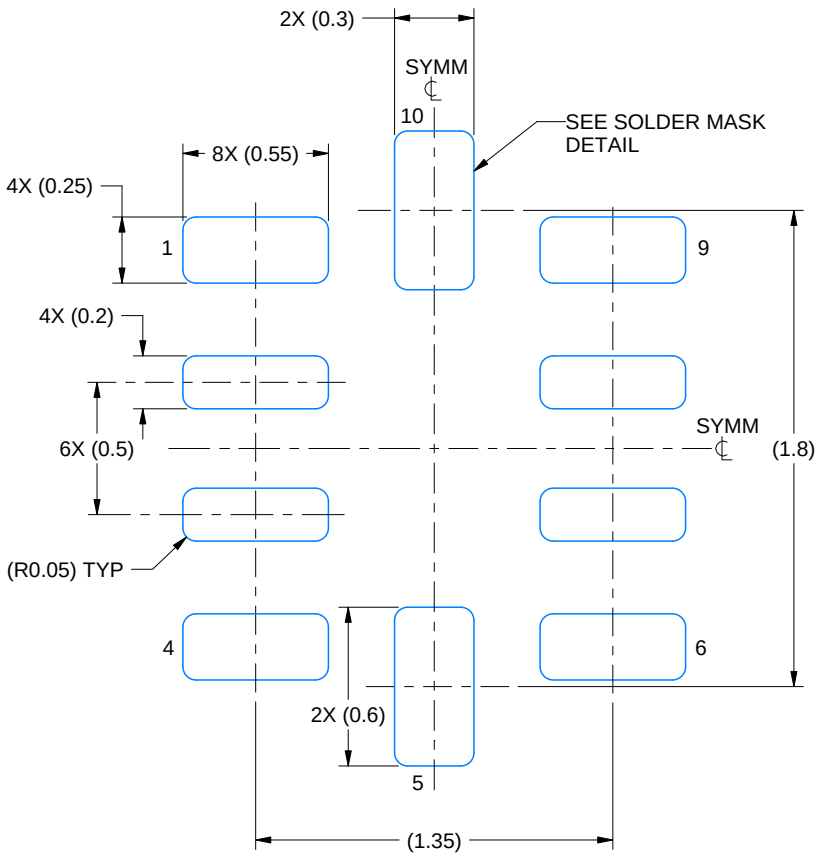
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

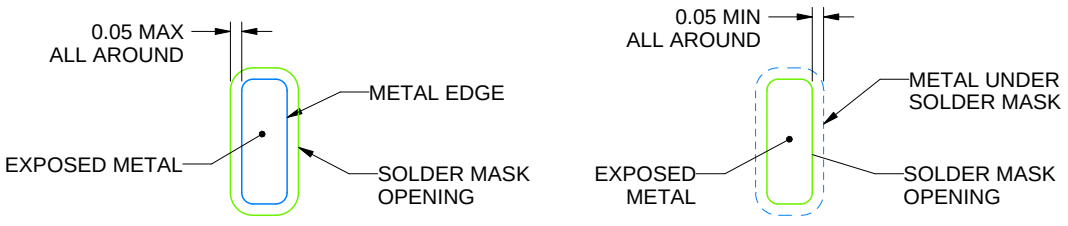


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 35X

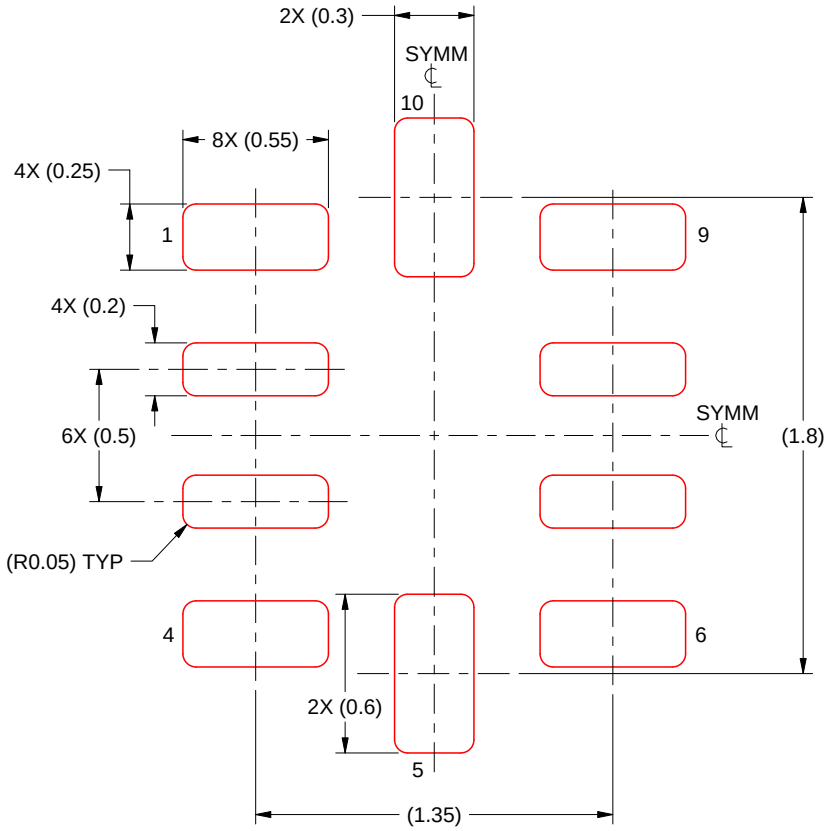


SOLDER MASK DETAILS

4231745/A 11/2025

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 35X

4231745/A 11/2025

NOTES: (continued)

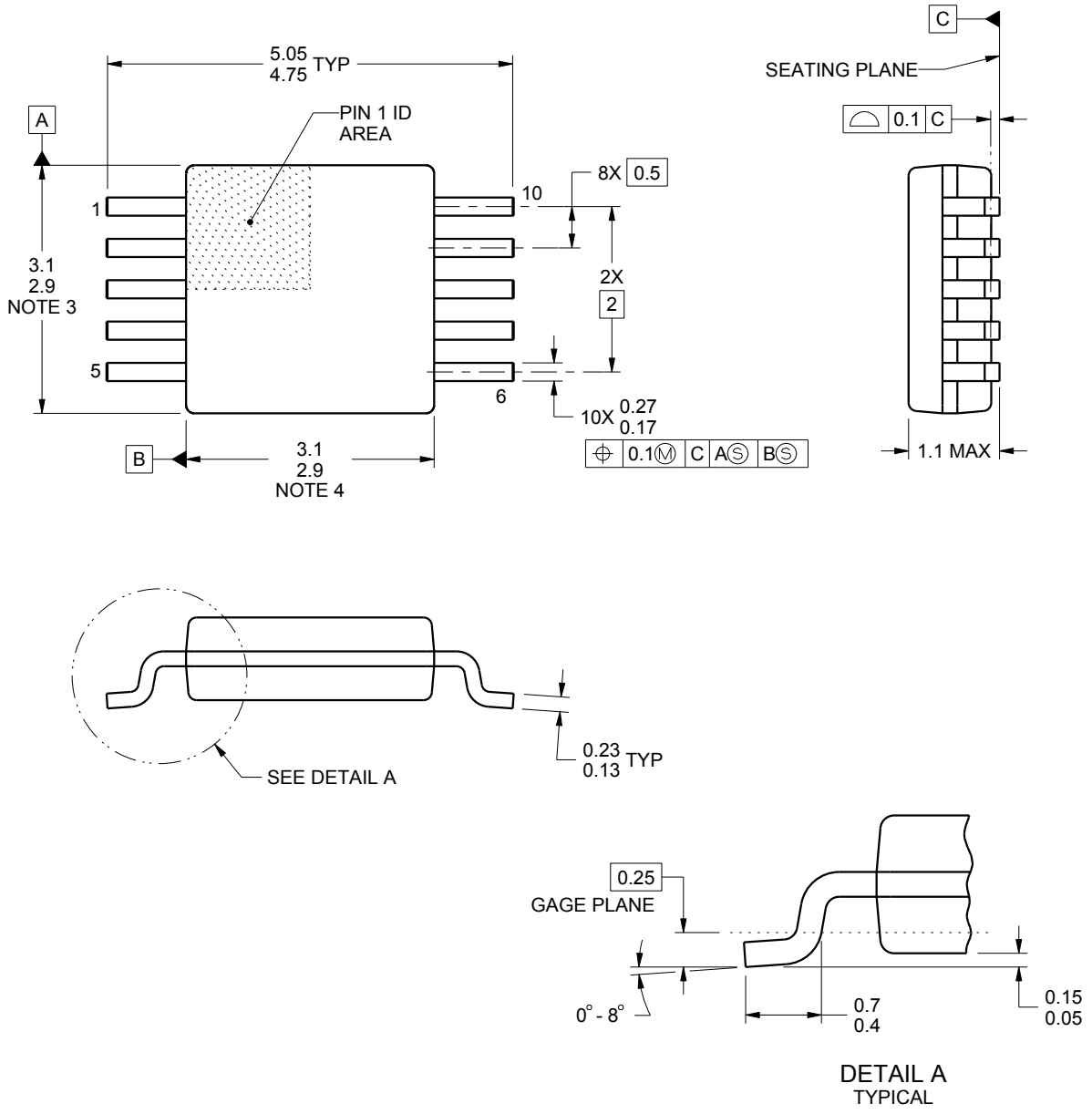
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0010A

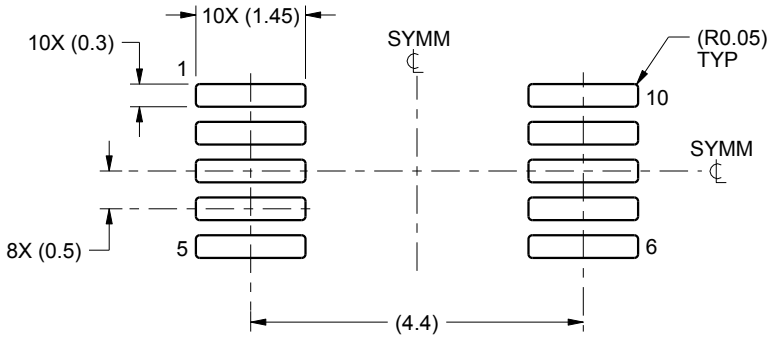
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

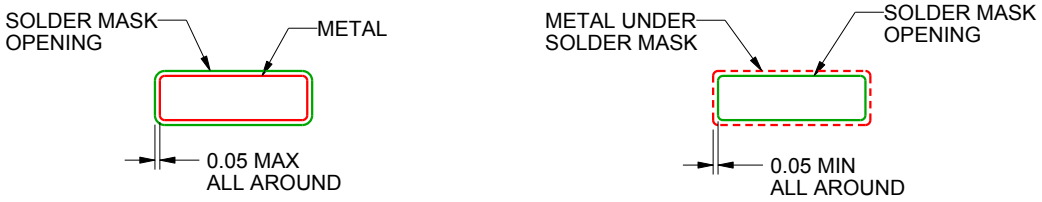


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

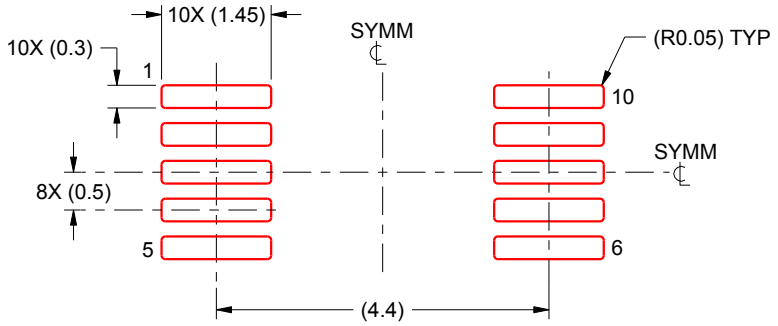


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

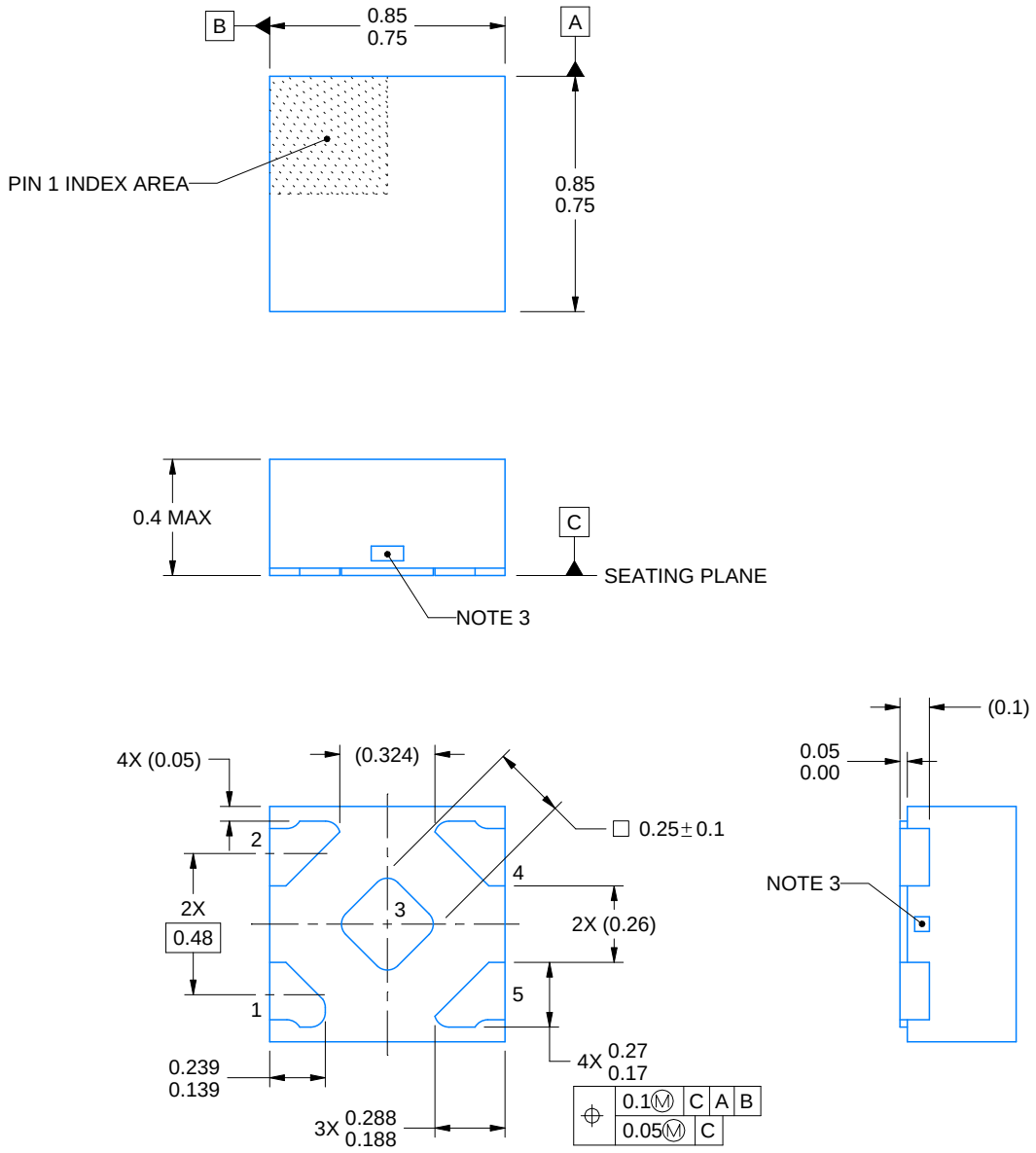
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

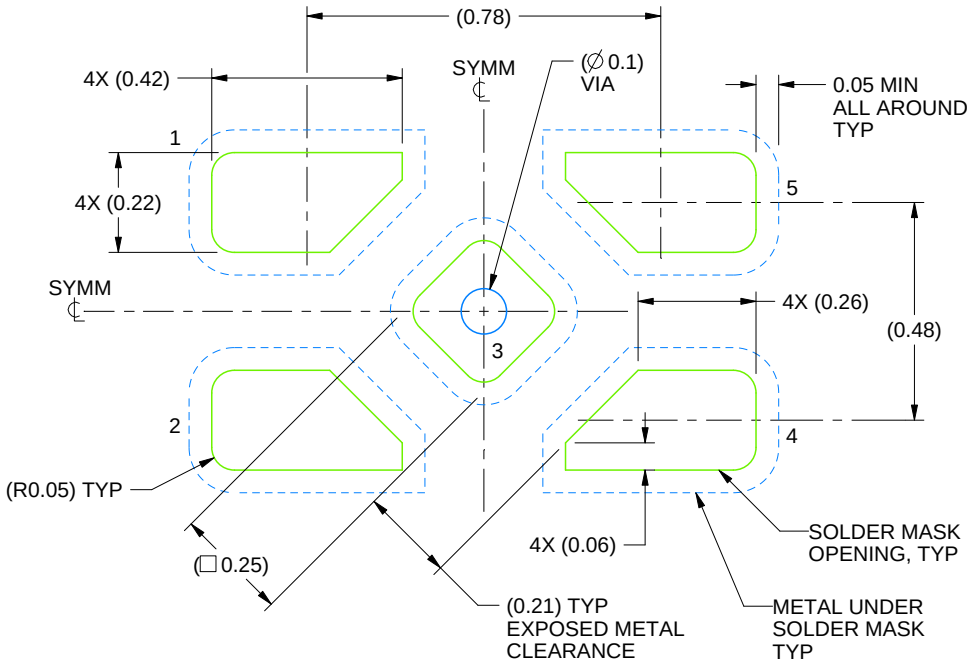
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

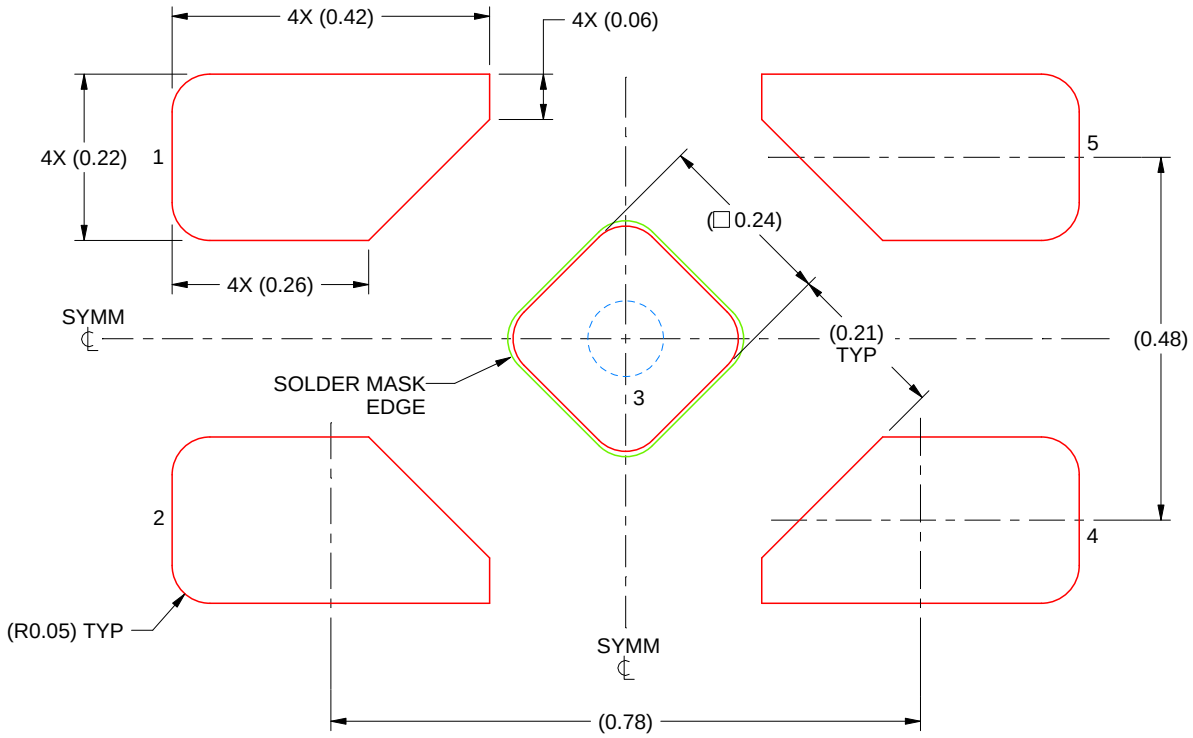
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

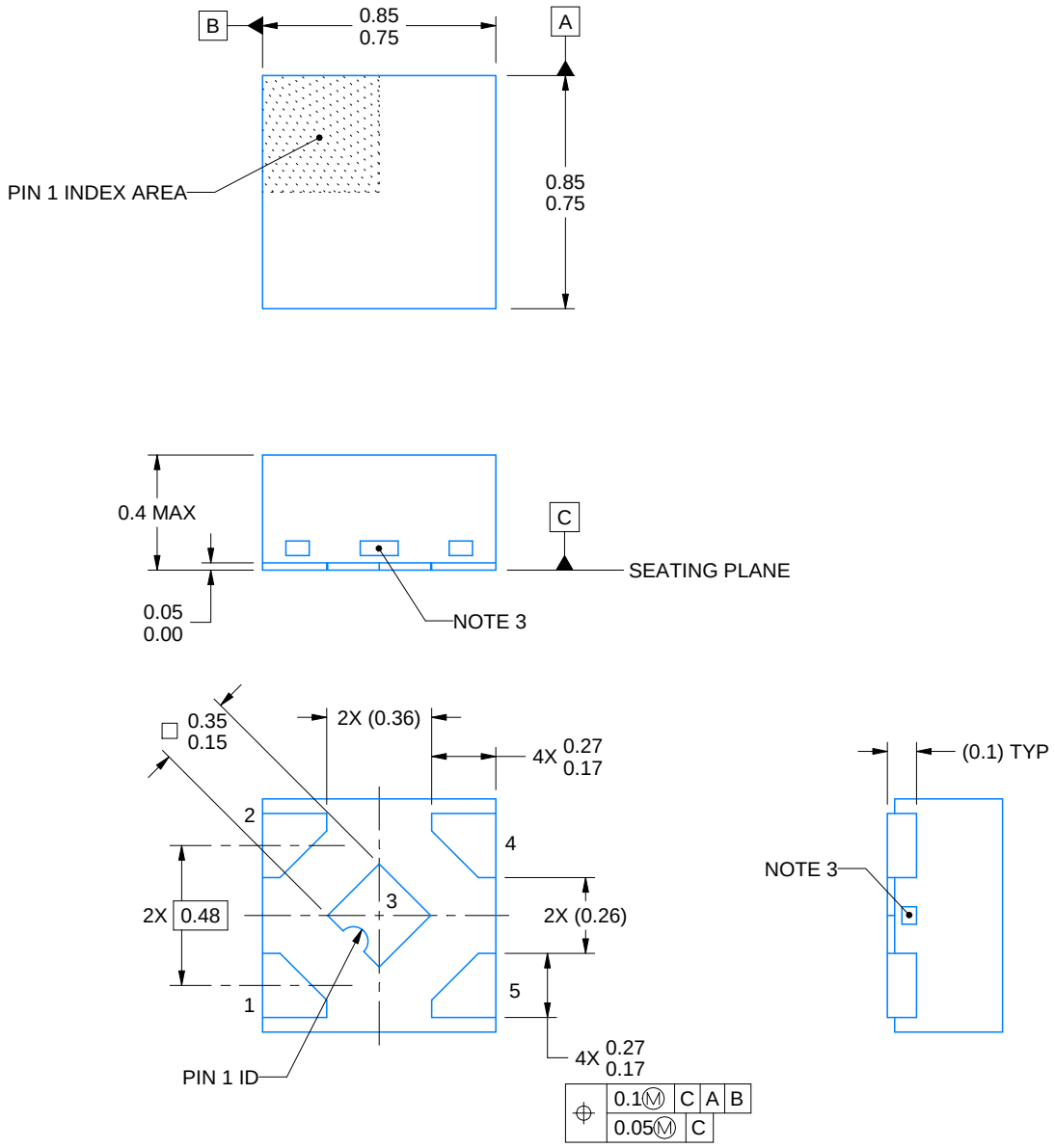
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DPW0005B

X2SON - 0.4 mm max height

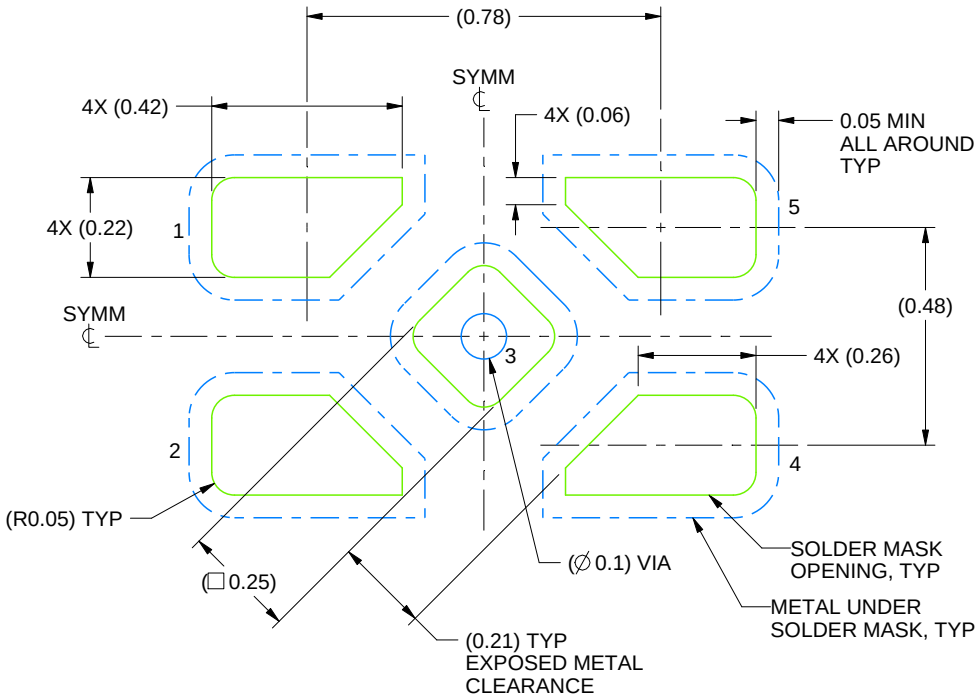
PLASTIC SMALL OUTLINE - NO LEAD



4228233/D 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

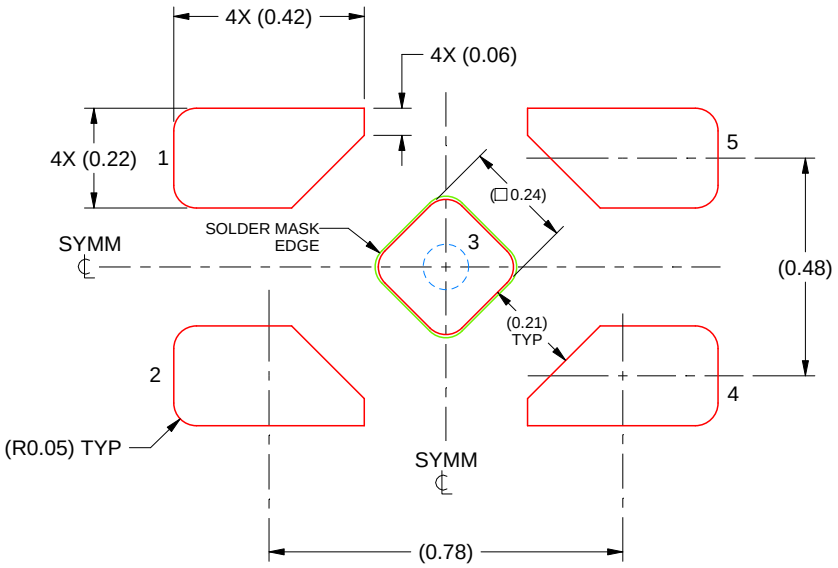


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

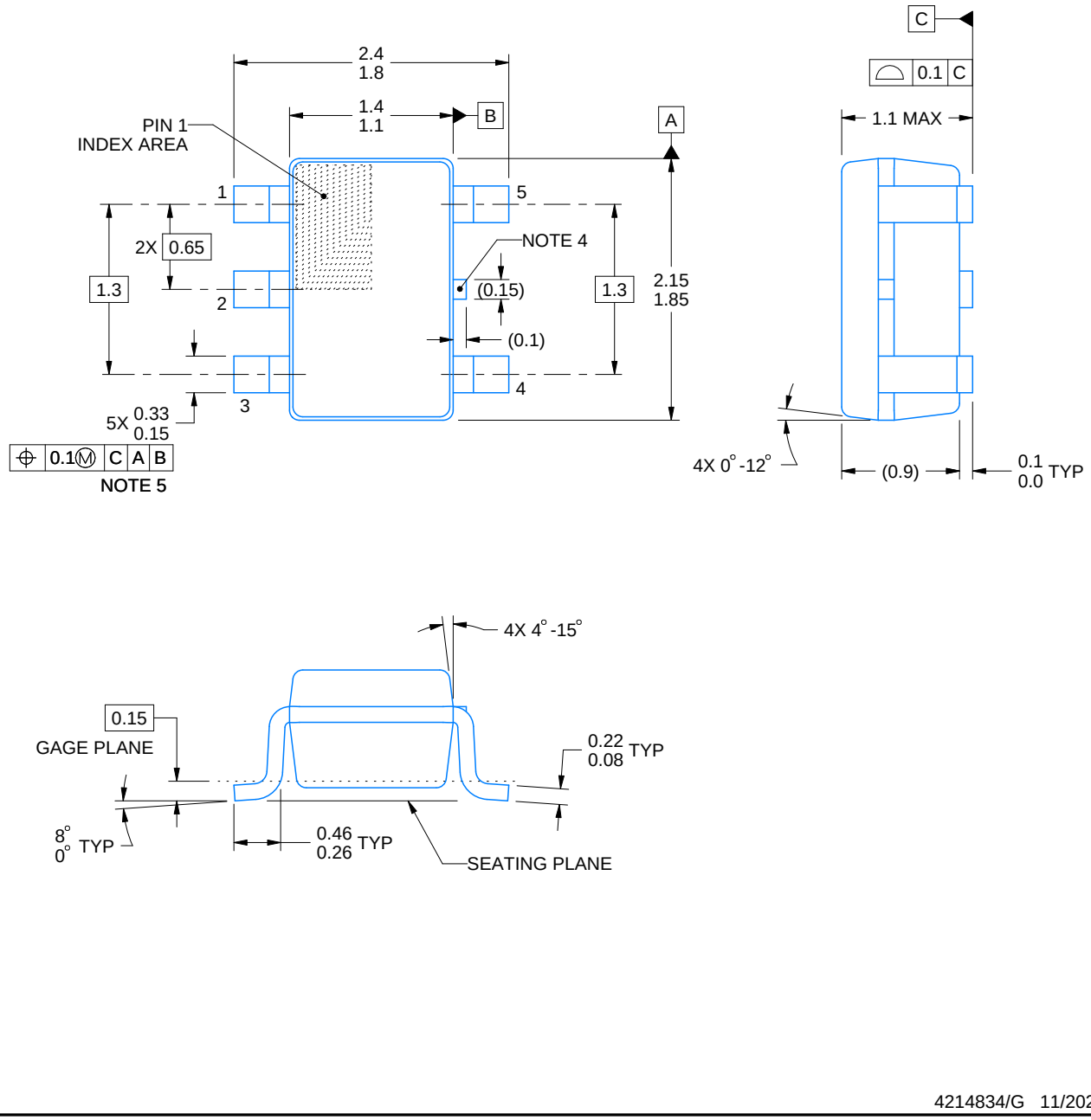
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

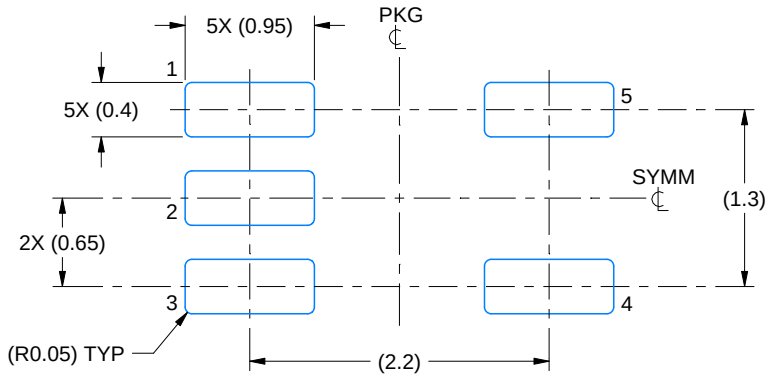
SMALL OUTLINE TRANSISTOR



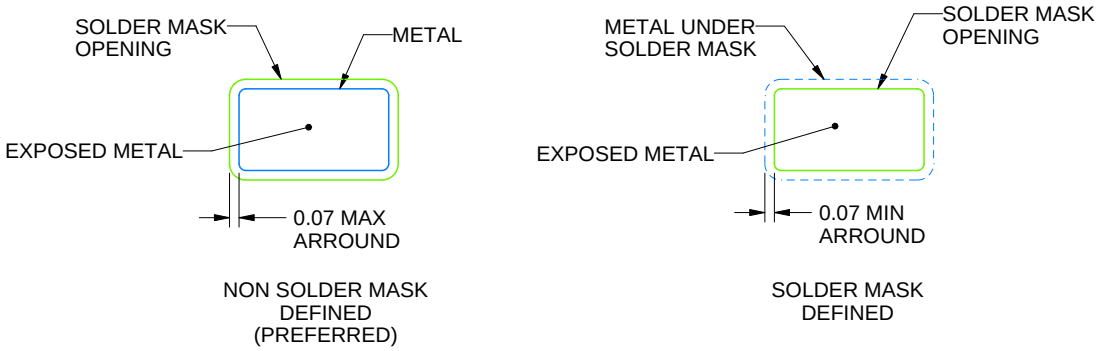
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

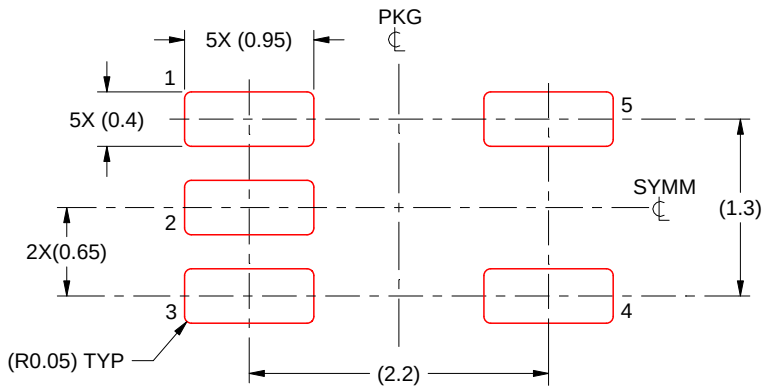


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

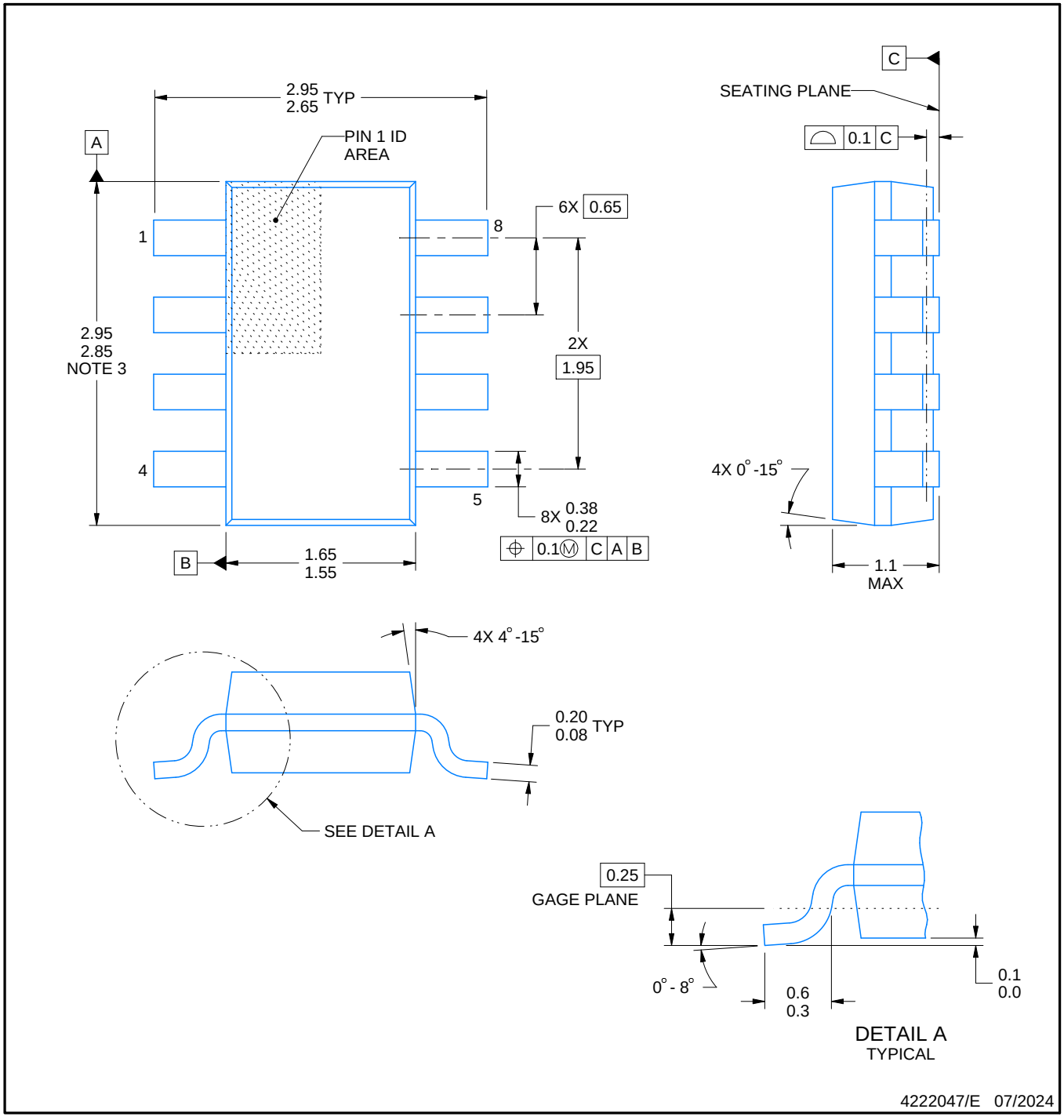
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

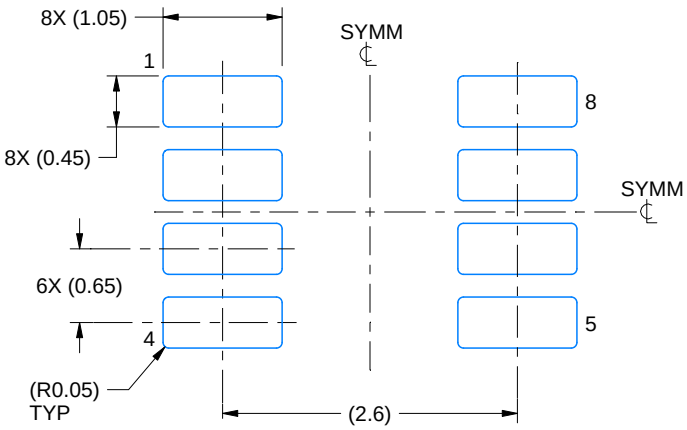
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

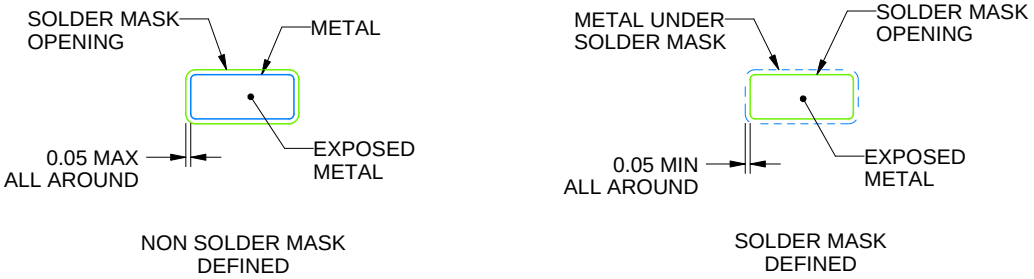


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

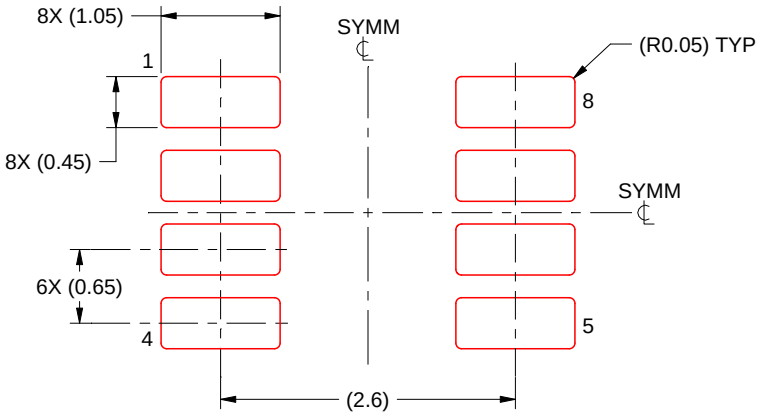
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

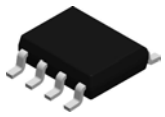


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

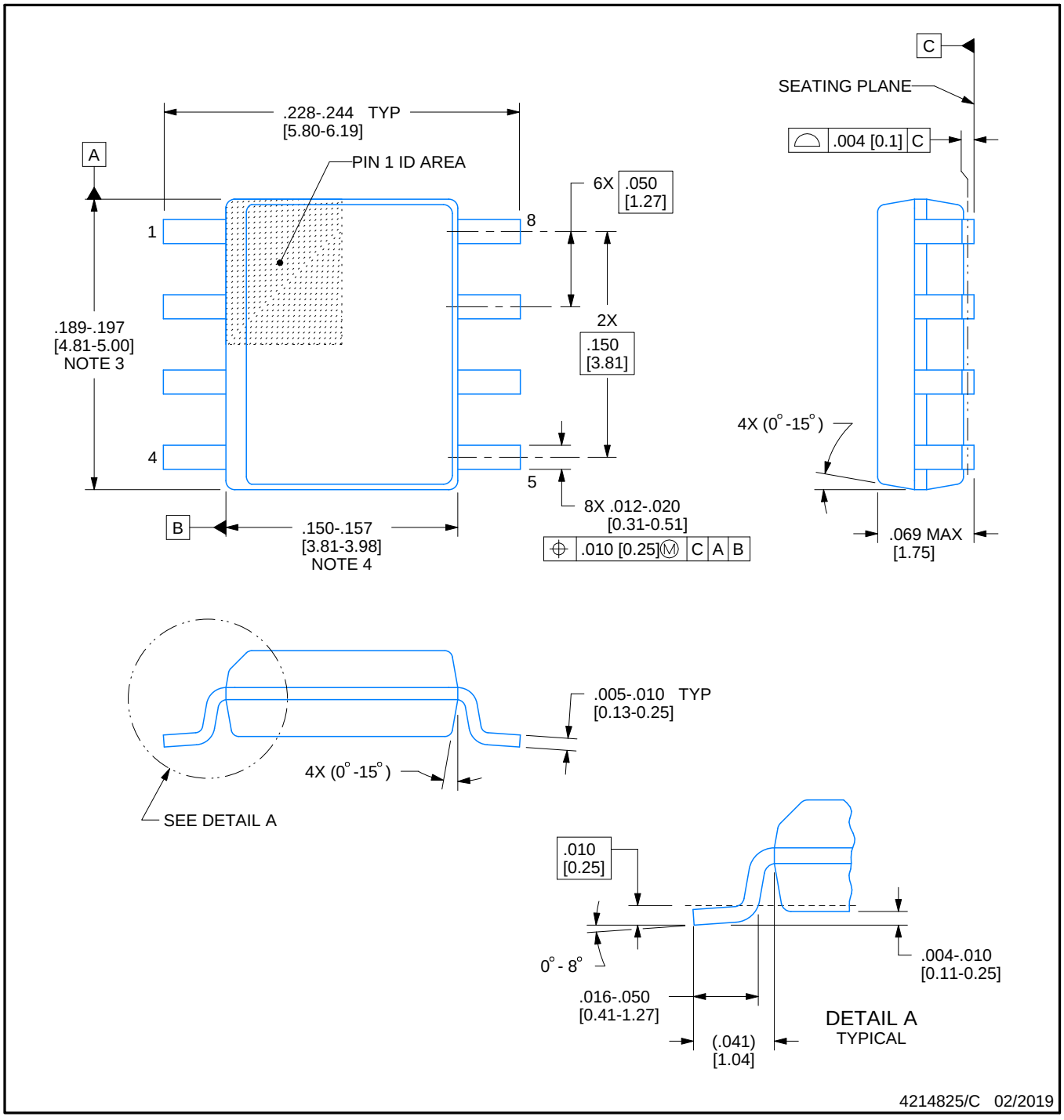


PACKAGE OUTLINE

D0008A

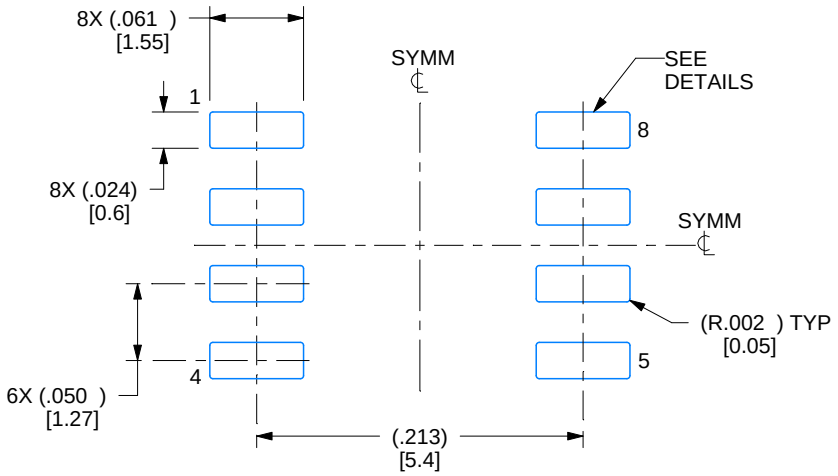
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

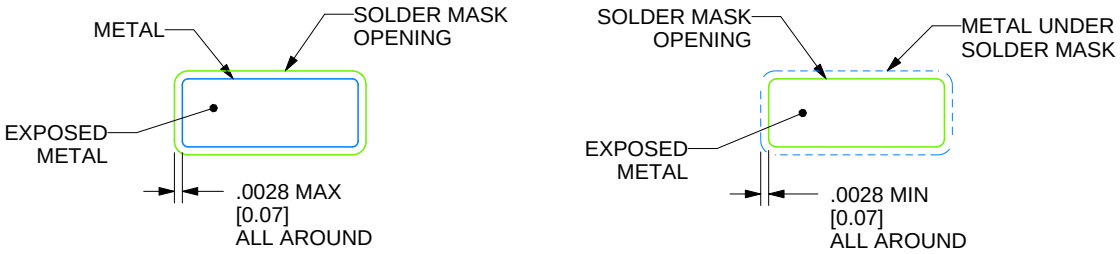


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

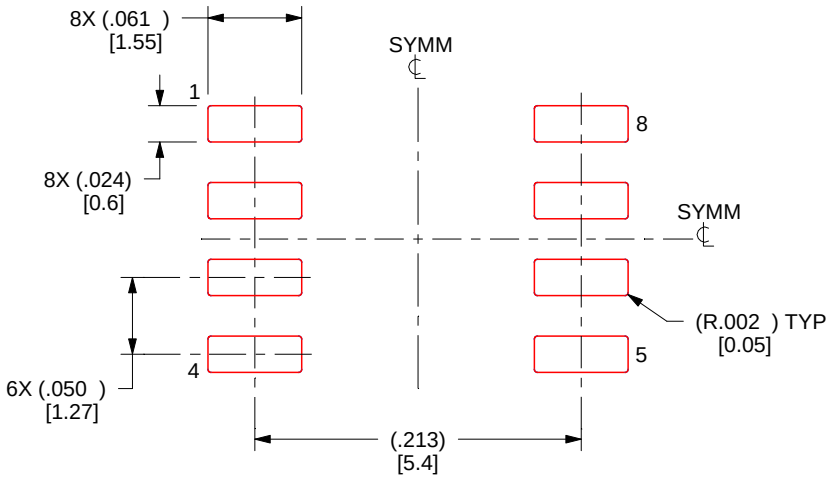
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

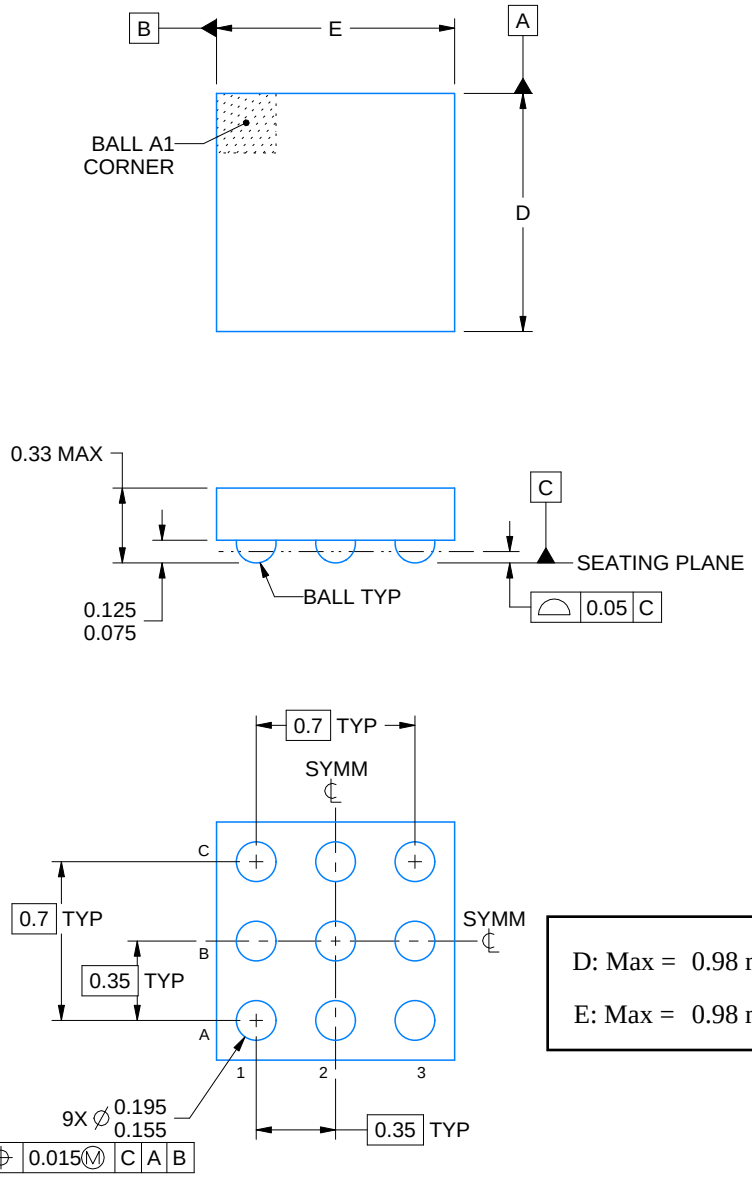
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

YCK0009

PACKAGE OUTLINE

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.98 mm, Min = 0.92 mm

E: Max = 0.98 mm, Min = 0.92 mm

4225837/A 04/2020

NOTES:

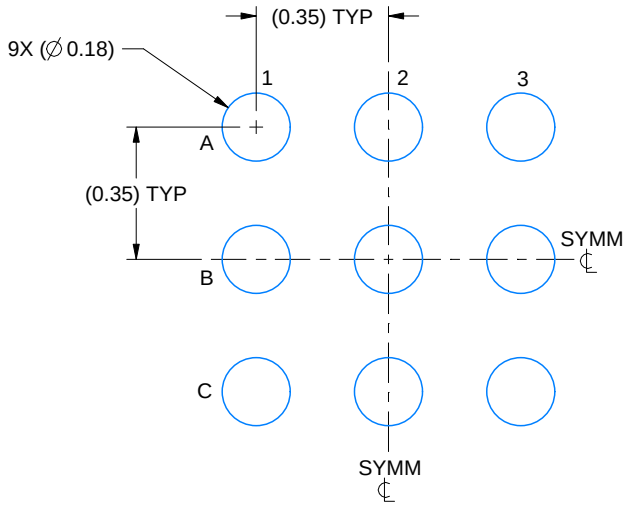
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

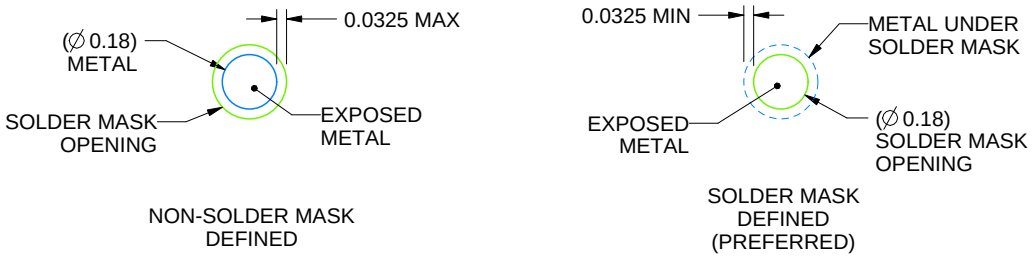
YCK0009

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4225837/A 04/2020

NOTES: (continued)

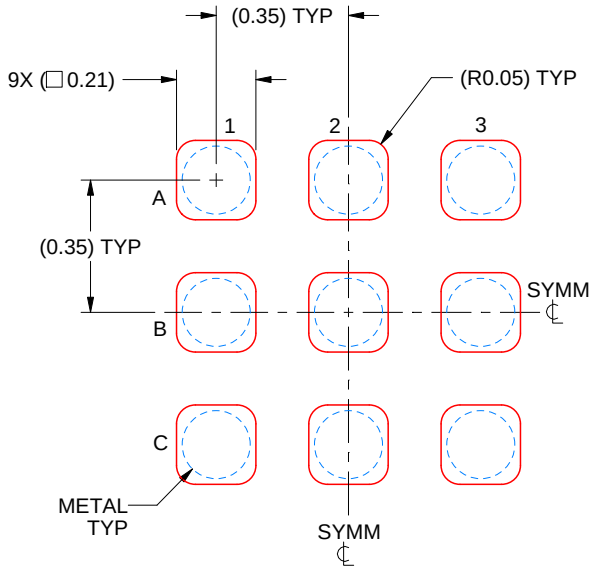
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCK0009

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4225837/A 04/2020

NOTES: (continued)

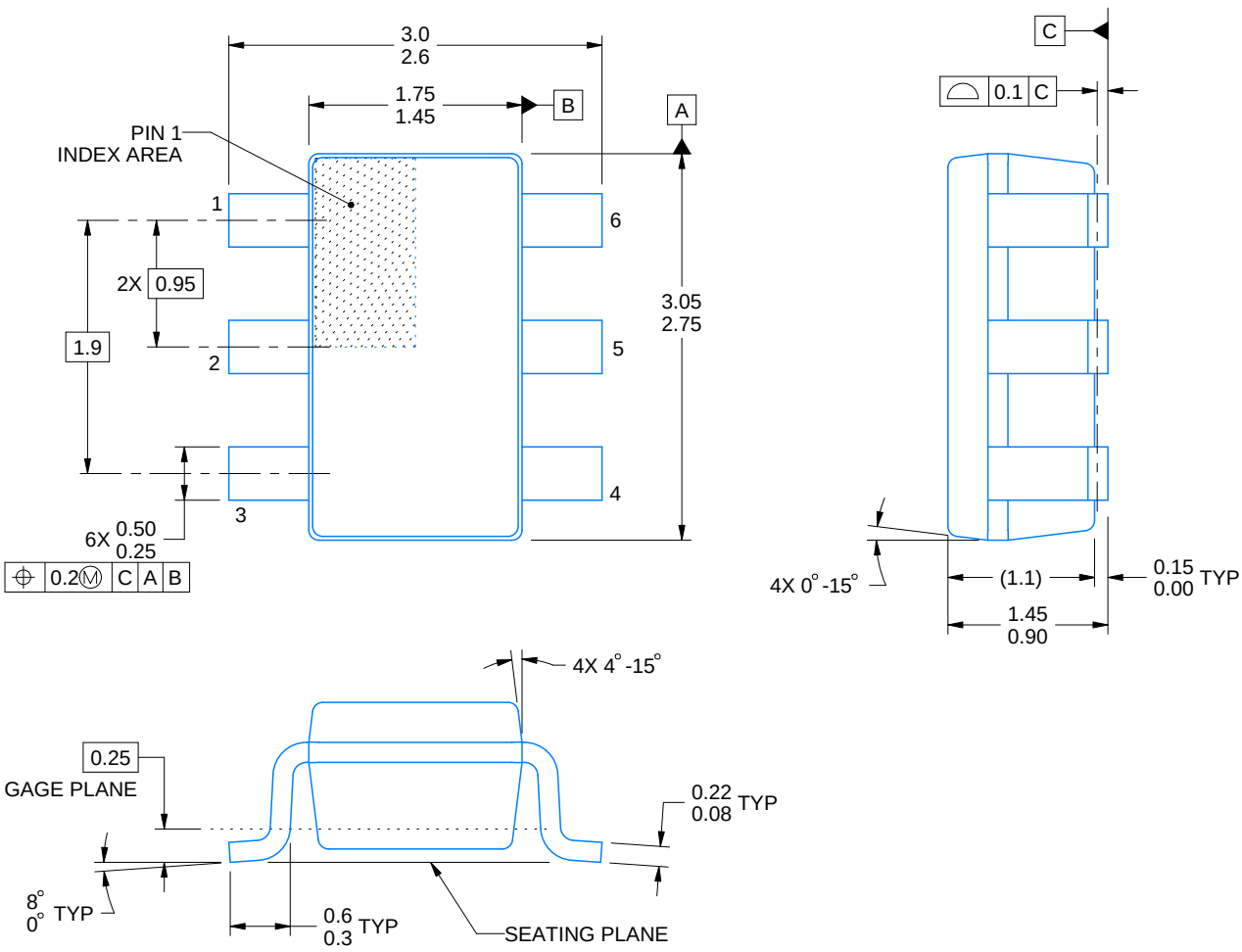
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

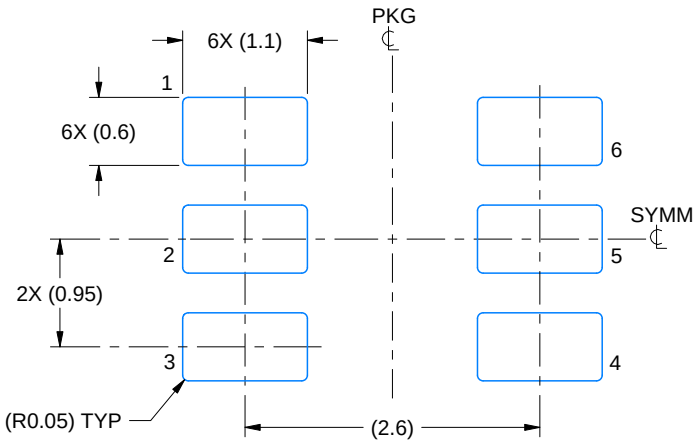
SMALL OUTLINE TRANSISTOR



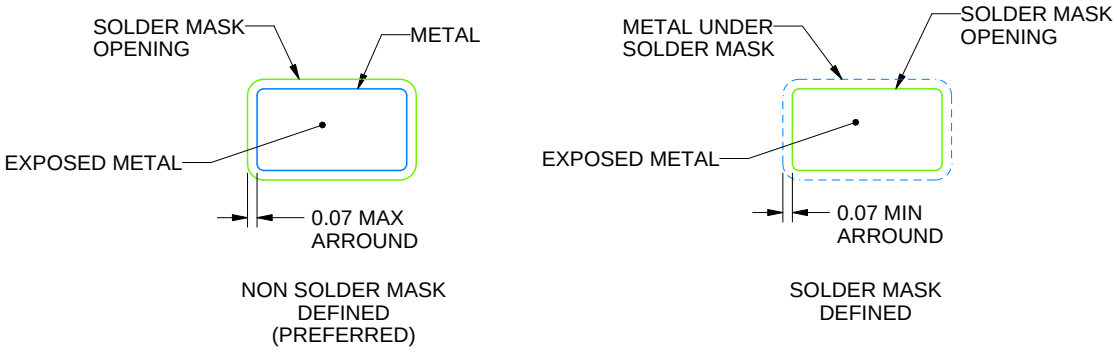
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

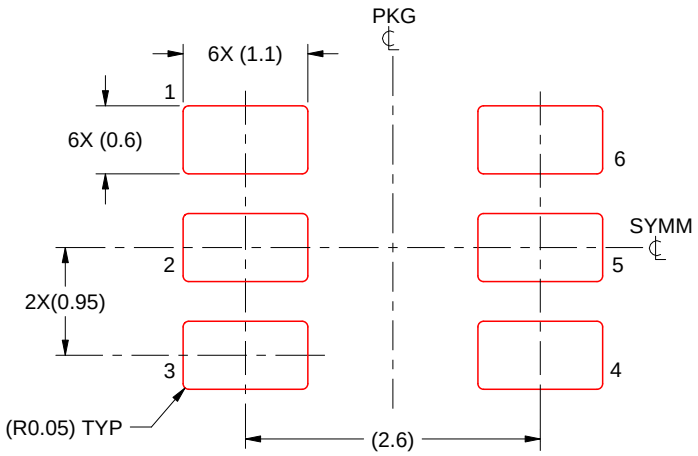


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

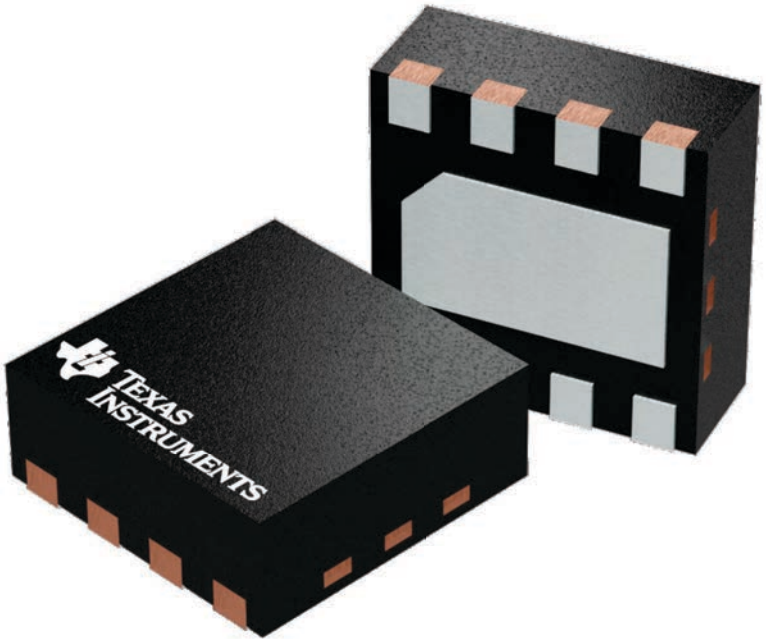
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



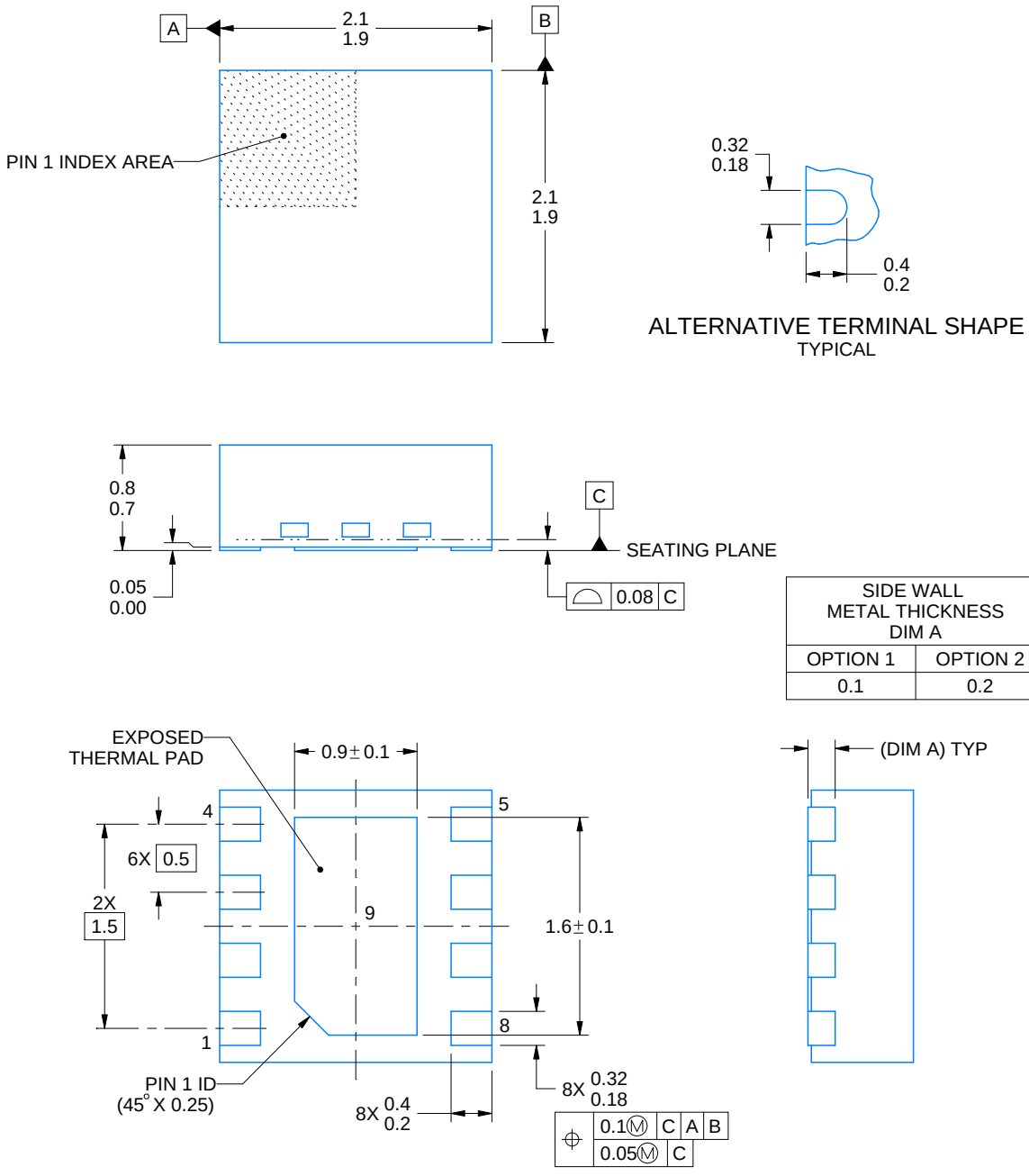
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

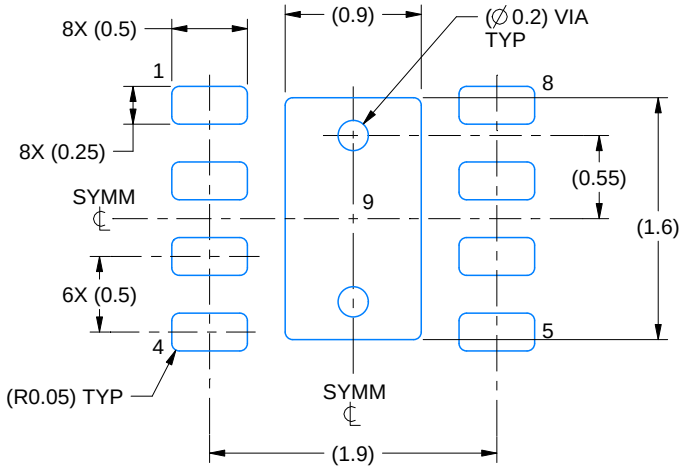
PLASTIC SMALL OUTLINE - NO LEAD



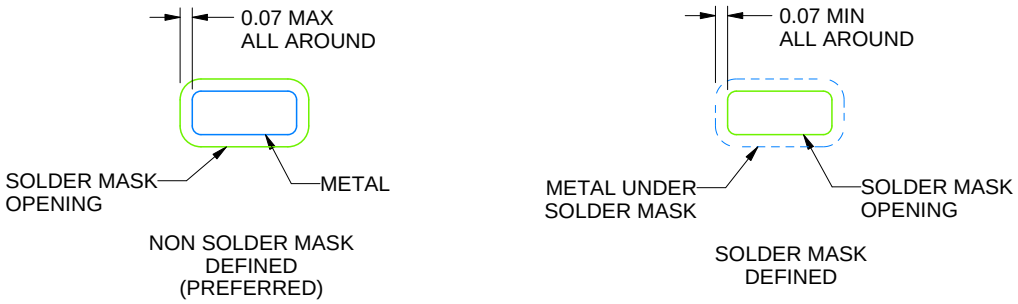
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

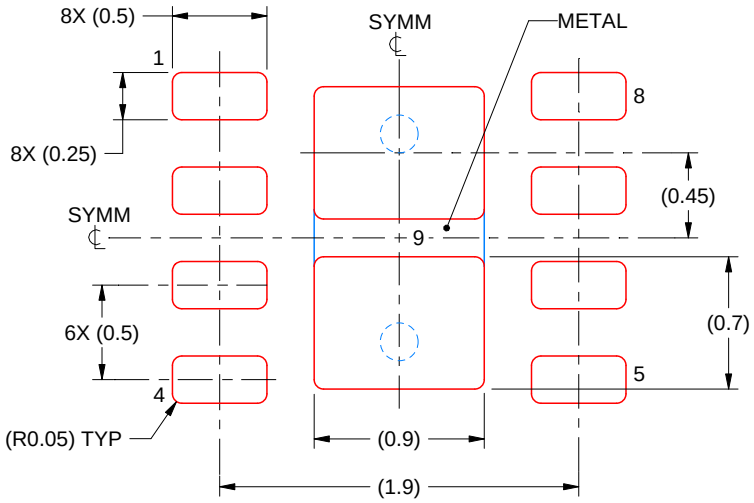


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

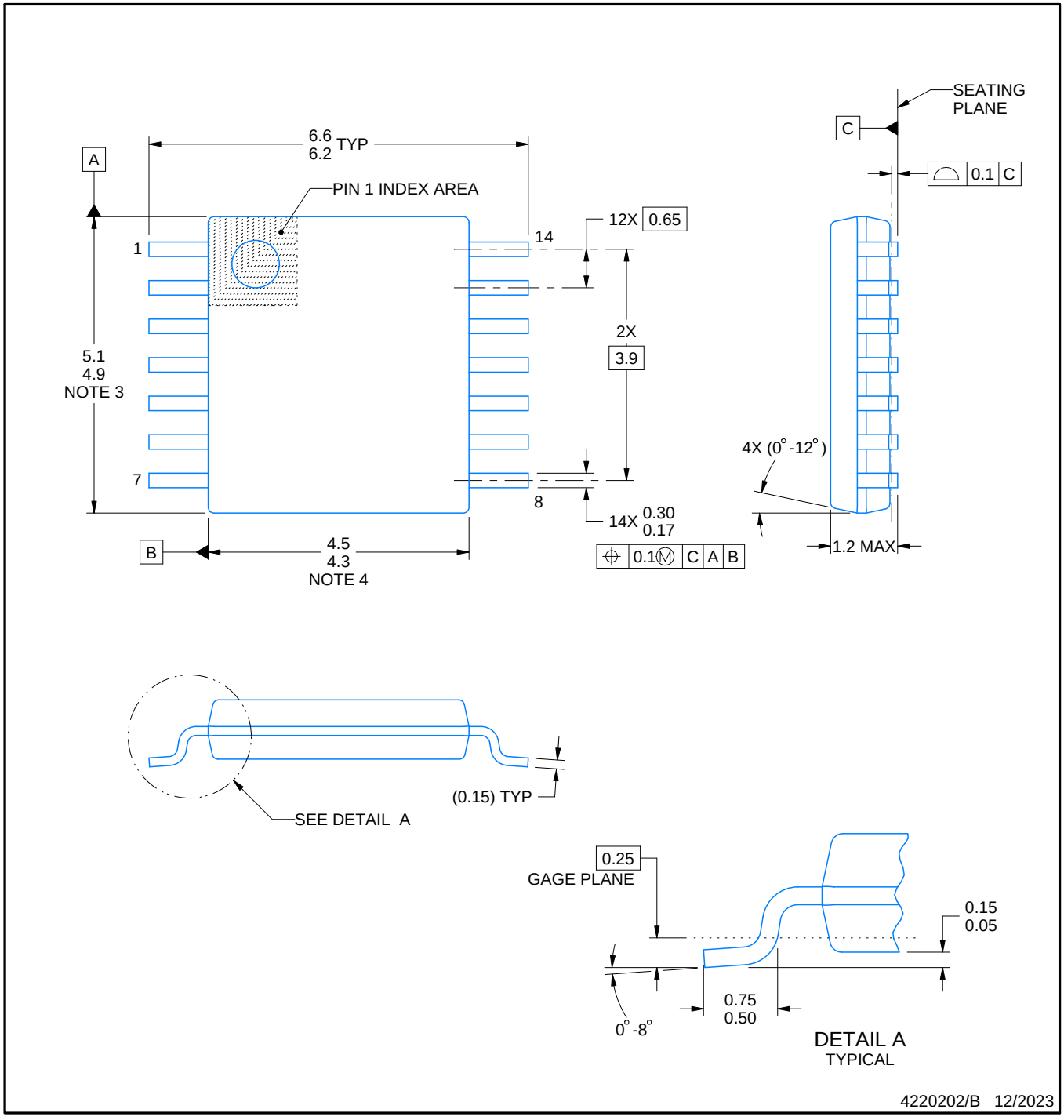
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

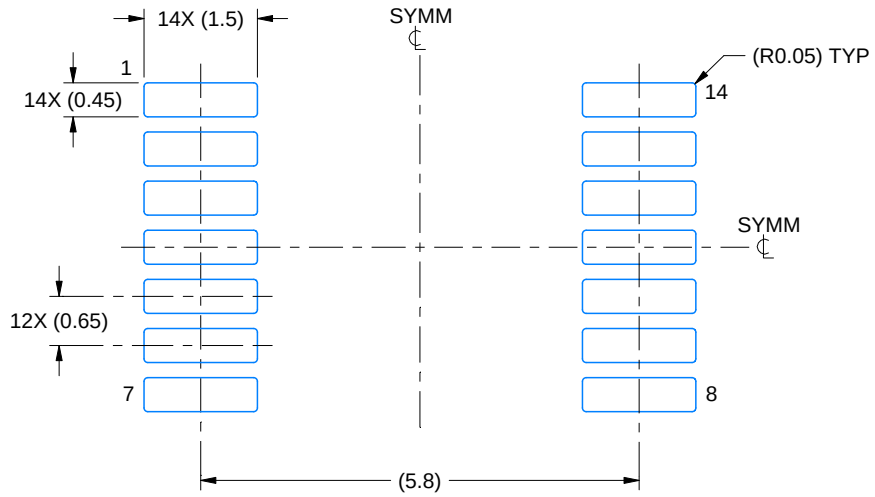
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

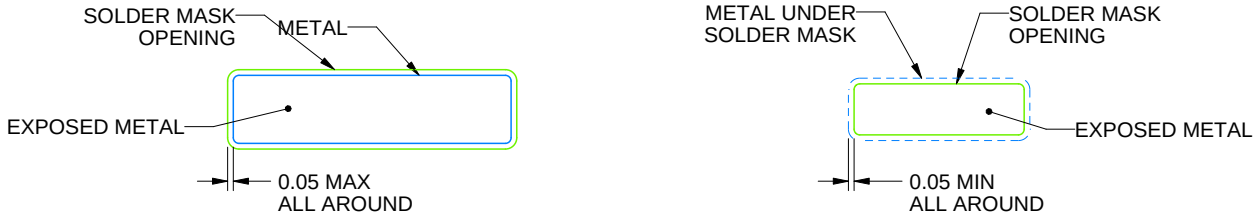


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

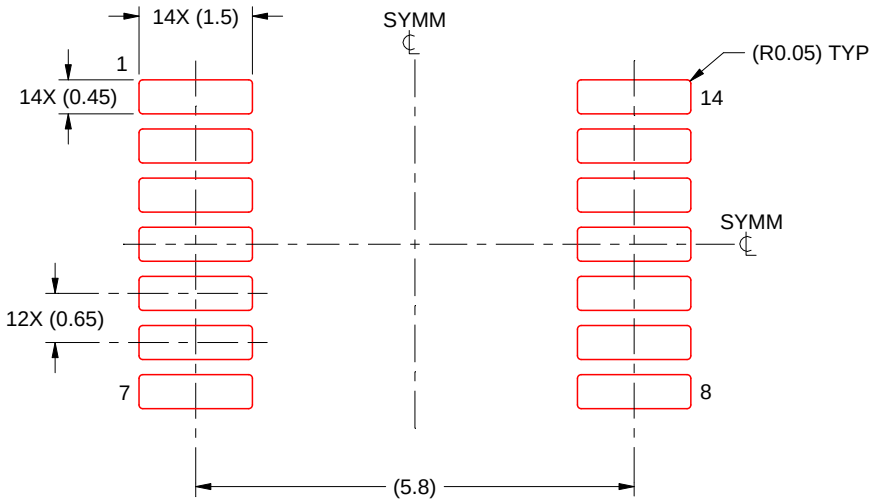


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

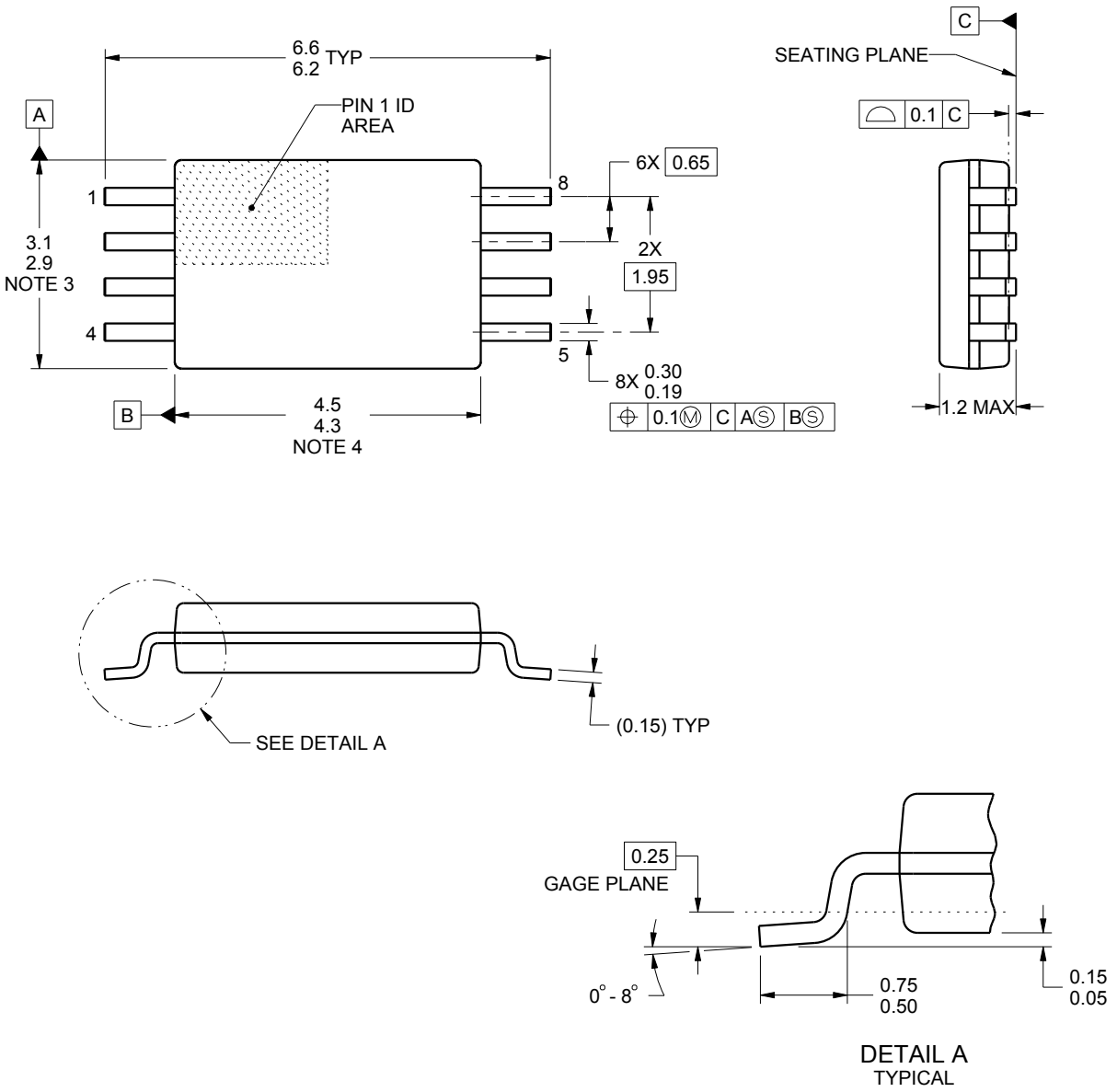
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

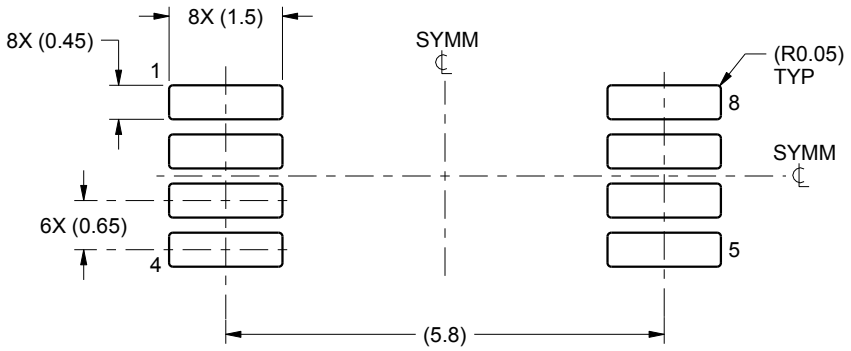
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

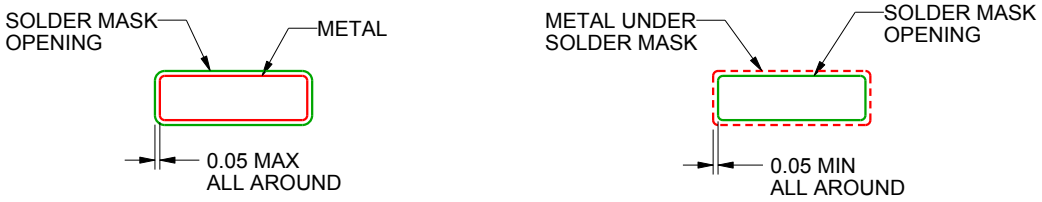


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

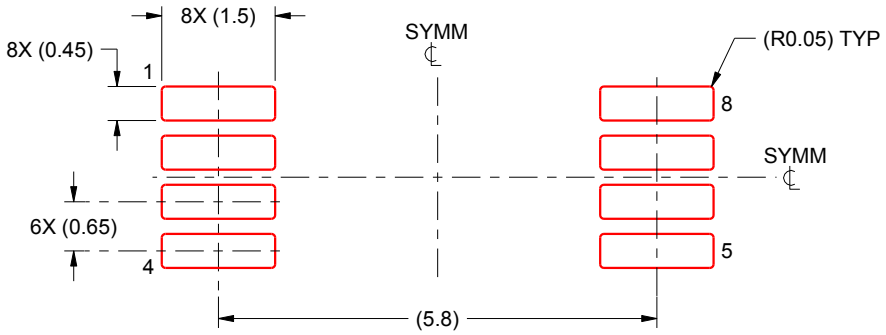


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

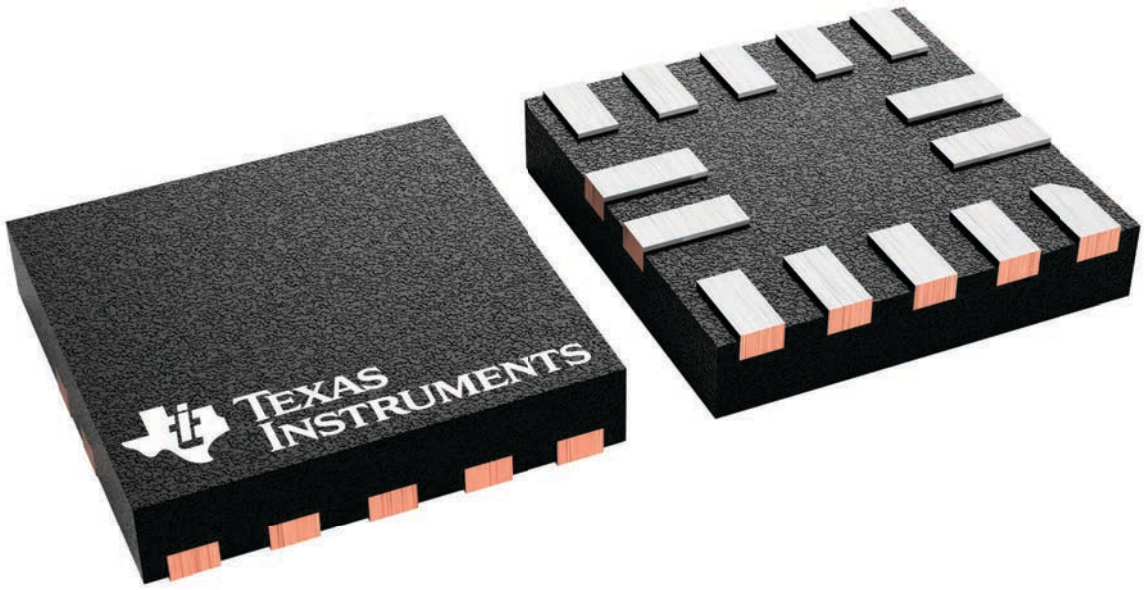
RUC 14

X2QFN - 0.4 mm max height

2 x 2, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

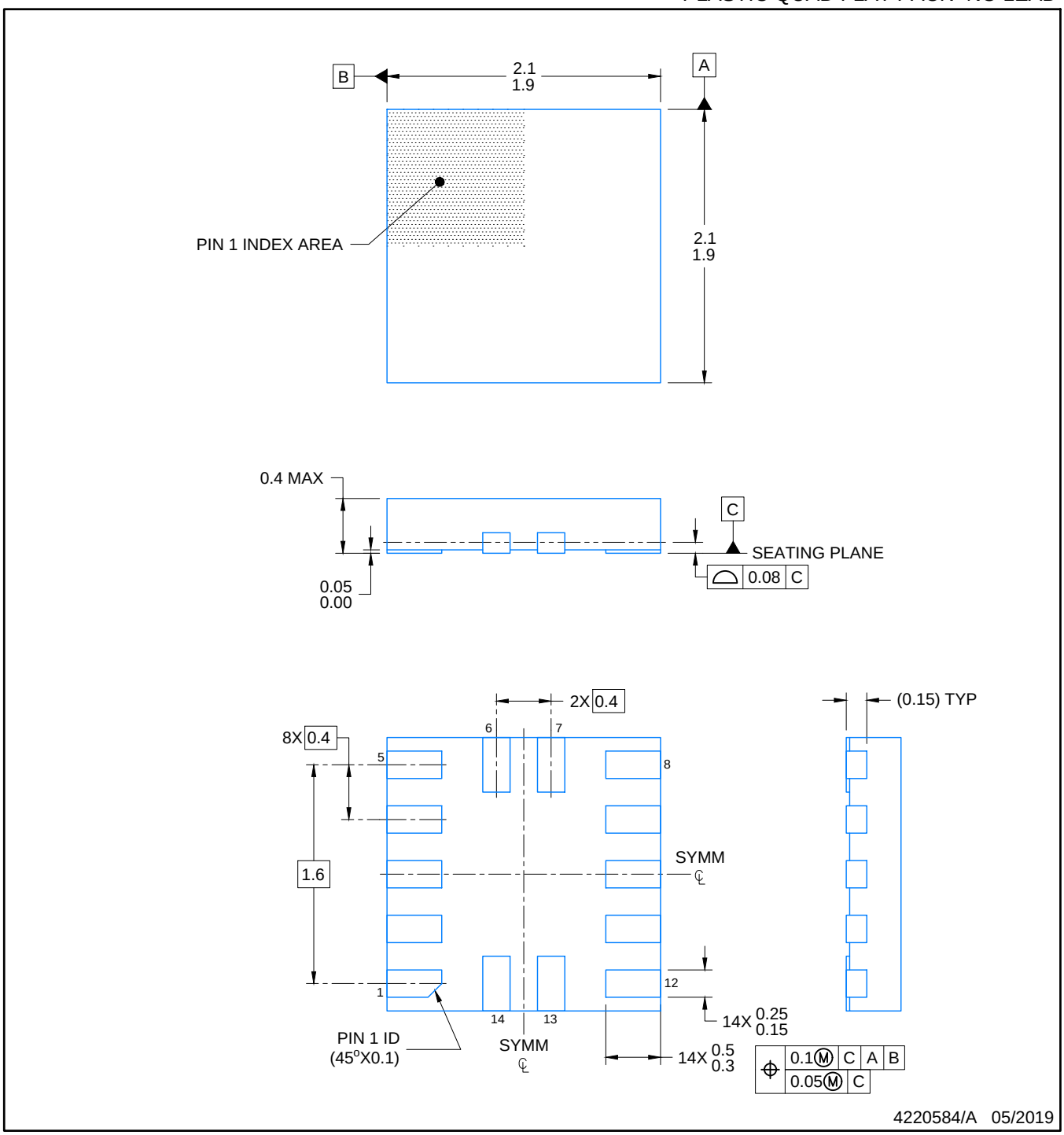


PACKAGE OUTLINE

RUC0014A

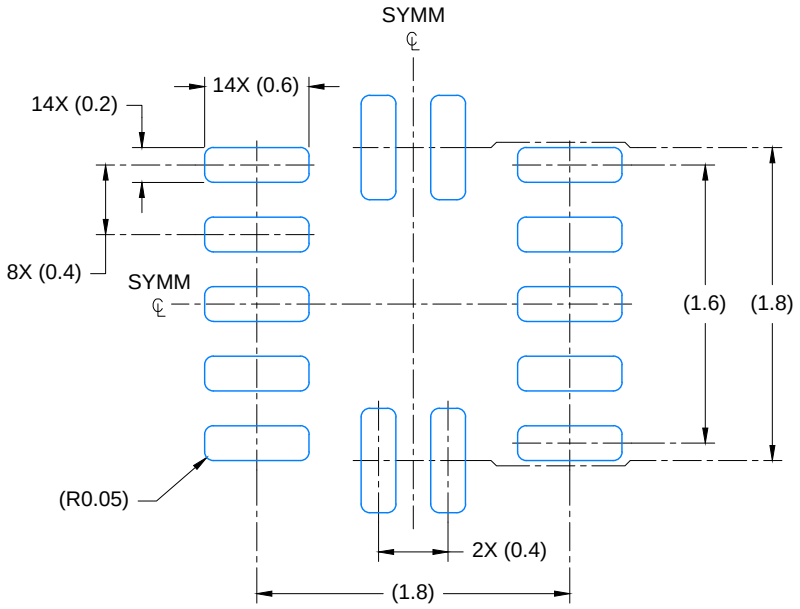
X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

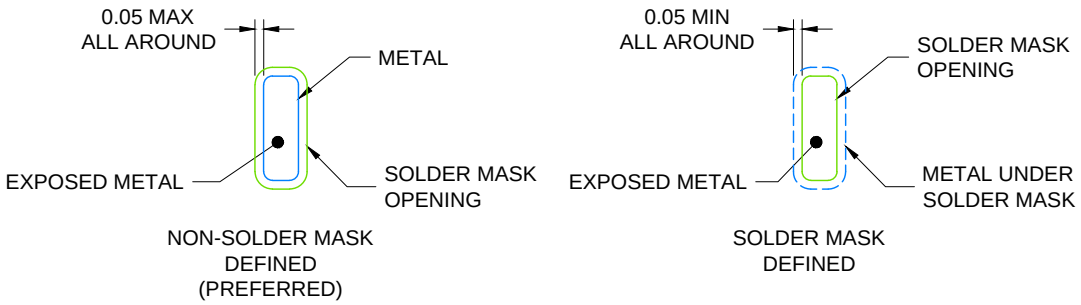


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X

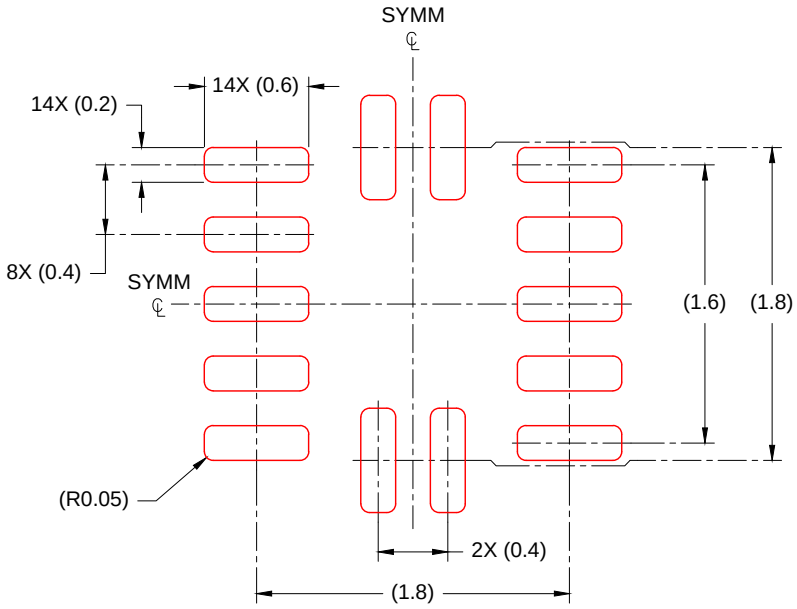


SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

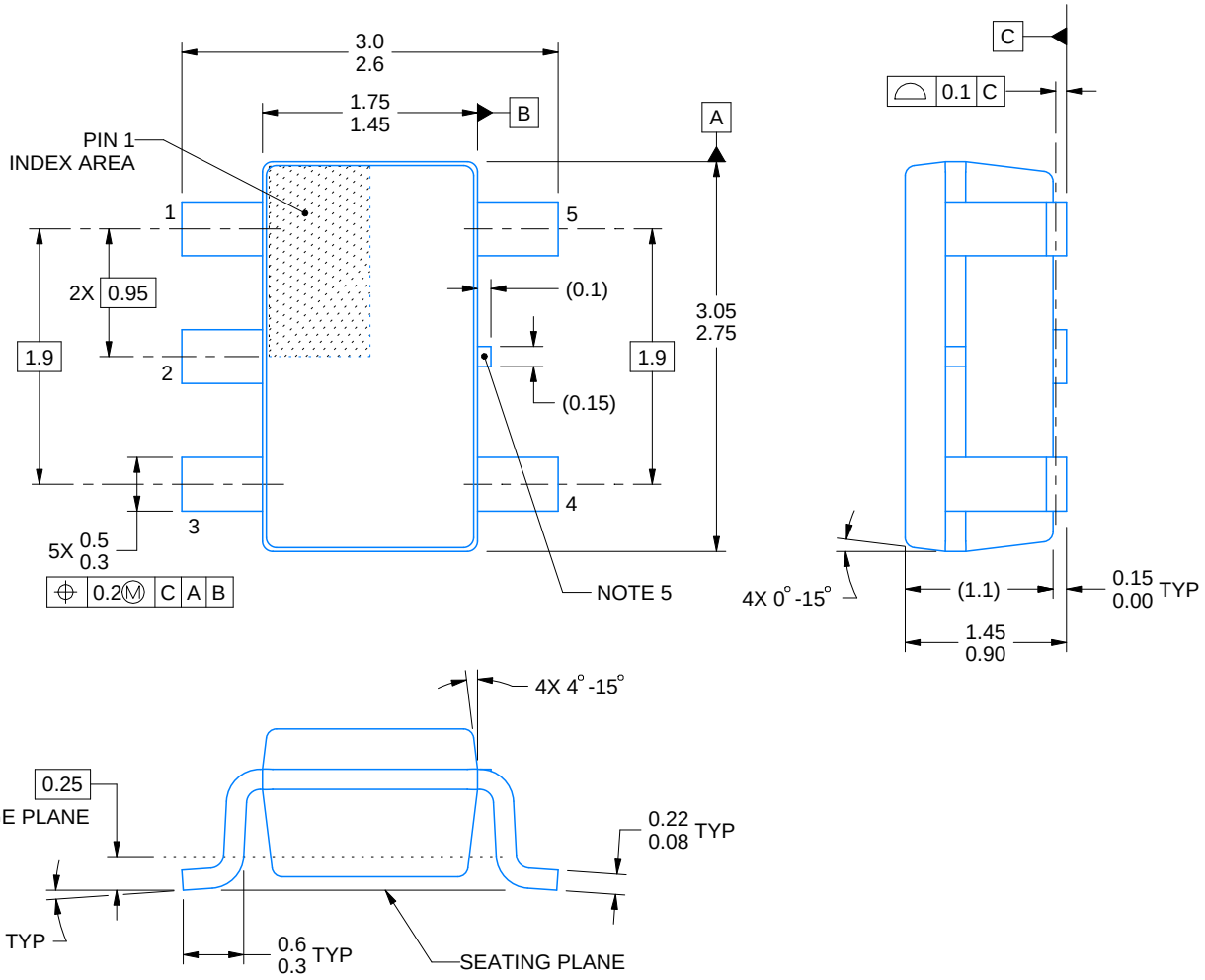
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

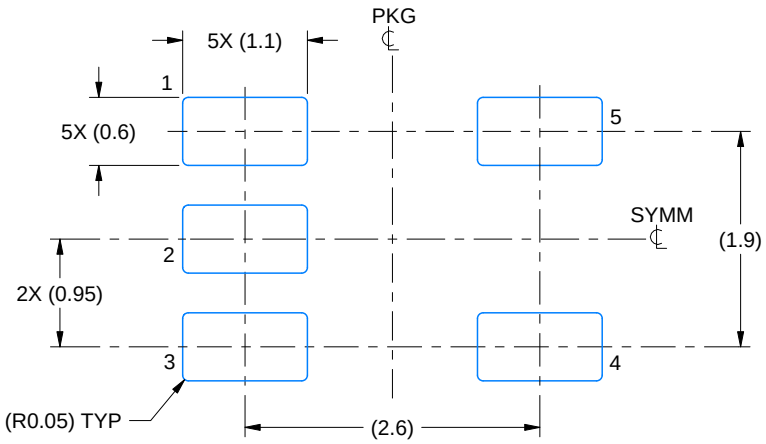
SMALL OUTLINE TRANSISTOR



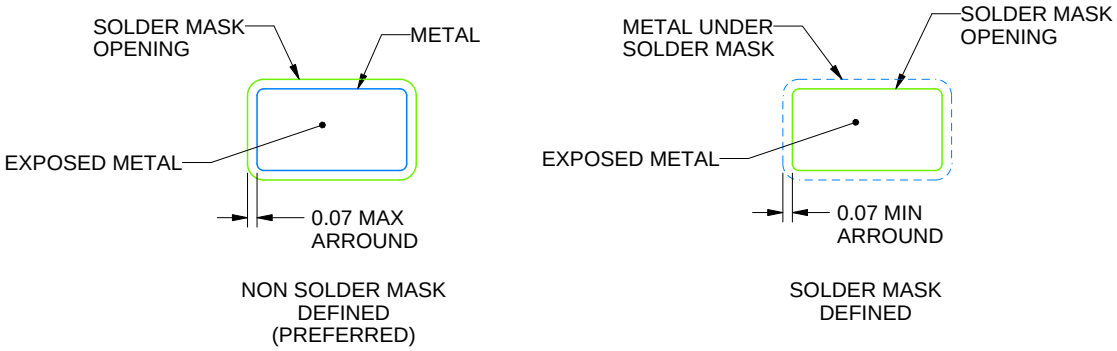
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

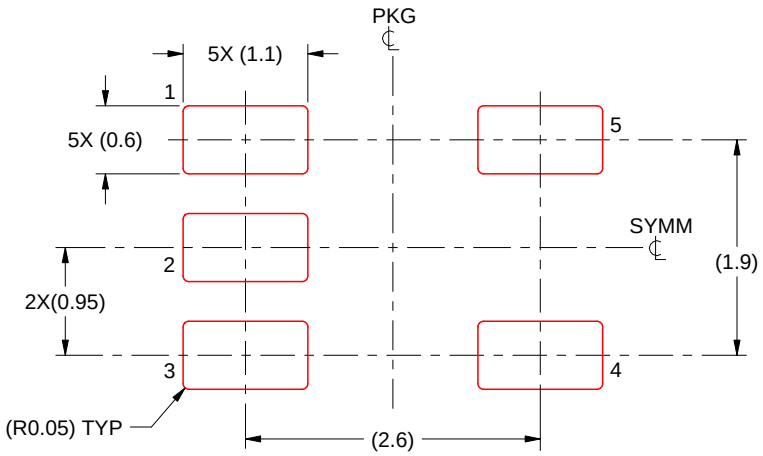


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

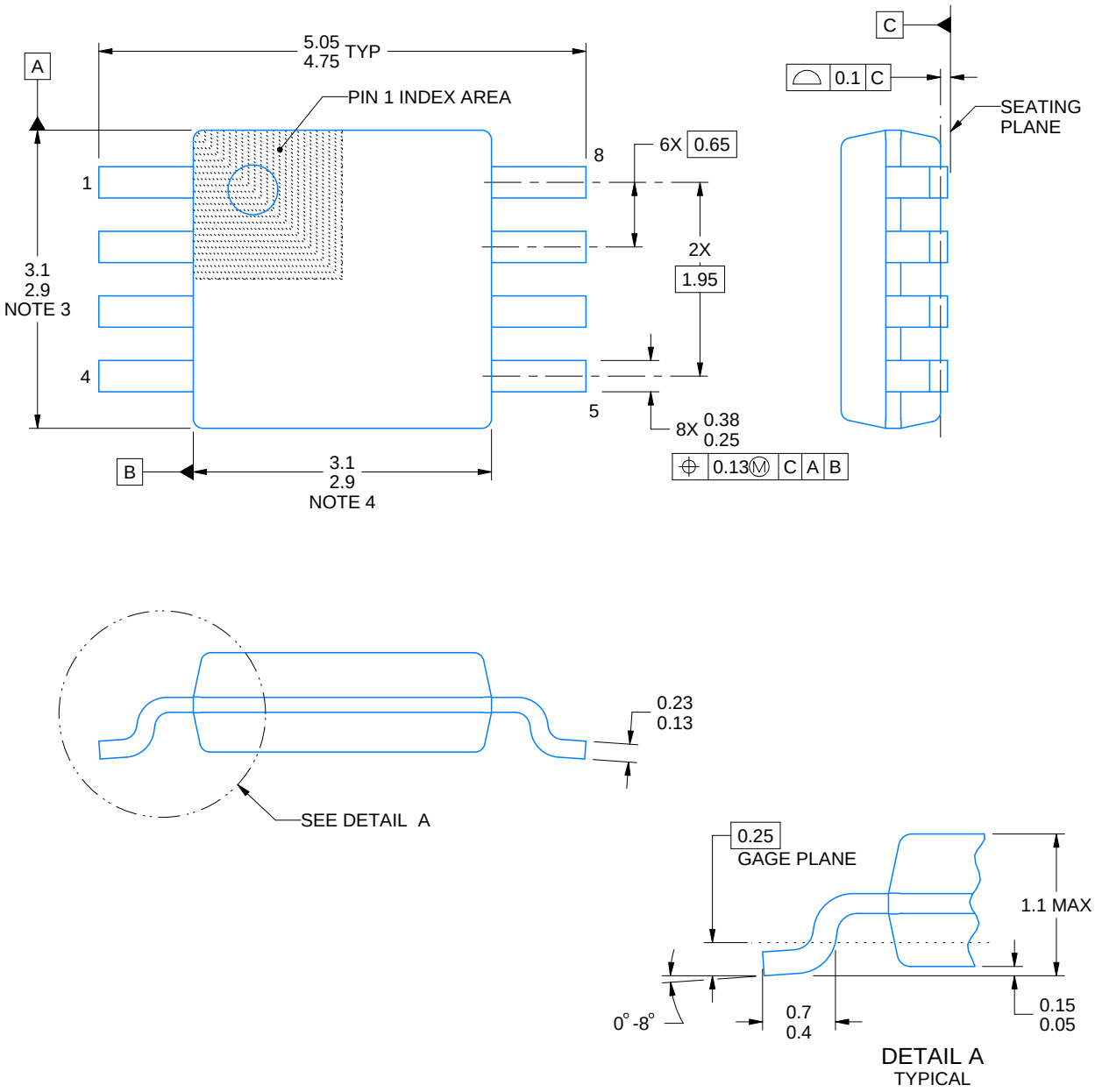
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

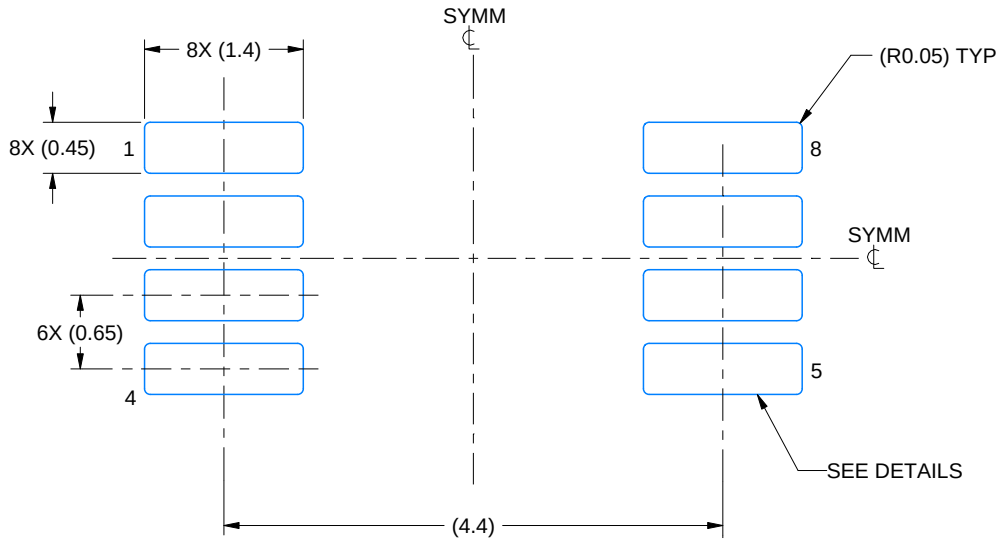
SMALL OUTLINE PACKAGE



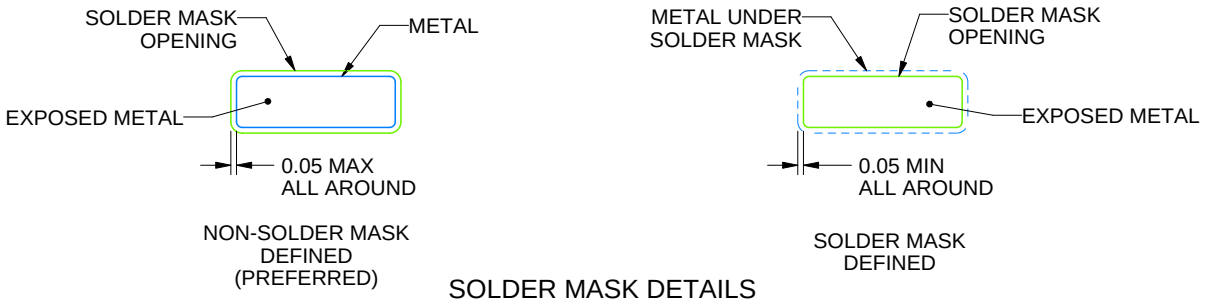
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

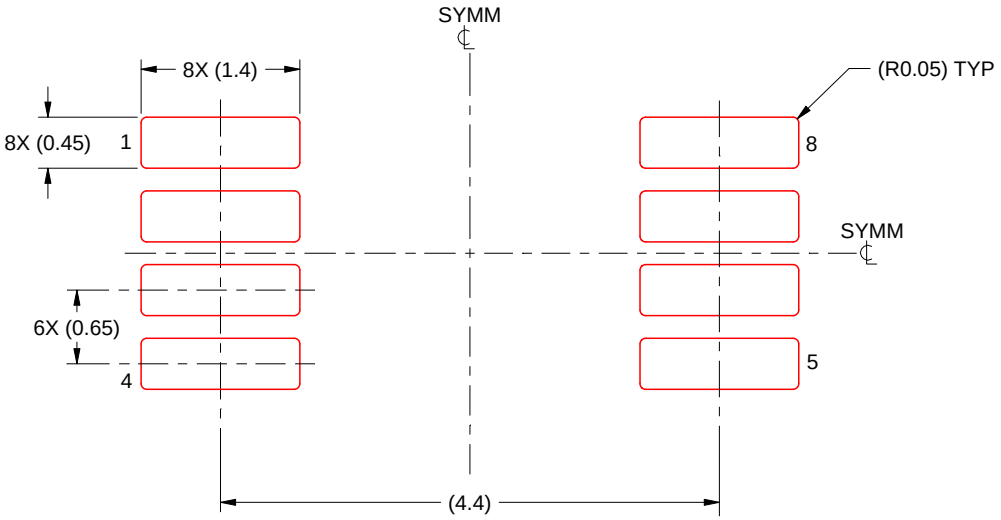


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

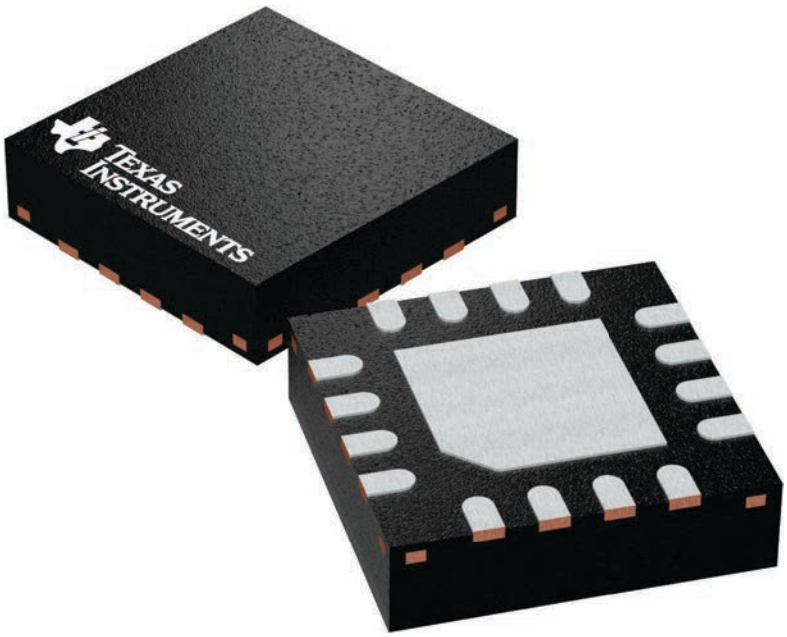
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

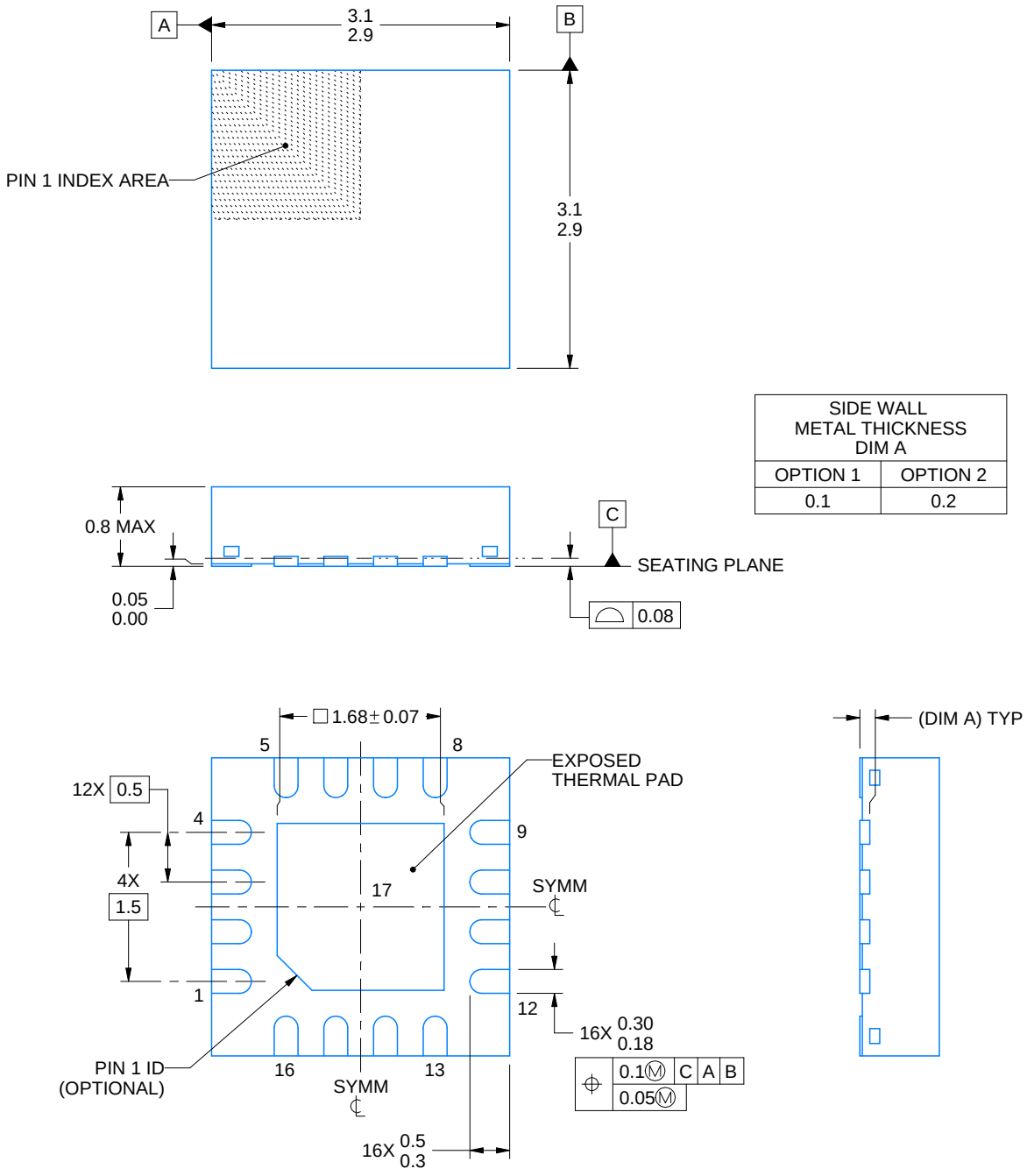


RTE0016C

PACKAGE OUTLINE

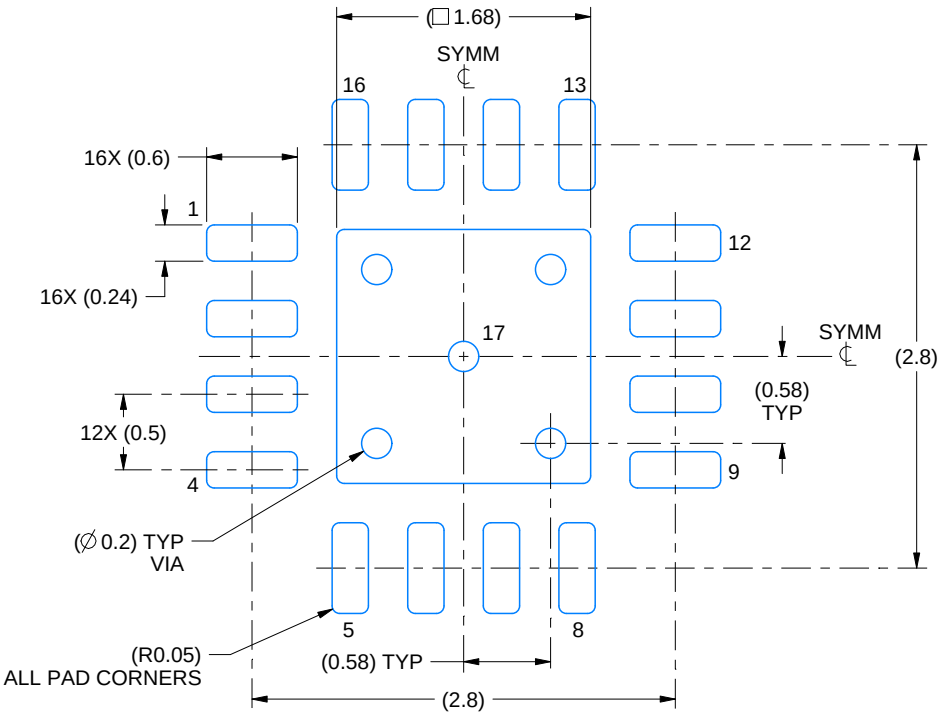
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

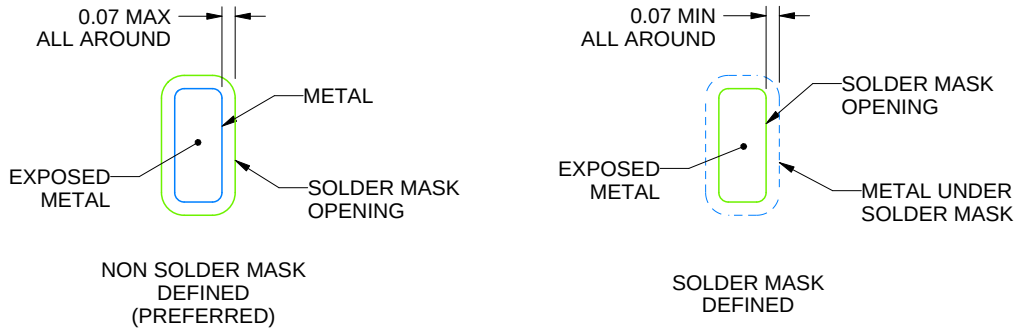


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

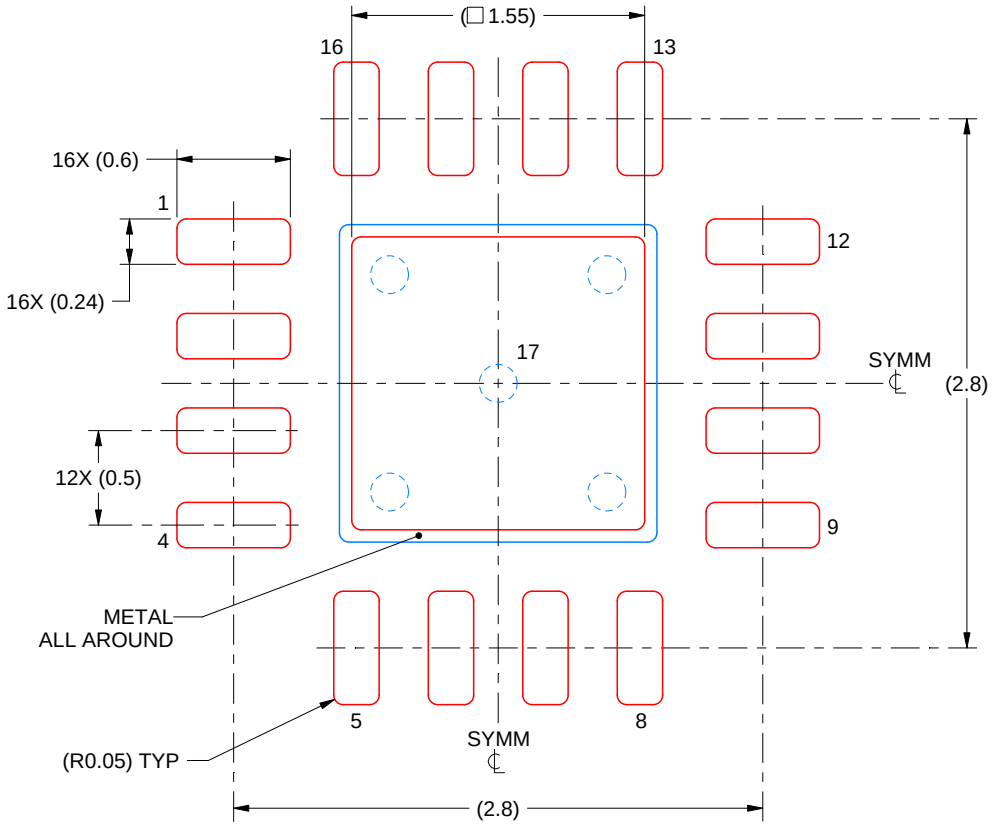


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月