TLV62095 采用 DCS-Control™ 拓扑的 4A 高效降压转换器

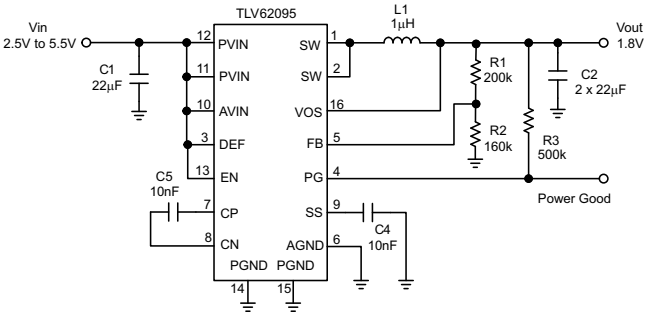
1 特性

- 2.5V 至 5.5V 输入电压范围
- DCS-Control™
- 效率高达 95%
- 省电模式
- 20μA 运行静态电流
- 针对最低压降的 100% 占空比
- 1.4MHz 典型开关频率
- 0.8V 至 V_{IN} 的可调输出电压
- 输出放电功能
- 可调软启动
- 自动切断短路保护功能
- 输出电压跟踪
- 与 TLV62090 和 TPS62095 引脚兼容
- 如需了解改进的特性集，请参见 TPS62095
- 借助 WEBENCH® Power Designer 并使用 TLV62095 创建定制设计方案

2 应用范围

- 电视 (TV)、机顶盒 (STB) 和计算机
- 固态硬盘 (SSD)
- 硬盘驱动器 (HDD)
- 电池供电类 应用

1.8V 输出应用



3 说明

TLV62095 器件是一款高频同步降压转换器，经优化具有小解决方案尺寸和高效率两大优点，非常适合电池供电类 应用。为了最大限度地提高效率，该转换器以 1.4MHz 的标称开关频率在脉宽调制 (PWM) 模式下工作，并且会在轻负载电流条件下自动进入节能工作模式。在分布式电源和负载点稳压应用中，该器件允许对其他电压轨的电压进行跟踪，并且允许采用介于 10μF 至 150μF 范围内甚至更高的输出电容。通过使用 DCS-Control™ 技术，此器件可实现出色的负载静态性能以及精确的输出电压调节。

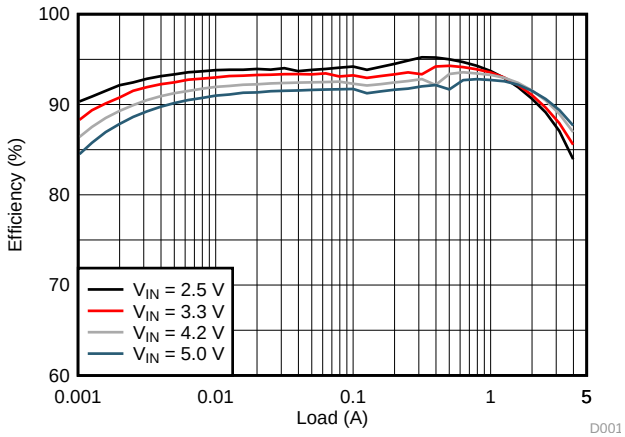
输出电压启动斜坡由软启动引脚控制，可由独立电源供电运行，也可在跟踪配置下运行。通过配置 EN 和 PG 引脚还可实现电源排序。在节能模式下，该器件静态工作电流的典型值为 20μA。在整个负载电流范围内，自动进入省电模式并且以无缝方式保持高效。

该器件采用 3mm x 3mm 16 引脚超薄四方扁平无引线 (VQFN) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV62095	VQFN (16)	3.00mm x 3.00mm

1.8V 输出应用效率



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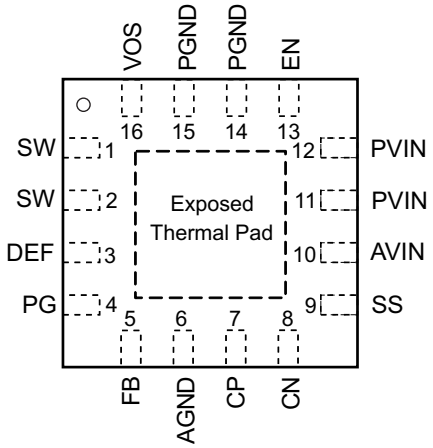
Changes from Original (March 2016) to Revision A **Page**

- 已添加 WEBENCH® 信息至*特性*、*详细设计流程和开发支持*部分 ... 1
- Added SW (AC, less than 10 ns) to the *Abolute Maximum Rating* table ... 4
- 已添加 表 1, Power Good Pin Logic ... 10

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5 Pin Configuration and Functions

16-Pin VQFN with Thermal PAD
RGT
(Top View)



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
SW	1, 2	Switch pin of the power stage.
DEF	3	This pin is used for internal logic and needs to be pulled high. This pin must be connected to the AVIN pin.
PG	4	Power good open drain output. A pull up resistor can not be connected to any voltage higher than the input voltage.
FB	5	Feedback pin for regulating the output voltage.
AGND	6	Analog ground.
CP	7	Internal charge pump's flying capacitor. Connect a 10nF capacitor between CP and CN.
CN	8	Internal charge pump's flying capacitor. Connect a 10nF capacitor between CP and CN.
SS	9	Soft-start control pin. A capacitor is connected to this pin and sets the soft startup time. Leaving this pin floating sets the minimum start-up time.
AVIN	10	Analog supply input voltage pin.
PVIN	11,12	Power supply input voltage pin.
EN	13	Enable pin. This pin has an active pull down resistor of typically 400kΩ, which is active when EN is low. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device.
PGND	14,15	Power ground.
VOS	16	Output voltage sense pin. This pin must be directly connected to the output voltage.
Exposed Thermal Pad		The exposed thermal pad must be connected to AGND. It must be soldered for mechanical reliability.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage at pins(2)	PVIN, AVIN, FB, SS, EN, DEF, VOS	– 0.3	7	V
	SW (DC), PG	– 0.3	V_{IN}+0.3	
	SW (AC, less than 10 ns)(3)	– 3.0	10	
	CN, CP	– 0.3	V_{IN}+7.0	
Sink current	PG		1.0	mA
Operating junction temperature range, T_J		– 40	150	°C
Storage temperature, T_{stg}		– 65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.
(3) While switching.

6.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommend Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage range	2.5	5.5	V
T_J	Operating junction temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV62095	UNIT
		VQFN (16 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60	
$R_{\theta JB}$	Junction-to-board thermal resistance	20	
ψ_{JT}	Junction-to-top characterization parameter	1.5	
ψ_{JB}	Junction-to-board characterization parameter	20	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

V_{IN} = 3.6V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
I_Q	Quiescent current into PVIN and AVIN	EN = High, Not switching, FB = FB +5%		20		µA
I_{SD}	Shutdown current Into PVIN and AVIN	EN = Low		0.6		µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling	2.1	2.2	2.3	V
	Undervoltage lockout hysteresis			200		mV
T_{SD}	Thermal shutdown	Temperature rising		150		ºC
	Thermal shutdown hysteresis			20		ºC
CONTROL SIGNAL EN						
V_H	High level input voltage	V_{IN} = 2.5 V to 5.5 V	1	0.65		V
V_L	Low level input voltage	V_{IN} = 2.5 V to 5.5 V		0.60	0.4	V
I_{lkg}	Input leakage current	EN = GND or V_{IN}		10	100	nA
R_{PD}	Pull down resistance	EN = Low		400		kΩ
SOFT STARTUP						
I_{SS}	Softstart current			7.5		µA
POWER GOOD						
V_{TH_PG}	Power good threshold	Output voltage rising		95%		
		Output voltage falling		90%		
V_L	Low level voltage	$I_{(sink)}$ = 1 mA			0.4	V
POWER SWITCH						
$R_{DS(on)}$	High side FET on-resistance	I_{SW} = 500 mA		50		mΩ
	Low side FET on-resistance	I_{SW} = 500 mA		40		mΩ
I_{LIM}	High side FET switch current limit		4.7	5.5		A
f_{SW}	Switching frequency	I_{OUT} = 3 A		1.4		MHz
OUTPUT						
V_{OUT}	Output voltage range		0.8		V_{IN}	V
R_{DIS}	Output discharge resistor	EN = GND, V_{OUT} = 1.8 V		200		Ω
V_{FB}	Feedback regulation voltage	I_{OUT} = 1 A, PWM mode	792	800	808	mV
	Line regulation	V_{OUT} = 1.8 V, PWM operation		0.016		%/V
	Load regulation	V_{OUT} = 1.8 V, PWM operation		0.04		%/A

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6.6 Typical Characteristics

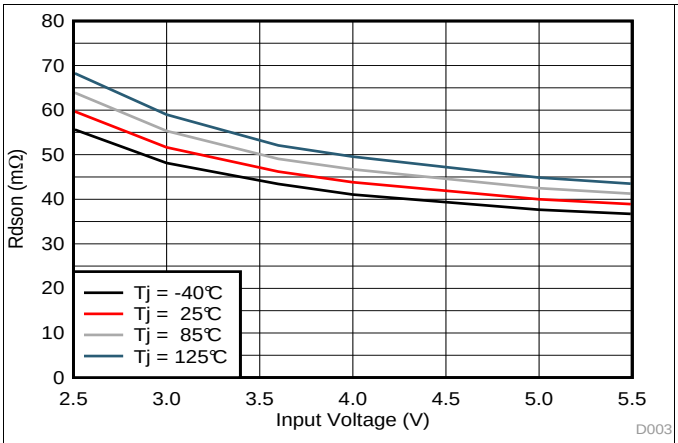


图 1. High-Side FET On Resistance

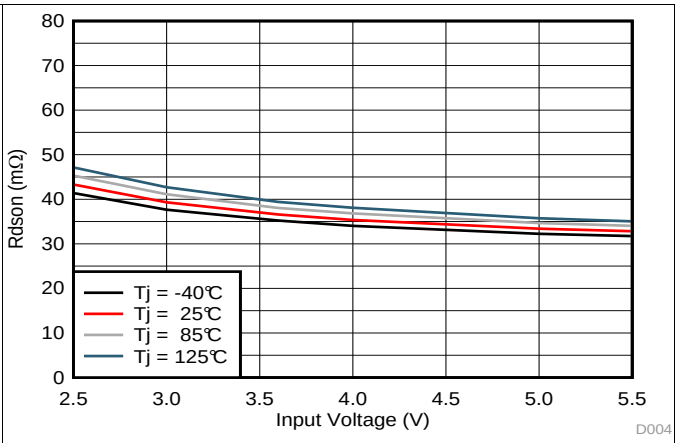


图 2. Low-Side FET On Resistance

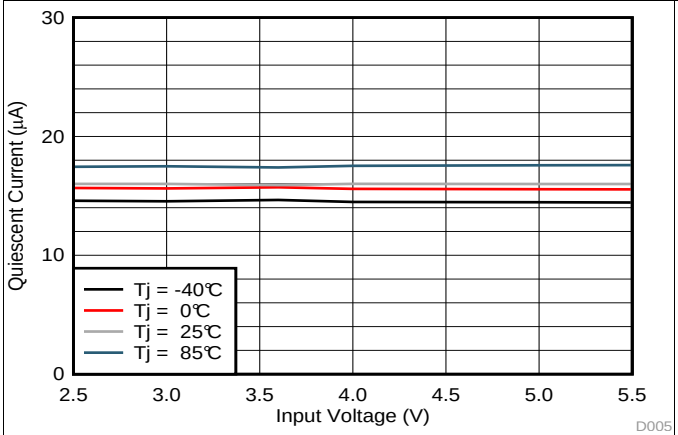


图 3. Quiescent Current

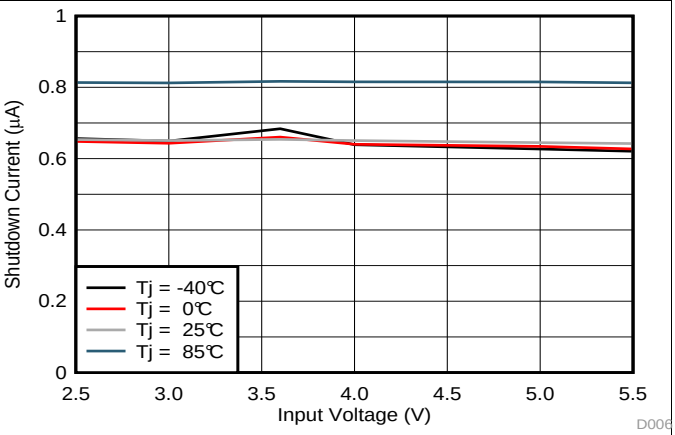


图 4. Shutdown Current

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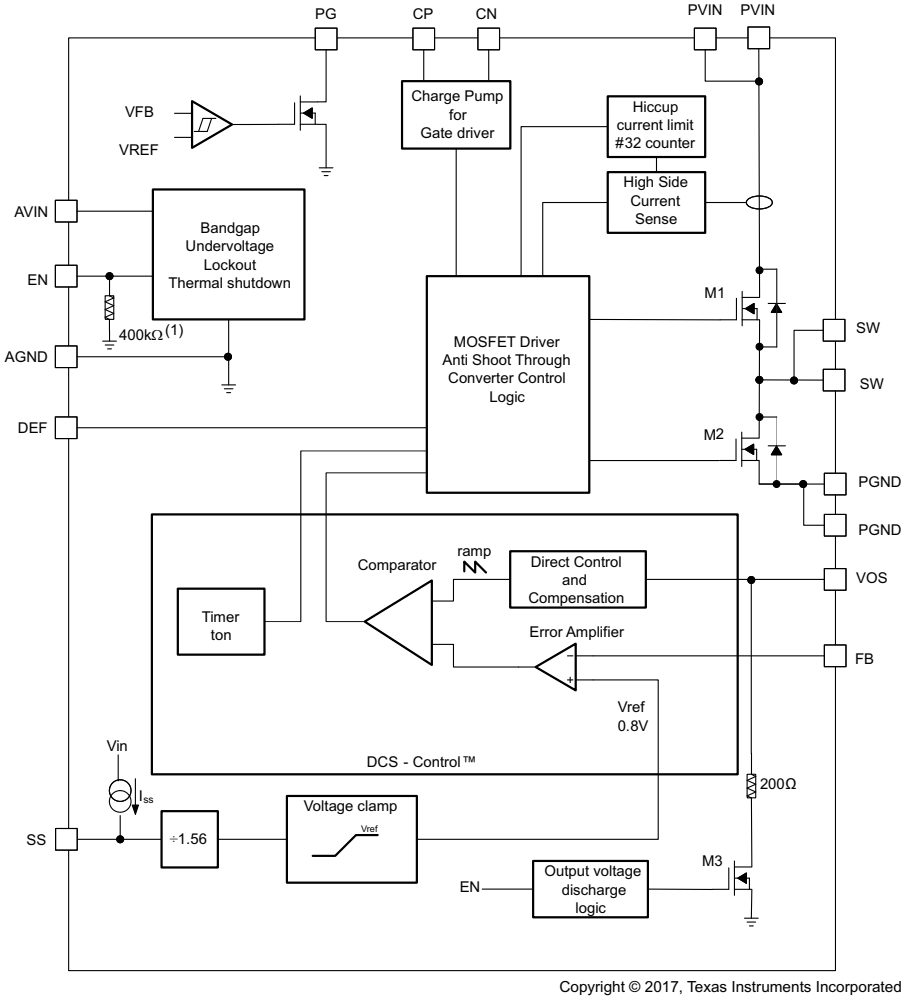
7 Detailed Description

7.1 Overview

The TLV62095 synchronous step down converter is based on DCS-Control™ (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control™ topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 1.4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the current consumption of the IC to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes using a single building block and therefore has a seamless transition from PWM to Power Save Mode without effects on the output voltage. The TLV62095 offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram



(1) The resistor is disconnected when EN is high.

7.3 Feature Description

7.3.1 PWM Operation

At medium to heavy load currents, the device operates with pulse width modulation (PWM) at a nominal switching frequency of 1.4 MHz. As the load current decreases, the converter enters power save mode operation reducing its switching frequency. The device enters power save mode at the boundary to discontinuous conduction mode (DCM).

7.3.2 Power Save Mode Operation

As the load current decreases, the converter enters Power Save Mode operation. During Power Save Mode, the converter operates with reduced switching frequency to maintain high efficiency. Power Save Mode is based on a fixed on-time architecture following 公式 1.

$$ton = \frac{V_{OUT}}{V_{IN}} \times 360ns \times 2$$

$$f = \frac{2 \times I_{OUT}}{ton^2 \left(1 + \frac{V_{IN} - V_{OUT}}{V_{OUT}} \right) \times \frac{V_{IN} - V_{OUT}}{L}} \quad (1)$$

In Power Save Mode, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance or the inductor value. This effect is also reduced by programming the output voltage of the TLV62095 lower than the target value.

7.3.3 Low Dropout Operation (100% Duty Cycle)

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode the high side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage where the output voltage falls below its set point is given by:

$$V_{IN(min)} = V_{OUT} + I_{OUT} \times (R_{DS(on)} + R_L) \quad (2)$$

Where

$R_{DS(on)}$ = High side FET on-resistance

R_L = DC resistance of the inductor

7.4 Device Functional Modes

7.4.1 Enable (EN)

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low with a shutdown current of typically 0.6 μA. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 200 Ω discharges the output through the VOS pin smoothly. An internal pull-down resistor of 400 kΩ is connected to the EN pin when the EN pin is low. The pull-down resistor is disconnected when the EN pin is high.

7.4.2 Soft Startup (SS) and Hiccup Current Limit During Startup

To minimize inrush current during startup, the device has an adjustable startup time depending on the capacitor value connected to the SS pin. The device charges the SS capacitor with a constant current of typically 7.5 μA. The feedback voltage follows this voltage divided by 1.56, until the internal reference voltage of 0.8 V is reached. The soft startup operation is completed once the voltage at the SS capacitor has reached typically 1.25 V. The soft startup time is calculated using 公式 3. The larger the SS capacitor, the longer the soft startup time. The relation between the SS pin voltage and the FB pin voltage is estimated using 公式 4.

$$t_{SS} = C_{SS} \times \frac{1.25V}{7.5\mu A} \quad (3)$$

$$V_{FB} = \frac{V_{SS}}{1.56} \quad (4)$$

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Device Functional Modes (接下页)

During startup the switch current limit is reduced to 1/3 of its typical current limit of 5.5A when the output voltage is less than 0.6V. Once the output voltage exceeds typically 0.6V, the switch current limit is released to its nominal value. Thus, the device provides a reduced load current of 1.8A when the output voltage is below 0.6V. Due to this, a small or no startup time may trigger this reduced switch current limit during startup, especially for larger output capacitor applications. This is avoided by using a larger soft start up capacitance which extends the soft startup time. See Short Circuit Protection (Hiccup-Mode) for details of the reduced current limit during startup. Leaving the SS pin floating sets the minimum startup time (around 50 µs).

7.4.3 Voltage Tracking (SS)

The SS pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 图 5. The internal reference voltage follows the voltage at the SS pin with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in 图 6.

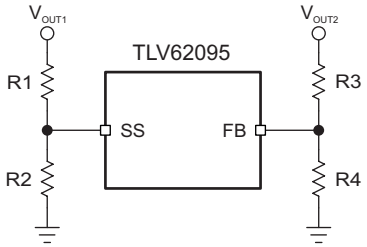


图 5. Output Voltage Tracking

The R2 value should be set properly to achieve accurate voltage tracking by taking 7.5 µA soft startup current into account. 1 kΩ or smaller is a sufficient value for R2.

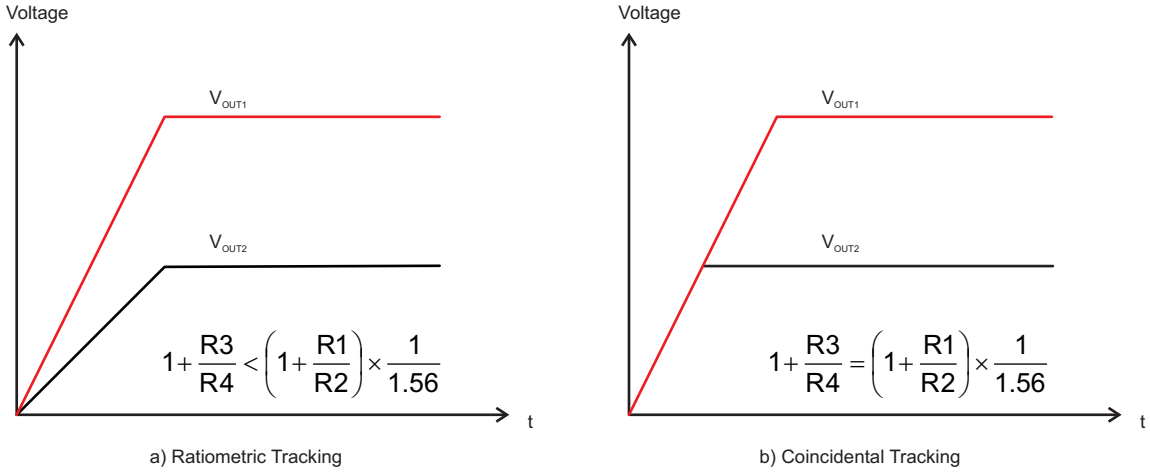


图 6. Voltage Tracking Options

For decreasing the SS pin voltage, the device doesn't sink current from the output when the device is in power save mode. So the resulting decrease of the output voltage may be slower than the SS pin voltage if the load is light. When driving the SS pin with an external voltage, do not exceed the voltage rating of the SS pin which is 7 V.

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Device Functional Modes (接下页)

7.4.4 Short Circuit Protection (Hiccup-Mode)

The device is protected against hard short circuits to GND and over-current events. This is implemented by a two level short circuit protection. During start-up and when the output is shorted to GND, the switch current limit is reduced to 1/3 of its typical current limit of 5.5 A. Once the output voltage exceeds typically 0.6 V the current limit is released to its nominal value. The full current limit is implemented as a hiccup current limit. Once the internal current limit is triggered 32 times, the device stops switching and starts a new start-up sequence after a typical delay time of 66 µs passed by. The device repeats these cycles until the high current condition is released.

7.4.5 Output Discharge Function

To make sure the device starts up under defined conditions, the output gets discharged via the VOS pin with a typical discharge resistor of 200 Ω whenever the device shuts down. This happens when the device is disabled or if thermal shutdown, undervoltage lockout or short circuit hiccup-mode is triggered.

7.4.6 Power Good Output

The power good output is low when the output voltage is below its nominal value. The power good becomes high impedance once the output is within 5% of regulation. The PG pin is an open drain output and is specified to sink up to 1mA. This output requires a pull-up resistor to be monitored properly. The pull-up resistor cannot be connected to any voltage higher than the input voltage of the device. The PG output can be left floating if unused. 表 1 shows the PG pin logic.

表 1. Power Good Pin Logic

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH_PG}$	√	
	$V_{FB} \leq V_{TH_PG}$		√
Shutdown (EN=Low)			√
UVLO	$0.7\ V < VIN \leq V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} \leq 0.7\ V$	√	

7.4.7 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. UVLO shuts down the device at input voltages lower than typically 2.2 V with a 200 mV hysteresis.

7.4.8 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically 150°C with a 20°C hysteresis.

7.4.9 Charge Pump (CP, CN)

The CP and CN pins must attach to an external 10 nF capacitor to complete a charge pump for the gate driver. This capacitor must be rated for the input voltage. It is not recommended to connect any other circuits to the CP or CN pins.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV62095 is a 4-A high frequency synchronous step-down converter optimized for small solution size, high efficiency and suitable for battery powered applications.

8.2 Typical Applications

8.2.1 1.8-V Output Converter

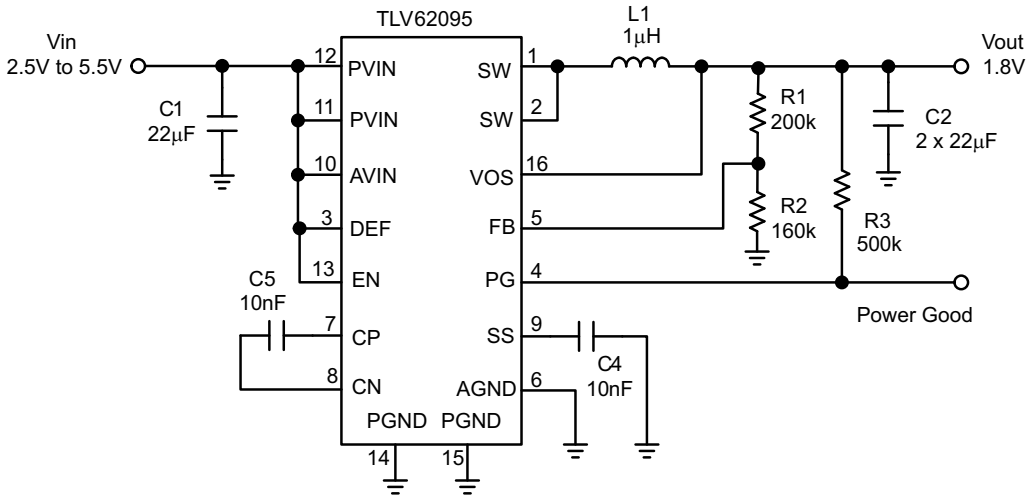


图 7. TLV62095 Typical Application Circuit

8.2.1.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions. For the typical application example, the following input parameters are used.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	< 30 mV
Output current rating	4 A

表 3 shows the list of components for the Application Characteristic Curves.

表 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
TLV62095	High efficiency step-down converter	Texas Instruments
L1	Inductor: 1 µH	Coilcraft XAL4020-102
C1, C2	Ceramic capacitor: 22 µF	(6.3V, X5R, 0805)

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表 3. List of Components (接下页)

REFERENCE	DESCRIPTION	MANUFACTURER
C4, C5	Ceramic capacitor, 10 nF	Standard
R1, R2, R3	Resistor	Standard

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLV62095 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Filter

The first step is the selection of the output filter components. To simplify this process, 表 4 outlines possible inductor and capacitor value combinations.

表 4. Output Filter Selection

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)				
	10	22	2 x 22	100	150
0.47					
1.0			√(3)	√	√
2.2					

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
(3) Typical application configuration. Other check mark indicates alternative filter combinations

8.2.1.2.3 Inductor Selection

The inductor selection is affected by several parameters like inductor ripple current, output voltage ripple, transition point into Power Save Mode, and efficiency. See 表 5 for typical inductors.

表 5. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER(1)	SIZE (LxWxH mm)	Isat / DCR
1 µH	Coilcraft XAL4020-102	4.0 x 4.0 x 2.1	8.75A / 13.2 mΩ
0.47 µH	TOKO DFE322512C	3.2 x 2.5 x 1.2	5.9A / 21 mΩ

(1) See Third-Party Products disclaimer

In addition, the inductor has to be rated for the appropriate saturation current and DC resistance (DCR). The inductor needs to be rated for a saturation current as high as the typical switch current limit of 5.5A or according to 公式 5 and 公式 6. 公式 5 and 公式 6 calculate the maximum inductor current under static load conditions. The formula takes the converter efficiency into account. The converter efficiency can be taken from the data sheet graphs or 80% can be used as a conservative approach. The calculation must be done for the maximum input voltage where the peak switch current is highest.

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$$I_L = I_{OUT} + \frac{\Delta I_L}{2} \quad (5)$$

$$I_L = I_{OUT} + \frac{\frac{V_{OUT}}{\eta} \times \left(1 - \frac{V_{OUT}}{V_{IN} \times \eta}\right)}{2 \times f \times L} \quad (6)$$

where

f = Converter switching frequency (typically 1.4MHz)
L = Inductor value
η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as a conservative assumption)

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. A margin of 20% should be added to cover for load transients during operation.

8.2.1.2.4 Input and Output Capacitor Selection

For best output and input voltage filtering, low ESR (X5R or X7R) ceramic capacitors are recommended. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 22-µF or larger input capacitor is recommended. The output capacitor value can range from 10 µF up to 150 µF and beyond. Load transient testing and measuring the bode plot are good ways to verify stability with larger capacitor values.

The recommended typical output capacitor value is 2 x 22 µF (nominal) and can vary over a wide range as outline in the output filter selection table. Ceramic capacitor have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating.

8.2.1.2.5 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (7)$$

$$R2 = \frac{V_{FB}}{I_{FB}} = \frac{0.8\ V}{5\ \mu A} \approx 160\ k\Omega \quad (8)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right) \quad (9)$$

When sizing R2, in order to achieve low quiescent current and acceptable noise sensitivity, use a minimum of 5 µA for the feedback current I_{FB}. Larger currents through R2 improve noise sensitivity and output voltage accuracy.

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8.2.1.3 Application Performance Curves

T_A = 25°C, V_{IN} = 3.6 V, VOUT = 1.8 V, unless otherwise noted.

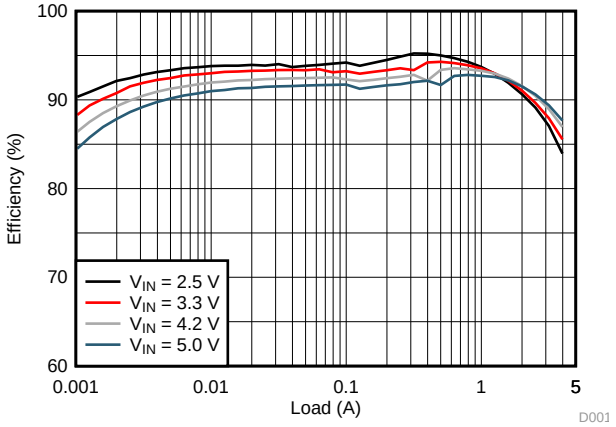


图 8. Efficiency, V_{OUT} = 1.8 V

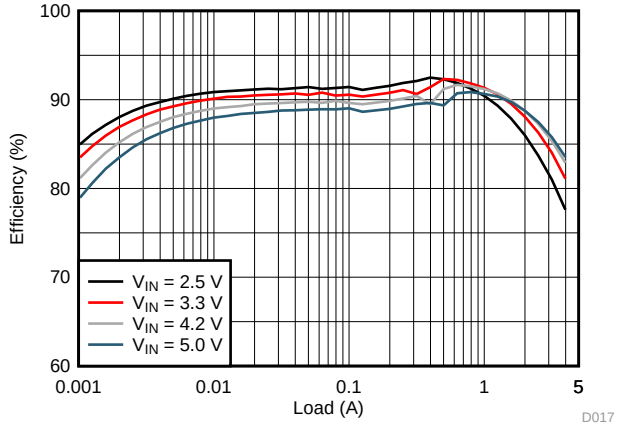


图 9. Efficiency, V_{OUT} = 1.2 V

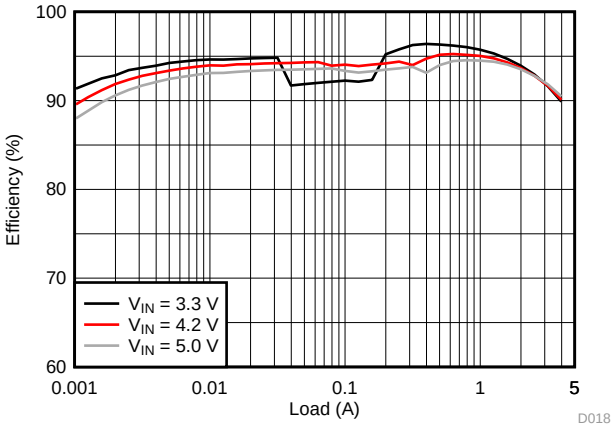


图 10. Efficiency, V_{OUT} = 2.6 V

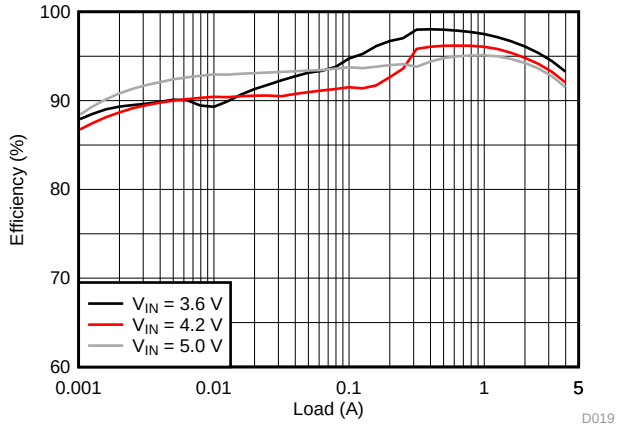


图 11. Efficiency, V_{OUT} = 3.3 V

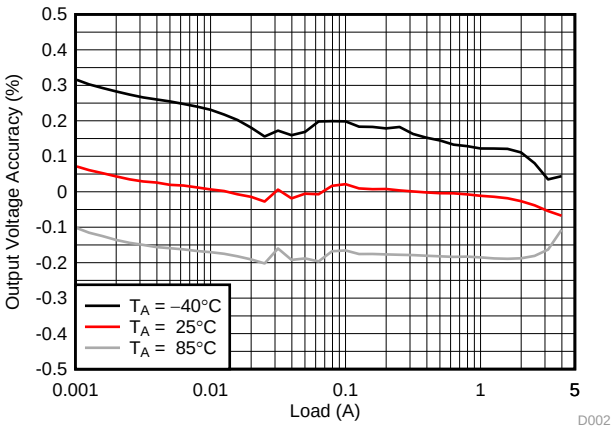


图 12. Load Regulation, V_{OUT} = 1.8 V, V_{IN} = 3.3 V

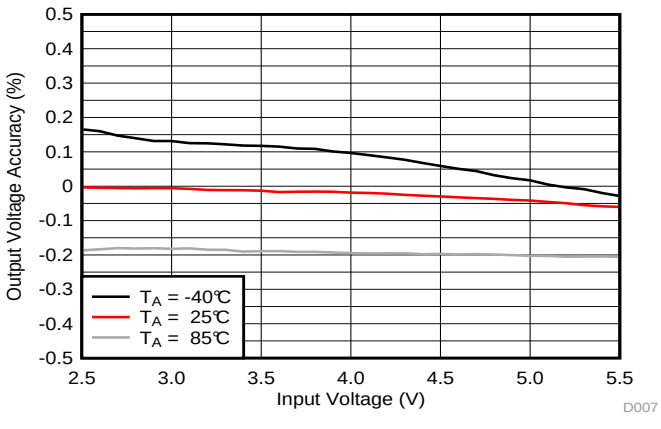


图 13. Line Regulation, V_{OUT} = 1.8 V, I_{OUT} = 1.0 A

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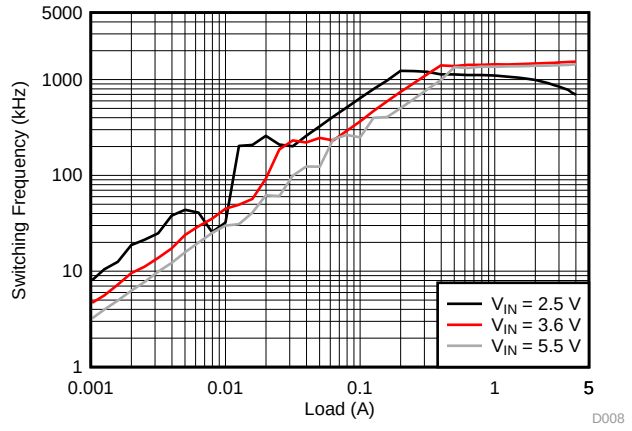


图 14. Switching Frequency, V_{OUT} = 1.8 V

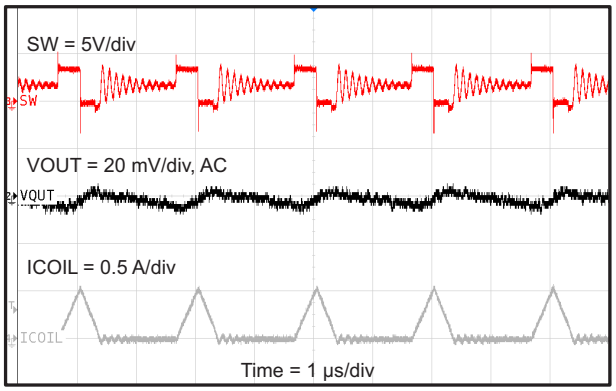


图 15. Output Ripple, V_{OUT} = 1.8 V, I_{OUT} = 100 mA

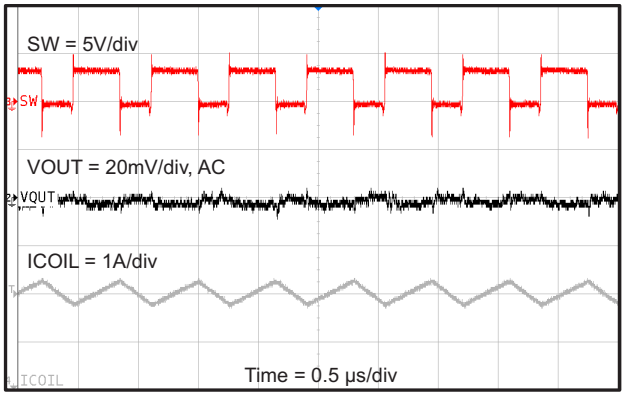


图 16. Output Ripple, V_{OUT} = 1.8 V, I_{OUT} = 3.5 A

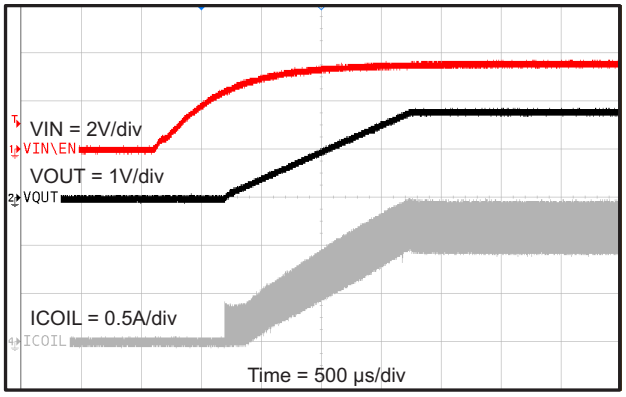


图 17. Startup, Relative to V_{IN}, R_{LOAD} = 1.5 Ω

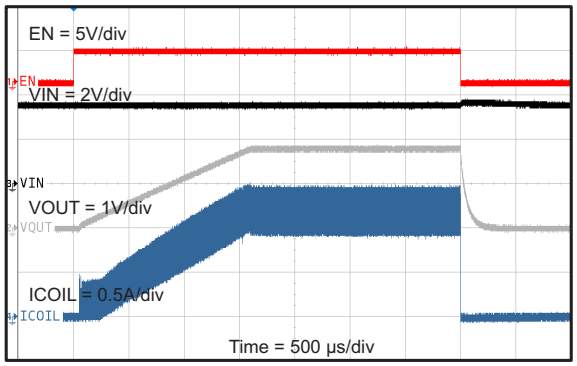


图 18. Startup, Relative to EN, R_{LOAD} = 1.5 Ω

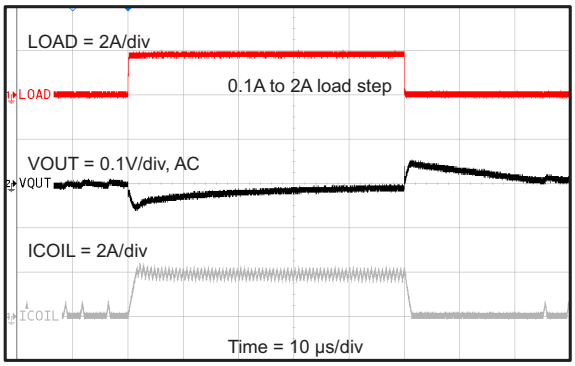


图 19. Load Transient, V_{OUT} = 1.8 V

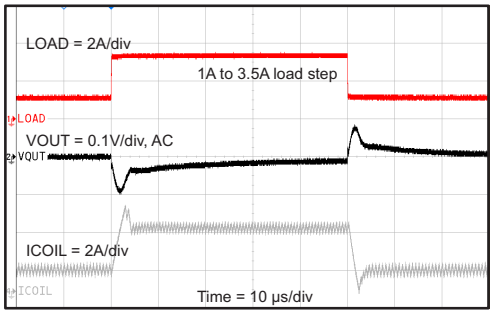


图 20. Load Transient, V_{OUT} = 1.8 V

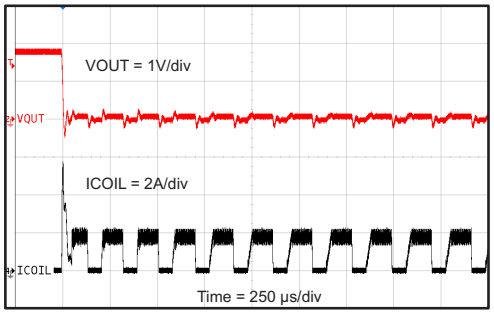


图 21. Short Circuit, HICCUP Protection Entry

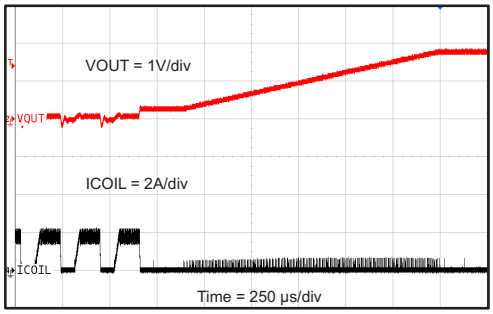


图 22. Short Circuit, HICCUP Protection Exit

9 Power Supply Recommendations

The TLV62095 device has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TLV62095.

10 Layout

10.1 Layout Guidelines

- It is recommended to place the input capacitor as close as possible to the IC pins PVIN and PGND.
- The VOS connection is noise sensitive and needs to be routed short and direct to the output terminal of the inductor.
- The exposed thermal pad of the package, analog ground (pin 6) and power ground (pin 14, 15) should have a single point connection at the exposed thermal pad of the package. This minimizes switch node jitter.
- The charge pump capacitor connected to CP and CN should be placed close to the IC to minimize coupling of switching waveforms into other traces and circuits.
- Refer to 图 23 for an example of component placement, routing and thermal design.

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10.2 Layout Example

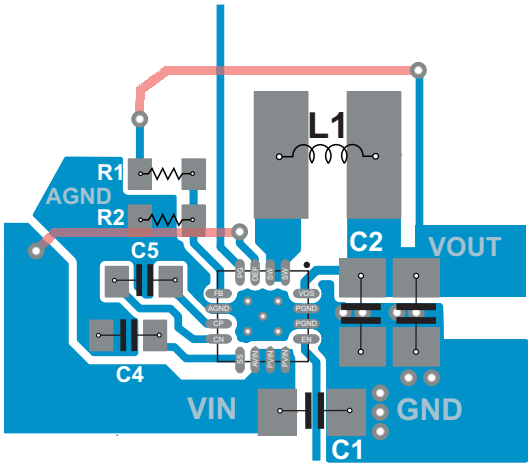


图 23. TLV62095 PCB Layout

10.3 Thermal Consideration

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component. The Thermal Information table provides the thermal metric of the device and its package based on JEDEC standard. For more details on how to use the thermal parameters in real applications, see the application notes: SZZA017 and SPRA953.

11 器件和文档支持

11.1 器件支持

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 开发支持

11.1.2.1 使用 WEBENCH® 工具定制设计方案

请单击此处，借助 WEBENCH® Power Designer 并使用 TLV62095 器件创建定制设计方案。

1. 在开始阶段键入输出电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

11.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV62095RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O
TLV62095RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O
TLV62095RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O
TLV62095RGTRG4	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O
TLV62095RGTRG4.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O
TLV62095RGTRG4.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O
TLV62095RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O
TLV62095RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O
TLV62095RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

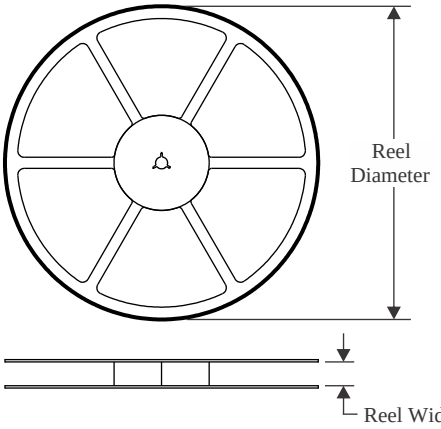
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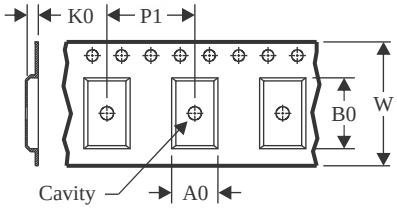
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

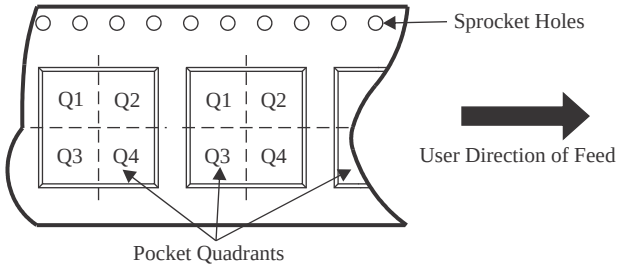


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

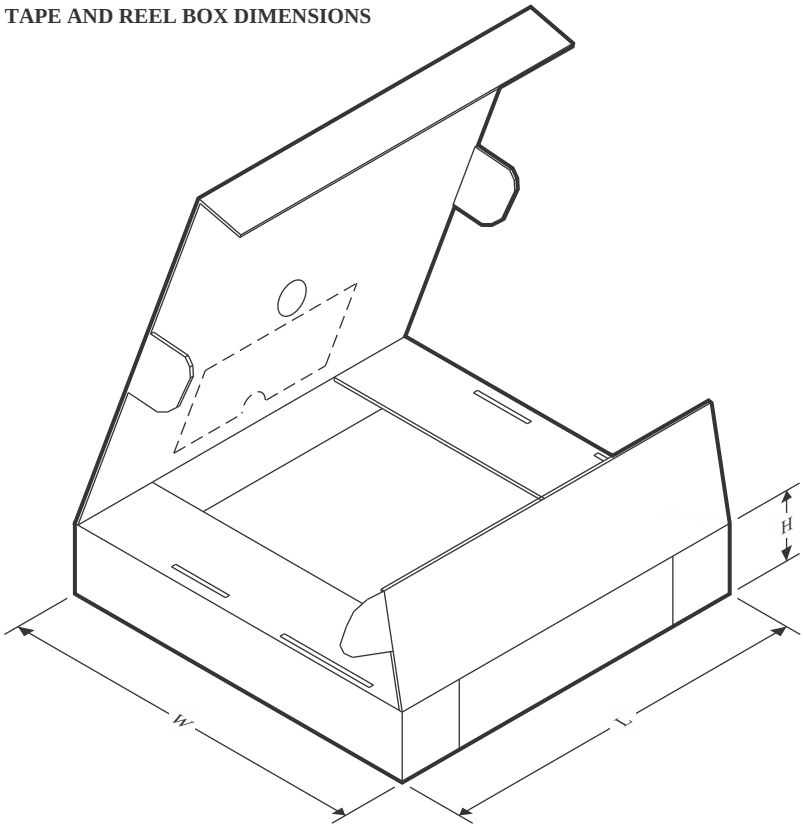
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62095RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62095RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62095RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62095RGTRG4	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62095RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62095RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

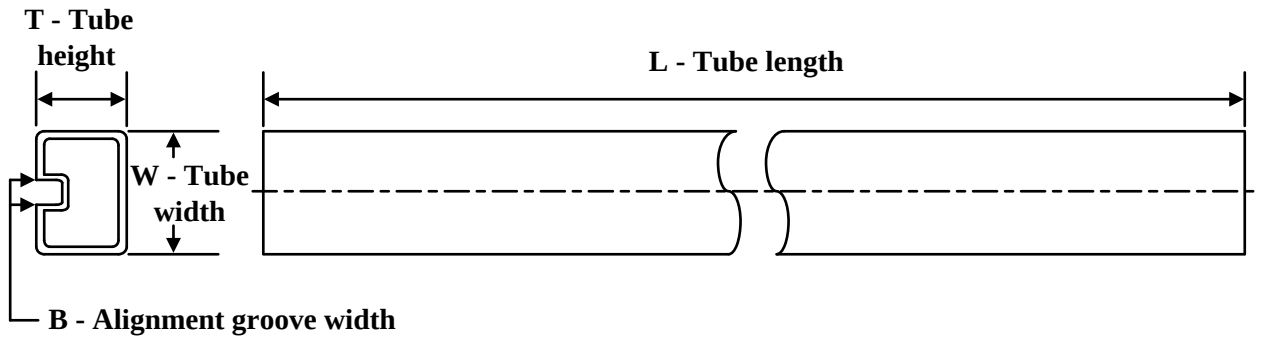
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62095RGTR	VQFN	RGT	16	3000	552.0	346.0	36.0
TLV62095RGTR	VQFN	RGT	16	3000	360.0	360.0	36.0
TLV62095RGTR	VQFN	RGT	16	3000	338.0	355.0	35.0
TLV62095RGTRG4	VQFN	RGT	16	3000	552.0	346.0	36.0
TLV62095RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TLV62095RGTT	VQFN	RGT	16	250	552.0	185.0	36.0

TUBE

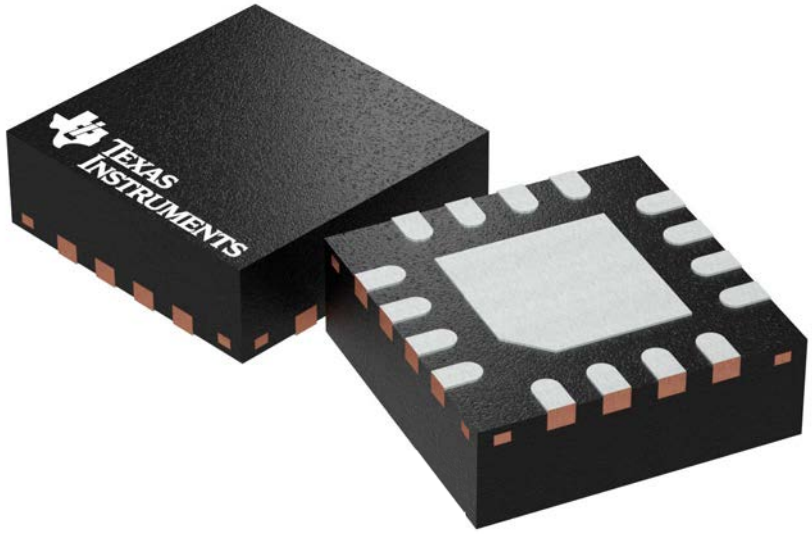


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV62095RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TLV62095RGTR.A	RGT	VQFN	16	3000	381	4.83	2286	0
TLV62095RGTR.B	RGT	VQFN	16	3000	381	4.83	2286	0
TLV62095RGTRG4	RGT	VQFN	16	3000	381	4.83	2286	0
TLV62095RGTRG4.A	RGT	VQFN	16	3000	381	4.83	2286	0
TLV62095RGTRG4.B	RGT	VQFN	16	3000	381	4.83	2286	0
TLV62095RGTT	RGT	VQFN	16	250	381	4.83	2286	0
TLV62095RGTT.A	RGT	VQFN	16	250	381	4.83	2286	0
TLV62095RGTT.B	RGT	VQFN	16	250	381	4.83	2286	0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



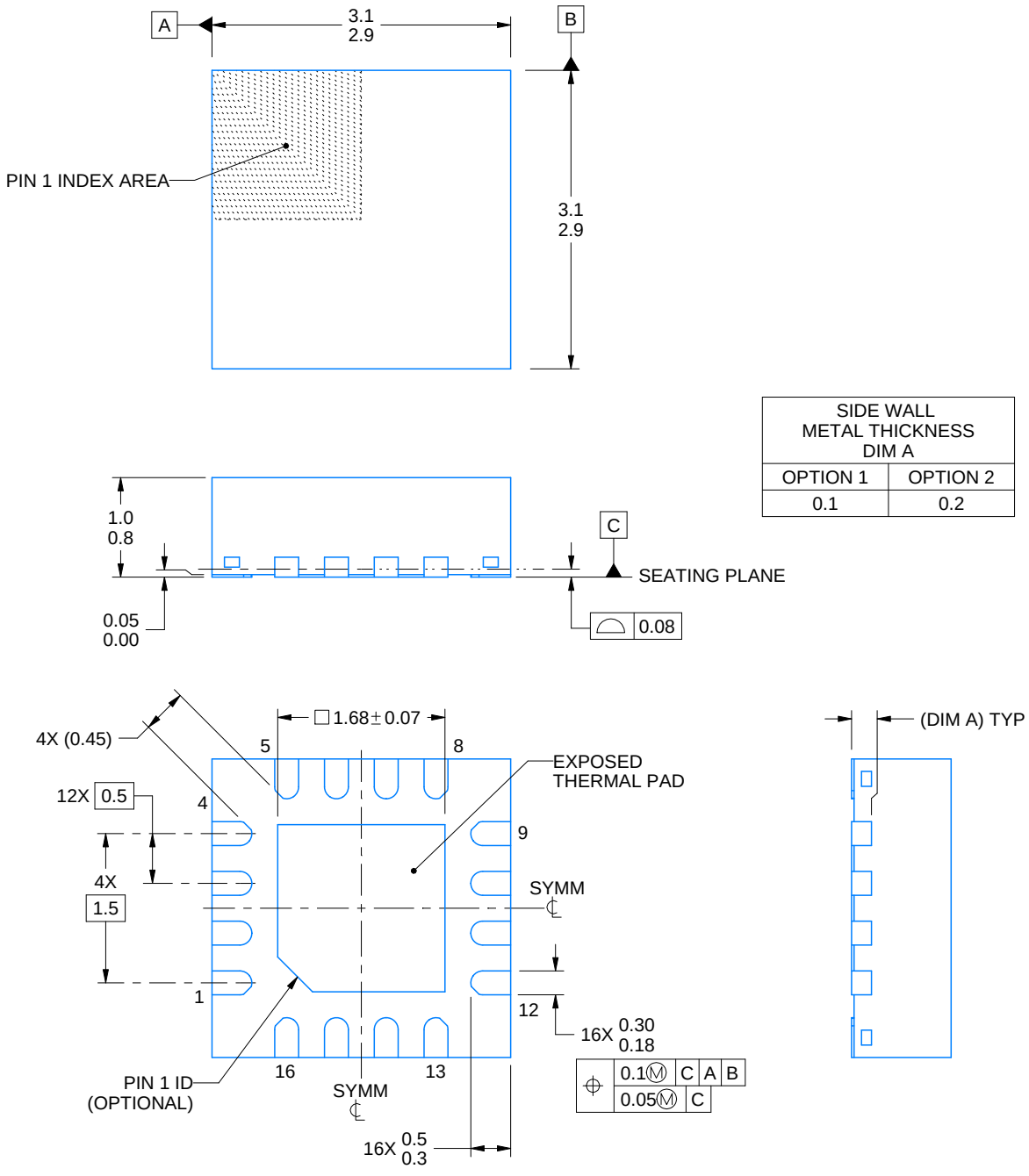
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

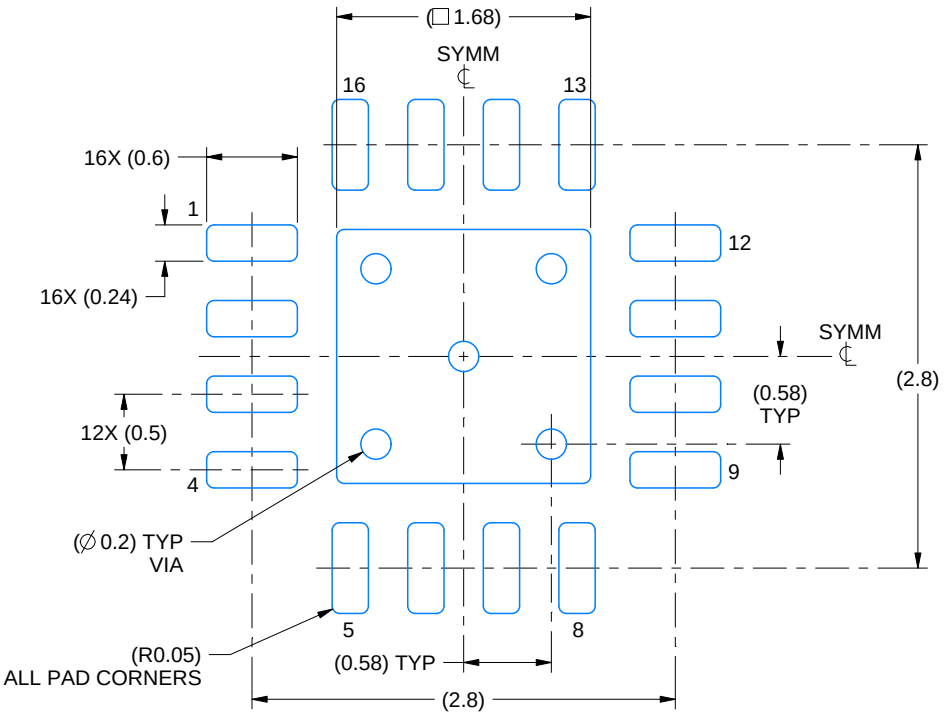
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

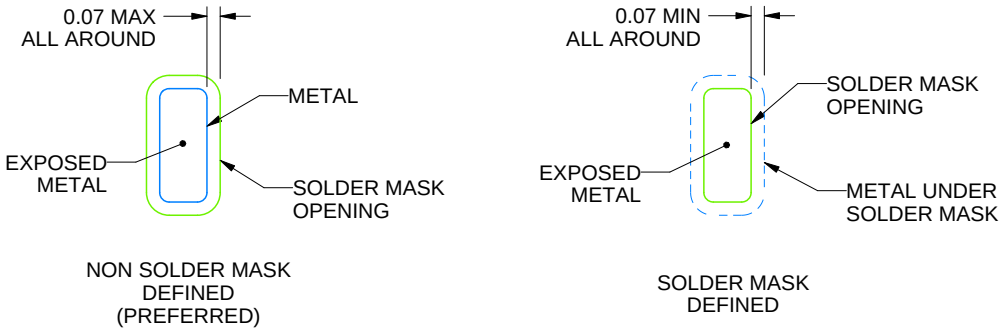


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

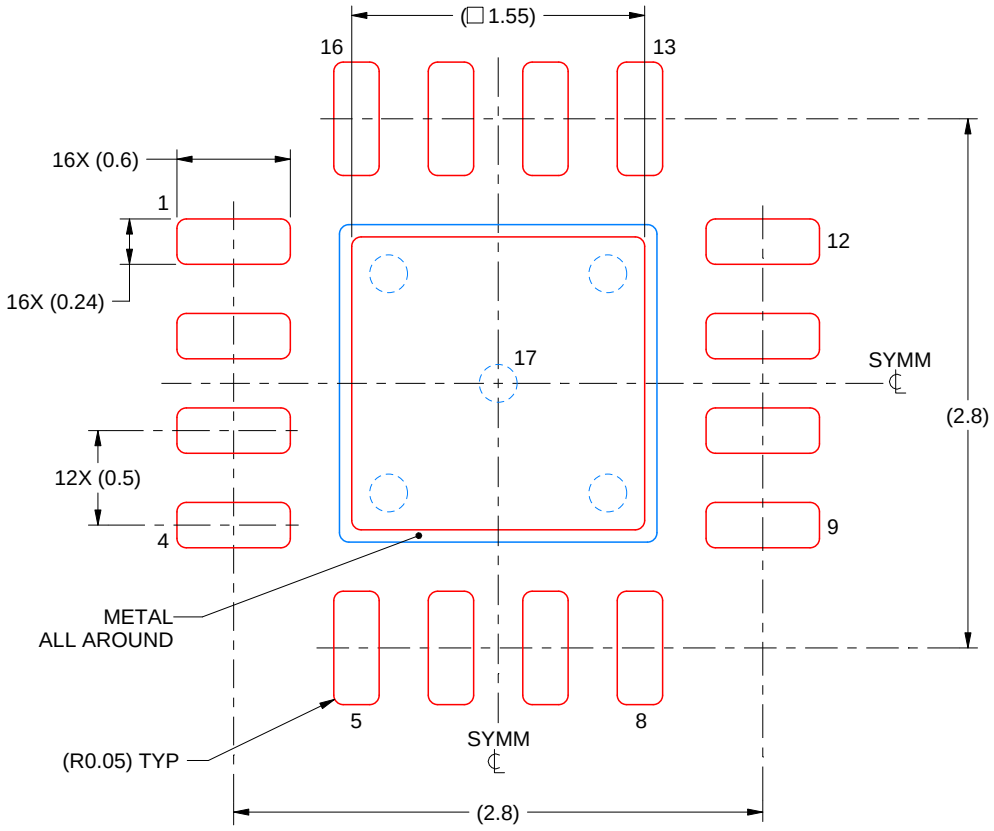


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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