# 适用于成本敏感型系统的 TLVx172 36V 单电源、低功耗运算放大器

## 1 特性

- 电源电压范围：4.5V 至 36V，±2.25V 至 ±18V
- 低噪声：9 nV/√Hz
- 低温漂：±1µV/°C（典型值）
- 抗电磁干扰 (EMI)
- 输入范围包括负电源
- 轨到轨输出
- 增益带宽：10MHz
- 转换速率：10V/µs
- 低静态电流：每个放大器 1.6mA
- 高共模抑制：116dB（典型值）
- 低输入偏压电流：10pA

## 2 应用

- 薄膜晶体管 (TFT) - 液晶显示屏 (LCD) 驱动电路
- 触摸屏显示屏
- 无线 LAN
- 便携式仪表
- 模数转换器 (ADC) 缓冲器
- 有源滤波器
- 线路驱动器或线路接收器
- 超声波
- 点钞机
- 变频器放大器

## 3 说明

TLVx172 系列 36V 单电源、低噪声抗电磁干扰 (EMI) 运算放大器在 1kHz 频率下 具有 0.0002% 的 THD+N，能够在 4.5V (±2.25V) 至 36V (±18V) 的电源电压范围内正常工作。这些 特性和低噪声、高 PSRR 特性，使TLVx172能够 在 HEV 和 EV 汽车及动力传动系统、医疗仪器等应用中放大毫伏级信号。TLVx172 器件具有良好的失调电压和温漂、10MHz 高带宽和 10V/µs 压摆率，且在工作温度范围内的静态电流仅有 2.3mA（最大值）

大多数运算放大器仅有一个额定电源电压，而 TLVx172器件的额定电压范围为 4.5V 至 36V。超过电源轨的输入信号不会导致相位反转。TLVx172器件可在容性负载高达 300pF 时保持稳定。输入可在负电源轨以下 100mV 以及正电源轨 2V 之内正常运行。请注意，此系列器件可在超出正电源轨 100mV 的完整轨至轨输入范围内运行，但是在正电源轨 2V 之内运行时，性能会受到影响。

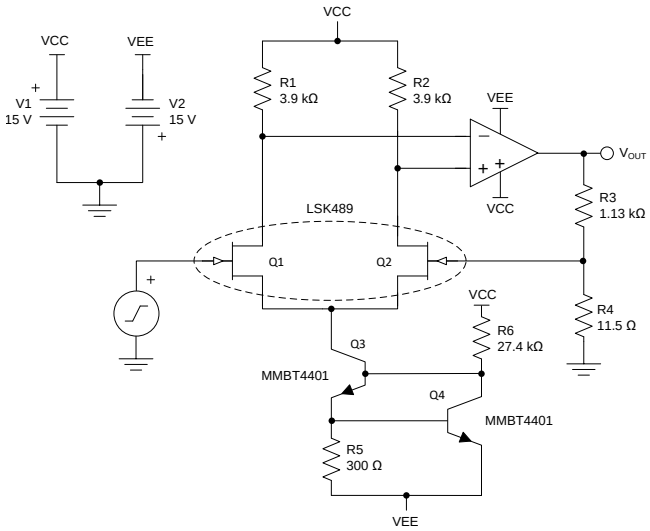
TLVx172运算放大器的额定工作温度范围为 –40°C 至 +125°C。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TLV172 | SOIC (8) | 4.90mm × 3.91mm |
| | SC70 (5) | 2.00mm × 1.25mm |
| | SOT-23 (5) | 2.90mm × 1.60mm |
| TLV2172 | SOIC (8) | 4.90mm × 3.91mm |
| | VSSOP (8) | 3.00mm × 3.00mm |
| TLV4172 | SOIC (14) | 8.65mm × 3.91mm |
| | TSSOP (14) | 5.00mm × 4.40mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图




本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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## 4 修订历史记录

**Changes from Revision B (September 2018) to Revision C** — **Page**

- 将数据表标题从“TLV2172 36V、单电源、低功耗...” 更改成了“TLVx172 36V、单电源、低功耗...” ... 1

**Changes from Revision A (May 2018) to Revision B** — **Page**

- Deleted the *Device Family Comparison* table ... 3
- Added the 5-pin SC70 and SOT-23, and the 8-pin SOIC pinout diagrams to the data sheet ... 4
- Added TLV172 Pin Functions table to the data sheet ... 4
- Added 14-pin SOIC and TSSOP pinout diagram to the data sheet ... 6

**Changes from Original (November 2016) to Revision A** — **Page**

- Updated supply voltage values in *Absolute Maximum Ratings* table ... 7


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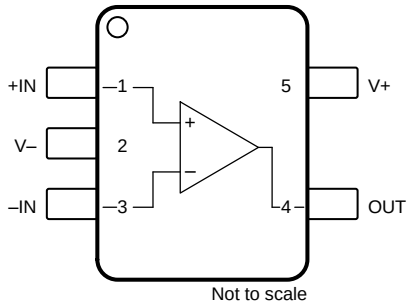
# 5 Device Comparison Table

| DEVICE | PACKAGE |
|---|---|
| TLV172 (single) | SC70-5, SOT-23-5, SOIC-8 |
| TLV2172 (dual) | SOIC-8, VSSOP-8 |
| TLV4172 (quad) | SOIC-14, TSSOP-14 |

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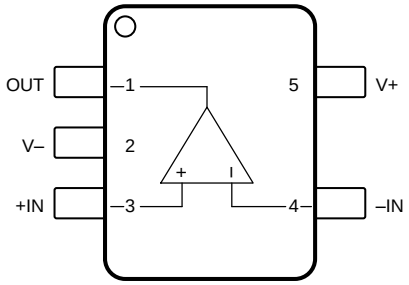
# 6 Pin Configuration and Functions

**TLV172 DCK Package**
**5-Pin SC70**
**Top View**



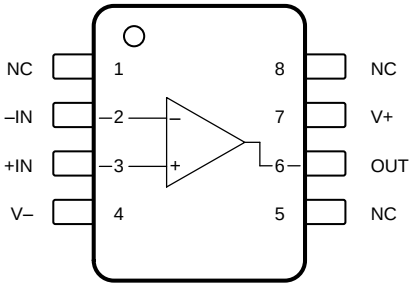

Not to scale

**TLV172 DBV Package**
**5-Pin SOT-23**
**Top View**




Not to scale

**TLV172 D Package**
**8-Pin SOIC**
**Top View**




Not to scale

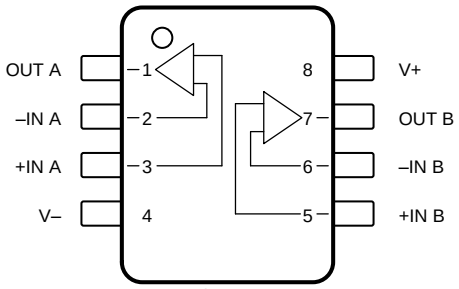
NC- no internal connection

**Pin Functions: TLV172**

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | SC70 | SOT-23 | SOIC | | |
| –IN | 3 | 4 | 2 | I | Negative (inverting) input |
| +IN | 1 | 3 | 3 | I | Positive (noninverting) input |
| NC | — | — | 1, 5, 8 | — | No internal connection (can be left floating) |
| OUT | 4 | 1 | 6 | O | Output |
| V– | 2 | 2 | 4 | — | Negative (lowest) power supply |
| V+ | 5 | 5 | 7 | — | Positive (highest) power supply |


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**TLV2172 D and DGK Packages**
**8-Pin SOIC and VSSOP**
**Top View**



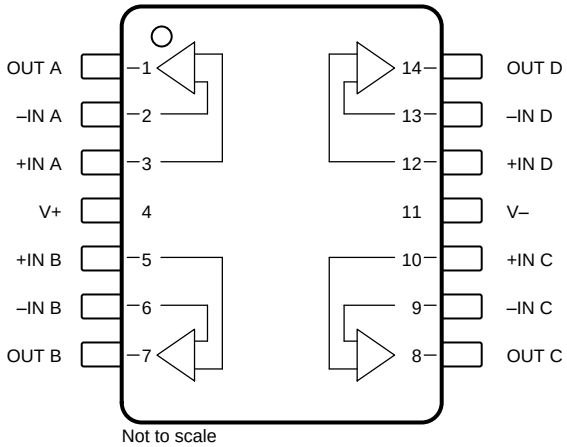

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## Pin Functions: TLV2172

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC (D) | VSSOP (DGK) | | |
| –IN A | 2 | 2 | I | Inverting input, channel A |
| –IN B | 6 | 6 | I | Inverting input, channel B |
| +IN A | 3 | 3 | I | Noninverting input, channel A |
| +IN B | 5 | 5 | I | Noninverting input, channel B |
| OUT A | 1 | 1 | O | Output, channel A |
| OUT B | 7 | 7 | O | Output, channel B |
| V– | 4 | 4 | — | Negative (lowest) power supply |
| V+ | 8 | 8 | — | Positive (highest) power supply |

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**TLV4172 D and PW Packages**
**14-Pin SOIC and TSSOP**
**Top View**




Not to scale

## Pin Functions: TLV4172

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC (D) | TSSOP (PW) | | |
| –IN A | 2 | 2 | I | Inverting input, channel A |
| –IN B | 6 | 6 | I | Inverting input, channel B |
| –IN C | 9 | 9 | I | Inverting input, channel C |
| –IN D | 13 | 13 | I | Inverting input, channel D |
| +IN A | 3 | 3 | I | Noninverting input, channel A |
| +IN B | 5 | 5 | I | Noninverting input, channel B |
| +IN C | 10 | 10 | I | Noninverting input, channel C |
| +IN D | 12 | 12 | I | Noninverting input, channel D |
| OUT A | 1 | 1 | O | Output, channel A |
| OUT B | 7 | 7 | O | Output, channel B |
| OUT C | 8 | 8 | O | Output, channel C |
| OUT D | 14 | 14 | O | Output, channel D |
| V– | 11 | 11 | — | Negative (lowest) power supply |
| V+ | 4 | 4 | — | Positive (highest) power supply |


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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage | Supply voltage, [(V+) – (V−)] | | | 40 | V |
| | Single-supply voltage | | | 40 | |
| | Signal input pin(2) | Common-mode | (V–) – 0.5 | (V+) + 0.5 | |
| | | Differential(3) | –0.5 | 0.5 | |
| Current | Signal input pin | | –10 | 10 | mA |
| | Output short-circuit(4) | | Continuous | | |
| Temperature | Operating, $T_A$ | | –55 | 150 | °C |
| | Junction, $T_J$ | | | 150 | |
| | Storage, $T_{stg}$ | | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient conditions that exceed these voltage ratings must be current limited to 10 mA or less.
(3) See the *Electrical Overstress* section for more information.
(4) Short-circuit to ground, one amplifier per package.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, (V+) – (V–) | Single-supply | 4.5 | | 36 | V |
| | Dual-supply | ±2.25 | | ±18 | |
| Specified temperature | | –40 | | 125 | °C |

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## 7.4 Thermal Information: TLV172

| THERMAL METRIC(1) | | TLV172 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | DBV (SOT-23) | DCK (SC70) | |
| | | 8 PINS | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 126.5 | 227.9 | 285.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 80.6 | 115.7 | 60.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 67.1 | 65.9 | 78.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 31.0 | 10.7 | 0.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 65.6 | 65.3 | 77.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Thermal Information: TLV2172

| THERMAL METRIC(1) | | TLV2172 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 116.1 | 158 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 69.8 | 48.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 56.6 | 78.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 22.5 | 3.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 56.1 | 77.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.6 Thermal Information: TLV4172

| THERMAL METRIC(1) | | TLV4172 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 82.7 | 111.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 42.3 | 40.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 37.3 | 54.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.9 | 3.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 37 | 53.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


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## 7.7 Electrical Characteristics

at $T_A$ = 25°C, $V_S$ = ±2.25 V to ±18 V, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 10 kΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | $T_A$ = 25°C | | | 0.5 | 1.7 | mV |
| | | $T_A$ = –40°C to +125°C | | | | 2 | |
| $dV_{OS}/dT$ | Input offset voltage drift | $T_A$ = –40°C to +125°C | | | 1 | | µV/°C |
| PSRR | Power-supply rejection ratio | $V_S$ = 4 V to 36 V, $T_A$ = –40°C to +125°C | | 100 | 120 | | dB |
| | Channel separation, dc | | | | 5 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | $T_A$ = 25°C | | | ±10 | | pA |
| $I_{OS}$ | Input offset current | $T_A$ = 25°C | | | ±2 | | pA |
| **NOISE** | | | | | | | |
| | Input voltage noise | f = 0.1 Hz to 10 Hz | | | 2.5 | | $\mu V_{PP}$ |
| $e_n$ | Input voltage noise density | f = 100 Hz | | | 14 | | $nV/\sqrt{Hz}$ |
| | | f = 1 kHz | | | 9 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input current noise density | f = 1 kHz | | | 1.6 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage range(1) | | | (V–) – 0.1 | | (V+) – 2 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = ±18 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V, $T_A$ = –40°C to +125°C | | 94 | 116 | | dB |
| **INPUT IMPEDANCE** | | | | | | | |
| | Differential | | | | 100 \|\| 4 | | MΩ \|\| pF |
| | Common-mode | | | | 6 \|\| 4 | | $10^{13}$ Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | (V–) + 0.35 V < $V_O$ < (V+) – 0.35 V, $T_A$ = –40°C to +125°C | | 97 | 115 | | dB |
| | | (V–) + 0.5 V < $V_O$ < (V+) – 0.5 V, $R_L$ = 2 kΩ, $T_A$ = –40°C to +125°C | | | 107 | | |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBP | Gain bandwidth product | | | | 10 | | MHz |
| SR | Slew rate | G = +1 | | | 10 | | V/µs |
| $t_S$ | Settling time | To 0.1%, $V_S$ = ±18 V, G = +1, 10-V step | | | 2 | | µs |
| | | To 0.01% (12-bit), $V_S$ = ±18 V, G = +1, 10-V step | | | 3.2 | | |
| | Overload recovery time | $V_{IN}$ × gain > $V_S$ | | | 200 | | ns |
| THD+N | Total harmonic distortion + noise | $V_S$ = 36 V, G = +1, f = 1 kHz, $V_O$ = 3.5 $V_{RMS}$ | | | 0.0002% | | |
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing from rail | $V_S$ = ±18 V, $R_L$ = 10 kΩ | $T_A$ = 25°C | | 70 | | mV |
| | | | $T_A$ = –40°C to +125°C | | 95 | | |
| | | $V_S$ = ±18 V, $R_L$ = 2 kΩ | $T_A$ = 25°C | | 330 | 400 | |
| | | | $T_A$ = –40°C to +125°C | | 470 | 530 | |
| $I_{SC}$ | Short-circuit current | | | | ±75 | | mA |
| $C_{LOAD}$ | Capacitive load drive | | | See *Typical Characteristics* | | | pF |
| $R_O$ | Open-loop output resistance | f = 1 MHz, $I_O$ = 0 A | | | 60 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $V_S$ | Specified voltage range | | | 4.5 | | 36 | V |
| $I_Q$ | Quiescent current per amplifier | $I_O$ = 0 A, $T_A$ = –40°C to +125°C | | | 1.6 | 2.3 | mA |

(1) The input range can be extended beyond (V+) – 2 V up to V+. See the *Typical Characteristics* and *Application and Implementation* sections for additional information.

## 7.8 Typical Characteristics

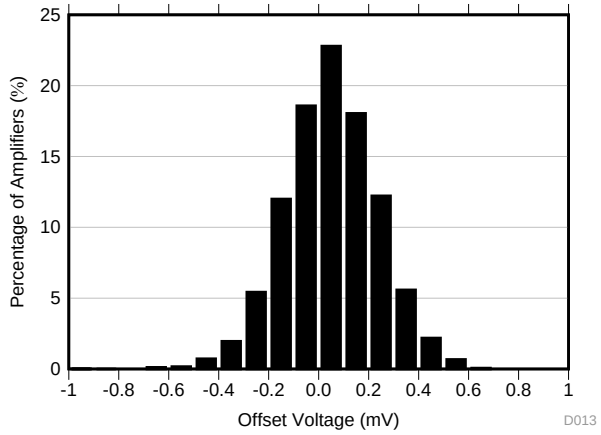
at $V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF (unless otherwise noted)

**表 1. Characteristic Performance Measurements**

| DESCRIPTION | FIGURE |
|---|---|
| Offset Voltage Production Distribution | 图 1 |
| Offset Voltage vs Common-Mode Voltage | 图 2 |
| Offset Voltage vs Common-Mode Voltage (Upper Stage) | 图 3 |
| Input Bias Current vs Temperature | 图 4 |
| Output Voltage Swing vs Output Current (Maximum Supply) | 图 5 |
| CMRR and PSRR vs Frequency (Referred-to-Input) | 图 6 |
| 0.1-Hz to 10-Hz Noise | 图 7 |
| Input Voltage Noise Spectral Density vs Frequency | 图 8 |
| Quiescent Current vs Supply Voltage | 图 9 |
| Open-Loop Gain and Phase vs Frequency | 图 10 |
| Closed-Loop Gain vs Frequency | 图 11 |
| Open-Loop Output Impedance vs Frequency | 图 12 |
| Small-Signal Overshoot vs Capacitive Load | 图 13, 图 14 |
| No Phase Reversal | 图 15 |
| Small-Signal Step Response (10 mV) | 图 16, 图 17 |
| Large-Signal Step Response | 图 18, 图 19 |
| Large-Signal Settling Time | 图 20, 图 21 |
| Short-Circuit Current vs Temperature | 图 22 |
| Maximum Output Voltage vs Frequency | 图 23 |
| EMIRR IN+ vs Frequency | 图 24 |

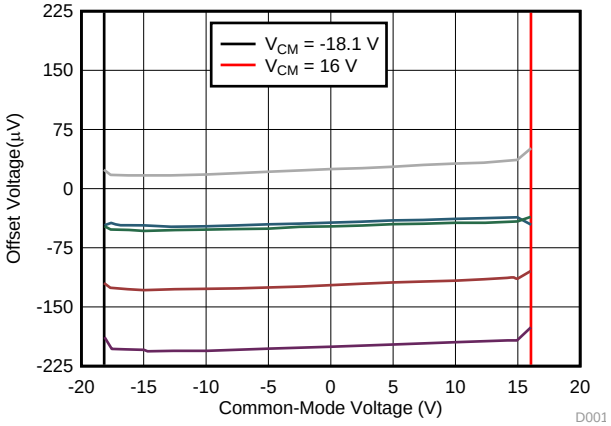

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at $V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF (unless otherwise noted)



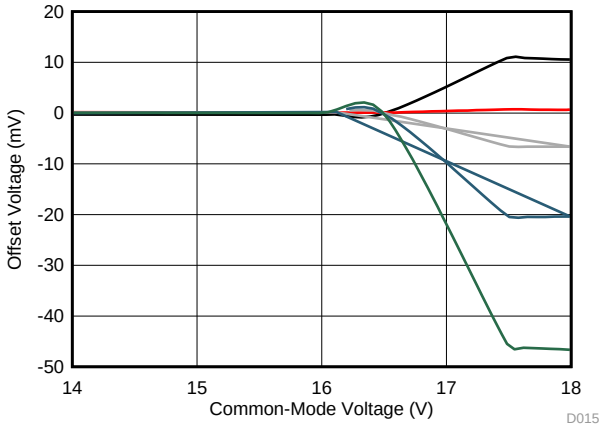

Distribution taken from 5185 amplifiers

**图 1. Offset Voltage Production Distribution Histogram**




5 typical units shown, $V_S$ = ±18 V

**图 2. Offset Voltage vs Common-Mode Voltage**




5 typical units shown, $V_S$ = ±18 V

**图 3. Offset Voltage vs Common-Mode Voltage (Upper Stage)**

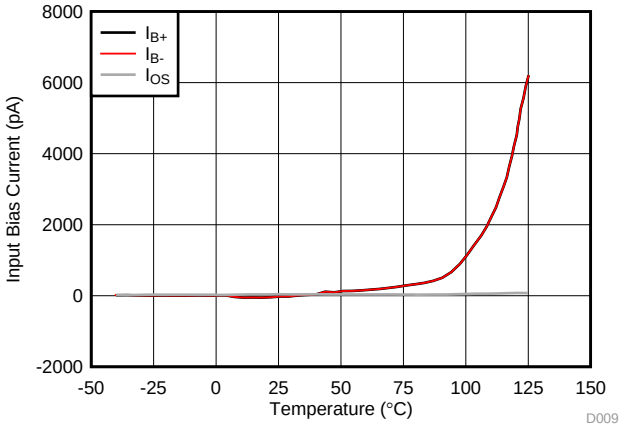



**图 4. Input Bias Current vs Temperature**

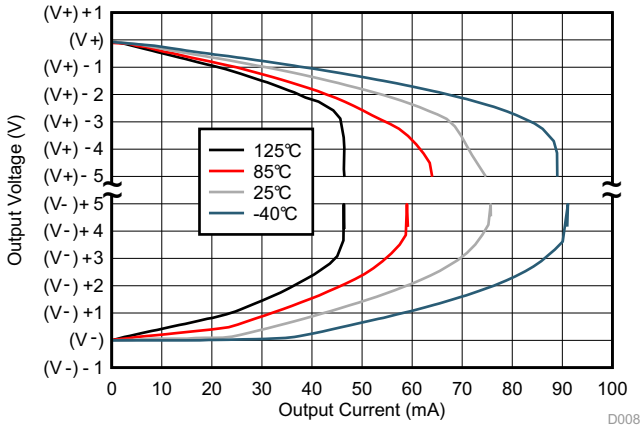



**图 5. Output Voltage Swing vs Output Current (Maximum Supply)**

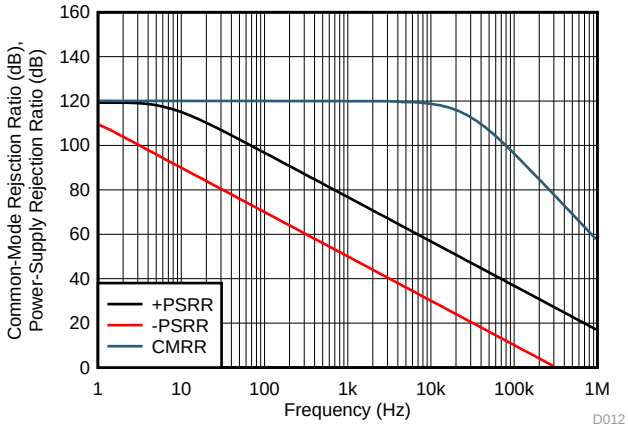



**图 6. CMRR and PSRR vs Frequency (Referred-to-Input)**

at $V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF (unless otherwise noted)

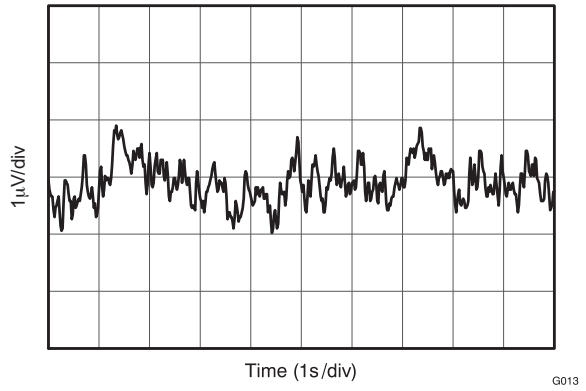



**图 7. 0.1-Hz to 10-Hz Noise**

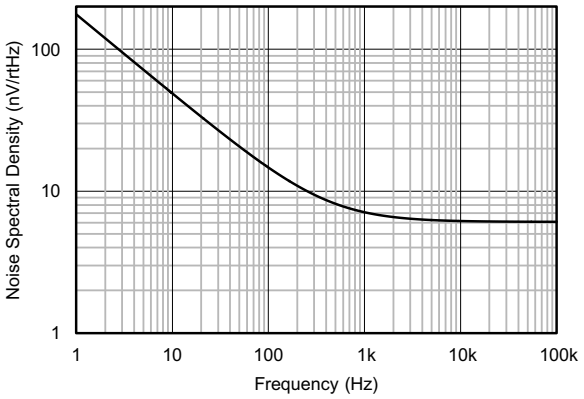



**图 8. Input Voltage Noise Spectral Density vs Frequency**

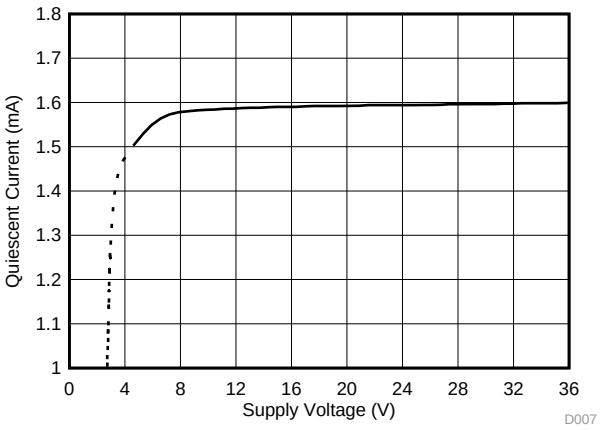
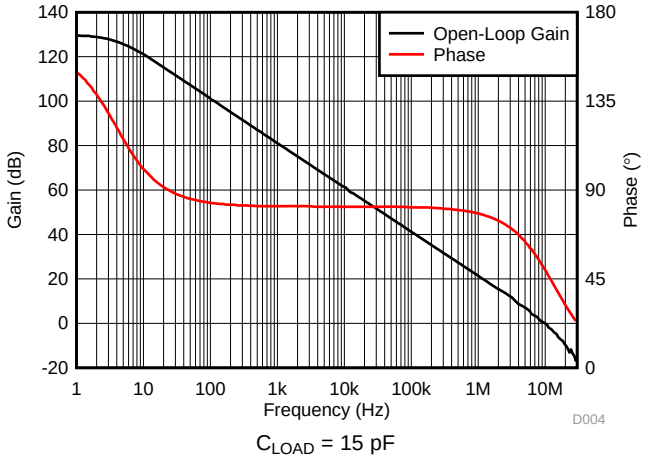



**图 9. Quiescent Current vs Supply Voltage**




$C_{LOAD}$ = 15 pF

**图 10. Open-Loop Gain and Phase vs Frequency**

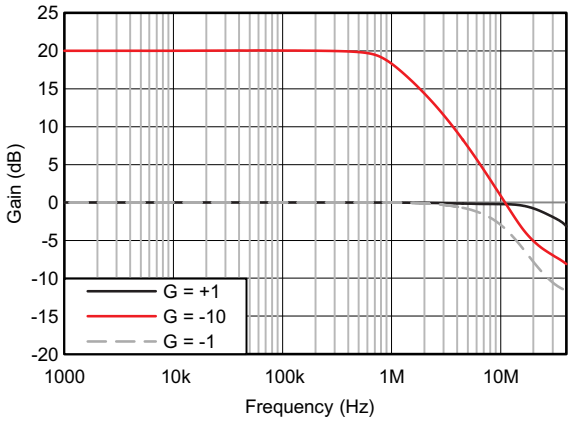



**图 11. Closed-Loop Gain vs Frequency**

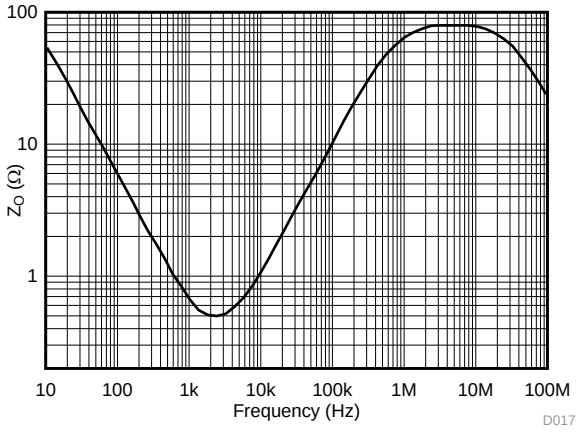
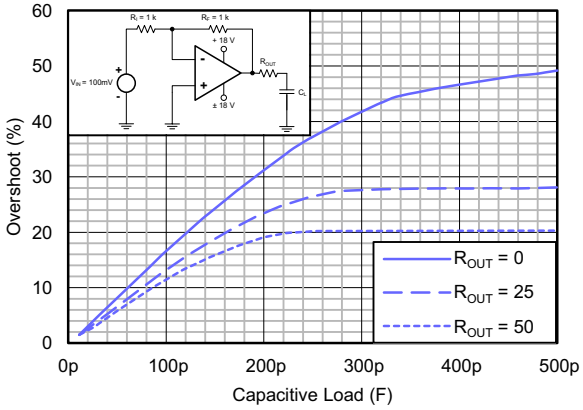



**图 12. Open-Loop Output Impedance vs Frequency**

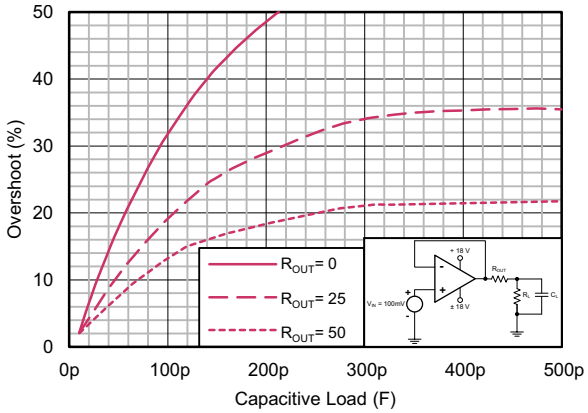

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at $V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF (unless otherwise noted)




100-mV output step, G = –1

**图 13. Small-Signal Overshoot vs Capacitive Load**




100-mV output step, G = 1

**图 14. Small-Signal Overshoot vs Capacitive Load**

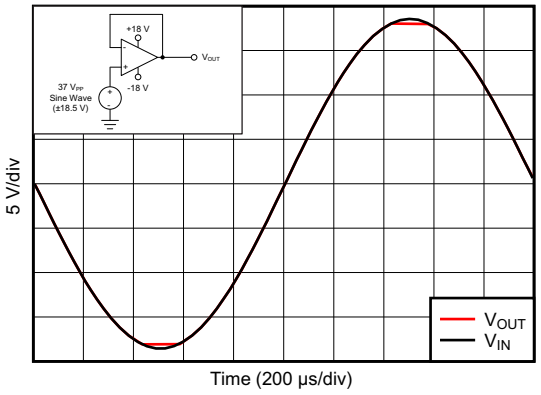
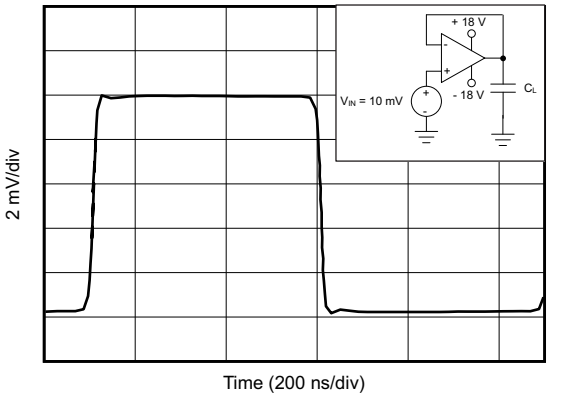
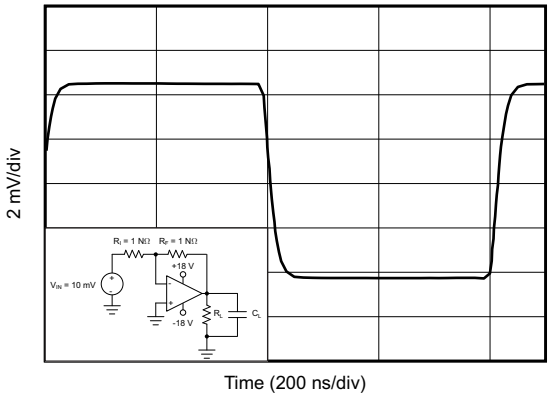



**图 15. No Phase Reversal**



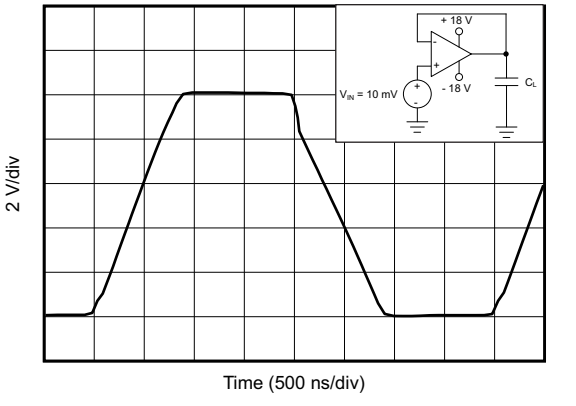

$C_L$ = 10 pF 10-mV step

**图 16. Small-Signal Step Response**




$R_L$ = 1 kΩ $C_L$ = 10 pF 10-mV step

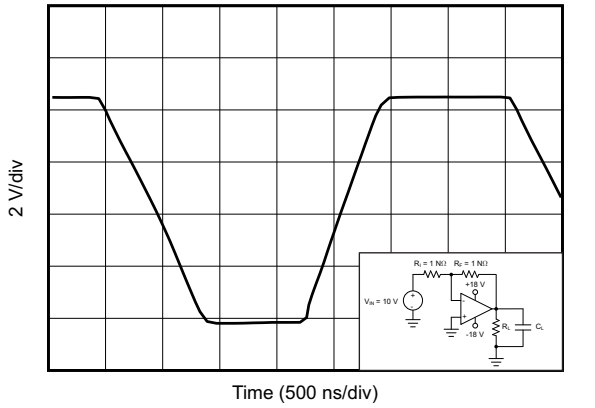
**图 17. Small-Signal Step Response**




$C_L$ = 10 pF

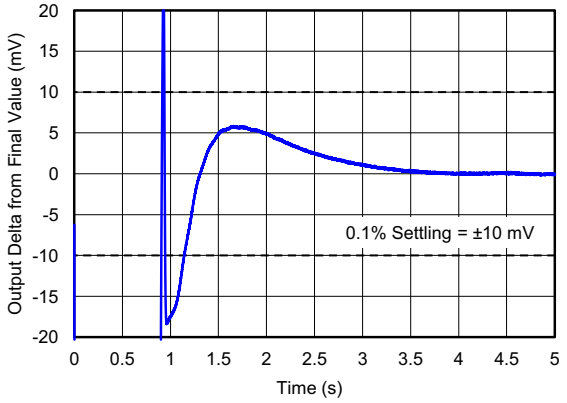
**图 18. Large-Signal Step Response**

at $V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF (unless otherwise noted)



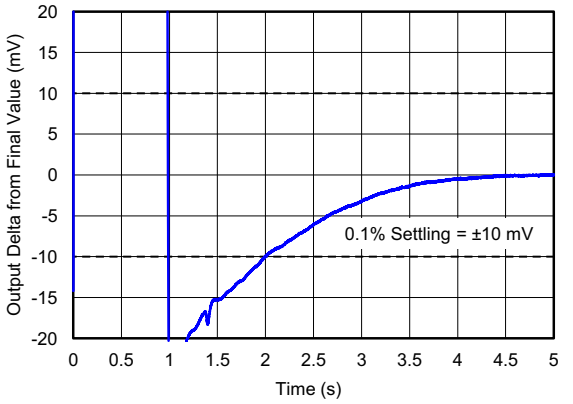

$R_L$ = 1 kΩ $C_L$ = 10 pF

**图 19. Large-Signal Step Response**




10-V positive step G = 1 $C_L$ = 10 pF

**图 20. Large-Signal Settling Time**




10-V negative step G = 1 $C_L$ = 10 pF

**图 21. Large-Signal Settling Time**

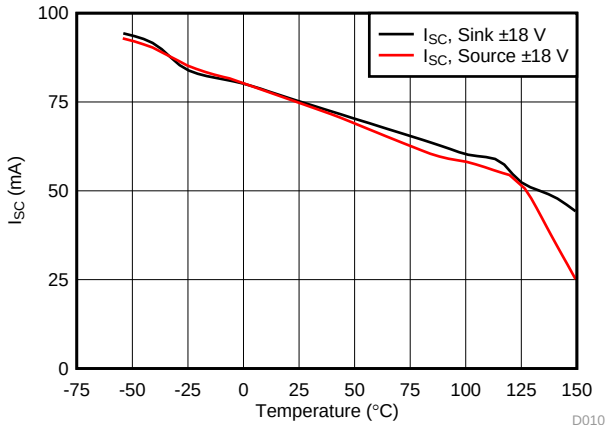



**图 22. Short-Circuit Current vs Temperature**

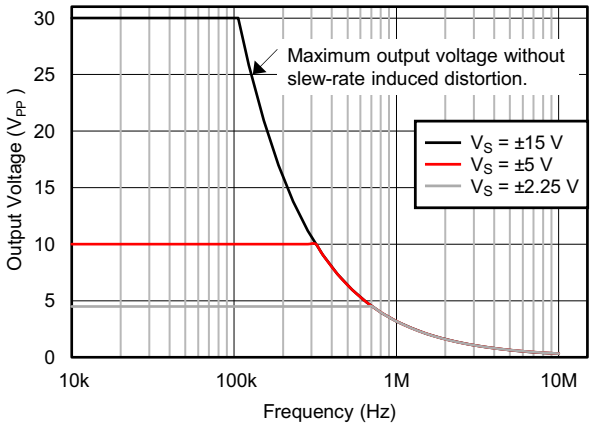
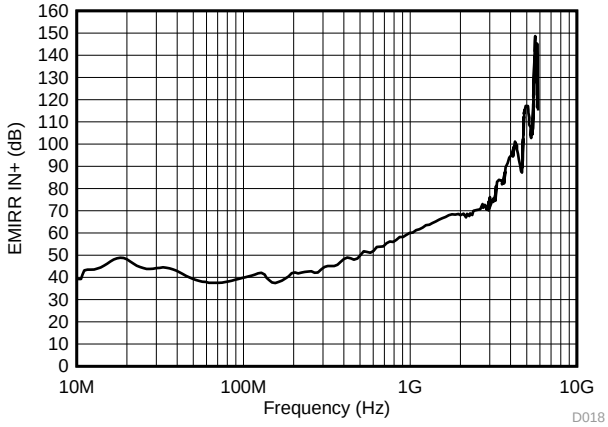



**图 23. Maximum Output Voltage vs Frequency**




$P_{RF}$ = –10 dBm $V_{SUPPLY}$ = ±18 V $V_{CM}$ = 0 V

**图 24. EMIRR IN+ vs Frequency**

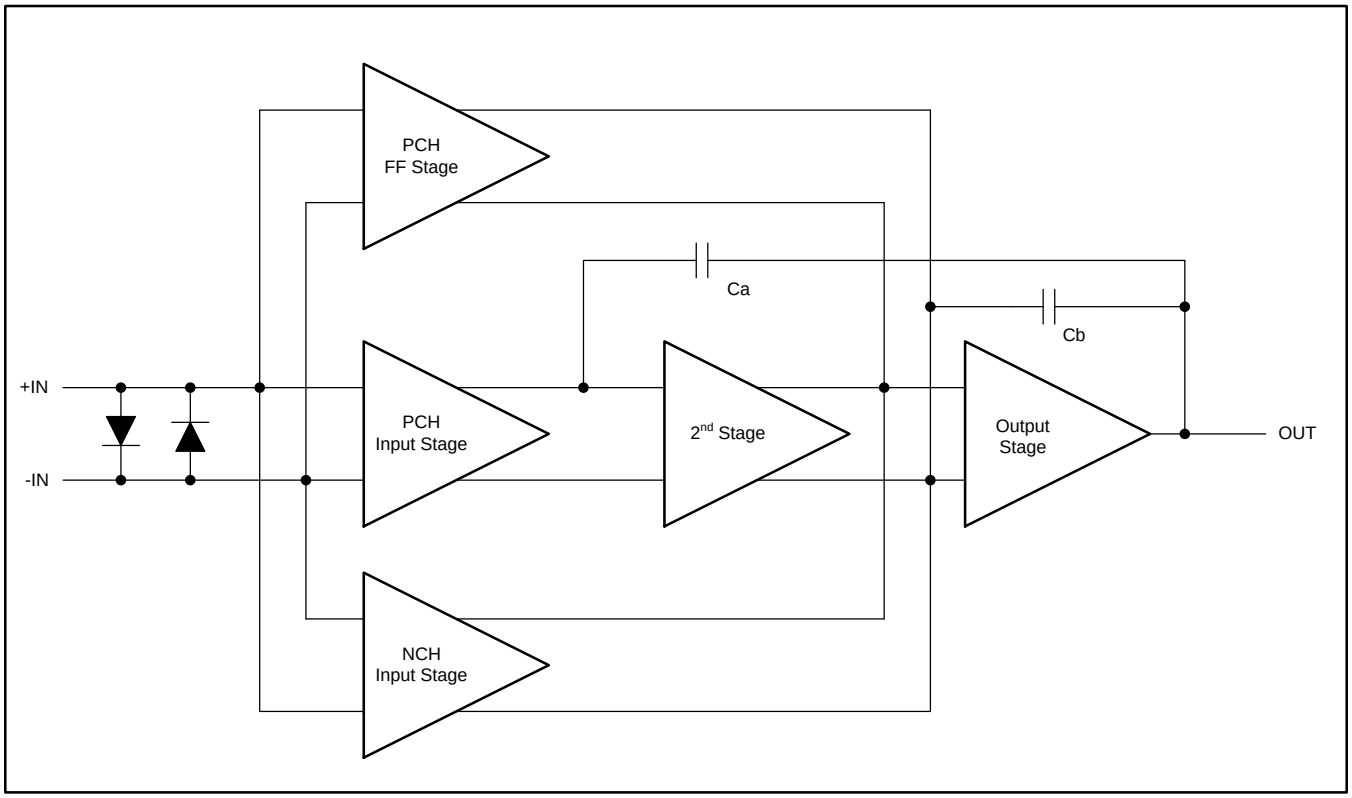

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# 8 Detailed Description

## 8.1 Overview

The TLVx172 operational amplifier provides high overall performance, making these devices designed for many general-purpose applications. The excellent offset drift of only 1 μV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and $A_{OL}$.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Operating Characteristics

The TLVx172 amplifier is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

### 8.3.2 Phase-Reversal Protection

The TLVx172 device has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the TLVx172 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in 图 25.

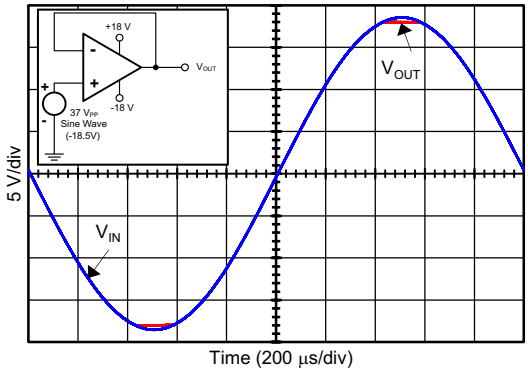



**图 25. No Phase Reversal**

### 8.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 图 26 shows the ESD circuits contained in the TLVx172 (indicated by the dashed box). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.


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## Feature Description (接下页)

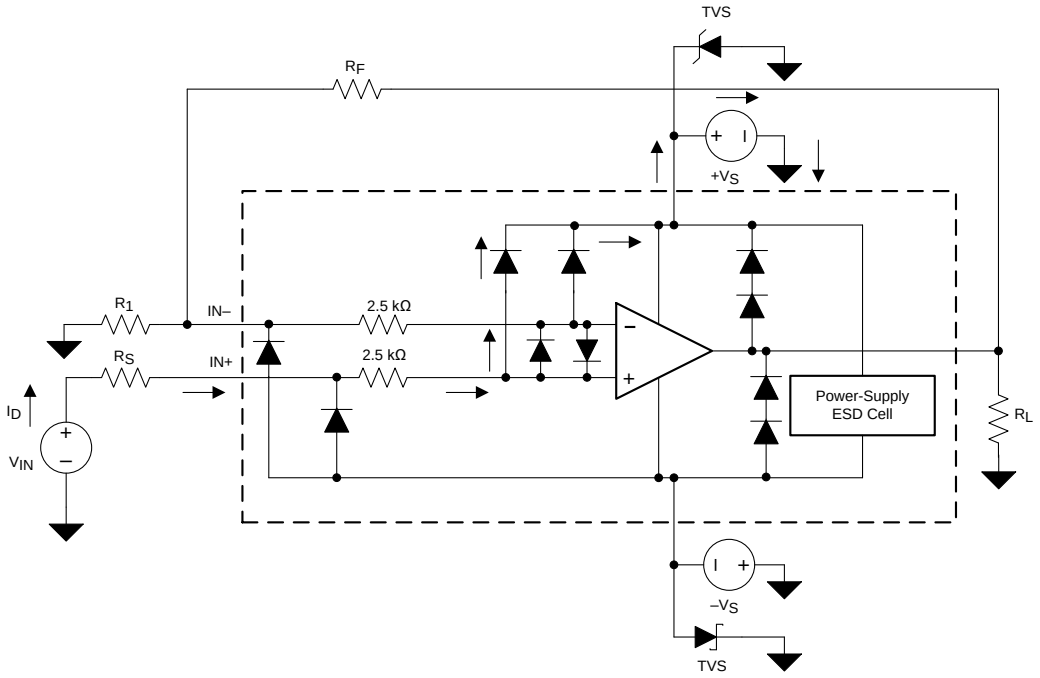



**图 26. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the TLVx172 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit, as shown in 图 26, the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

图 26 shows a specific example where the input voltage ($V_{IN}$) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, then one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher $V_{IN}$. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, $V_{IN}$ can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current and any resistance in the input path.

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## Feature Description (接下页)

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 图 26. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The input pins of the TLVx172 are protected from excessive differential voltage with back-to-back diodes; see 图 26. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, then limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can limit the input signal current. This input series resistor degrades the low-noise performance of the TLVx172. 图 26 shows an example configuration that implements a current-limiting feedback resistor.

### 8.3.4 Capacitive Load and Stability

The dynamic characteristics of the TLVx172 are optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, $R_{OUT}$ equal to 50 Ω) in series with the output. 图 27 and 图 28 show graphs of small-signal overshoot versus capacitive load for several values of $R_{OUT}$. See the *Feedback Plots Define Op Amp AC Performance* application note for details of analysis techniques and application circuits.

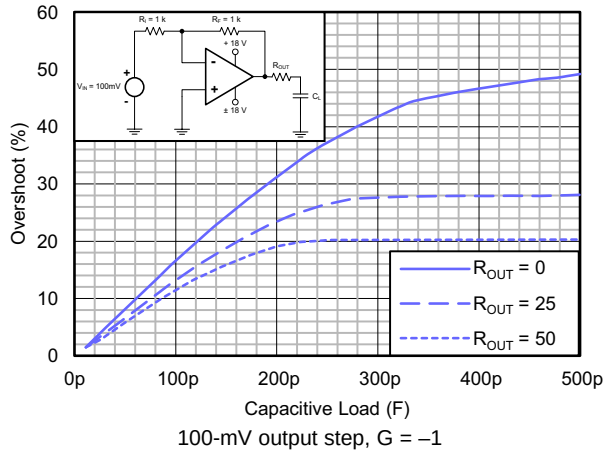



**图 27. Small-Signal Overshoot vs Capacitive Load**

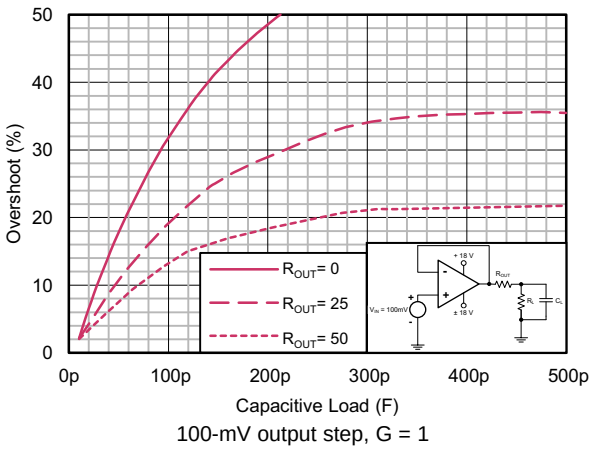



**图 28. Small-Signal Overshoot vs Capacitive Load**


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## 8.4 Device Functional Modes

### 8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the TLVx172 device extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. 表 2 lists the typical performances in this range.

**表 2. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Input common-mode voltage | (V+) – 2 | | (V+) + 0.1 | V |
| Offset voltage | | 7 | | mV |
| Offset voltage vs temperature | | 12 | | µV/°C |
| Common-mode rejection | | 65 | | dB |
| Open-loop gain | | 60 | | dB |
| Gain-bandwidth product | | 0.3 | | MHz |
| Slew rate | | 0.3 | | V/µs |

### 8.4.2 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from the saturated state to the linear state. The output devices of the operational amplifier enter the saturation region when the output voltage exceeds the rated operating voltage, which is a result from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. As a result, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLVx172 is approximately 2 µs.

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# 9 Application and Implementation

**注**

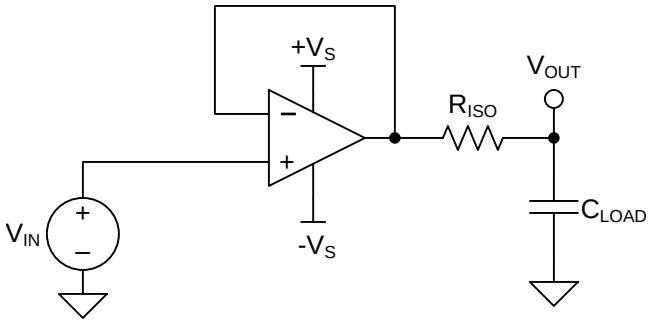
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TLVx172 operational amplifier provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Follow the additional recommendations in the *Layout Guidelines* section to achieve the maximum performance from this device. Many applications introduce capacitive loading to the output of the amplifier (which potentially causes instability). To stabilize the amplifier, add an isolation resistor between the amplifier output and the capacitive load. *Typical Application* section shows the process for selecting a resistor.

## 9.2 Typical Application

This circuit can drive capacitive loads (such as cable shields, reference buffers, MOSFET gates, and diodes). The circuit uses an isolation resistor ($R_{ISO}$) to stabilize the output of an operational amplifier. $R_{ISO}$ modifies the open-loop gain of the system to ensure that the circuit has sufficient phase margin.




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**图 29. Unity-Gain Buffer With $R_{ISO}$ Stability Compensation**

### 9.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

### 9.2.2 Detailed Design Procedure

图 29 shows a unity-gain buffer driving a capacitive load. 公式 1 shows the transfer function for the circuit in 图 29.图 29 does not show the open-loop output resistance of the operational amplifier ($R_o$).

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in 公式 1 has a pole and a zero. The frequency of the pole ($f_p$) is determined by ($R_o$ + $R_{ISO}$) and $C_{LOAD}$. The $R_{ISO}$ and $C_{LOAD}$ components determine the frequency of the zero ($f_z$). A stable system is obtained by selecting $R_{ISO}$ so that the rate of closure (ROC) between the open-loop gain ($A_{OL}$) and 1/β is 20 dB per decade. 图 30 shows the concept. The 1/β curve for a unity-gain buffer is 0 dB.


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## Typical Application (接下页)

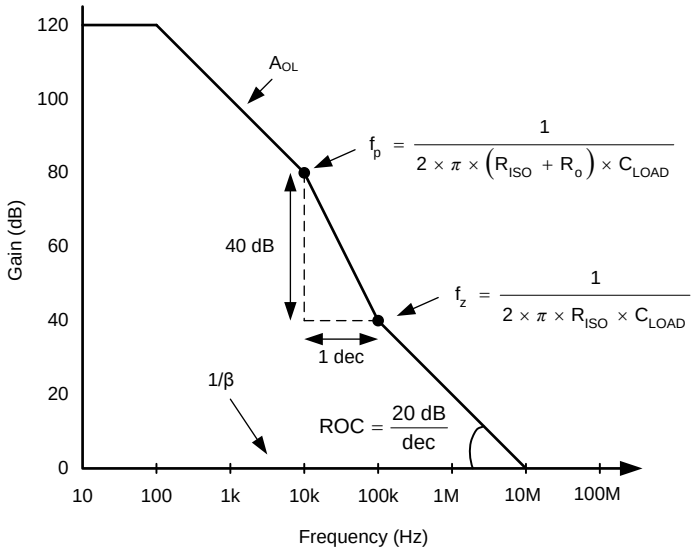



**图 30. Unity-Gain Amplifier With $R_{ISO}$ Compensation**

Typically, ROC stability analysis is simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of $R_o$. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. 表 3 shows the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can replace the TLVx172, see the *Capacitive Load Drive Solution Using an Isolation Resistor* precision design.

**表 3. Phase Margin versus Overshoot and AC Gain Peaking**

| PHASE MARGIN | OVERSHOOT | AC GAIN PEAKING |
|---|---|---|
| 45° | 23.3% | 2.35 dB |
| 60° | 8.8% | 0.28 dB |

### 9.2.3 Application Curve

The values of $R_{ISO}$ that yield phase margins of 45º and 60º for various capacitive loads are determined using the described methodology. 图 31 shows the results.

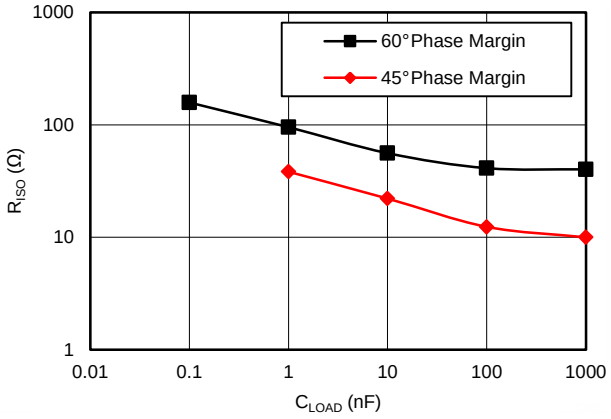



**图 31. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin**

# 10 Power Supply Recommendations

The TLVx172 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

**CAUTION**

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

# 11 Layout

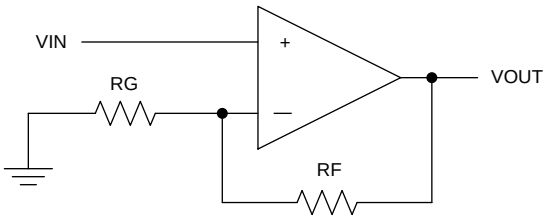
## 11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 图 33, keeping $R_F$ and $R_G$ close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

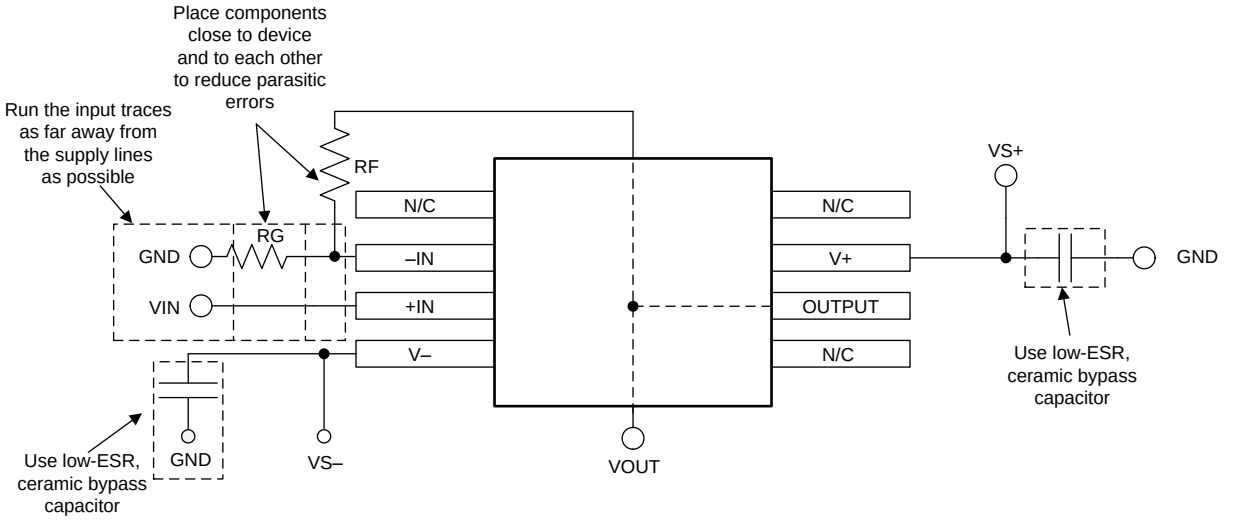

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## 11.2 Layout Example




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**图 32. Schematic Representation**




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**图 33. Operational Amplifier Board Layout for a Noninverting Configuration**

# 12 器件和文档支持

## 12.1 器件支持

### 12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

### 12.1.2 开发支持

#### *12.1.2.1 TINA-TI™（免费软件下载）*

TINA-TI™ 是一款基于 SPICE 引擎的电路仿真程序，简单易用并且功能强大。 TINA-TI™是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI™ 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI™ 提供全面的后处理能力，便于用户以多种方式获得结果，用户可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的功能，从而构建一个动态快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI™ 软件。请下载 TINA-TI™ 文件夹中的免费 TINA-TI™ 软件。

#### *12.1.2.2 DIP 适配器 EVM*

DIP 适配器 EVM 工具为小型表面贴装器件的原型设计提供了一种简易的低成本方法。评估工具使用以下 TI 封装：D 或 U (SOIC-8)、PW (TSSOP-8)、DGK (VSSOP-8)、DBV（SOT23-6、SOT23-5 和 SOT23-3）、DCK（SC70-6 和 SC70-5）以及 DRL (SOT563-6)。DIP 适配器 EVM 也可搭配引脚排使用，或者直接与现有电路相连。

#### *12.1.2.3 通用运放 EVM*

通用运放 EVM 是一系列通用空白电路板，可简化采用各种器件封装类型的电路板原型设计。借助评估模块电路板设计，可以轻松快速地构造多种不同电路。共有 5 个模型可供选用，每个模型都对应一种特定封装类型。支持 PDIP、SOIC、VSSOP、TSSOP 和 SOT23 封装。

注

这些电路板均为空白电路板，用户必须自行提供相关器件。TI 建议您在订购通用运算放大器 EVM 时申请几个运算放大器器件样品。

#### *12.1.2.4 TI 高精度设计*

TI 高精度设计是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。TI 高精度设计可从 http://www.ti.com.cn/ww/analog/precision-designs/ 在线获取。

#### *12.1.2.5 WEBENCH®滤波器设计器*

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。借助 WEBENCH 滤波设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源组件打造最佳滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® 滤波器设计器。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

## 12.2 文档支持

### 12.2.1 相关文档

如需相关文档，请参阅：


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文档支持 (接下页)

- 《反馈曲线图定义运算放大器交流性能》
- 《运算放大器的 EMI 抑制比》
- 《用直观方式补偿跨阻放大器》
- 《高速运算放大器噪声分析》

## 12.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 4. 相关链接

| 器件 | 产品文件夹 | 立即订购 | 技术文档 | 工具与软件 | 支持和社区 |
|---|---|---|---|---|---|
| TLV172 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| TLV2172 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| TLV4172 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

## 12.4 接收文档更新通知

如需接收文档更新通知，请访问 TI.com.cn 上的器件产品文件夹。单击右上角的“通知我”进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.5 社区资源

**下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。**

**TI E2E™ 在线社区** ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

**设计支持** ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

## 12.6 商标

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
DesignSoft is a trademark of DesignSoft, Inc.

## 12.7 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

# 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV172IDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 18VV |
| TLV172IDBVR.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 18VV |
| TLV172IDBVRG4.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | 18VV |
| TLV172IDBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 18VV |
| TLV172IDBVT.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 18VV |
| TLV172IDCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 15W |
| TLV172IDCKR.B | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 15W |
| TLV172IDCKRG4 | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 15W |
| TLV172IDCKRG4.B | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 15W |
| TLV172IDCKT | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 15W |
| TLV172IDCKT.B | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 15W |
| TLV172IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV172 |
| TLV172IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV172 |
| TLV2172IDGKR | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 14P6 |
| TLV2172IDGKR.B | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14P6 |
| TLV2172IDGKT | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU \| SN \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 14P6 |
| TLV2172IDGKT.B | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14P6 |
| TLV2172IDGKTG4 | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14P6 |
| TLV2172IDGKTG4.B | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 14P6 |
| TLV2172IDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TL2172 |
| TLV2172IDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TL2172 |
| TLV2172IDRG4 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TL2172 |
| TLV2172IDRG4.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TL2172 |
| TLV4172IDR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TLV4172 |
| TLV4172IDR.B | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TLV4172 |
| TLV4172IPWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV4172 |
| TLV4172IPWR.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV4172 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV2172 :**

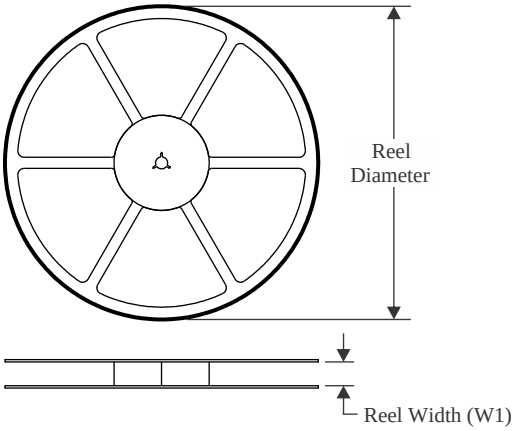
- Automotive : TLV2172-Q1

NOTE: Qualified Version Definitions:

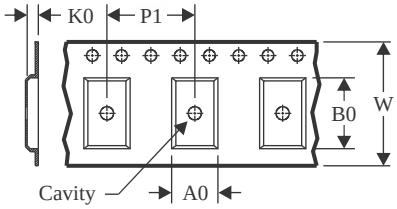
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

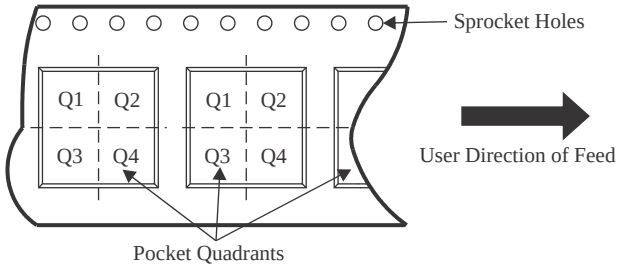



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

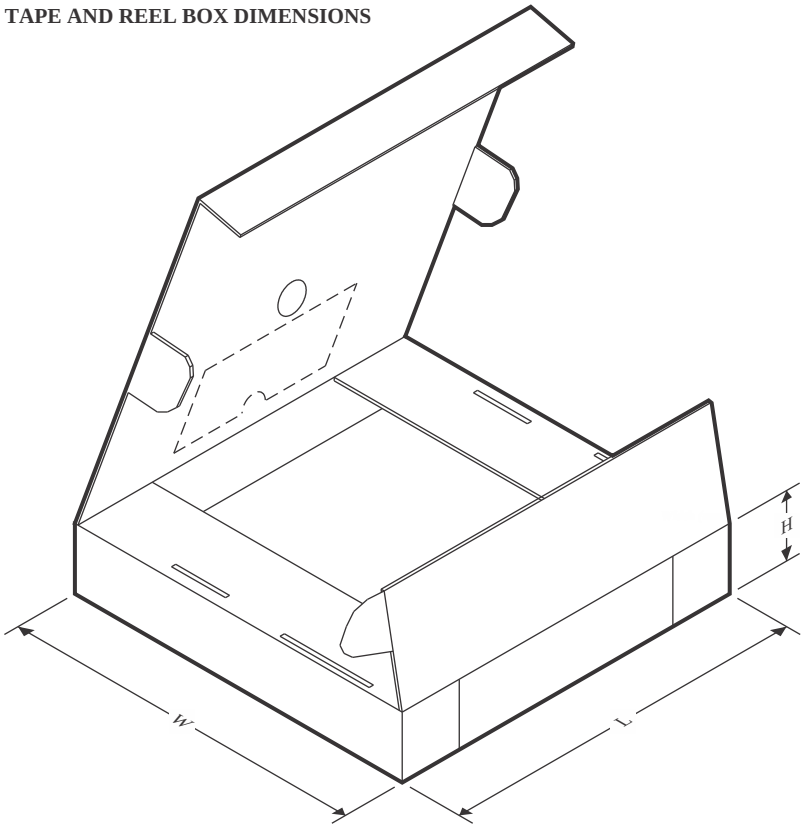
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV172IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV172IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV172IDCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV172IDCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV172IDCKRG4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV172IDCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV172IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2172IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2172IDGKT | VSSOP | DGK | 8 | 250 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2172IDGKTG4 | VSSOP | DGK | 8 | 250 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2172IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2172IDRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV4172IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV4172IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

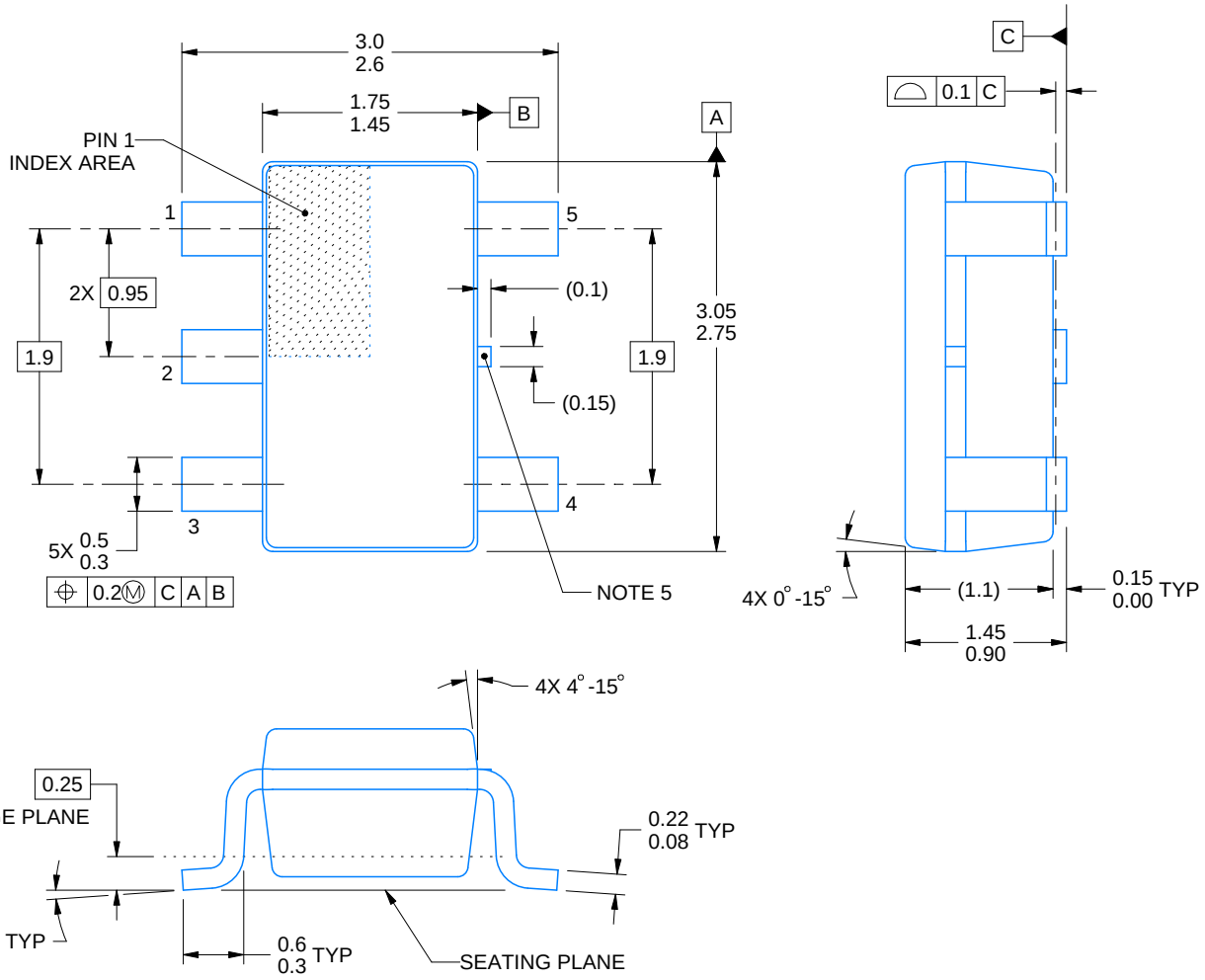
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV172IDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV172IDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV172IDCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV172IDCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV172IDCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV172IDCKT | SC70 | DCK | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV172IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV2172IDGKR | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV2172IDGKT | VSSOP | DGK | 8 | 250 | 353.0 | 353.0 | 32.0 |
| TLV2172IDGKTG4 | VSSOP | DGK | 8 | 250 | 353.0 | 353.0 | 32.0 |
| TLV2172IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV2172IDRG4 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV4172IDR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV4172IPWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

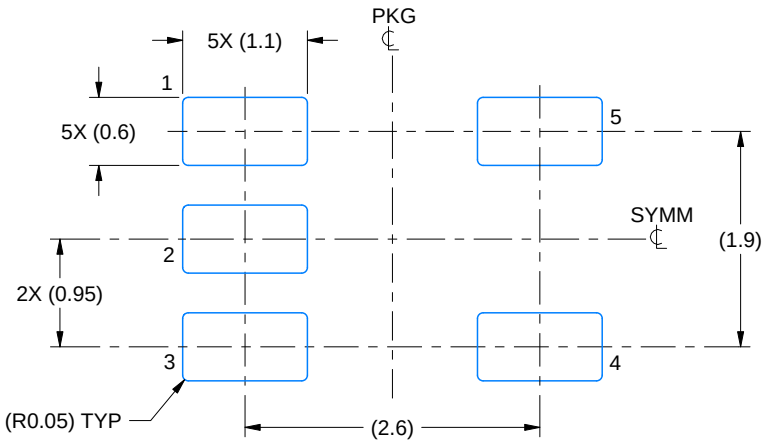
SMALL OUTLINE TRANSISTOR



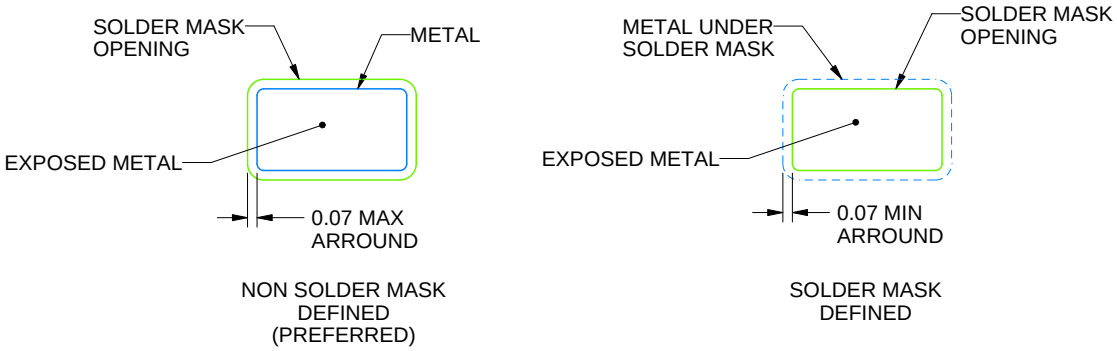

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

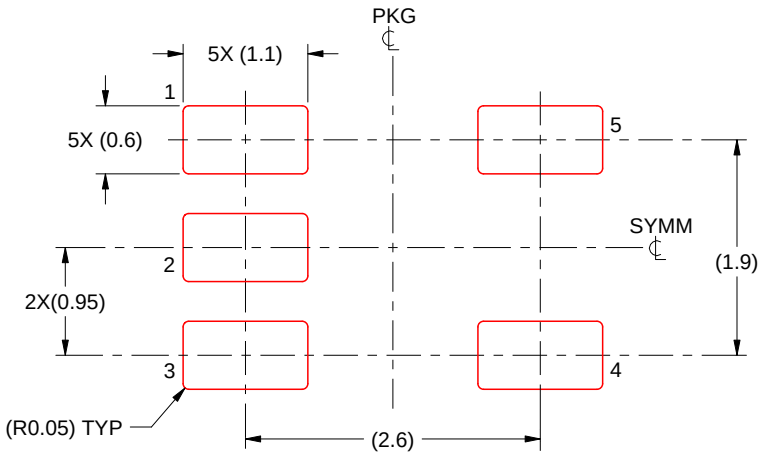



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

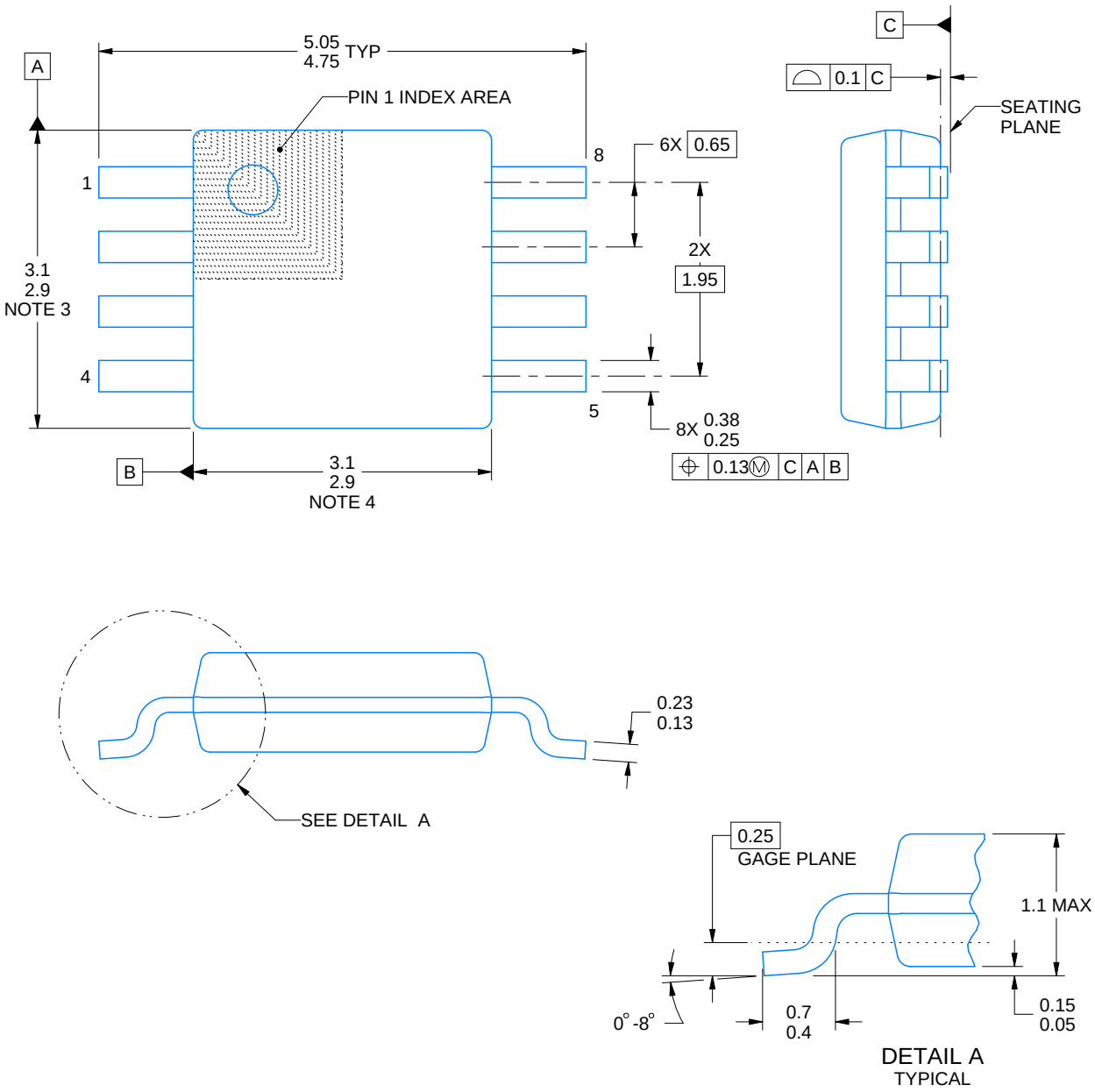
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

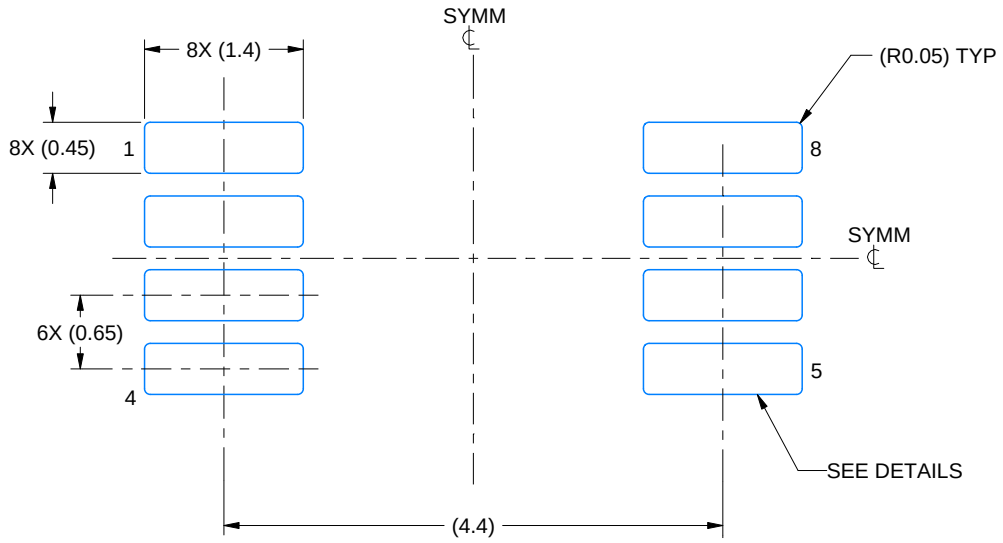
SMALL OUTLINE PACKAGE



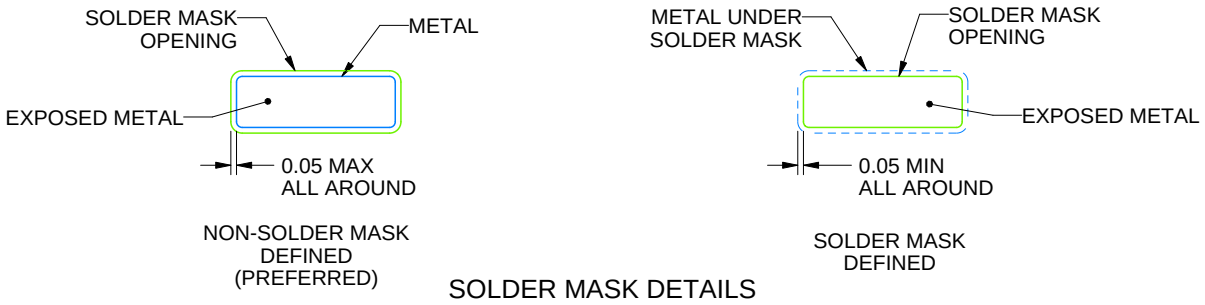

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

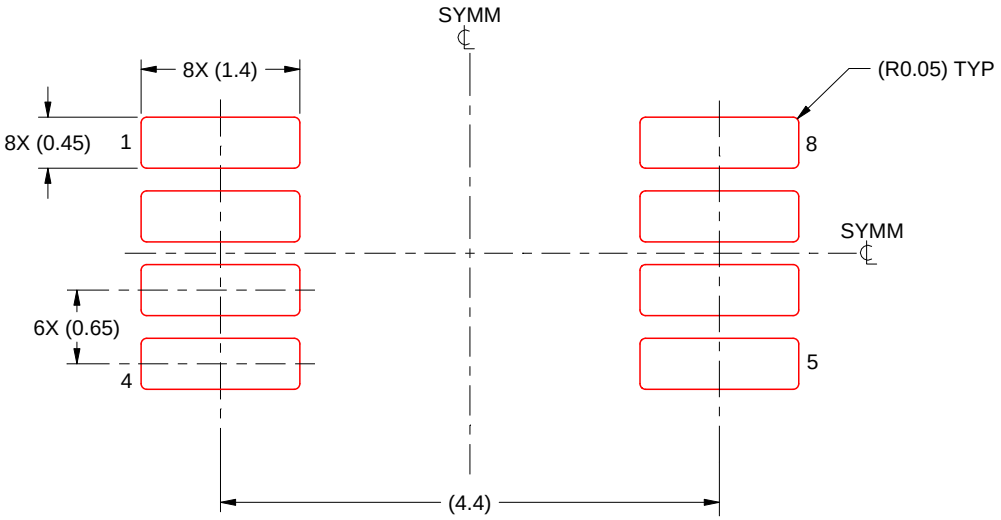



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

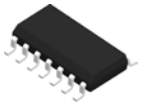



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

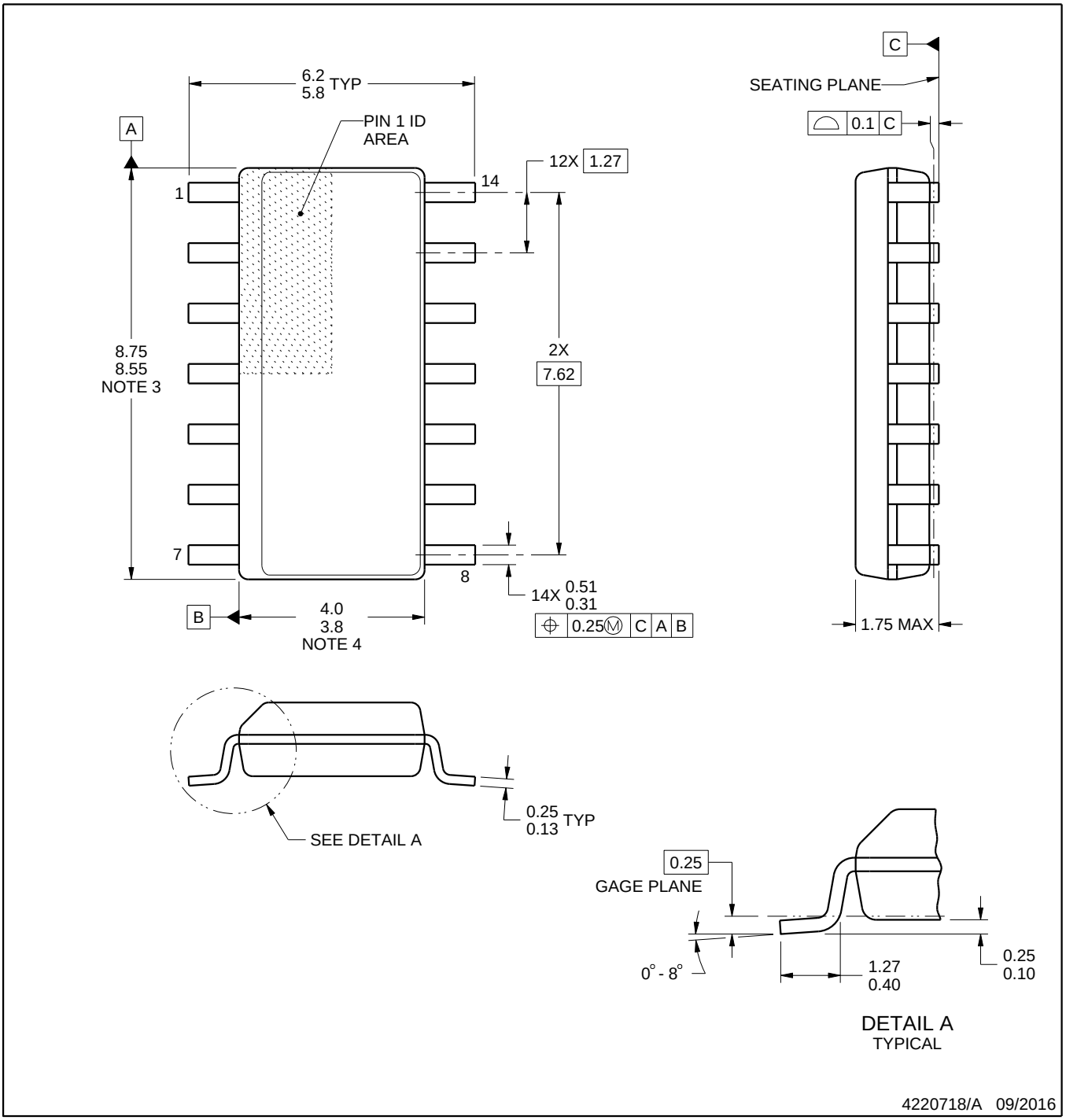


# PACKAGE OUTLINE

## D0014A

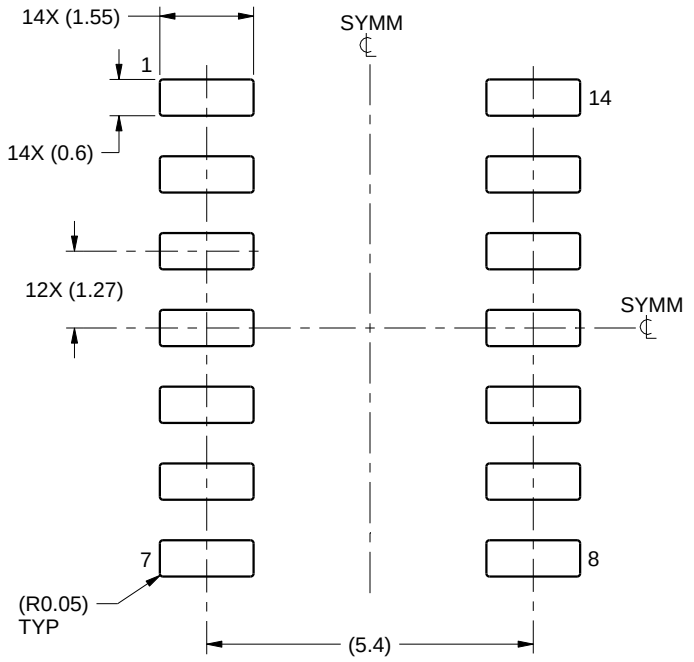
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

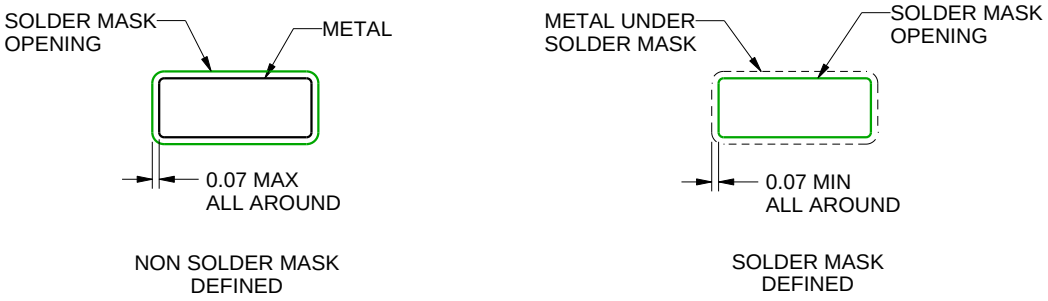



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

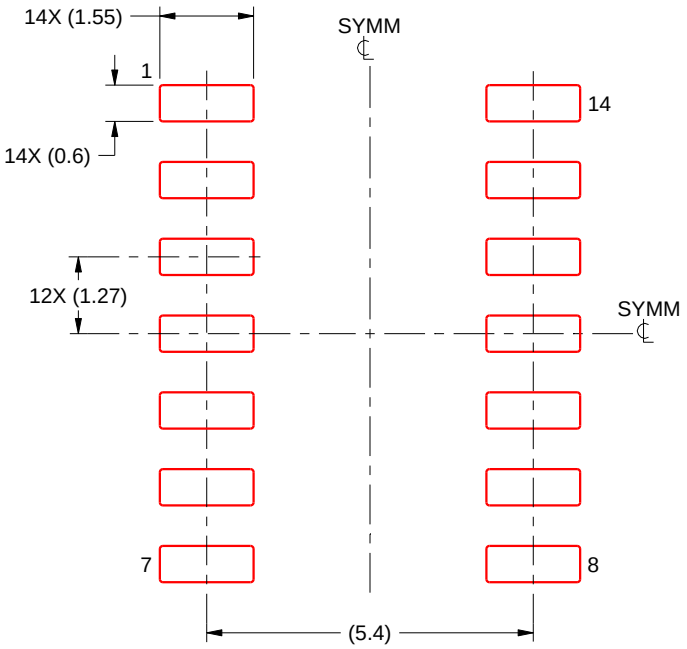
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

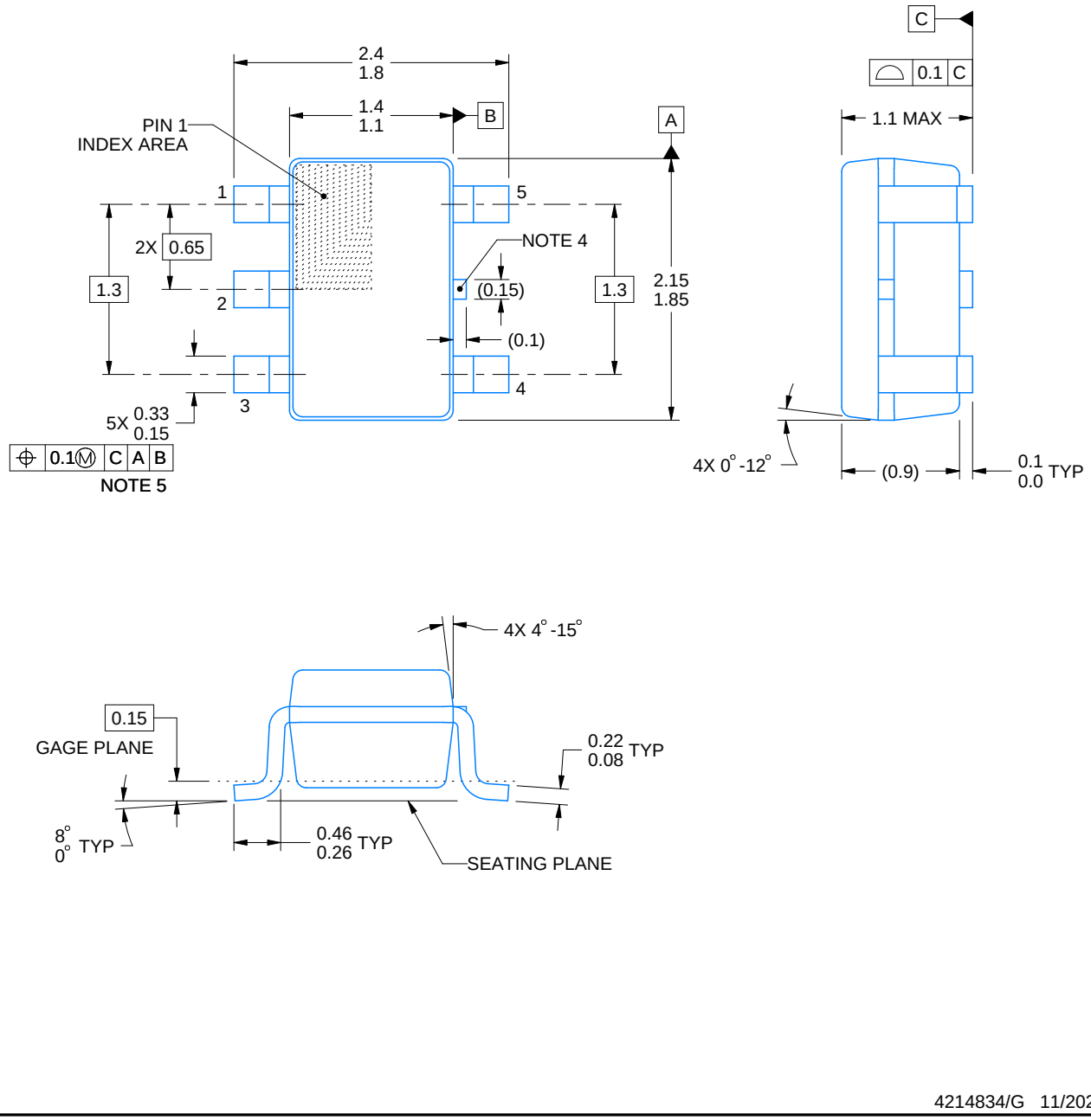
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

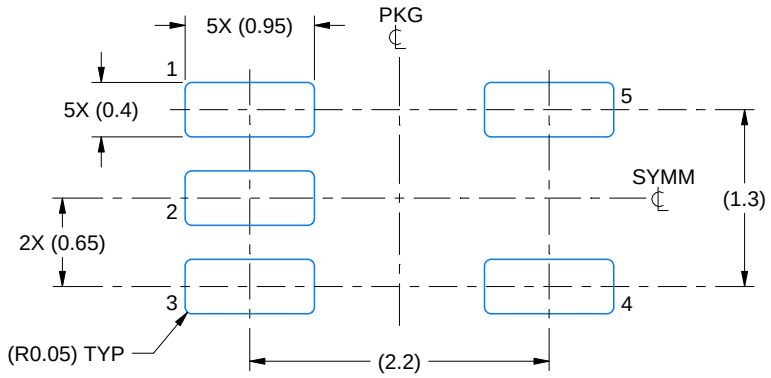
SMALL OUTLINE TRANSISTOR



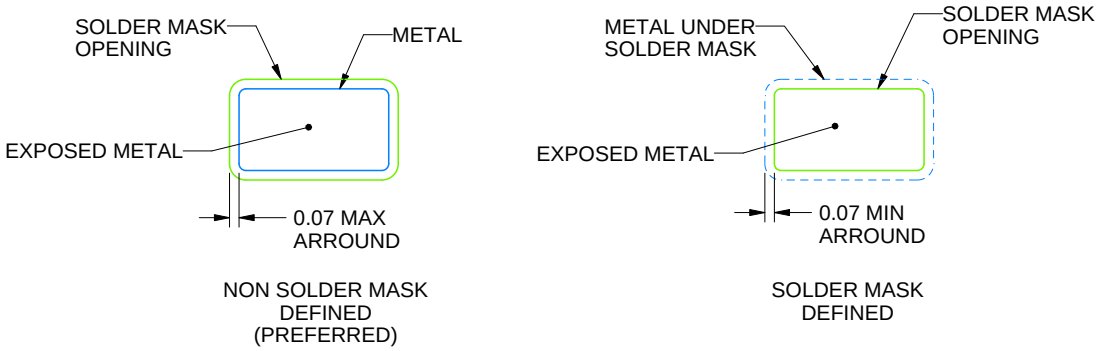

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

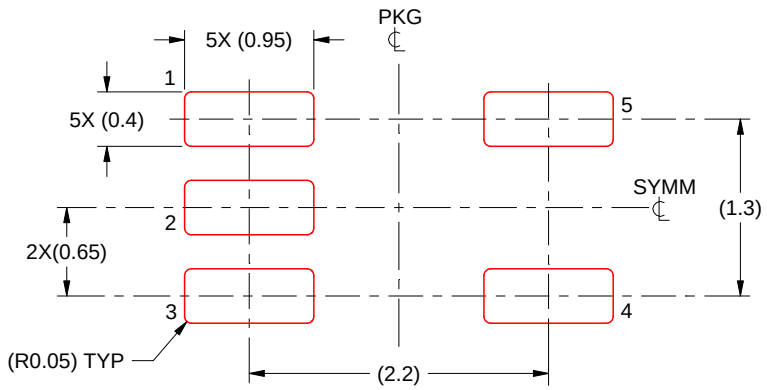



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

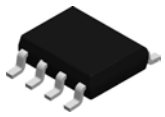



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

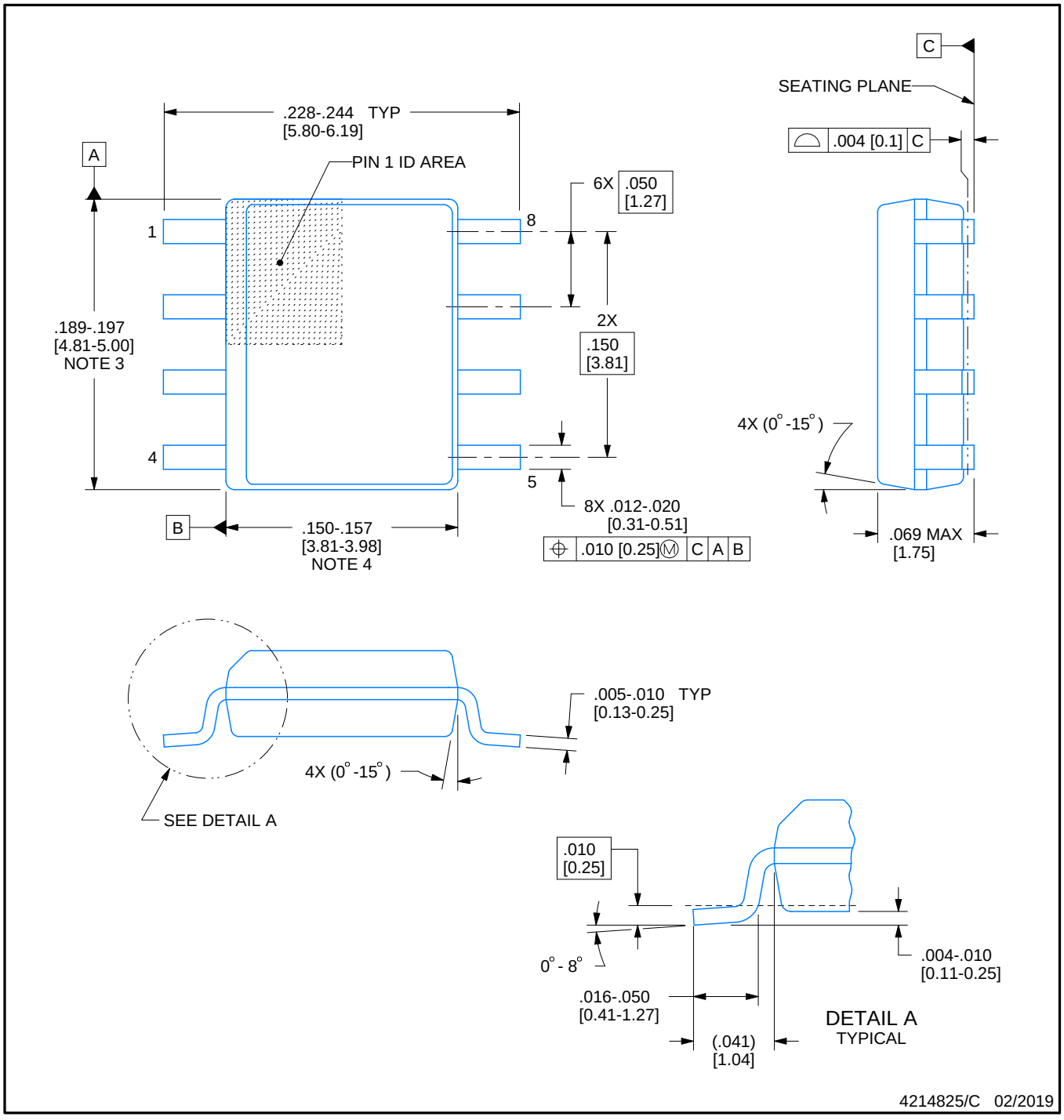


# PACKAGE OUTLINE

## D0008A

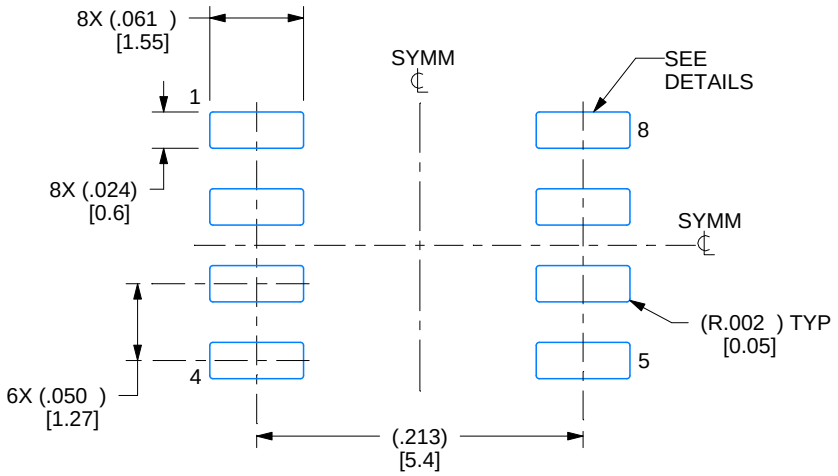
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

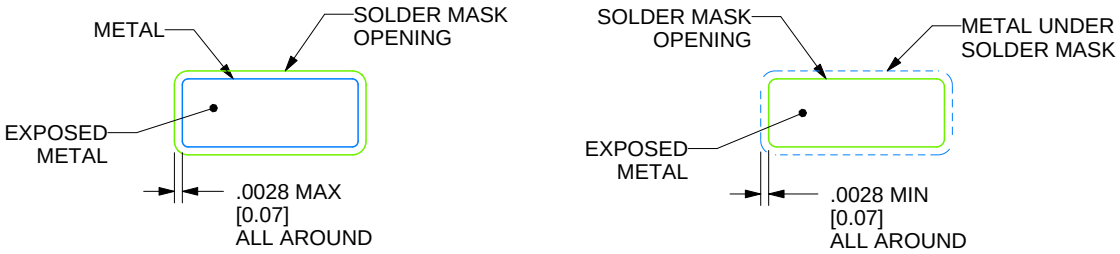



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

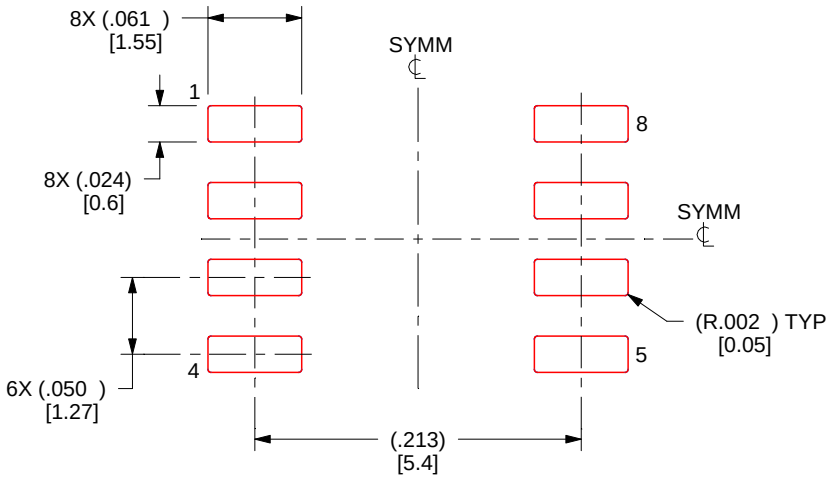
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

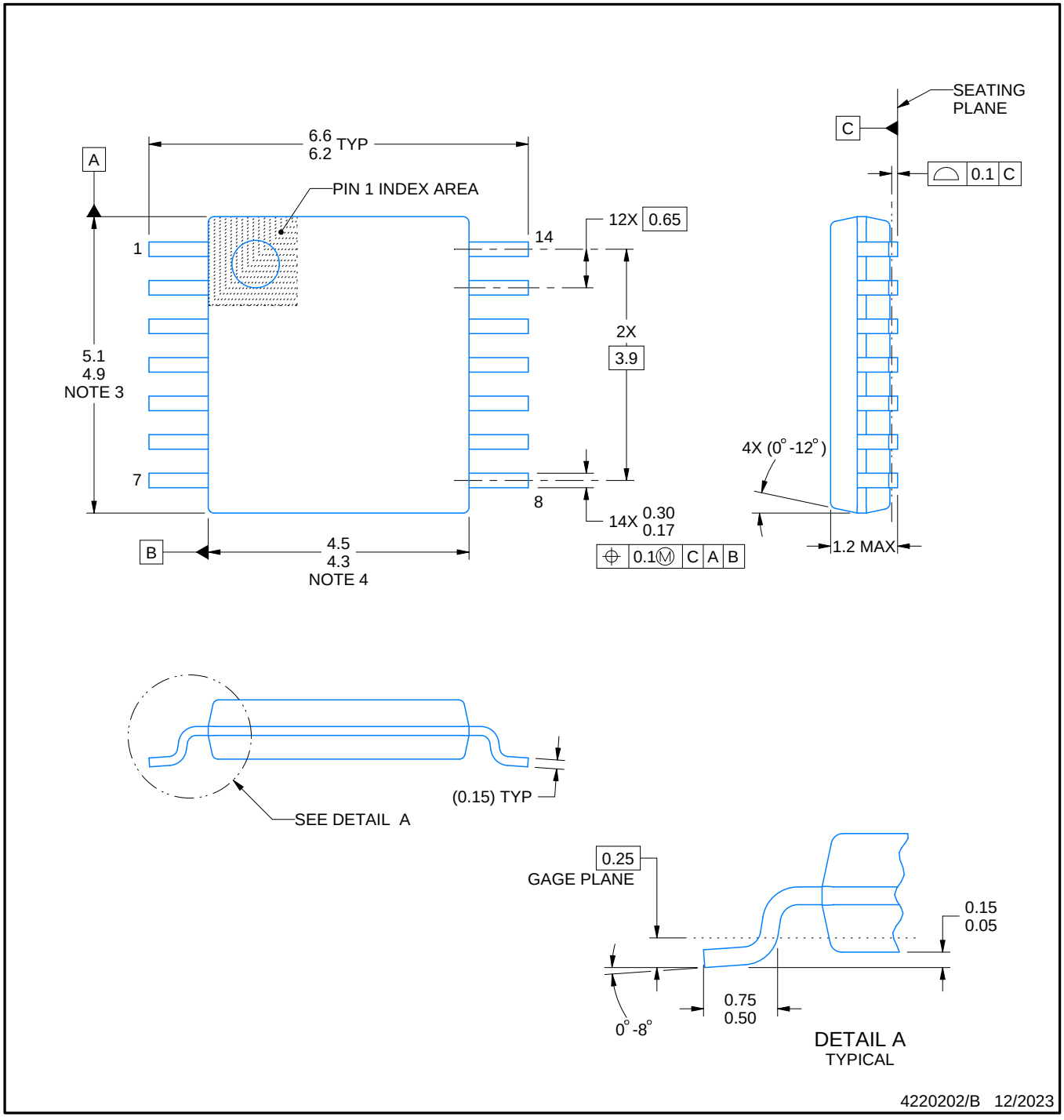
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0014A

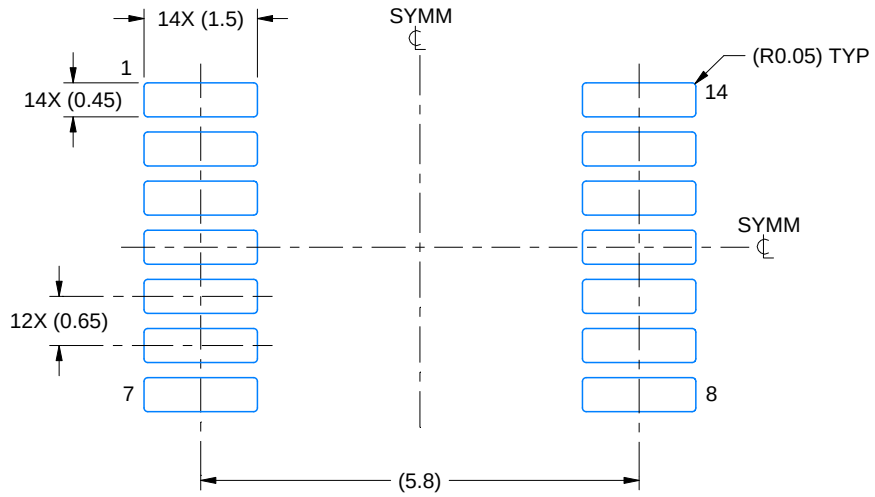
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

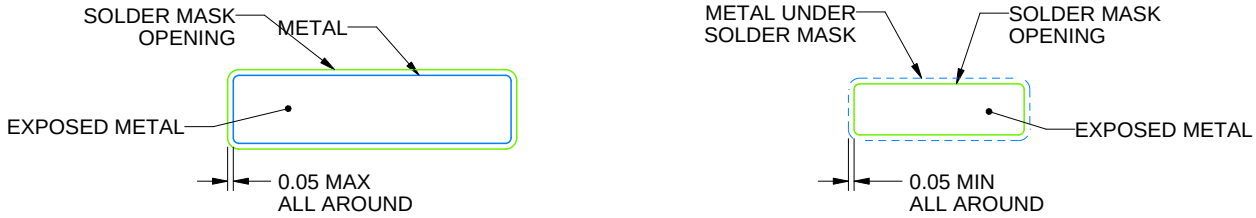



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

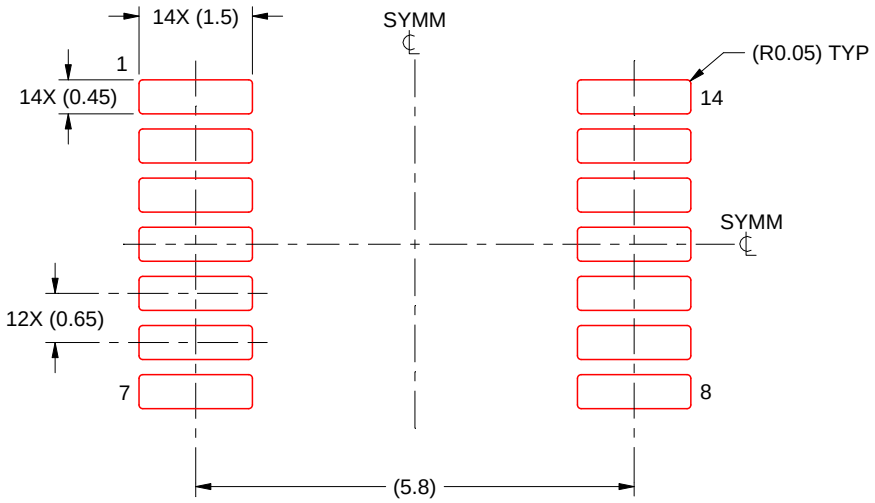



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月