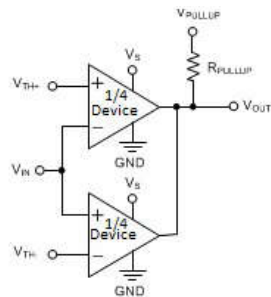


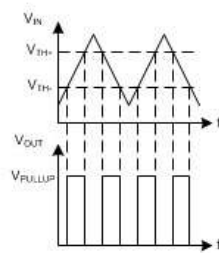
TLV1704-SEP 采用增强型航天塑料的 2.2V 至 24V 耐辐射微功耗 四路比较器

1 特性

- VID V62/18613
- 耐辐射
 - 单粒子闩锁 (SEL) 在 125°C 下的抗扰度可达 43MeV-cm²/mg
 - 在高达 30krad (Si) 的条件下无 ELDRS
 - 每个晶圆批次的总电离剂量 (TID) 高达 30krad (Si)
- 增强型航天塑料
 - 受控基线
 - 金线
 - NiPdAu 铅涂层
 - 一个封装测试厂
 - 一个制造基地
 - 支持军用 (- 55°C 至 125°C) 温度范围
 - 延长了产品生命周期
 - 延长了产品变更通知
 - 产品可追溯性
 - 采用增强型模塑化合物实现低释气
- 电源电压范围：2.2V 至 24V
- 低静态电流：每个比较器 55μA
- 输入共模范围包括两个电源轨
- 低传播延迟：560ns
- 低输入失调电压：300μV
- 集电极开路输出：
 - 最多可高出负电源电压 24V 且不受电源电压影响
- 小型封装：
 - 四通道：TSSOP-14



TLV1704-SEP 用作窗口比较器



2 应用

- 命令和数据处理 (C&DH)
- 飞行器驾驶舱显示屏
- 飞行控制单元
- 卫星电力系统 (EPS)

3 说明

TLV1704-SEP (四路) 器件具有宽电源电压范围、轨到轨输入、低静态电流和低传播延迟。所有这些特性均采用业界通用的 TSSOP-14 塑料封装，使这些器件适用于对尺寸、重量和设计灵活性要求较高的应用。

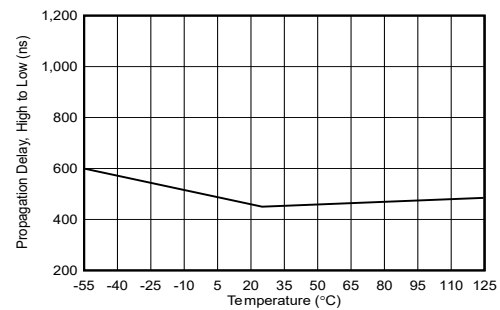
集电极开路输出带来了能够将输出电平转换为任意电压轨 (最高可高出负电源 24V) 且不受 TLV1704-SEP 电源电压影响的优势。同样，输出可连接在一起，形成单个警报信号。

此器件是一款微功耗比较器。TLV1704-SEP 器件具有低输入偏移电压、低输入偏置电流、低电源电流和集电极开路配置，非常适合电压监测、电流检测和过零检测等系统诊断。

器件信息

器件型号	等级 ⁽¹⁾	封装 ⁽²⁾
TLV1704AMPWTPSEP	30krad(Si) RLAT	TSSOP (14)
TLV1704AMPWPSEP		

- (1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。
- (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



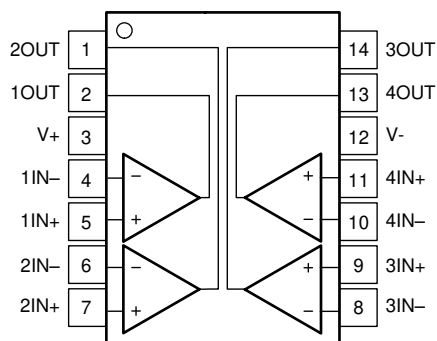
稳定传播延迟与温度



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4 Pin Configuration and Functions



**图 4-1. TLV1704-SEP PW Package
14-Pin TSSOP
Top View**

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	—	I	Noninverting input.
1IN+	5	I	Noninverting input, channel 1.
2IN+	7	I	Noninverting input, channel 2.
3IN+	9	I	Noninverting input, channel 3.
4IN+	11	I	Noninverting input, channel 4.
IN -	—	I	Inverting input.
1IN -	4	I	Inverting input, channel 1.
2IN -	6	I	Inverting input, channel 2.
3IN -	8	I	Inverting input, channel 3.
4IN -	10	I	Inverting input, channel 4.
OUT	—	O	Output.
1OUT	2	O	Output, channel 1.
2OUT	1	O	Output, channel 2.
3OUT	14	O	Output, channel 3.
4OUT	13	O	Output, channel 4.
V+	3	—	Positive (highest) power supply.
V -	12	—	Negative (lowest) power supply.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage			24	V
Signal input pins	Voltage ⁽²⁾	$(V_S -) - 0.5$	$(V_S +) + 0.5$	V
	Current ⁽²⁾		±10	mA
Output short-circuit ⁽³⁾			Continuous	mA
Operating Junction temperature, T_J		- 55	125	°C
Storage temperature, T_{stg}		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
- (3) Short-circuit to ground; one comparator per package.

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±1000	V
	Charged-device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage $V_S = (V_{S+}) - (V_{S-})$	2.2		24	V
Specified temperature	- 55		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV1704-SEP	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

at $T_A = -55^\circ\text{C}$ to 125°C , $V_S = 2.2\text{V}$ to 24V , $C_L = 15\text{pF}$, $R_{\text{PULLUP}} = 5.1\text{k}\Omega$, $V_{\text{CM}} = V_S / 2$, and $V_S = V_{\text{PULLUP}}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage	T _A = 25°C, V _S = 2.2V		±0.5	±3.5	mV
		T _A = 25°C, V _S = 24V		±0.3	±2.5	mV
		T _A = - 55°C to 125°C			±5.5	mV
dV _{OS} /dT	Input offset voltage drift	T _A = - 55°C to 125°C		±4	±20	μ V/°C
PSRR	Power-supply rejection ratio	T _A = 25°C		15	100	μ V/V
		T _A = - 55°C to 125°C		20		μ V/V
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range	T _A = - 55°C to 125°C	(V -)		(V+)	V
INPUT BIAS CURRENT						
I _B	Input bias current	T _A = 25°C		5	15	nA
		T _A = - 55°C to 125°C			20	nA
I _{OS}	Input offset current	T _A = 25°C		0.5		nA
C _{LOAD}	Capacitive load drive			See # 5.7		
OUTPUT						
V _O	Voltage output swing from rail	I _O ≤ 4mA, input overdrive = 100mV, V _S = 24V			1100	mV
		I _O = 0mA, input overdrive = 100mV, V _S = 24V			700	mV
I _{SC}	Short circuit sink current	T _A = 25°C		20		mA
	Output leakage current	V _{IN+} > V _{IN-} , T _J = 25°C		70		nA
POWER SUPPLY						
V _S	Specified voltage range		2.2		24	V
I _Q	Quiescent current (per channel)	I _O = 0A , T _A = 25°C		55	75	μ A
		I _O = 0A, T _A = - 55°C to 125°C			100	μ A

5.6 Switching Characteristics

at $T_A = -55^\circ\text{C}$ to 125°C , $V_S = 2.2\text{V}$ to 24V , $C_L = 15\text{pF}$, $R_{\text{PULLUP}} = 5.1\text{k}\Omega$, $V_{\text{CM}} = V_S / 2$, and $V_S = V_{\text{PULLUP}}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHL} Propagation delay time, high-to-low	Input overdrive = 100mV, $T_A = 25^\circ\text{C}$		460		ns
t_{pLH} Propagation delay time, low-to-high	Input overdrive = 100mV, $T_A = 25^\circ\text{C}$		560		ns
t_R Rise time	Input overdrive = 100mV, $T_A = 25^\circ\text{C}$		365		ns
t_F Fall time	Input overdrive = 100mV, $T_A = 25^\circ\text{C}$		240		ns

5.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $R_{\text{PULLUP}} = 5.1\text{k}\Omega$, and input overdrive = 100mV (unless otherwise noted)

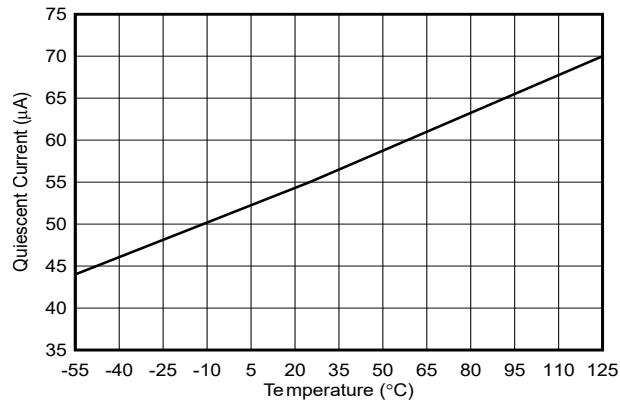


图 5-1. Quiescent Current vs Temperature

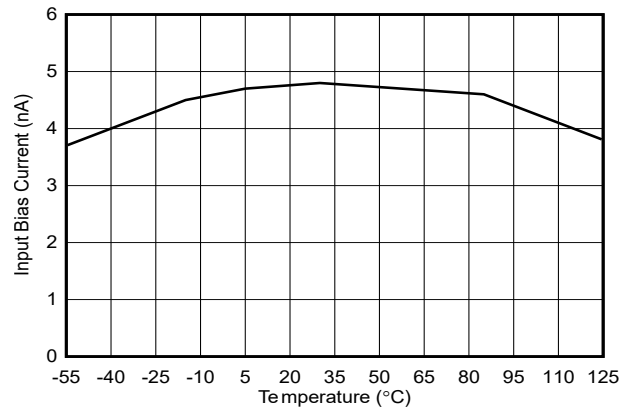


图 5-2. Input Bias Current vs Temperature

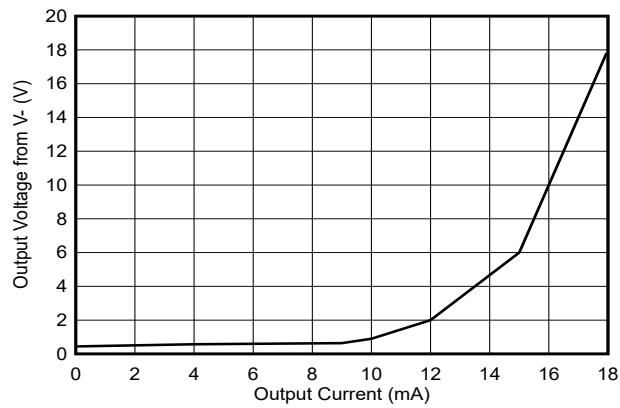


图 5-3. Output Voltage vs Output Current

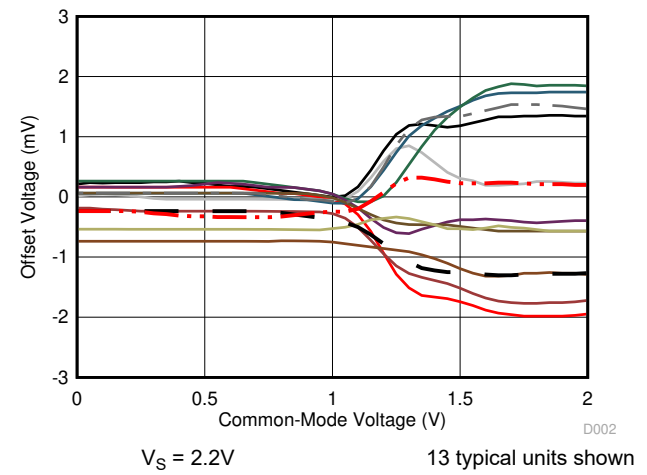


图 5-4. Offset Voltage vs Common-Mode Voltage

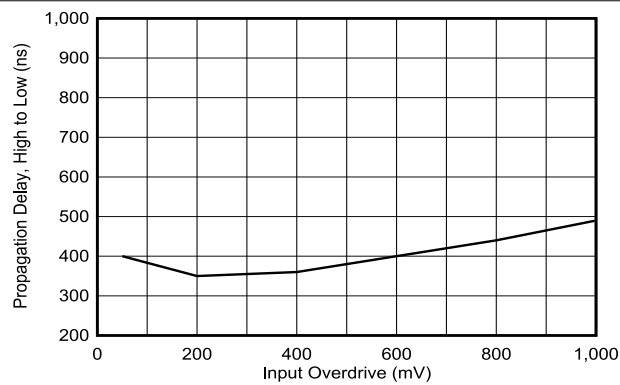


图 5-5. Propagation Delay vs Input Overdrive

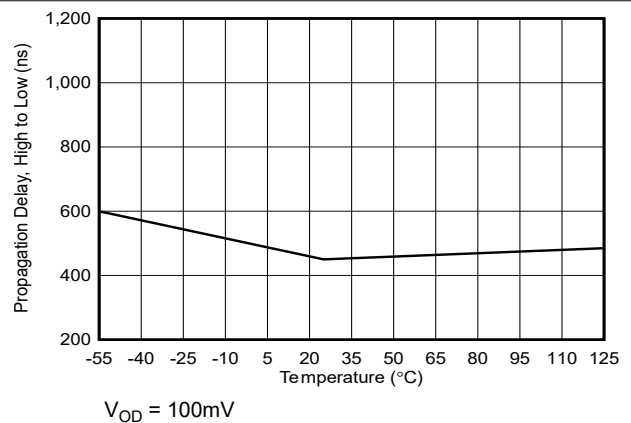
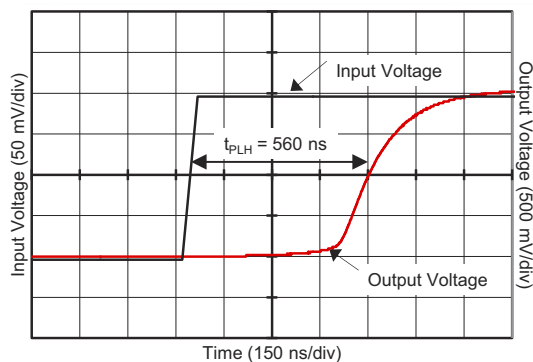


图 5-6. Propagation Delay vs Temperature

5.7 Typical Characteristics (continued)

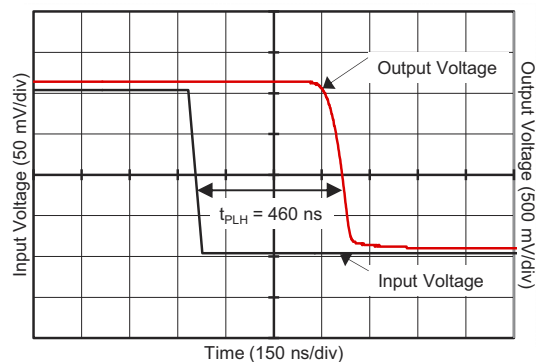
at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $R_{\text{PULLUP}} = 5.1\text{k}\Omega$, and input overdrive = 100mV (unless otherwise noted)



C009

$V_S = 2.2\text{V}$ Overdrive = 100mV

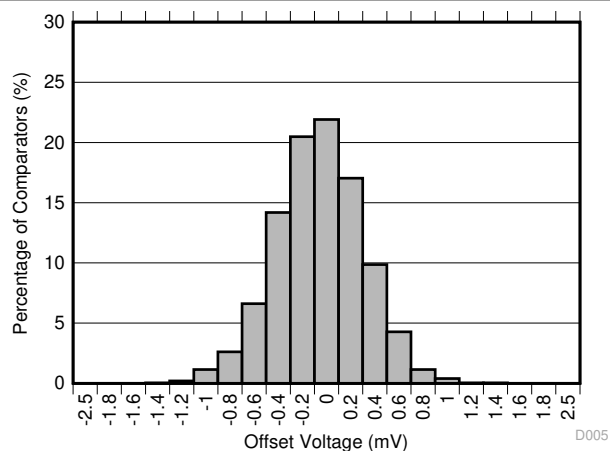
图 5-7. Propagation Delay (T_{pLH})



C010

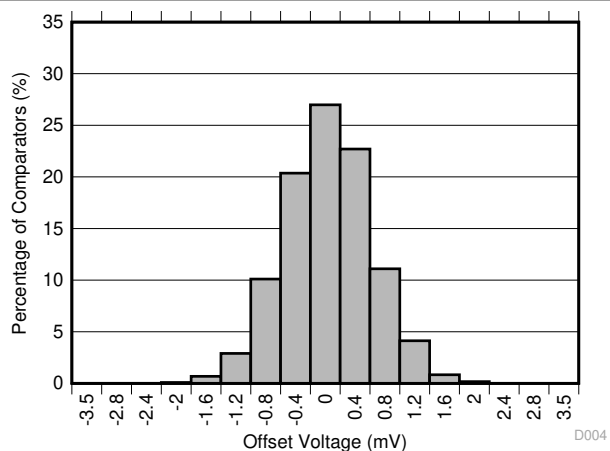
$V_S = 2.2\text{V}$ Overdrive = 100mV

图 5-8. Propagation Delay (T_{pHL})



$V_S = 24\text{V}$ Distribution taken from 2524 comparators

图 5-9. Offset Voltage Production Distribution



$V_S = 2.2\text{V}$ Distribution taken from 2524 comparators

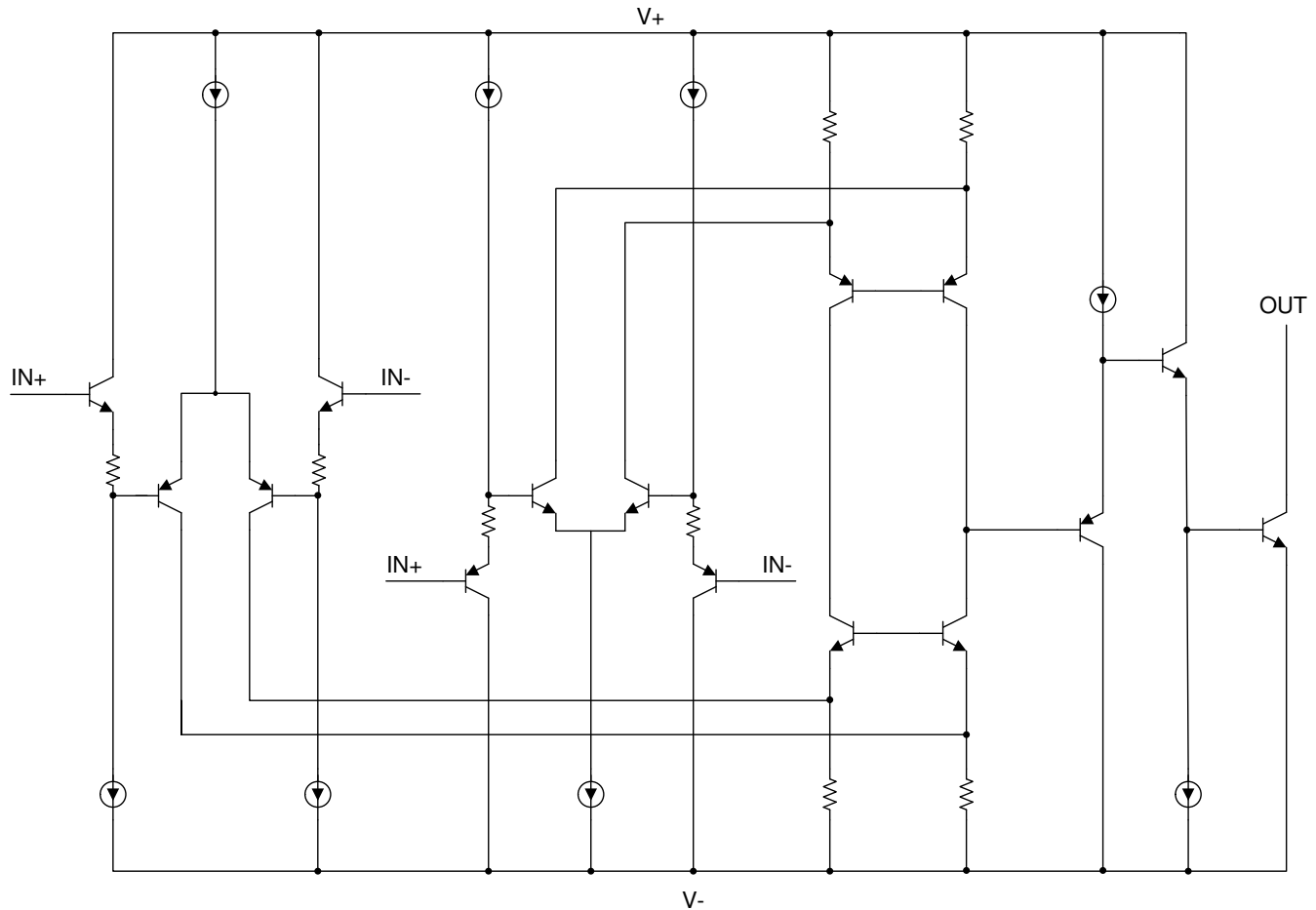
图 5-10. Offset Voltage Production Distribution

6 Detailed Description

6.1 Overview

The TLV1704-SEP comparator features rail-to-rail input and output on supply voltages as high as 24V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open-collector configuration allows the device to be used in wired-OR configurations, such as a window comparator. A low supply current of 55 μ A per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Comparator Inputs

The TLV1704-SEP device is a rail-to-rail input comparator, with an input common-mode range that includes the supply rails. The TLV1704-SEP device is designed to prevent phase inversion when the input pins exceed the supply voltage. 图 6-1 shows the TLV1704-SEP device response when input voltages exceed the supply, resulting in no phase inversion.

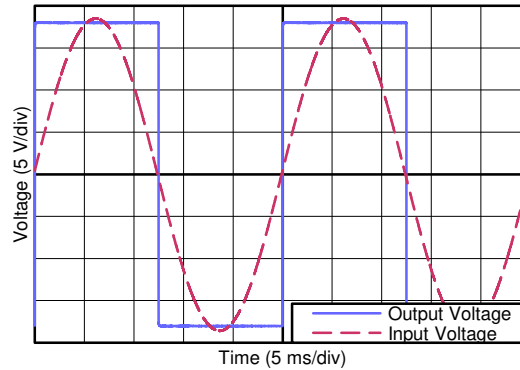


图 6-1. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

6.4 Device Functional Modes

6.4.1 Setting Reference Voltage

Using a stable reference is important when setting the transition point for the TLV1704-SEP device. The REF3333, as shown in 图 6-2, provides a 3.3V reference voltage with low drift and only 3.9 μ A of quiescent current.

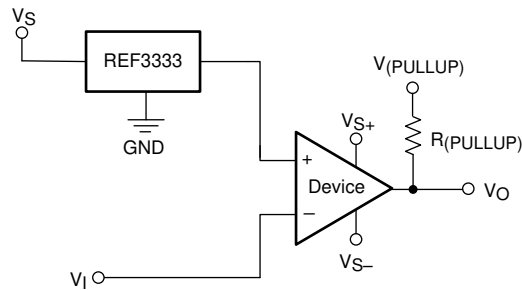


图 6-2. Reference Voltage for the TLV1704-SEP

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TLV1704-SEP device can be used in a wide variety of applications, such as zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

7.2 Typical Application

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an overtemperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

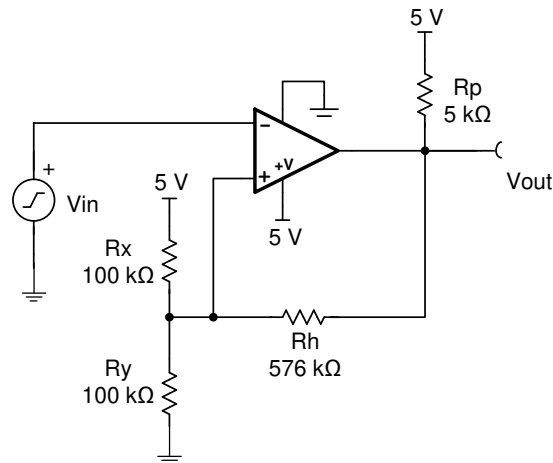


图 7-1. Comparator Schematic With Hysteresis

7.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5V
- Input: 0V to 5V
- Lower threshold (V_L) = $2.3V \pm 0.1V$
- Upper threshold (V_H) = $2.7V \pm 0.1V$
- $V_H - V_L = 2.4V \pm 0.1V$
- Low-power consumption

7.2.2 Detailed Design Procedure

Make a small change to the comparator circuit to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (VH) to transition low, or below the lower threshold (VL) to transition high.

图 7-1 illustrates hysteresis on a comparator. Resistor Rh sets the hysteresis level. An open-collector output stage requires a pullup resistor (Rp). The pullup resistor creates a voltage divider at the comparator output that introduces an error when the output is at logic high. This error can be minimized if $R_h > 100 R_p$.

When the output is at a logic high (5V), Rh is in parallel with Rx (ignoring Rp). This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7V. The input signal must drive above VH = 2.7V to cause the output to transition to logic low (0V).

When the output is at logic low (0V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3V. The input signal must drive below VL = 2.3V to cause the output to transition to logic high (5V).

For more details on this design and other alternative devices that can be used in place of the TLV1702, refer to Precision Design [TIPD144](#), *Comparator with Hysteresis Reference Design*.

7.2.3 Application Curve

图 7-2 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76V and the lower threshold is 2.34V, both of which are close to the design target.

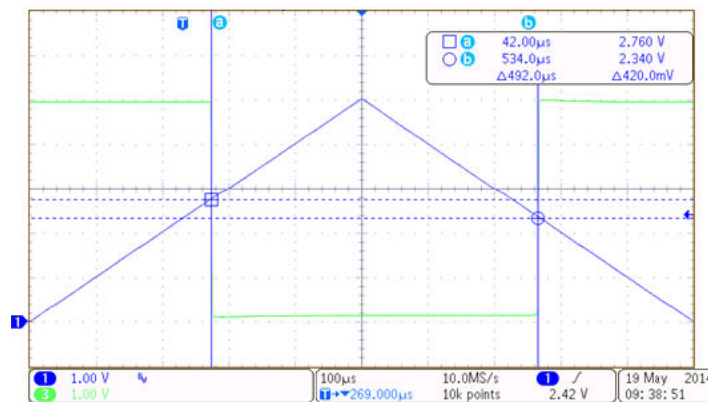


图 7-2. TLV1701 Upper and Lower Threshold With Hysteresis

7.3 Power Supply Recommendations

The TLV1704-SEP device is specified for operation from 2.2V to 24V; many specifications apply from -55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [节 5.7](#) section.

小心

Supply voltages larger than 40V can permanently damage the device; see the [节 5.1](#).

Place 0.1 μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the [节 7.4.1](#) section.

7.4 Layout

7.4.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV1704-SEP device.
- To minimize supply noise, place a decoupling capacitor (0.1 μ F ceramic, surface-mount capacitor) as close as possible to V_S as shown in 图 7-3.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

7.4.2 Layout Example

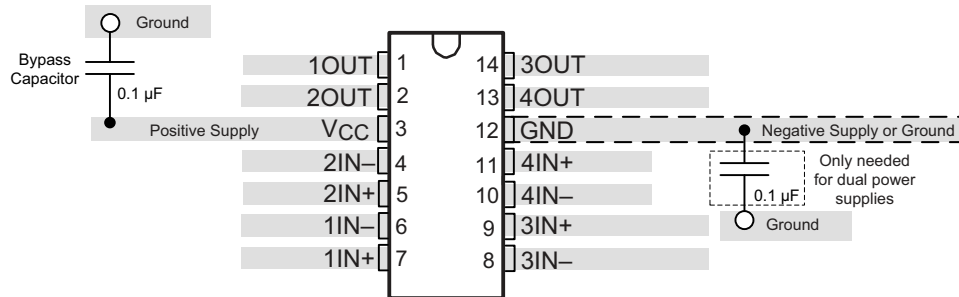


图 7-3. Comparator Board Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- [Precision Design, Comparator with Hysteresis Reference Design](#), TIDU020
- [REF33xx 3.9- \$\mu\$ A, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/ \$^{\circ}\$ C Drift Voltage Reference](#), SBOS392

8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (November 2022) to Revision B (July 2024)	Page
• 将最大电源电压从 36V 更改成了 24V.....	1
• 将 器件信息 表中的器件等级从 20krad (Si) RLAT 更改为 30krad (Si) RLAT.....	1
• 更新了整个文档中测量值的格式.....	1
• Updated the <i>Typical Performance Characteristics</i> graphs.....	6

Changes from Revision * (November 2018) to Revision A (November 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 将标题从“抗辐射”更新为“耐辐射”.....	1
• 使用链接更新了“应用”部分.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1704AMPWPSEP	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP
TLV1704AMPWTPSEP	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP
V62/18613-01XE	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP
V62/18613-01XE-T	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV1704-SEP :

- Automotive : [TLV1704-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

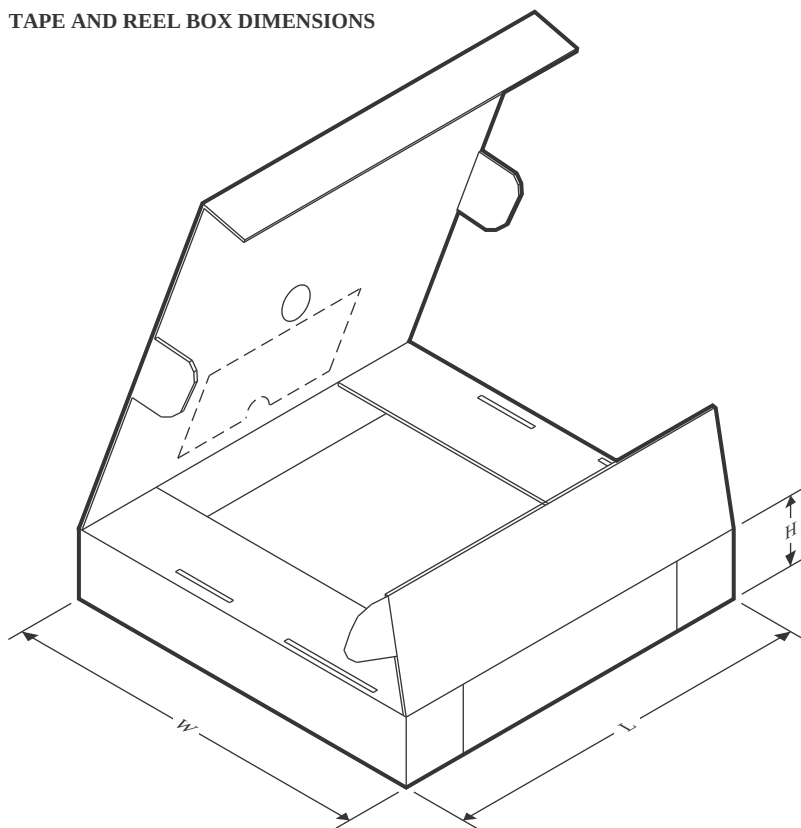
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1704AMPWTPSEP	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1704AMPWTPSEP	TSSOP	PW	14	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

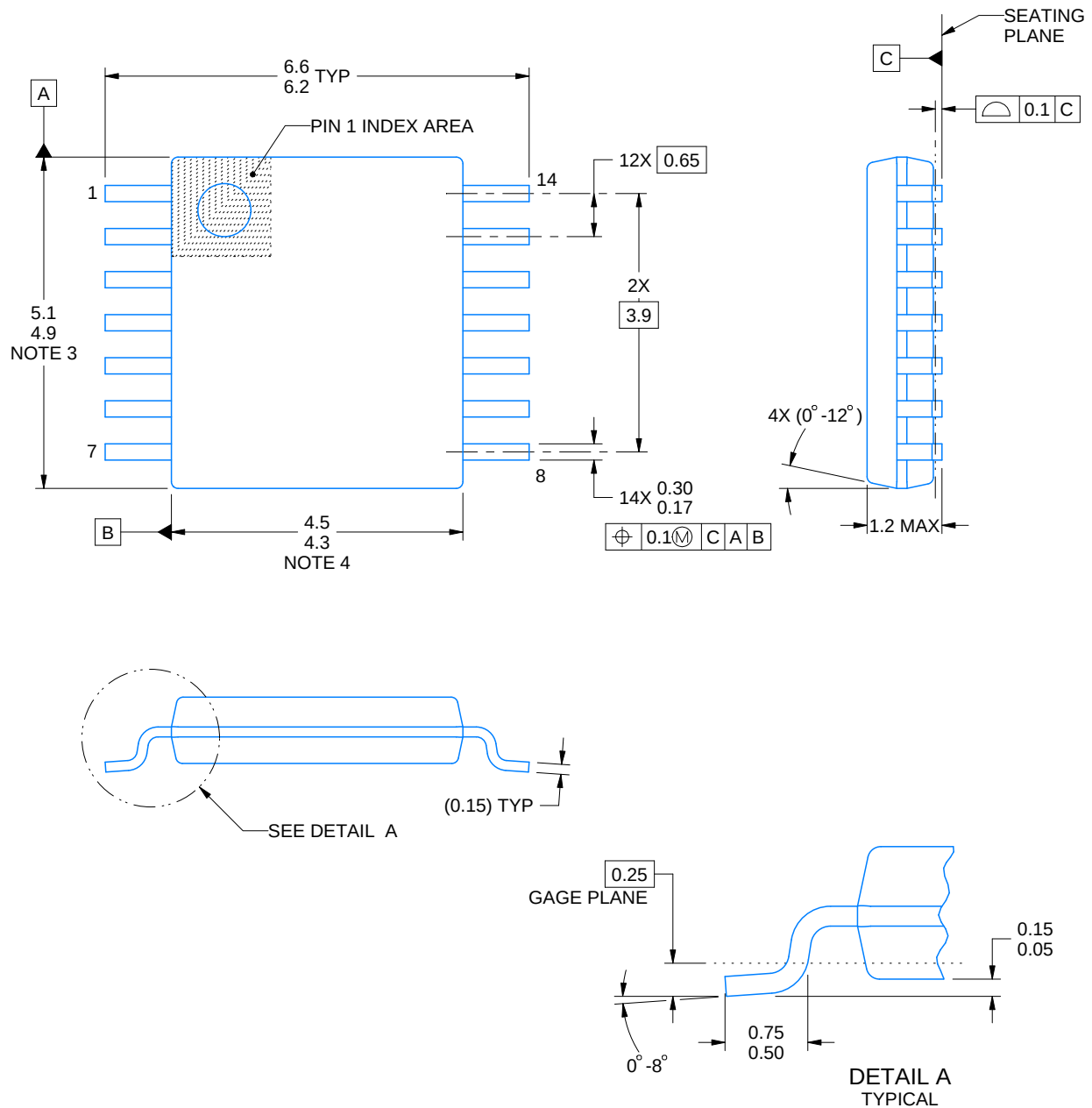
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV1704AMPWPSEP	PW	TSSOP	14	90	530	10.2	3600	3.5
V62/18613-01XE-T	PW	TSSOP	14	90	530	10.2	3600	3.5

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

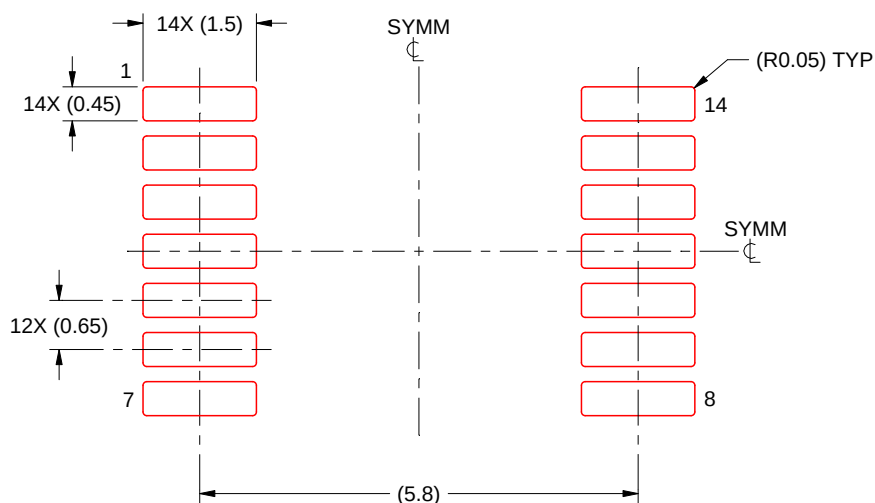
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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