TEXAS INSTRUMENTS
TLIN2024A-Q1
ZHCSNE4 – JUNE 2022

TLIN2024A-Q1 具有显性状态超时的四路本地互连网络 (LIN) 收发器

1 特性

- 符合面向汽车应用的 AEC-Q100（1 级）标准
- 符合 LIN 2.0、LIN 2.1、LIN 2.2、LIN2.2A 和 ISO/DIS 17987 – 4 电气物理层 (EPL) 规格标准
- 符合 SAE J2602-1 面向汽车应用的 LIN 网络标准
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 支持 12V 和 24V 电池应用
- LIN 传输数据速率高达 20kbps
- LIN 接收数据速率高达 100kbps
- 宽工作电源电压范围：4 V 至 48 V
- 睡眠模式：超低电流消耗支持以下类型的唤醒事件：
  - LIN 总线
  - 通过 EN 引脚实现本地唤醒
- 集成 45kΩ LIN 上拉电阻器
- 在 LIN 总线和 RXD 输出上实现上电和断电无干扰运行
- 保护特性：
  - ±60V LIN 总线容错
  - V_{SUP} 欠压保护
  - TXD 显性超时 (DTO) 保护
  - 热关断保护
  - 系统级未供电节点或接地断开失效防护。
- 3.5mm × 5.5mm VQFN 封装，提高了自动光学检测 (AOI) 能力

2 应用

- 车身电子装置和照明
- 混合动力电动汽车和动力总成系统
- 信息娱乐系统与仪表组
- 电器

3 说明

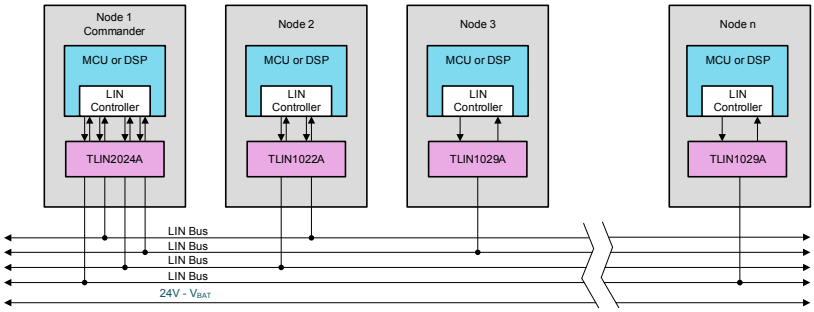
TLIN2024A-Q1 器件是一款四路本地互连网络 (LIN) 物理层收发器，集成了唤醒和保护功能，符合 LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2A 和 ISO/DIS 17987 – 4 标准。LIN 是一根单线制双向总线，通常用于低速车载网络，数据传输速率高达 20kbps。TLIN2024A-Q1 旨在为 12V 和 24V 应用提供支持，具有更宽的工作电压范围和额外的总线故障保护。该器件具有两个独立的双路 LIN 收发器模块。$V_{SUP1/2}$ 可控制独立的双路收发器模块。

TLIN2024A-Q1 接收器支持高达 100kbps 的数据速率，从而更快速地执行内联编程。该器件通过使用可降低电磁发射 (EME) 的限流波形整形驱动器，将 TXD 输入上的 LIN 协议数据流转化为 LIN 总线信号。接收器将数据流转化为逻辑电平信号，此信号通过开漏 RXD 引脚发送到微处理器。睡眠模式可实现超低电流消耗，该模式允许通过 LIN 总线或 EN 引脚实现唤醒。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TLIN2024A-Q1	VQFN (24)	3.50mm × 5.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
June 2022	*	Initial release

5 说明（续）

TLIN2024A-Q1 集成了适用于 LIN 响应者节点应用的电阻器，还集成了 ESD 保护和故障保护功能，有助于减少应用中的外部元件数量。一旦发生接地漂移或电源电压断开，该器件可防止反馈电流经 LIN 流向电源输入。器件还包含欠压保护、过热关断保护和接地失效保护功能。

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6 Pin Configuration and Functions

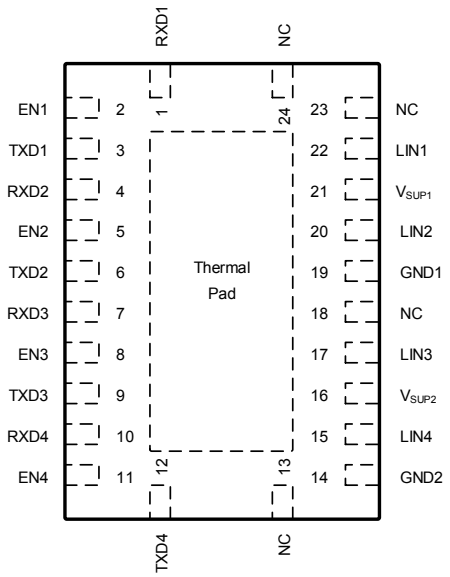


图 6-1. RGY Package, 24-Pin RGY (VQFN)
(Top View)

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
RXD1	1	O	Channel 1 RXD Output (open-drain) interface reporting state of LIN1 bus voltage
EN1	2	I	Channel 1 Enable Input
TXD1	3	I	Channel 1 TXD input interface to control state of LIN output
RXD2	4	O	Channel 2 RXD Output (open-drain) interface reporting state of LIN2 bus voltage
EN2	5	I	Channel 2 Enable Input
TXD2	6	I	Channel 2 TXD input interface to control state of LIN2 output
RXD3	7	O	Channel 3 RXD Output (open-drain) interface reporting state of LIN3 bus voltage
EN3	8	I	Channel 3 Enable Input
TXD3	9	I	Channel 3 TXD input interface to control state of LIN3 output
RXD4	10	O	Channel 4 RXD Output (open-drain) interface reporting state of LIN4 bus voltage
EN4	11	I	Channel 4 Enable Input
TXD4	12	I	Channel 4 TXD input interface to control state of LIN4 output
GND2	14	G	Ground pin for Channels 3 and 4
LIN4	15	I/O	Channel 4 LIN Bus single-wire transmitter and receiver
V_{SUP2}	16	Supply	Channels 3 and 4 Supply Voltage (connected to battery in series with external reverse blocking diode)
LIN3	17	I/O	Channel 3 LIN Bus single-wire transmitter and receiver
GND1	19	G	Ground pin for Channels 1 and 2
LIN2	20	I/O	Channel 2 LIN Bus single-wire transmitter and receiver
V_{SUP1}	21	Supply	Channels 1 and 2 Supply Voltage (connected to battery in series with external reverse blocking diode)
LIN1	22	I/O	Channel 1 LIN Bus single-wire transmitter and receiver
NC	13, 18, 23, 24	–	Not Connected
Thermal Pad		–	Can be connected to the PCB ground plane to improve thermal coupling

(1) I = Input, O = Output, I/O = Input or Output, G = Ground.

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7 Specifications

7.1 Absolute Maximum Ratings

(1) (2)

Symbol	Parameter	MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO/DIS 17987 Param 10)	–0.3	60	V
V_{LIN}	LIN bus input voltage (ISO/DIS 17987 Param 82)	–60	60	V
V_{LOGIC}	Logic pin voltage (RXD, TXD, EN)	–0.3	6	V
I_O	Logic pin output current		8	mA
T_J	Junction temperature range	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to ground terminal.

7.2 ESD Ratings

ESD Ratings				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) classification level 3A: TXD, RXD, EN Pins, per AEC Q100-002(1)		±4000	V
		Human body model (HBM) classification level 3B: LIN and V_{SUP} Pin with respect to ground		±8000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD Ratings - IEC

ESD and Surge Protection Ratings			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge, LIN, V_{SUP} to GND(1)	IEC 62228-2 per ISO 10605 Contact discharge R = 330 Ω, C = 150 pF	±8000	V

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7.3 ESD Ratings - IEC (continued)

ESD and Surge Protection Ratings			VALUE	UNIT
V_{TRAN}	ISO 7637-2 and IEC 62228-2 per IEC 62215-3 transients according to IBEE LIN EMC test specifications (2) (V_{SUP} to GND)	IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 1	– 100	V
		IEC 62215-3 24 V electrical systems (2) Pulse 1	– 450	
		IEC 62228-2 per IEC 62215-3 12 V electrical systems 24 V electrical systems (2) Pulse 2	75	
		IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 3a	– 150	
		IEC 62215-3 24 V electrical systems (2) Pulse 3a	-225	
		IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 3b	100	
		IEC 62215-3 24 V electrical systems (2) Pulse 3b	225	

(1) Results given here are specific to the IEC 62228-2 Integrated circuits – EMC evaluation of transceivers – Part 2: LIN transceivers. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
(2) Verified during characterization.

7.4 Thermal Information

THERMAL METRIC(1)		TLIN2024A RGY (QFN) 24-PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	34.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	30.8	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	13.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.3	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Recommended Operating Conditions

parameters valid across -40℃ ⩽ T_A ⩽ 125℃ (unless otherwise noted)

PARAMETER - DEFINITION		MIN	NOM	MAX	UNIT
$V_{SUP1/2}$	Supply voltage	4		48	V
V_{LINx}	LIN Bus input voltage	0		48	V
V_{LOGIC}	Logic Pin Voltage (RXDx, TXDx, ENx)	0		5.25	V
T_A	Ambient temperature range	-40		125	°C
TSD	Thermal shutdown rising threshold	165			°C
$TSD_{(HYS)}$	Thermal shutdown hysteresis		15		°C

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7.6 Electrical Characteristics

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
$V_{SUP1/2}$	Operational supply voltage (ISO/DIS 17987 Param 10)	Device is operational beyond the LIN defined nominal supply voltage range; See Figure 8-1 and Figure 8-2	4		48	V
$V_{SUP1/2}$	Nominal supply voltage (ISO/DIS 17987 Param 10)	Normal and Standby Modes: ramp V_{SUP} while LIN signal is a 10 kHz square wave with 50 % duty cycle and 36V swing; See Figure 8-1 and Figure 8-2	4		48	V
		Sleep Mode	4		48	V
UV_{SUP}	Under voltage V_{SUP} threshold		2.9		3.85	V
UV_{HYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.2		V
I_{SUP}	Supply current (6)	Normal Mode: EN = High, bus dominant: total bus load where R_{LIN} > 500 Ω and C_{LIN} < 10 nF		1.2	8.5	mA
		Standby Mode: EN = Low, bus dominant: total bus load where R_{LIN} > 500 Ω and C_{LIN} < 10 nF		1.1	3.75	mA
I_{SUP}	Supply current (6)	Normal Mode: EN = High, Bus Recessive: LIN = V_{SUP}		670	1600	µA
		Standby Mode: EN = Low, Bus Recessive LIN = V_{SUP}		20	40	µA
		Sleep Mode: 4.0 V < V_{SUP} < 14 V, LIN = V_{SUP}, EN = 0 V, TXD and RXD Floating		10	20	µA
		Sleep Mode: 14 V < V_{SUP} < 36 V, LIN = V_{SUP}, EN = 0 V, TXD and RXD floating			30	µA
RXDx OUTPUT PIN (OPEN DRAIN)						
V_{OL}	Output Low voltage	Based upon External pull up to V_{CC} (4)			0.6	V
I_{OL}	Low level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{ILG}	Leakage current, high-level	LIN = V_{SUP}, RXD = 5 V	–5	0	5	µA
TXDx INPUT PIN						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.25	V
V_{HYS}	Input threshold voltage, normal modes & selective wake modes			50	500	mV
I_{ILG}	Low level input leakage current	TXD = Low	–5	0	5	µA
R_{TXD}	Internal pull-down resistor value		125	350	800	kΩ
ENx INPUT PIN						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.25	V
V_{HYS}	Hysteresis voltage	By design and characterization		50	500	mV
I_{ILG}	Low level input current	EN = Low	–5	0	5	µA
R_{EN}	Internal Pulldown resistor		125	350	800	kΩ
LINx PIN						
V_{OH}	LIN recessive high-level output voltage (3)	TXD = high, I_O = 0 mA, 7 V ≤ V_{SUP} ≤ 48 V	0.85			V_{SUP}

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7.6 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	LIN recessive high-level output voltage (1) (2)	TXD = high, I_O = 0 mA, 7 V ≤ V_{SUP} ≤ 18 V	0.8			V_{SUP}
V_{OH}	LIN recessive high-level output voltage (3)	TXD = high, I_O = 0 mA, 4 V ≤ V_{SUP} < 7 V	3			V
V_{OL}	LIN dominant low-level output voltage (3)	TXD = low, 7 V ≤ V_{SUP} ≤ 48 V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage (1) (2)	TXD = low, 7 V ≤ V_{SUP} ≤ 18 V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage (3)	TXD = low, 4 V ≤ V_{SUP} < 7 V			1.2	V
$V_{SUP_NON_OP}$	V_{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	TXD & RXD open, LIN = 4 V to 58 V	-0.3		58	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 57)	TXD = 0 V, V_{LIN} = 48 V, R_{MEAS} = 440 Ω, V_{SUP} = 48 V, V_{BUSdom} < 4.518 V	75	120	300	mA
$I_{BUS_PAS_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	LIN = 0 V, V_{SUP} = 24 V Driver off/ recessive; See Figure 8-6	-2			mA
$I_{BUS_PAS_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	LIN > V_{SUP}, 8 V ≤ V_{SUP} ≤ 48 V, Driver off; See Figure 8-7			20	µA
$I_{BUS_PAS_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	LIN = V_{SUP}, Driver off; See Figure 8-7	-5		5	µA
$I_{BUS_NO_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 60)	GND = V_{SUP}, 0 V ≤ V_{LIN} < 36 V, V_{SUP} = 24 V; Figure 8-8	-2		2	mA
$I_{leak\ gnd(dom)}$	Leakage current, loss of ground (5)	V_{SUP} = 8 V, GND = open, V_{SUP} = 18 V, GND = open $R_{Commander}$ = 1 kΩ, C_L = 1 nF $R_{Responder}$ = 20 kΩ, C_L = 1 nF LIN = dominant	-1		1	mA
$I_{leak\ gnd(rec)}$	Leakage current, loss of ground (5)	V_{SUP} = 8 V, GND = open, V_{SUP} = 18 V, GND = open $R_{Commander}$ = 1 kΩ, C_L = 1 nF $R_{Responder}$ = 20 kΩ, C_L = 1 nF LIN = recessive	-100		100	µA
$I_{BUS_NO_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 61)	0 V ≤ V_{LIN} ≤ 48 V, V_{SUP} = GND; See; Figure 8-9			5	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 62) (3)	LIN dominant (including LIN dominant for wake-up); See Figure 8-4 and Figure 8-3			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 63) (3)	LIN recessive; See Figure 8-4 and Figure 8-3	0.6			V_{SUP}
V_{IH}	LIN recessive high-level input voltage (1) (2)	7 V ≤ V_{SUP} ≤ 18 V	0.47		0.6	V_{SUP}
V_{IL}	LIN dominant low-level input voltage (1) (2)	7 V ≤ V_{SUP} ≤ 18 V	0.4		0.53	V_{SUP}
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 64)	V_{BUS_CNT} = (V_{BUSdom} + V_{BUSrec})/2 See Figure 8-4 and Figure 8-3	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 65)	V_{HYS} = (V_{BUSrec} - V_{BUSdom}) See Figure 8-4 and Figure 8-3			0.175	V_{SUP}
V_{HYS}	Hysteresis voltage (SAE J2602)	V_{HYS} = V_{IH} - V_{IL} See Figure 8-4 and Figure 8-3	0.07		0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN termination pullup path	I_{SERIAL_DIODE} = 10 µA	0.4	0.7	1	V
R_{PU}	Pullup resistor to V_{SUP} (ISO/DIS 17987 Param 26)	Normal and Standby modes	20	45	60	kΩ
I_{RSLEEP}	Pullup current source to V_{SUP}	Sleep mode, V_{SUP} = 27 V, LIN = GND	-20		-2	µA

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7.6 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{LINPIN}	Capacitance of the LIN pin	V_{SUP} = 14 V			25	pF

(1) SAE 2602 commander node load conditions: 5.5 nF/4 kΩ and 899 pF/20 kΩ
(2) SAE 2602 responder node load conditions: 5.5 nF/875 Ω and 899 pF/900 Ω
(3) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1 nF/1 kΩ; 6.8 nF/660 Ω; 10 nF/500 Ω.
(4) RXD uses open drain output structure therefore V_{OL} level is based upon microcontroller supply voltage V_{CC}.
(5) $I_{leak\ gnd}$ = (V_{BAT} - V_{LIN})/R_{Load}
(6) Values are for each V_{SUP} pin

7.7 Duty Cycle Characteristics

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D1_{12V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27)(3)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP} $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.396			
$D1_{12V}$	Duty Cycle 1 (3) (4)	$TH_{REC(MAX)}$ = 0.625 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.396			
D1	Duty Cycle 1 (1) (2) (4)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 52 µs D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.396			
$D2_{12V}$	Duty Cycle 2 (ISO/DIS 17987 Param 28) (3)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.581	
$D2_{12V}$	Duty Cycle 2 (3) (4)	$TH_{REC(MIN)}$ = 0.546 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.4 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.581	
D2	Duty Cycle 2 (1) (2) (4)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 52 µs D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.581	
$D3_{12V}$	Duty Cycle 3 (ISO/DIS 17987 Param 29) (3)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.417			
$D3_{12V}$	Duty Cycle 3 (3) (4)	$TH_{REC(MAX)}$ = 0.645 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.417			
D3	Duty Cycle 3 (1) (2) (4)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.417			
$D4_{12V}$	Duty Cycle 4 (ISO/DIS 17987 Param 30) (3)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.59	

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7.7 Duty Cycle Characteristics (continued)

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D4_{12V}$	Duty Cycle 4 (3) (4)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.59	
D4	Duty Cycle 4 (1) (2) (4)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.59	
$D1_{24V}$	Duty Cycle 1 (ISO/DIS 17987 Param 72)	$TH_{REC(MAX)}$ = 0.710 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.544 x V_{SUP}, V_{SUP} = 15 V to 36 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.33			
$D2_{24V}$	Duty Cycle 2 (ISO/DIS 17987 Param 73)	$TH_{REC(MIN)}$ = 0.446 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.302 x V_{SUP}, V_{SUP} = 15.6 V to 36 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.642	
$D3_{24V}$	Duty Cycle 3 (ISO/DIS 17987 Param 74)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 36 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.386			
$D4_{24V}$	Duty Cycle 4 (ISO/DIS 17987 Param 75) (4)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7.6 V to 36 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.591	
$D1_{LB}$	Duty cycle 1 at low battery (1) (2) (4)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 52 µs	0.396			
$D2_{LB}$	Duty cycle 2 at low battery(1) (2) (4)	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1 V to 7 V, t_{BIT} = 52 µs			0.581	
$D3_{LB}$	Duty cycle 3 at low battery (1) (2) (4)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 96 µs	0.396			
$D4_{LB}$	Duty cycle 4 at low battery (1) (2) (4)	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1 V to 7 V, t_{BIT} = 96 µs			0.581	
Tr-d max	Transmitter propagation delay timings for the duty cycle (1) (2) (4) Recessive to dominant	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 52 µs $t_{REC(MAX)_D1}$ - $t_{DOM(MIN)_D1}$			10.8	µs
Td-r max	Transmitter propagation delay timings for the duty cycle (1) (2) (4) Dominant to recessive	$TH_{REC(MAX)}$ = 0.422 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.284 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 52 µs $t_{DOM(MAX)_D2}$ - $t_{REC(MIN)_D2}$			8.4	µs
Tr-d max	Transmitter propagation delay timings for the duty cycle (1) (2) (4) Recessive to dominant	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 96 µs $t_{REC(MAX)_D3}$ - $t_{DOM(MIN)_D3}$			15.9	µs
Td-r max	Transmitter propagation delay timings for the duty cycle (1) (2) (4) Dominant to recessive	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 96 µs $t_{DOM(MAX)_D4}$ - $t_{REC(MIN)_D4}$			17.28	µs

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7.7 Duty Cycle Characteristics (continued)

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Tr-d max_low	Low battery transmitter propagation delay timings for the duty cycle (1) (2) (4) Recessive to dominant	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} 5.5 V ≤ V_{SUP} ≤ 7 V, t_{BIT} = 52 µs $t_{REC(MAX)_low}$ - $t_{DOM(MIN)_low}$			10.8	µs
Td-r max_low	Low battery transmitter propagation delay timings for the duty cycle (1) (2) (4) Dominant to recessive	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} 6.1 V ≤ V_{SUP} ≤ 7 V, t_{BIT} = 52 µs $t_{DOM(MAX)_low}$ - $t_{REC(MIN)_low}$			8.4	µs

(1) SAE 2602 commander node load conditions: 5.5 nF/4 kΩ and 899 pF/20 kΩ
(2) SAE 2602 responder node load conditions: 5.5 nF/875 Ω and 899 pF/900 Ω
(3) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1 nF/1 kΩ; 6.8 nF/660 Ω; 10 nF/500 Ω.
(4) Specified by design

7.8 Switching Characteristics

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{rx_pdr}	Receiver rising propagation delay time (ISO/DIS 17987 Param 31)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF; (See Figure 8-12 and Figure 8-13)			6	µs
t_{rx_pdf}	Receiver falling propagation delay time (ISO/DIS 17987 Param 31)				6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time	Rising edge with respect to falling edge, (trx_sym = trx_pdf – trx_pdr), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF; (See Figure 8-12 and Figure 8-13)	–2		2	µs
t_{LINBUS}	LIN wake-up time (Minimum dominant time on LIN bus for wake-up)	See Figure 8-16, 图 9-2, and 图 9-3	25	100	150	µs
t_{CLEAR}	Time to clear false wake-up prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See 图 9-3	8	17	50	µs
t_{DST}	Dominant state time out		20	34	80	ms
t_{MODE_CHANGE}	Mode change delay time	Time to change from standby mode to normal mode or normal mode to sleep mode through EN pin; See Figure 8-14 and 图 9-4	2		15	µs
t_{NOMINT}	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid; See Figure 8-14			35	µs
t_{PWR}	Power up time	Upon power up time it takes for valid data on RXD			1.5	ms

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8 Parameter Measurement Information

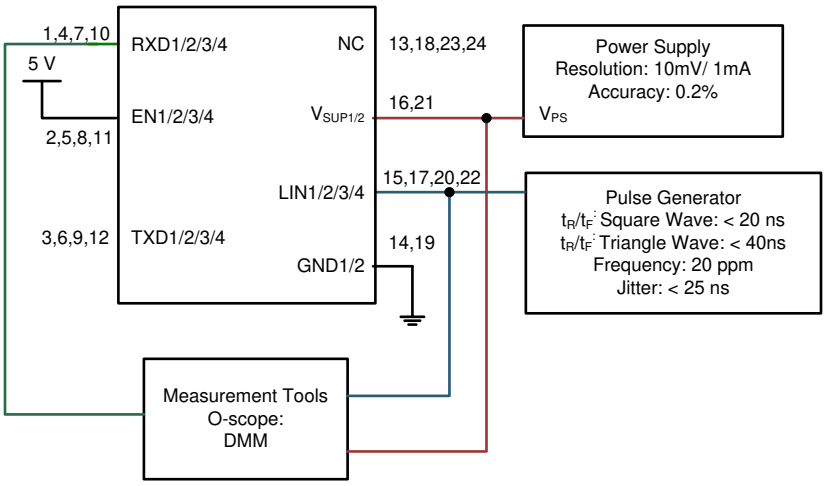


图 8-1. Test System: Operating Voltage Range with RX and TX Access

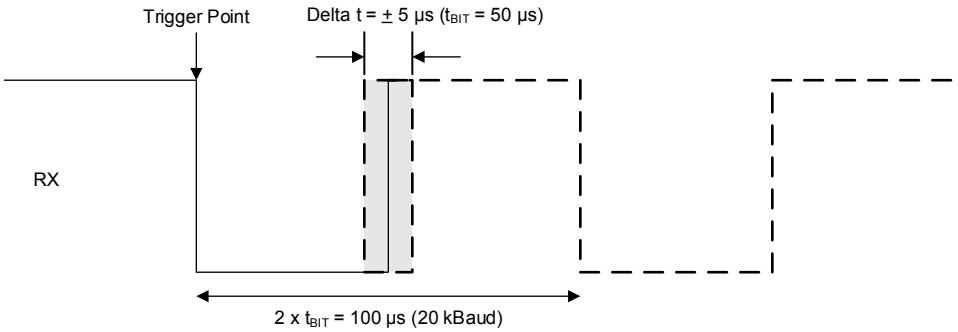


图 8-2. RX Response: Operating Voltage Range

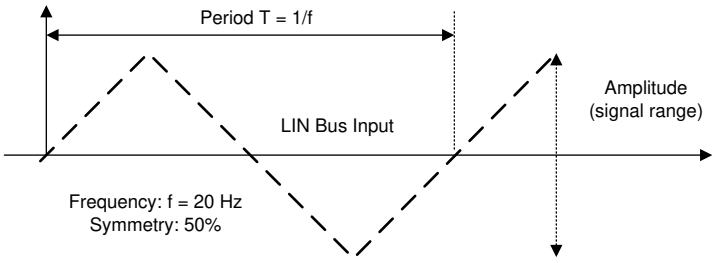


图 8-3. LIN Bus Input Signal

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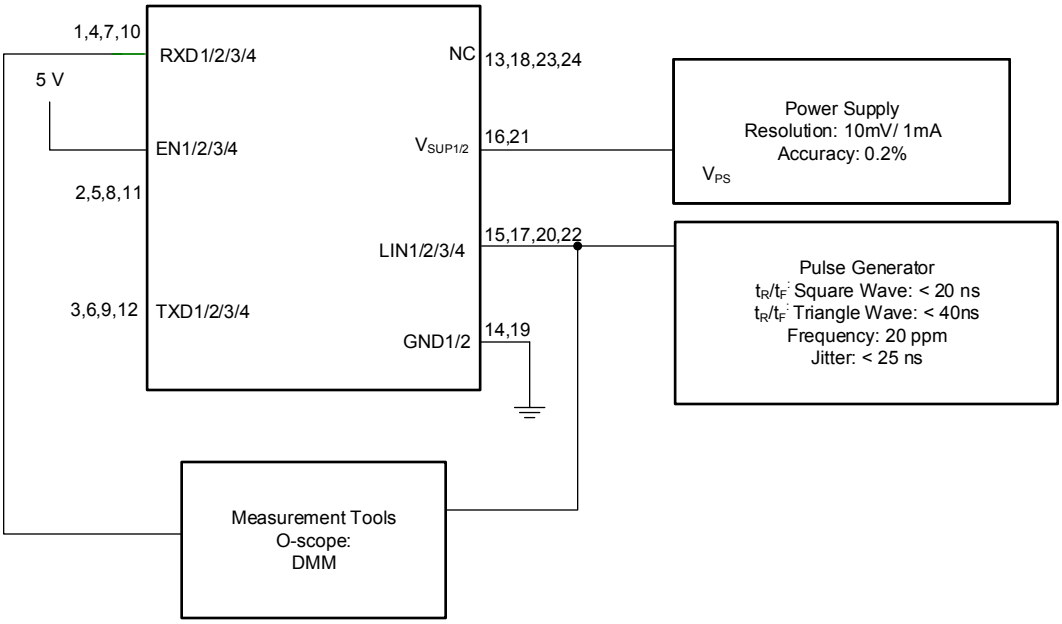


图 8-4. LIN Receiver Test with RX Access

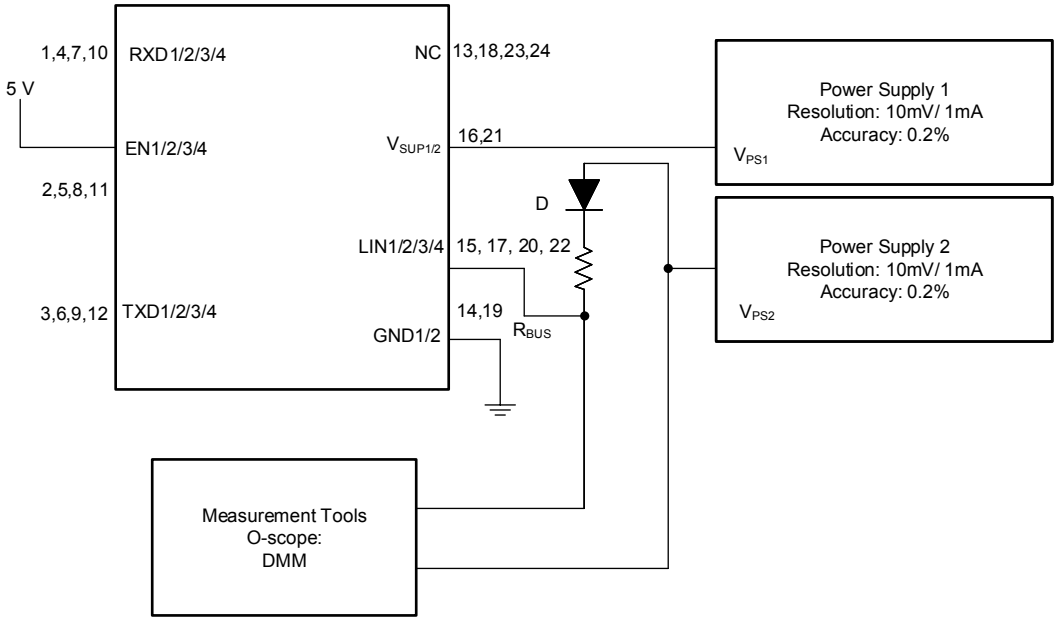


图 8-5. $V_{SUP_NON_OP}$

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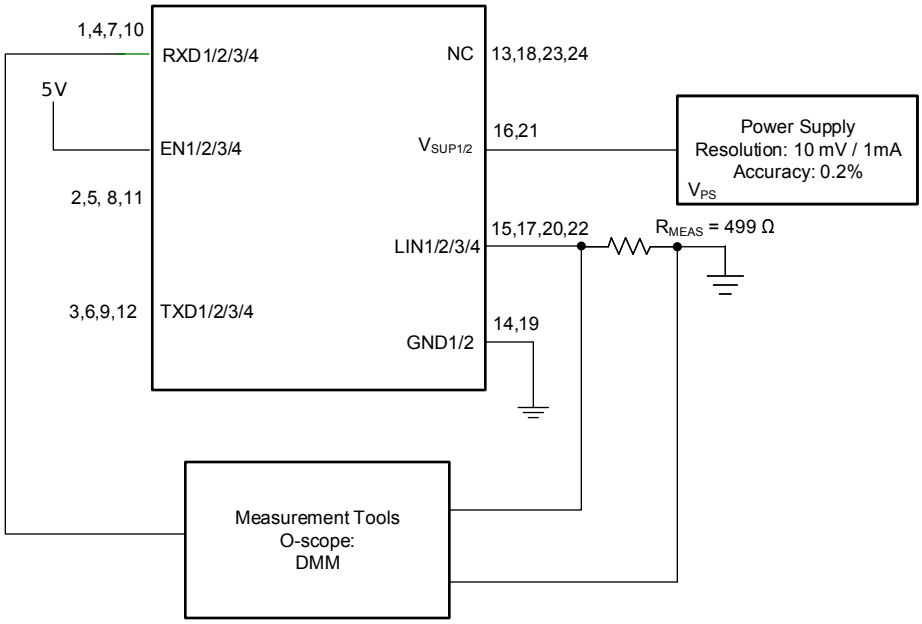


图 8-6. Test Circuit for $I_{BUS_PAS_dom}$; TXD = Recessive State V_{BUS} = 0 V

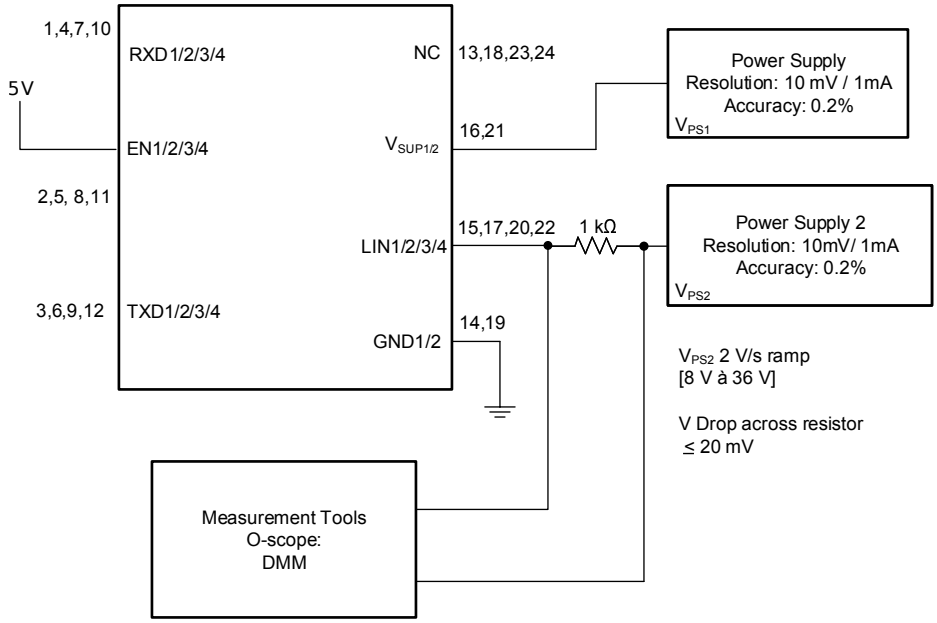


图 8-7. Test Circuit for $I_{BUS_PAS_rec}$

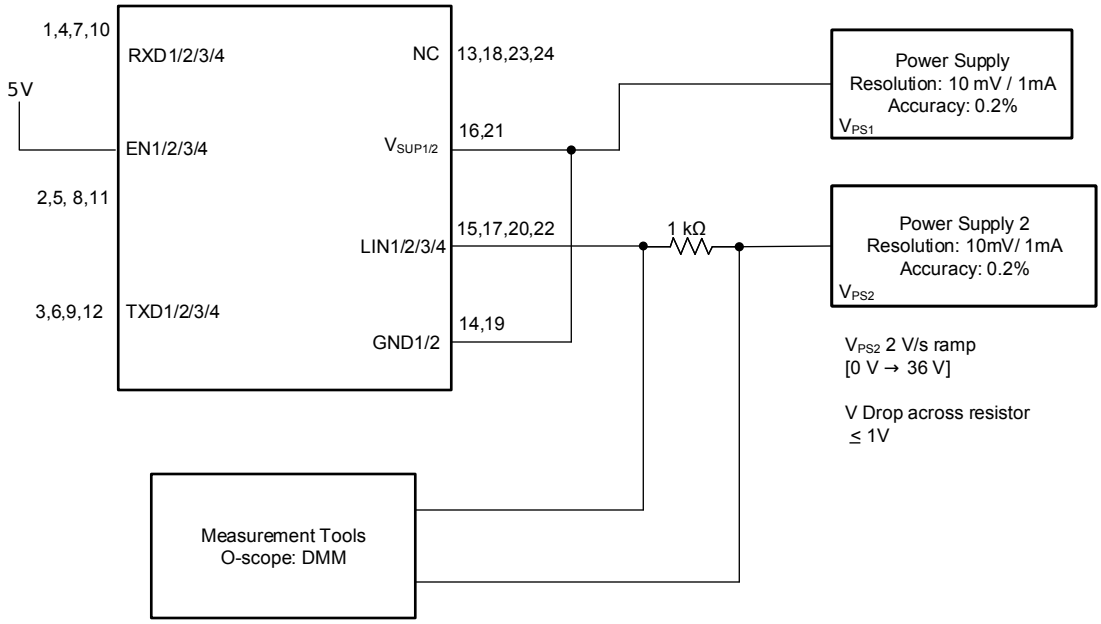


图 8-8. Test Circuit for $I_{BUS_NO_GND}$ Loss of GND

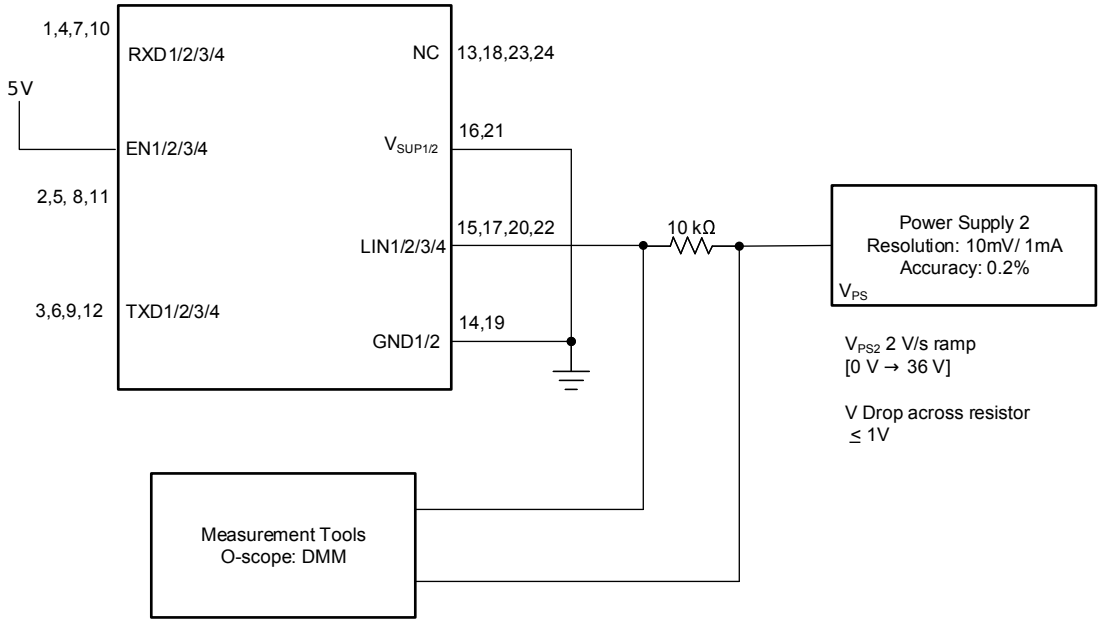


图 8-9. Test Circuit for $I_{BUS_NO_BAT}$ Loss of Battery

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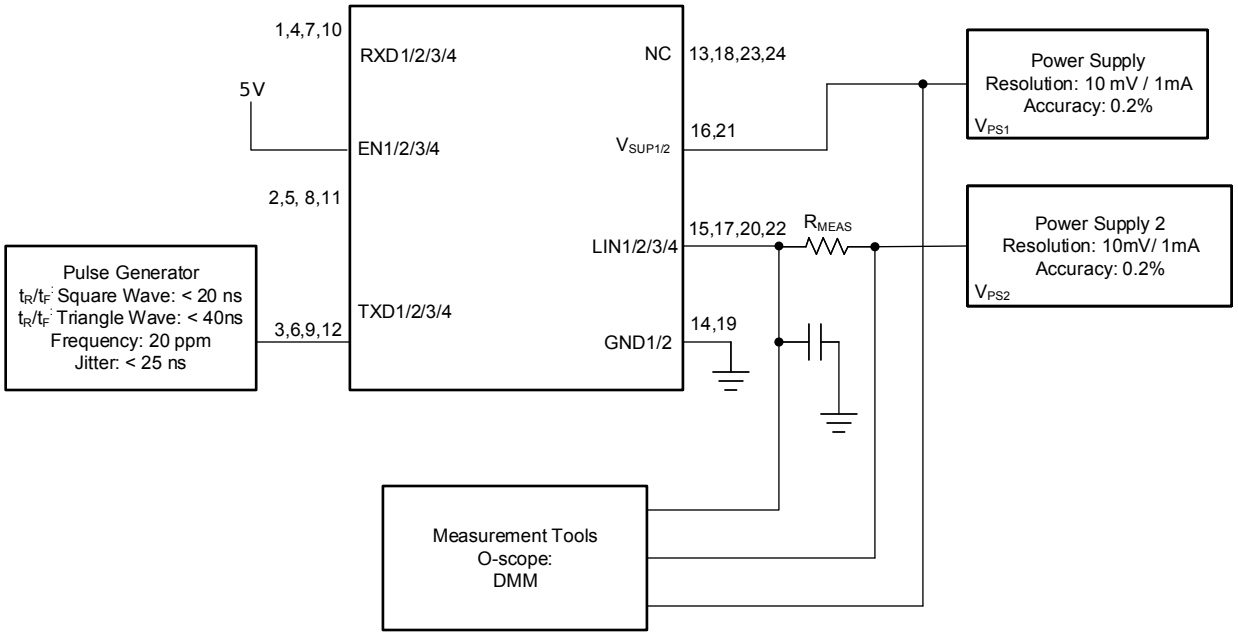


图 8-10. Test Circuit Slope Control and Duty Cycle

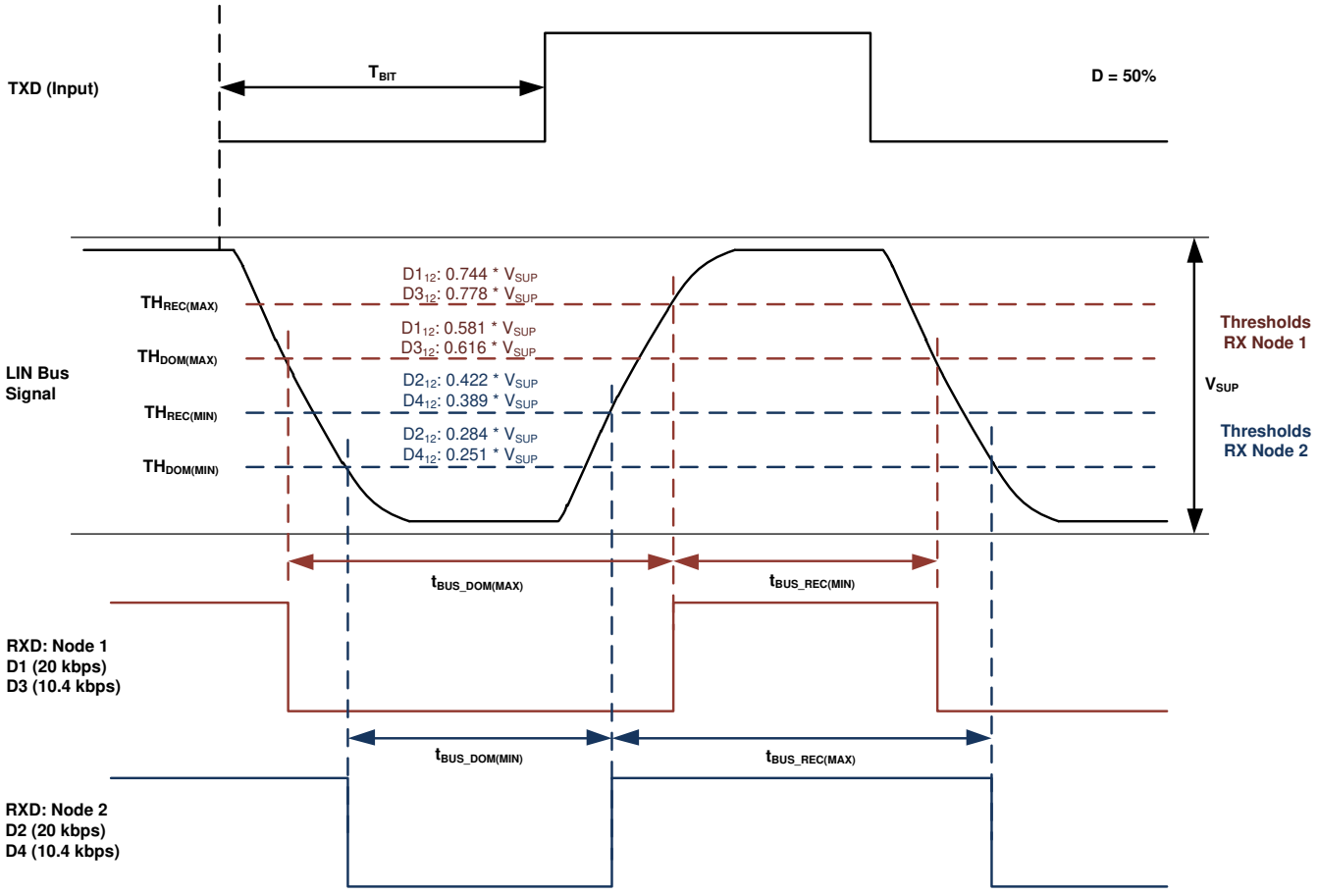


图 8-11. Definition of Bus Timing Parameters

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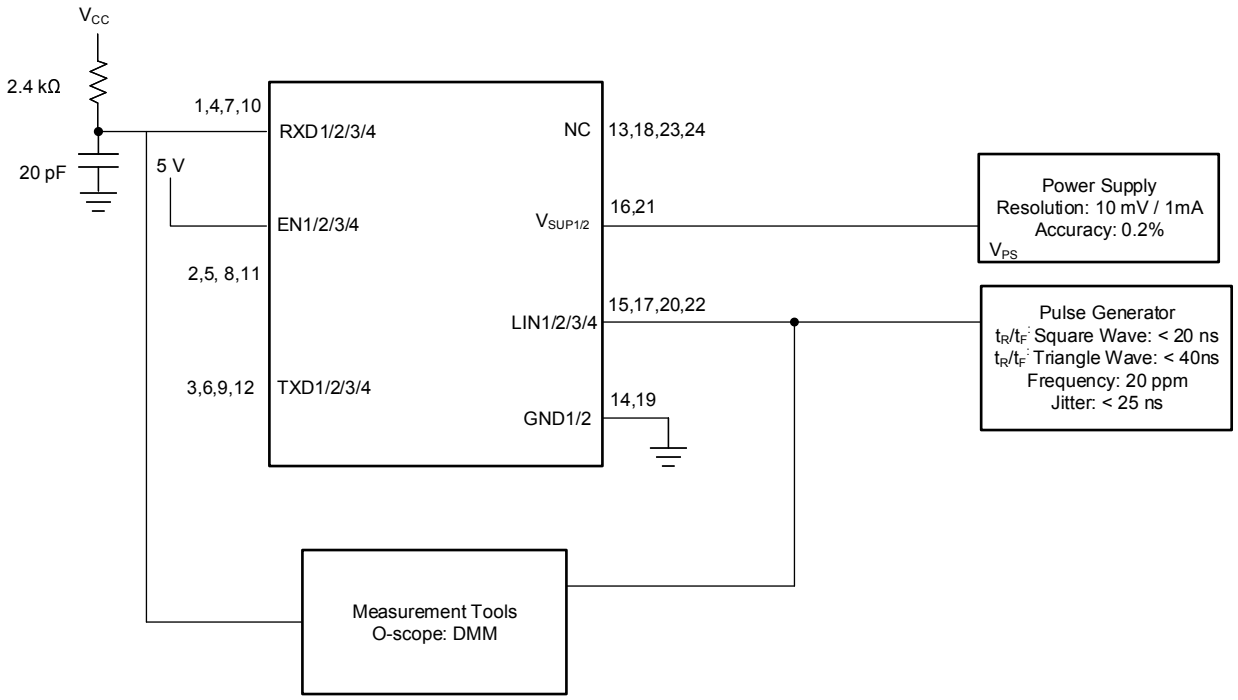


图 8-12. Propagation Delay Test Circuit

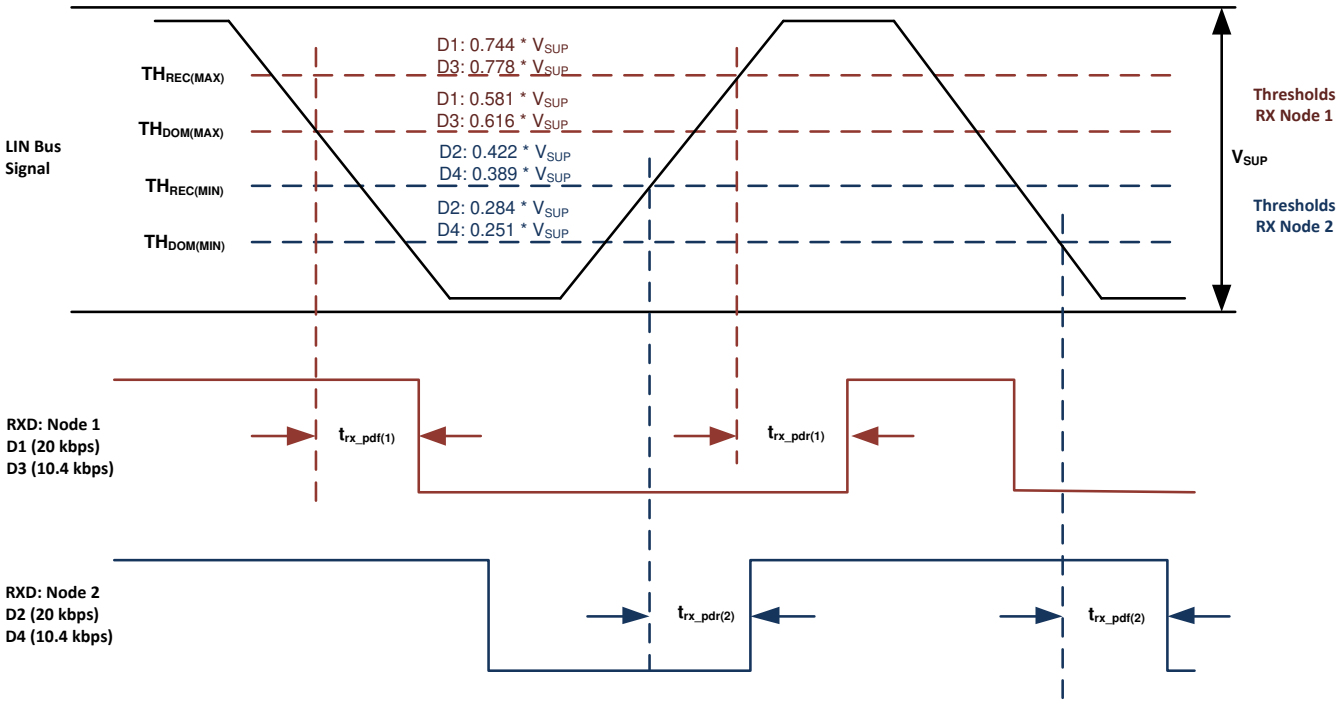


图 8-13. Propagation Delay

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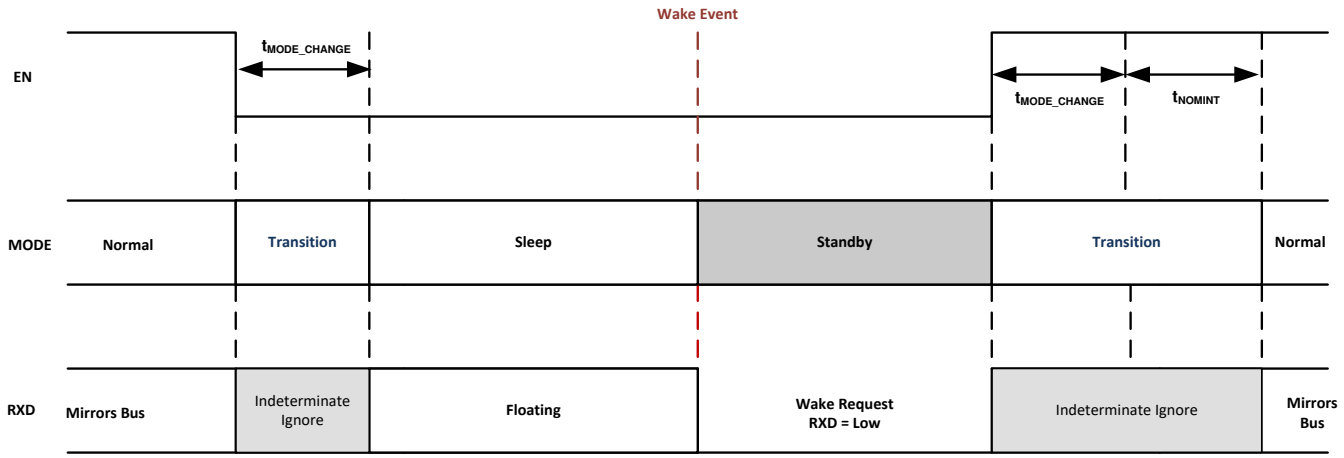


图 8-14. Mode Transitions

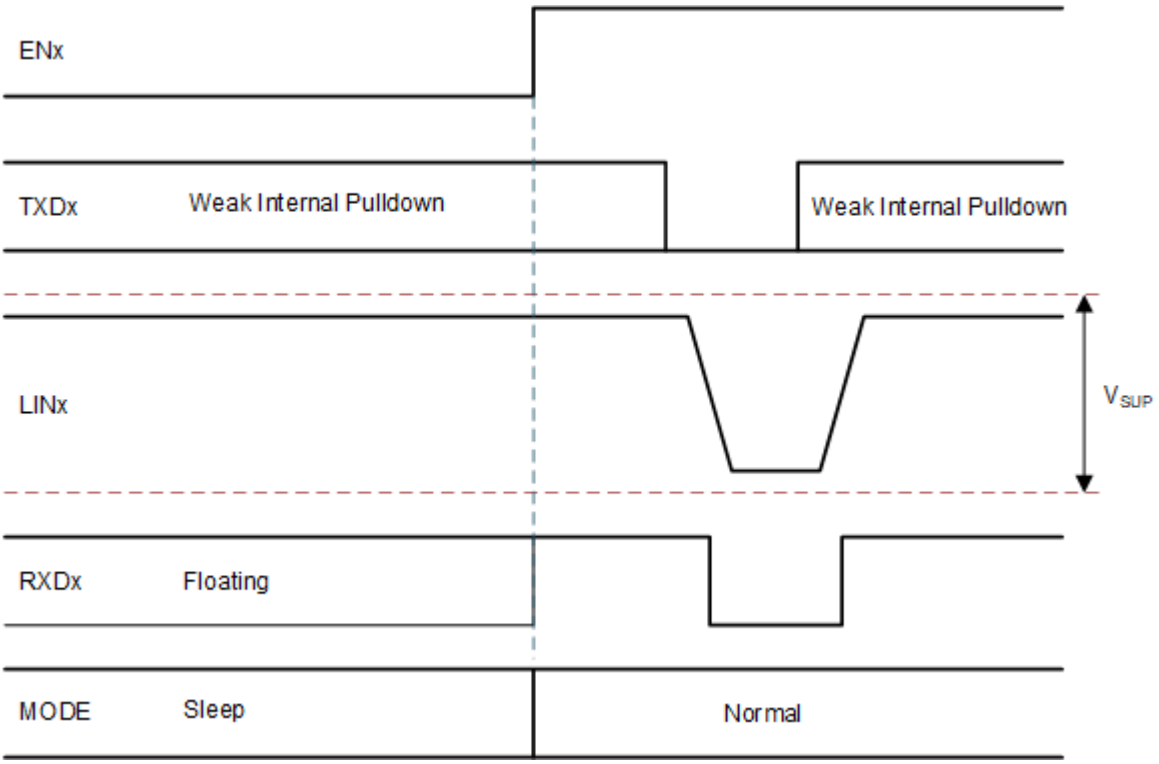


图 8-15. Wake-Up Through EN

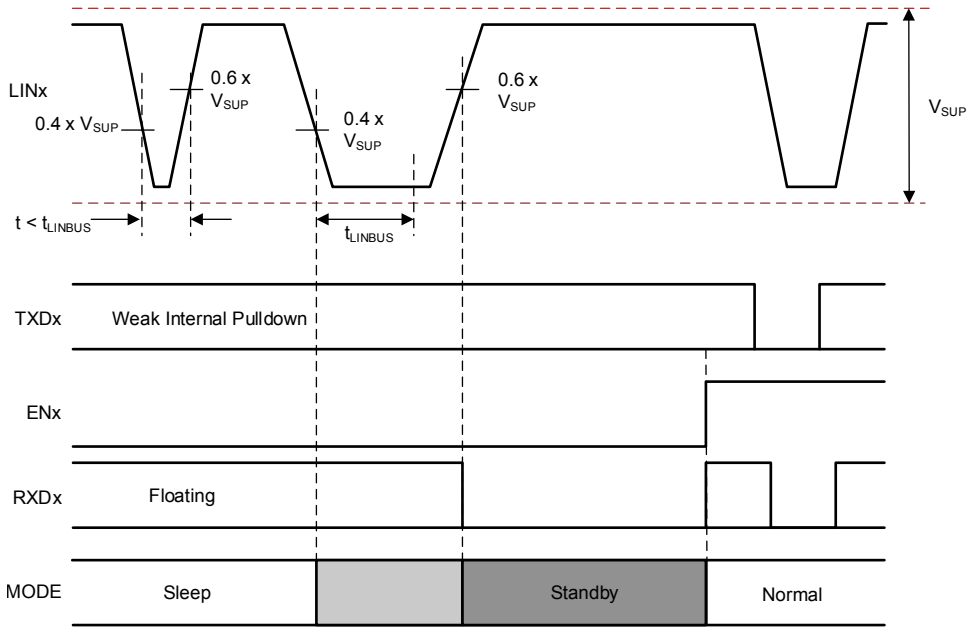


图 8-16. Wake-Up Through LIN

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9 Detailed Description

9.1 Overview

The TLIN2024A-Q1 device is a Quad Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987 – 4 standards, with integrated wake-up and protection features. The device has two separate dual LIN transceiver blocks. $V_{SUP1/2}$ provides power to the separate dual transceiver blocks. The LIN bus is a single wire bidirectional bus typically used for low speed in-vehicle networks using data rates up to 20 kbps. The device's LIN receivers work up to 100 kbps supporting in-line programming. The LIN protocol output data stream on the TXD in converted by the device into LIN bus signal using a current-limited wave shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for responder node applications. Commander node applications require an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification.

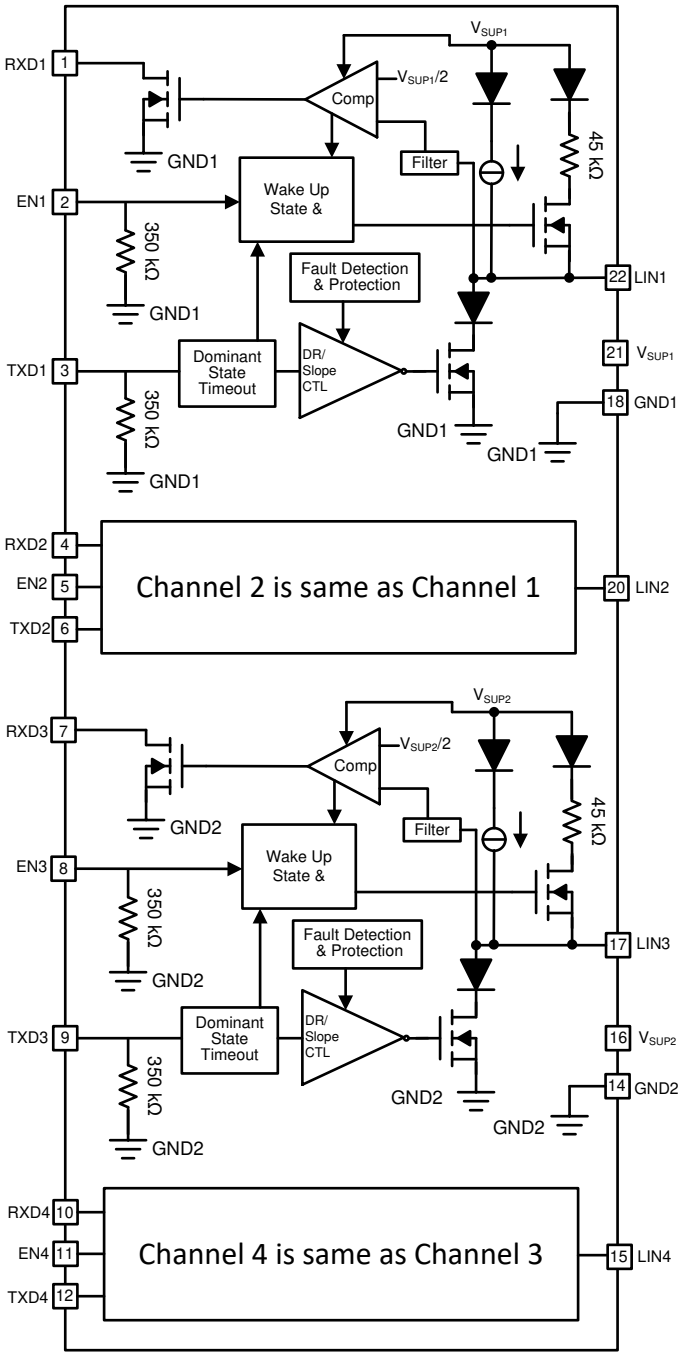
The device is designed to support 12-V and 24-V applications with a wide input voltage operating range and also supports low-power sleep mode. The device also provides two methods to wake-up: EN pin and from the LIN bus.

The TLIN2024A-Q1 integrates ESD protection and fault protection which allow for a reduction in the required external components in the applications. In the event of a ground shift or supply voltage disconnection, the device prevents back-feed current through LIN to the supply input. The device also includes undervoltage detection, temperature shutdown protection, and loss-of-ground protection.

V_{SUP1} and GND1 supplies transceivers 1 and 2 while V_{SUP2} and GND2 supplies transceiver 3 and 4. The device is part of the LIN family that includes the TLIN2022A and TLIN2029A LIN transceivers.

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9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 LIN (Local Interconnect Network) Bus

These high voltage input/output pins are single wire LIN bus transmitters and receivers. The LIN pins can survive excessive DC and transient voltages up to 60 V. Reverse currents from the LIN pins to supply ($V_{SUP1/2}$) are minimized with blocking diodes, even in the event of a ground shift or loss of supply ($V_{SUP1/2}$).

9.3.1.1 LIN Transmitter Characteristics

The transmitter has thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with and internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure

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to $V_{SUP1/2}$, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor and series diode to $V_{SUP1/2}$ must be added when the device is used for a commander node application.

9.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are proportional with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAE J2602 specifications. This allows the TLIN2024A-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to $V_{SUP1/2}$, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1 kΩ) and a series diode to $V_{SUP1/2}$ must be added when the device is used for commander node applications as per the LIN specification.

图 9-1 shows a commander node configuration and how the voltage levels are defined

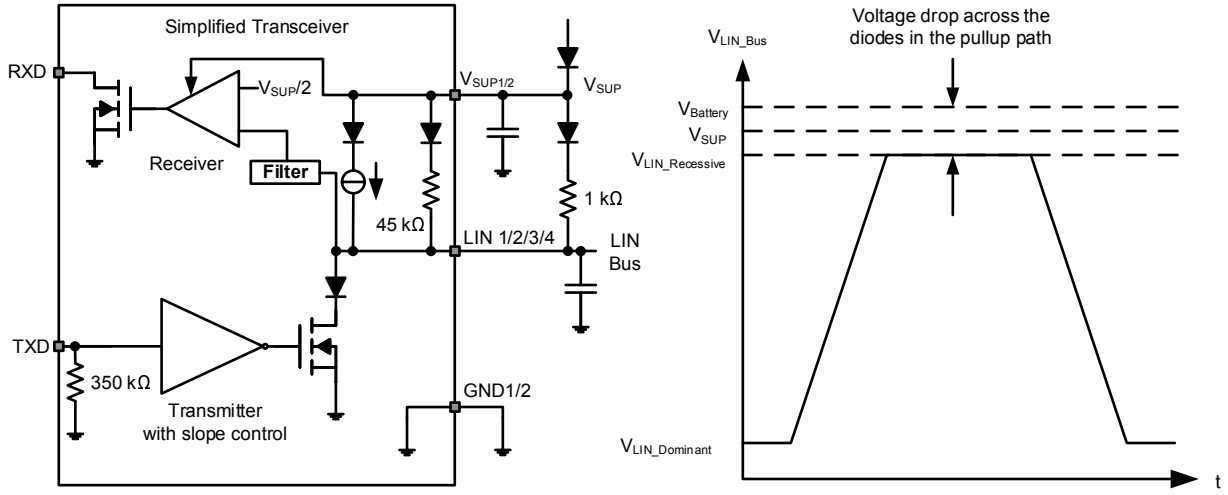


图 9-1. Commander Node Configuration with Voltage Levels

9.3.2 TXD (Transmit Input and Output)

TXD is the interface to the processor's LIN protocol controller or SCI/UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground). When TXD is high the LIN output is recessive (near $V_{Battery}$). See 图 9-1. The TXD input structure is compatible with microprocessors with 3.3 V and 5 V I/O. TXD has an internal pull-down resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timeout timer.

9.3.3 RXD (Receive Output)

RXD is the interface to the processor's LIN protocol controller or SCI/UART, which reports the state of the LIN bus voltage. LIN recessive (near $V_{Battery}$) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 V I/O microprocessors. If the microprocessor’s RXD pin does not have an integrated pull-up, an external pull-up resistor to the microprocessor I/O supply voltage is required. In standby mode the RXD pin is driven low to indicate a wake-up request from the LIN bus.

9.3.4 $V_{SUP1/2}$ (Supply Voltage)

$V_{SUP1/2}$ are the power supply pins. $V_{SUP1/2}$ is connected to the battery through and external reverse battery blocking diode (See 图 9-1). If there is a loss of power at the ECU level, the device has extremely low leakage

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from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.5 GND1/2 (Ground)

GND1 and GND2 are the ground connections for LIN1/2 and LIN3/4 channels respectively. V_{SUP1} is referred to GND1 and V_{SUP2} is referred to GND2. The device can operate with a ground shift as long as the ground shift does not reduce $V_{SUP1/2}$ below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has a low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN (Enable Input)

EN1, EN2, EN3 and EN4 control the operational modes of the respective LIN channel. When EN1/EN2/EN3/EN4 is high, the LIN1/LIN2/LIN3/LIN4 channel is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When either of the EN pins is low, the respective LIN channel is put into sleep mode and there is no transmission path available. The device can enter normal mode only after wake-up. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN floats.

9.3.7 Protection Features

The TLIN2024A-Q1 has several protection features.

9.3.8 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{DST}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{DST} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

9.3.9 Bus Stuck Dominant System Fault: False Wake-Up Lockout

The TLIN2024A-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. 图 9-2 and 图 9-3 show the behavior of this protection.

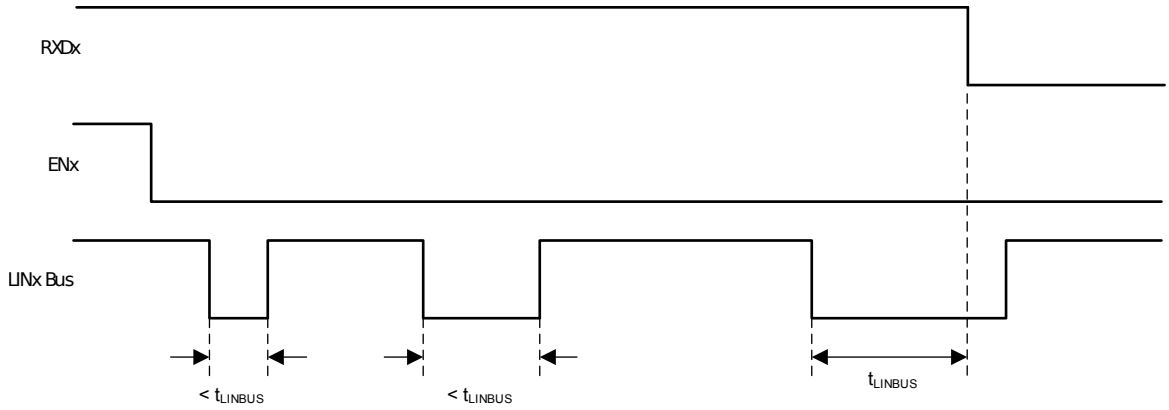


图 9-2. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake-up

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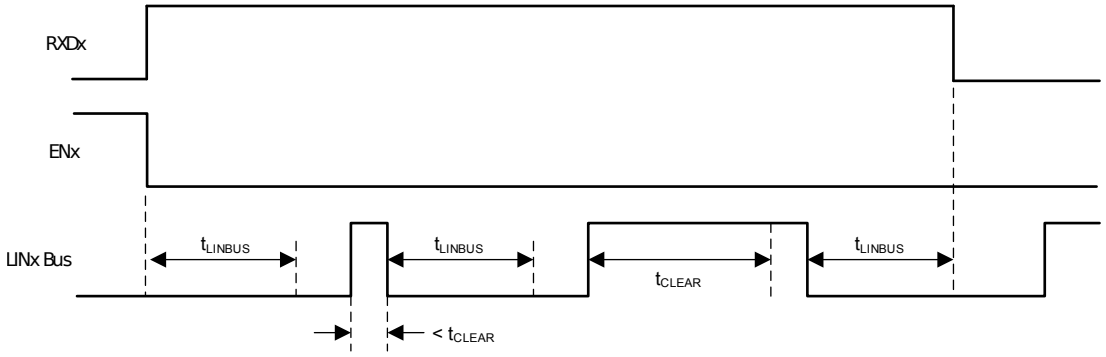


图 9-3. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wake-up

9.3.10 Thermal Shutdown

The LIN transmitter is protected by limiting the current; however if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remains in the normal operation mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is in recessive state, the RXD pin reflects the LIN bus and LIN bus pull-up termination remains on.

9.3.11 Under Voltage on V_{SUP}

The TLIN2024A-Q1 contains a power on reset circuit to avoid false bus messages during under voltage conditions when $V_{SUP1/2}$ is less than $UV_{SUP1/2}$.

9.3.12 Unpowered Device and LIN Bus

In automotive applications some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remains powered by the battery. The TLIN2024A-Q1 has a low unpowered leakage current from the bus so an unpowered node does not affect the network or load it down.

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9.4 Device Functional Modes

The TLIN2024A-Q1 has three functional modes of operation, normal, sleep, and standby. The next sections describe these modes as well as how the device moves between the different modes. 图 9-4 graphically shows the relationship while 表 9-1 shows the state of pins.

表 9-1. Operating Modes

MODE	ENx	RXDx	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Floating	Weak Current Pull-up	Off	
Standby	Low	Low	45 kΩ (typical)	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	LINx Bus Data	45 kΩ (typical)	On	LINx transmission up to 20 kbps

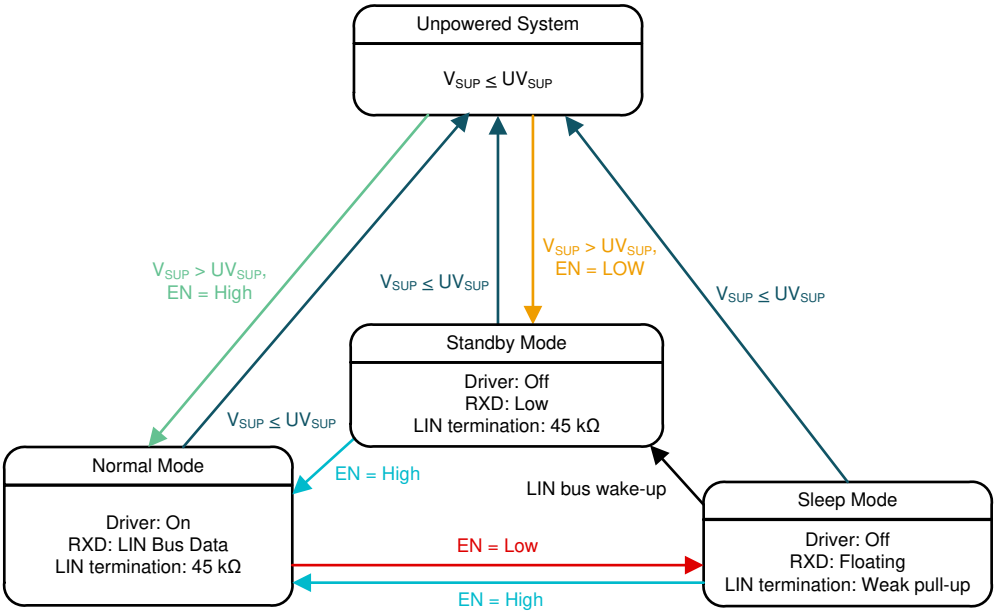


图 9-4. Operating State Diagram

9.4.1 Normal Mode

The EN pin controls the mode of the channel. If the EN1/EN2/EN3/EN4 pin is high at power up, the channel powers up in normal mode. In normal operational mode, the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a digital high and a dominant signal on the LIN bus is a digital low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the LIN channel is in sleep or standby mode for > t_{MODE_CHANGE} plus t_{NOMINT}.

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9.4.2 Sleep Mode

Sleep Mode is the power saving mode for the TLIN2024A-Q1. Even with extremely low current consumption in this mode, the LIN channel can still wake-up from LIN bus through a wake-up signal or if EN is set high for > t_{MODE_CHANGE}. The LIN bus is filtered to prevent false wake-up events. The wake-up events must be active for the respective time periods (t_{LINBUS}).

The sleep mode is entered by setting EN low for longer than t_{MODE_CHANGE}.

While the device is in sleep mode, the following conditions exist.

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake-up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake-up receiver are active.

9.4.3 Standby Mode

If the device powers up with any of the ENx pins held low, the corresponding LINx channel is in standby mode. Standby mode is also entered whenever a wake-up event occurs through the LIN bus while the device is in sleep mode. The LIN bus responder termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See Standby Mode Application Note for more application information.

When EN is set high for longer than t_{MODE_CHANGE} while the device is in standby mode the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

9.4.4 Wake-Up Events

There are two ways to wake-up from sleep mode:

- Remote wake-up initiated by the falling edge of a recessive (high) to dominant (low) state transition on LIN bus where the dominant state is be held for t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake-up event, eliminating false wake-ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake-up through EN being set high for longer than t_{MODE_CHANGE}.

9.4.4.1 Wake-Up Request (RXD)

When the TLIN2024A-Q1 encounters a wake-up event from the LIN bus, RXD goes low and the channel transitions to standby mode until EN is reasserted high and the channel enters normal mode. Once the channel enters normal mode the RXD pin releases the wake-up request signal and the RXD pin then reflects the receiver output from the LIN bus.

9.4.4.2 Mode Transitions

When the TLIN2024A-Q1 is transitioning between modes the device needs the time, t_{MODE_CHANGE}, to allow the change to fully propagate from the EN pin through the device into the new state. When transitioning from sleep or standby mode to normal mode the transition time is the sum of t_{MODE_CHANGE} and t_{NOMINT}.

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10 Application and Implementation Disclaimer

备注

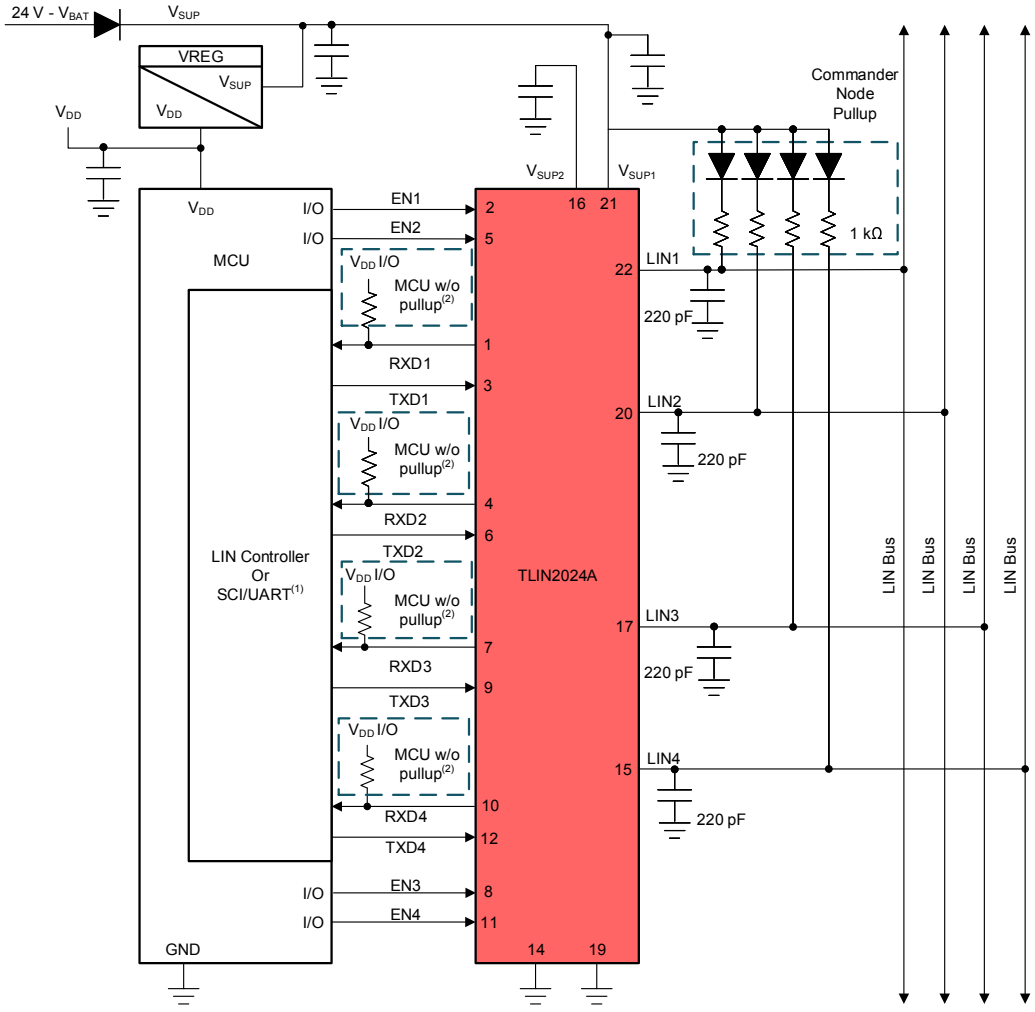
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10.1 Application Information

The TLIN2024A-Q1 can be used as both a responder device and a commander device in a LIN network. The device comes with the ability to support both remote wake-up request and local wake-up request.

10.2 Typical Application

The device comes with an integrated 45 kΩ pull-up resistor and series diode for responder node applications. For commander node applications, an external 1 kΩ pull-up resistor with series blocking diode can be used. Typical LIN Bus shows the device being used in both commander and responder applications.



(1) If RXD on MCU, or LIN transceiver, has an internal pull-up, then an external pull-up resistor is not required.
(2) If RXD on MCU, or LIN transceiver, does not have an internal pull-up, then an external pull-up resistor is required.
(3) Commander node applications require an external 1 kΩ pull-up resistor and serial diode.
(4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥10 µF

图 10-1. Typical LIN Bus

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10.2.1 Design Requirements

The RXD output structure is an open-drain output stage. This allows the TLIN2024A-Q1 to be used with 3.3 V and 5 V I/O microprocessors. If the RXD pin of the microprocessor does not have an integrated pull-up, an external pull-up resistor to the microprocessor I/O supply voltage is required.

The $V_{SUP1/2}$ pins of the device should be decoupled with a 100 nF capacitor as close to the supply pin on the device as possible. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements.

10.2.1.1 Detailed Design Procedures

10.2.1.2 Normal Mode Application Note

When using the TLIN2024A-Q1 in systems which are monitoring the RXD pin for a wake-up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake-up request until t_{MODE_CHANGE} when going from sleep or standby to normal mode. This is shown in Mode Transitions

10.2.1.3 Standby Mode Application Note

If the TLIN2024A-Q1 detects an under voltage on $V_{SUP1/2}$, the RXD pin transitions low and would signal to the software that the device is in standby mode and should be returned to sleep mode for the lowest power state.

10.2.1.4 TXD Dominant State Timeout Application Note

The maximum dominant TXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for commander and responder applications thus there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

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10.2.2 Application Curves

图 10-2 and 图 10-3 show the propagation delay from the TXD pin to the LIN pin for both dominant to recessive and recessive to dominant edges. Waveforms are for 1 channel of the device configured in commander mode with external pull-up resistor (1 kΩ) and 680 pF bus capacitance.

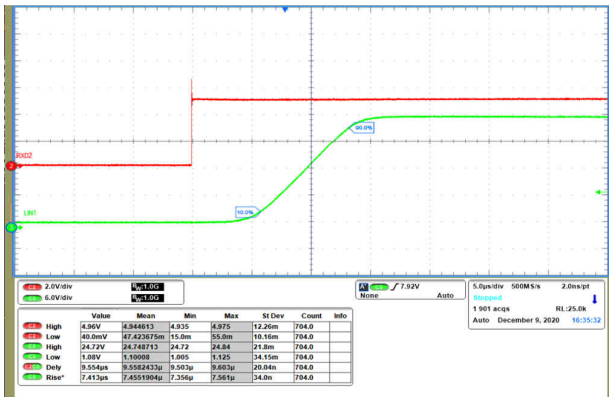


图 10-2. Dominant to Recessive Propagation

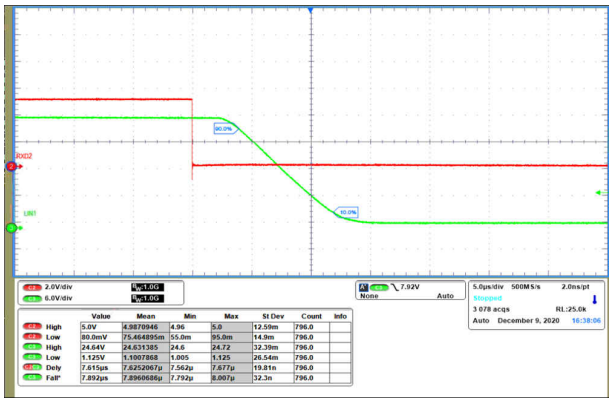


图 10-3. Recessive to Dominant Propagation

10.3 Power Supply Recommendations

The TLIN2024A-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 4 V to 48 V. A 100 nF decoupling capacitor should be placed as close to the $V_{SUP1/2}$ pin of the device as possible. It is good practice for some applications with noisier supplies to include 1 µF and 10 µF decoupling capacitor.

10.4 Layout

In order for the PCB design to be successful, start with the design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

10.4.1 Layout Guidelines

- **Pins 1, 4, 7 and 10 (RXD1/2/3/4):** The pins are open drain outputs and require an external pull-up resistor in the range of 1 kΩ and 10 kΩ to function properly. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pins 2, 5, 8 and 11 (EN1/2/3/4):** EN is an input pin that is used to place the device in a low power sleep mode. If this feature is not used the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor, values between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pinto limit current on the digital lines in the case of an over voltage fault.
- **Pin 13, 18, 23 and 24 (NC):** Not Connected
- **Pins 3, 6, 9 and 12 (TXD1/2/3/4):** The TXD pins are the transmitter input signals to the device from the microprocessor. A series resistor can be placed to limit the input current to the device in the case of an overvoltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 14, 19 (GND2/1):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pins 22, 20, 17 and 15 (LIN1/2/3/4):** This pin connects to the LIN bus. For responder node applications a 220 pF capacitor to ground is implemented. For commander node applications and additional series resistor and blocking diode should be placed between the LIN pin and the $V_{SUP1/2}$ pin.
- **Pin 21, 160 ($V_{SUP1/2}$):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.

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备注

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

10.4.2 Layout Example

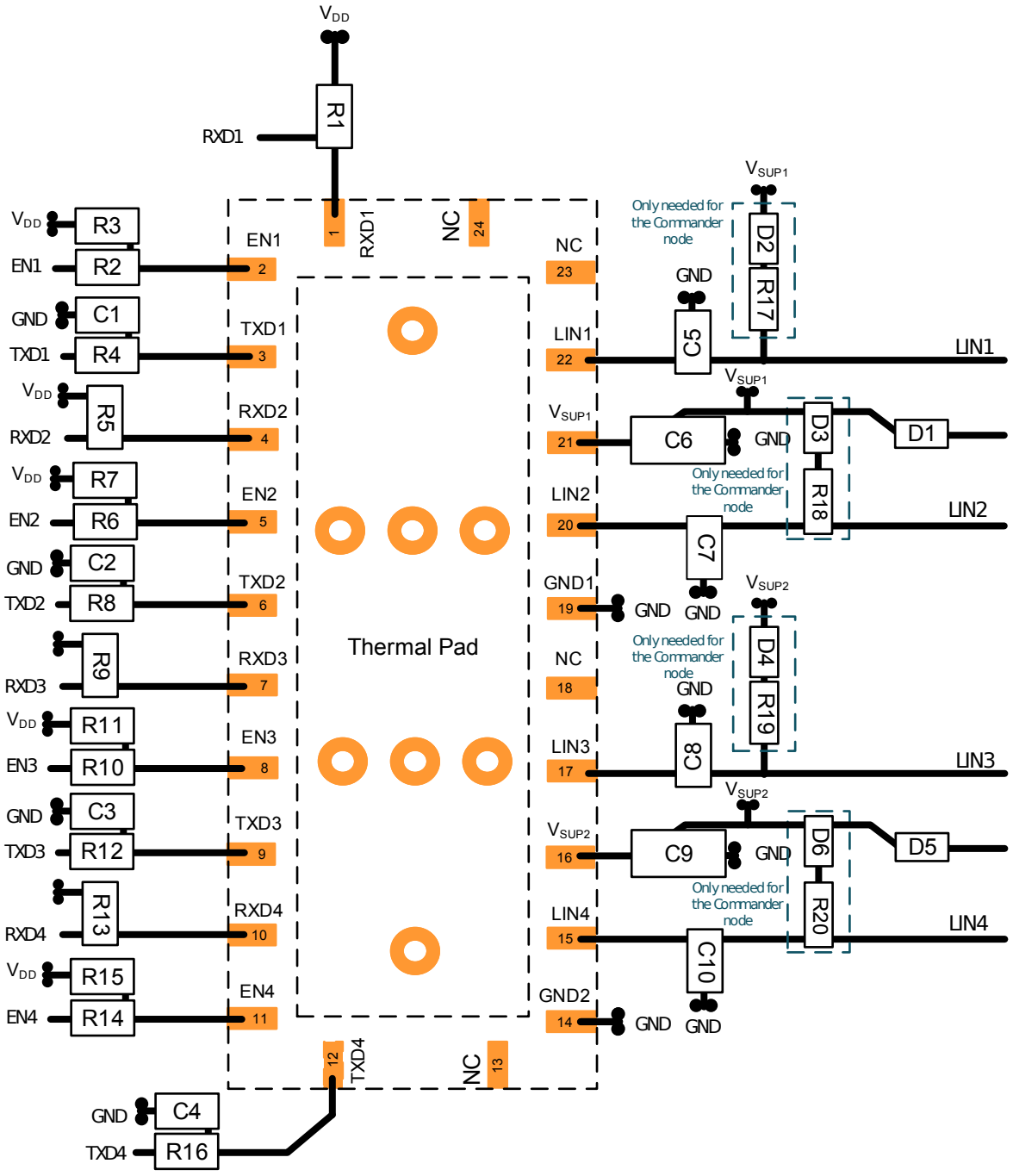


图 10-4. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

This device will conform to the following LIN standards. The core of what is needed is covered within this system spec, however reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed.

11.1.1 Related Documentation

For related documentation see the following:

LIN Standards:

- ISO/DIS 17987-1: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
- ISO/DIS 17987-4: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
- SAE J2602-1: LIN Network for Vehicle Applications

EMC requirements:

- SAE J2962-1
- ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
- ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
- ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
- ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
- IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
- IEC 6100-4-2
- IEC 61967-4
- CISPR25

Conformance Test requirements:

- ISO/DIS 17987-7: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
- SAE J2602-2: LIN Network for Vehicle Applications Conformance Test

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLIN2024ARGYRQ1	Active	Production	VQFN (RGY) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL2024A
TLIN2024ARGYRQ1.A	Active	Production	VQFN (RGY) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL2024A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

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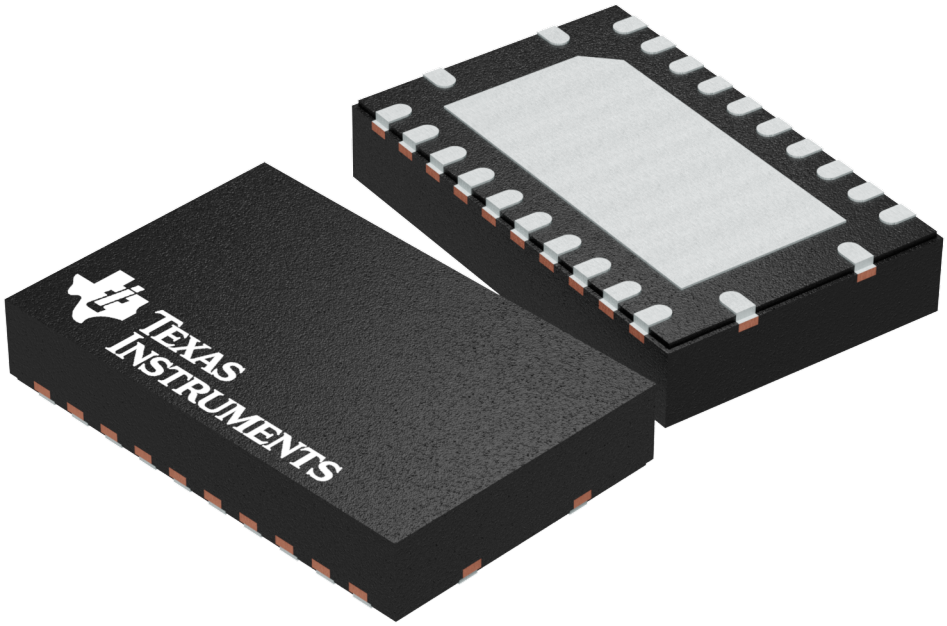
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RGY 24

VQFN - 1 mm max height

5.5 x 3.5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



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Refer to the product data sheet for package details.

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