

# TLC694x 16 通道 32/48 路复用 16 位 ES-PWM 恒定电流 LED 驱动器

## 1 特性

- 电源电压范围
  - $V_{CC}$  电压范围: 3V 至 5.5V
  - $V_{LED}$  电压范围: 高达  $V_{CC} + 0.3V$
- 16 个恒定电流阱通道
  - 0.3mA 至 25mA ( $3V \leq V_{CC} \leq 5.5V$ )
  - 通道电流偏差:  $\pm 1\%$  (典型值)
  - 器件电流偏差:  $\pm 1\%$  (典型值)
  - 膝点电压低: 10mA 时为 0.3V (典型值)
- 7 位 (128 级) 全局亮度控制功能 (BC)
- 16 位 (65,536 级) 增强频谱 PWM 灰度控制
- 内置存储器支持 TLC6946 32 路复用, 支持 TLC6948 48 路复用
- 增强的 LED 显示性能
  - 改善了低灰度均匀性
  - 低灰度耦合问题消除
  - 去除了重影和毛虫问题
- 高速串行数据接口
  - 数据移位时钟: 33MHz (最大值)
  - 灰度控制时钟: 33MHz (最大值)
  - 支持双边灰度控制
- 诊断和保护
  - LED 开路检测 (LOD)
  - IREF 电阻器短路保护 (ISP)
  - 热关断 (TSD)

- 智能省电模式

## 2 应用

- 单色、多色、全色 LED 显示
- 高刷新率 LED 视频显示
- 高密度、小间距 LED 矩阵显示

## 3 说明

在密度、小间距 LED 面板 应用中, 人们对多通道 LED 驱动器的性能要求在不断提高, 以期实现高多路复用、高 PWM 分辨率和高刷新率。为了满足严格的显示质量要求, LED 驱动器必须能够解决不同 LED 矩阵应用场景中的各种问题。

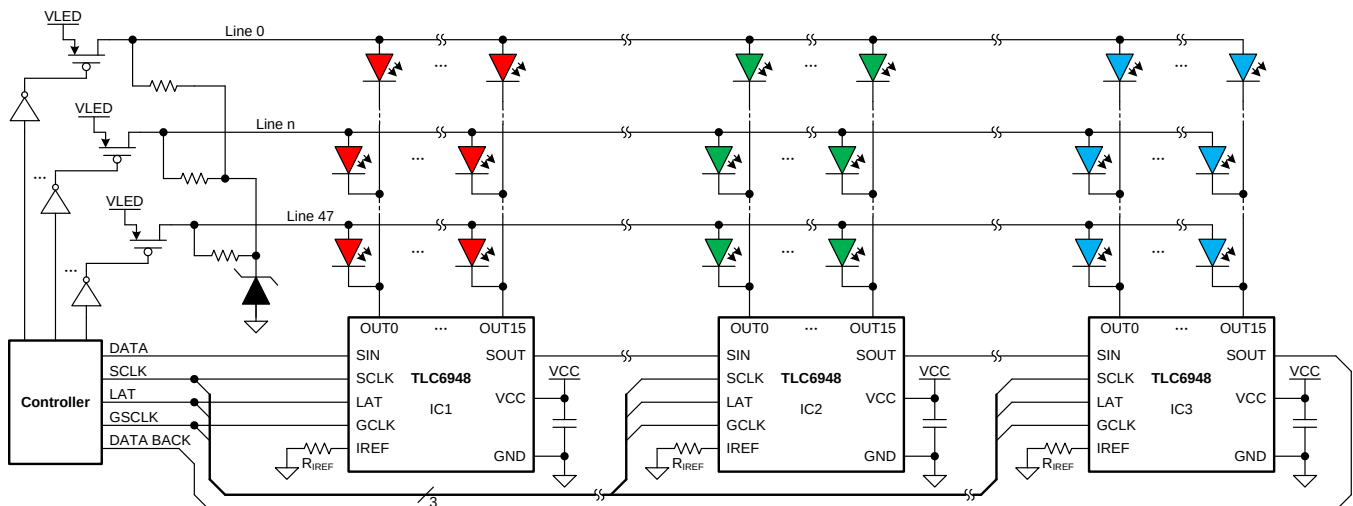
TLC694x 器件是一款 16 通道、恒定电流阱 LED 驱动器。每个通道都有独立可调的 65,536 级 PWM 灰度控制。所有 16 个通道的最大恒定电流值由一个具有 128 级全局亮度控制的外部电阻设置, 电流范围为 0.3mA 至 25mA。

器件信息<sup>(1)</sup>

| 器件型号    | 封装        | 封装尺寸 (标称值)      |
|---------|-----------|-----------------|
| TLC6946 | SSOP (24) | 8.65mm × 3.90mm |
|         | VQFN (24) | 4.00mm × 4.00mm |
| TLC6948 | SSOP (24) | 8.65mm × 3.90mm |
|         | VQFN (24) | 4.00mm × 4.00mm |

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

T48 路多路复用 LC6948 典型应用原理图



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## 4 修订历史记录

### Changes from Original (June 2018) to Revision A

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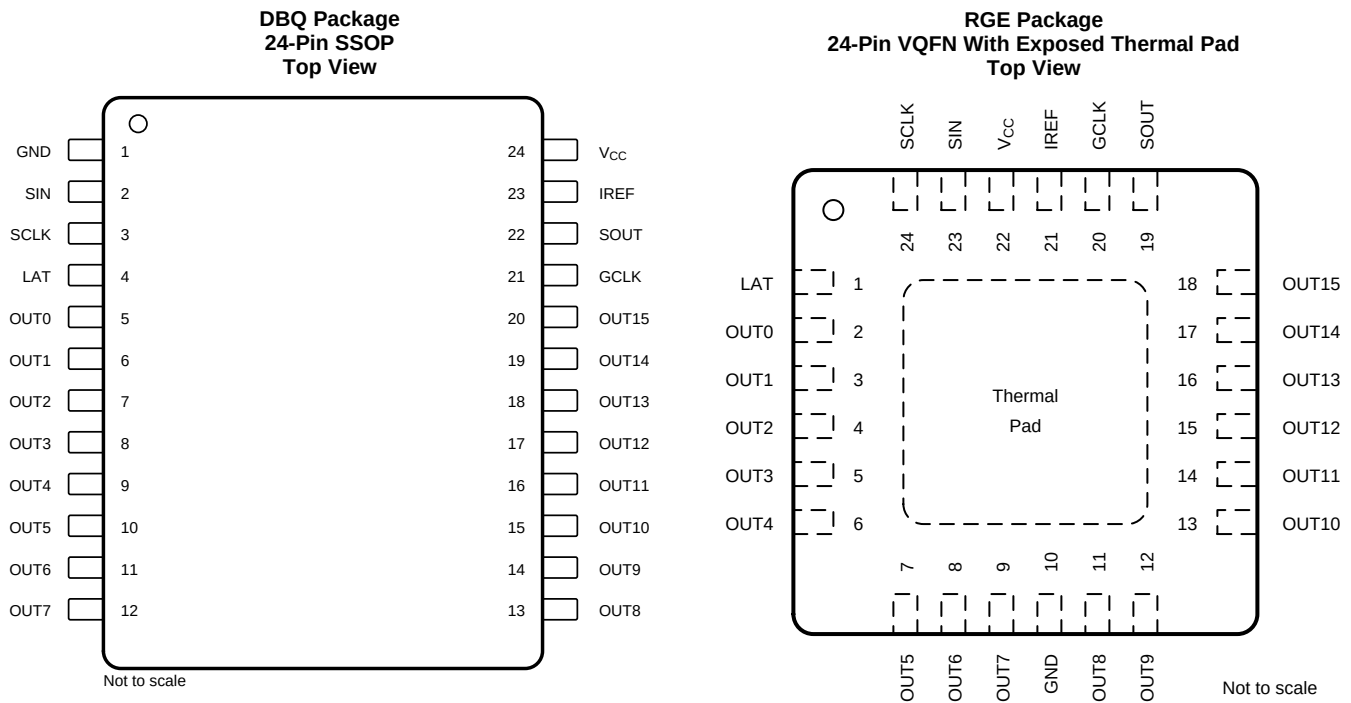
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|---------------------|----------|
| • 首次发布生产数据数据表 ..... | <b>1</b> |
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## 5 说明（续）

TLC694x 器件集成了增强型电路来解决小间距 LED 显示应用中的 各种显示问题：低灰度均匀性问题、耦合问题、重影问题和卡特彼勒问题。

TLC694x 器件 具有 LED 开路检测功能，错误检测结果可以通过串行数据接口读取。热关断和 IREF 电阻短路保护可确保实现更高的系统可靠性。TLC694x 器件还具有智能省电模式，可以在所有输出关断的情况下将总电流消耗设置为 1mA（典型值）。

## 6 Pin Configuration and Functions



### Pin Functions

| NAME | PIN NO. |     | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                     |
|------|---------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | DBQ     | RGE |     |                                                                                                                                                                                                                                                                                                                 |
| GCLK | 21      | 20  | I   | Grayscale (GS) pulse-width modulation (PWM) reference-clock-signal input pin. In the default operating mode, each GCLK rising edge increments the GS counter for PWM control. GCLK supports dual-edge operation.                                                                                                |
| GND  | 1       | 10  | —   | Power-ground reference                                                                                                                                                                                                                                                                                          |
| IREF | 23      | 21  | I   | Pin for setting the maximum constant-current value. Connecting an external resistor between IREF and GND sets the maximum current for each constant-current output channel. When this pin is connected directly to GND, all outputs are forced off. The external resistor should be placed close to the device. |
| LAT  | 4       | 1   | I   | Data latch pin. The falling edge of LAT latches the data from the common shift register into the GS data memory or the function control register.                                                                                                                                                               |

**Pin Functions (continued)**

| PIN             |     |     | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                            |
|-----------------|-----|-----|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME            | NO. |     |     |                                                                                                                                                                                                                                                                                                        |
|                 | DBQ | RGE |     |                                                                                                                                                                                                                                                                                                        |
| OUT0            | 5   | 2   | O   | Constant-current output. Each output can be tied together with others to increase the constant current. A different voltage can be applied to each output.                                                                                                                                             |
| OUT1            | 6   | 3   | O   |                                                                                                                                                                                                                                                                                                        |
| OUT2            | 7   | 4   | O   |                                                                                                                                                                                                                                                                                                        |
| OUT3            | 8   | 5   | O   |                                                                                                                                                                                                                                                                                                        |
| OUT4            | 9   | 6   | O   |                                                                                                                                                                                                                                                                                                        |
| OUT5            | 10  | 7   | O   |                                                                                                                                                                                                                                                                                                        |
| OUT6            | 11  | 8   | O   |                                                                                                                                                                                                                                                                                                        |
| OUT7            | 12  | 9   | O   |                                                                                                                                                                                                                                                                                                        |
| OUT8            | 13  | 11  | O   |                                                                                                                                                                                                                                                                                                        |
| OUT9            | 14  | 12  | O   |                                                                                                                                                                                                                                                                                                        |
| OUT10           | 15  | 13  | O   |                                                                                                                                                                                                                                                                                                        |
| OUT11           | 16  | 14  | O   |                                                                                                                                                                                                                                                                                                        |
| OUT12           | 17  | 15  | O   |                                                                                                                                                                                                                                                                                                        |
| OUT13           | 18  | 16  | O   |                                                                                                                                                                                                                                                                                                        |
| OUT14           | 19  | 17  | O   |                                                                                                                                                                                                                                                                                                        |
| OUT15           | 20  | 18  | O   |                                                                                                                                                                                                                                                                                                        |
| SCLK            | 3   | 24  | I   | Clock-signal input pin. Serial data present on SIN are shifted to the LSB of the internal 16-bit common shift register on the SCLK rising edge. All data in the shift register are shifted toward the MSB of the internal 16-bit common shift register on each SCLK rising edge.                       |
| SIN             | 2   | 23  | I   | Serial-data input pin of the internal 16-bit common shift register. When SIN is high, the LSB of the internal 16-bit common shift register is set to 1 on the SCLK input rising edge. When SIN is low, the LSB of the internal 16-bit common shift register is set to 0 on the SCLK input rising edge. |
| SOUT            | 22  | 19  | O   | Serial data output pin of the internal 16-bit common shift register. The MSB of the internal 16-bit common shift register appears on SOUT.                                                                                                                                                             |
| V <sub>CC</sub> | 24  | 22  | I   | Power supply pin                                                                                                                                                                                                                                                                                       |
| Thermal pad     | —   | —   | —   | Internally connected to GND in the RGE package only. The thermal pad and the GND pin must be connected together on the board.                                                                                                                                                                          |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                                                |                                  | MIN  | MAX                   | UNIT |
|------------------------------------------------|----------------------------------|------|-----------------------|------|
| Voltage                                        | V <sub>CC</sub>                  | −0.3 | 6                     | V    |
|                                                | GCLK, IREF, LAT, SCLK, SIN, SOUT | −0.3 | V <sub>CC</sub> + 0.3 | V    |
|                                                | OUT0 to OUT15                    | −0.3 | V <sub>CC</sub> + 0.3 | V    |
| Current                                        | OUT0 to OUT15                    | 0    | 27                    | mA   |
| Operating junction temperature, T <sub>J</sub> |                                  | −40  | 150                   | °C   |
| Storage temperature, T <sub>stg</sub>          |                                  | −55  | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

### 7.2 ESD Ratings

|                    |                         |                                                                                | VALUE | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±7000 | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                       |                                                           |                                    | MIN                   | NOM | MAX                   | UNIT |
|-----------------------|-----------------------------------------------------------|------------------------------------|-----------------------|-----|-----------------------|------|
| V <sub>CC</sub>       | Supply voltage                                            | Supply voltage                     | 3                     |     | 5.5                   | V    |
| V <sub>OUTn</sub>     | Voltage applied to OUT0 to OUT15                          | Voltage applied to OUT0 to OUT15   | 0                     |     | V <sub>CC</sub>       | V    |
| V <sub>IH</sub>       | High-level input voltage                                  | GCLK, LAT, SCLK, SIN               | 0.7 × V <sub>CC</sub> |     | V <sub>CC</sub>       | V    |
| V <sub>IL</sub>       | Low-level input voltage                                   | GCLK, LAT, SCLK, SIN               | 0                     |     | 0.3 × V <sub>CC</sub> | V    |
| I <sub>OH</sub>       | High-level output current                                 | SOUT                               |                       |     | −2                    | mA   |
| I <sub>OL</sub>       | Low-level output current                                  | SOUT                               |                       |     | 2                     | mA   |
| I <sub>OLC, max</sub> | Maximum constant-output sink current                      | OUT0 to OUT15                      | 0.3                   |     | 25                    | mA   |
| f <sub>SCLK</sub>     | Data-shift clock frequency                                | SCLK                               |                       |     | 33                    | MHz  |
| f <sub>GCLK</sub>     | Grayscale control clock frequency                         | GCLK                               |                       |     | 33                    | MHz  |
| f <sub>GCLK,B</sub>   | Grayscale control clock frequency for dual-edge operation | GCLK                               |                       |     | 25                    | MHz  |
| t <sub>w(H0)</sub>    | Pulse width duration                                      | SCLK                               | 10                    |     |                       | ns   |
| t <sub>w(L0)</sub>    | Pulse width duration                                      | SCLK                               | 10                    |     |                       | ns   |
| t <sub>w(H1)</sub>    | Pulse width duration                                      | GCLK                               | 10                    |     |                       | ns   |
| t <sub>w(L1)</sub>    | Pulse width duration                                      | GCLK                               | 10                    |     |                       | ns   |
| t <sub>w(H2)</sub>    | Pulse width duration                                      | GCLK (for dual-edge operation)     | 18                    |     |                       | ns   |
| t <sub>w(L2)</sub>    | Pulse width duration                                      | GCLK (for dual-edge operation)     | 18                    |     |                       | ns   |
| t <sub>SU(0)</sub>    | Setup time                                                | SIN to SCLK↑                       | 2                     |     |                       | ns   |
| t <sub>SU(1)</sub>    | Setup time                                                | LAT↑ to SCLK↑                      | 5                     |     |                       | ns   |
| t <sub>SU(2)</sub>    | Setup time                                                | LAT↓ to SCLK↑                      | 5                     |     |                       | ns   |
| t <sub>SU(3)</sub>    | Setup time                                                | LAT↓ to SCLK↑, read data from SOUT | 50                    |     |                       | ns   |
| t <sub>SU(4)</sub>    | Setup time                                                | LAT↓ (WRTGS) to LAT↓ (WRTGS)       | 1.5                   |     |                       | μs   |

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

|             |                                |                                                                                                     | MIN | NOM | MAX | UNIT |
|-------------|--------------------------------|-----------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $t_{SU(5)}$ | Setup time                     | LAT ↓ (WRTGS) to LAT ↓ (VSYNC)                                                                      | 1.5 |     |     | μs   |
| $t_{SU(6)}$ | Setup time                     | LAT ↓ (VSYNC) to GCLK ↑                                                                             | 2.5 |     |     | μs   |
| $t_{SU(7)}$ | Setup time                     | LAT ↓ (VSYNC) to LAT ↓ (WRTGS)                                                                      | 2.5 |     |     | μs   |
| $t_{SU(8)}$ | Setup time                     | Last LAT (non-0 GS data latched) ↓ to the first GCLK ↑ of next frame (wake up from power-save mode) | 50  |     |     | μs   |
| $t_{LSW}$   | Line switching time            | Last GCLK ↓ to the first GCLK ↑ of next line                                                        | 1   |     |     | μs   |
| $t_{h(0)}$  | Hold time                      | SCLK ↑ to SIN                                                                                       | 2   |     |     | ns   |
| $t_{h(1)}$  | Hold time                      | SCLK ↑ to LAT ↑                                                                                     | 2   |     |     | ns   |
| $t_{h(2)}$  | Hold time                      | SCLK ↑ to LAT ↓                                                                                     | 10  |     |     | ns   |
| $T_A$       | Operating ambient temperature  | Operating ambient temperature                                                                       | –40 |     | 85  | °C   |
| $T_J$       | Operating junction temperature | Operating junction temperature                                                                      | –40 |     | 125 | °C   |

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TLC6946    |            | UNIT |
|-------------------------------|----------------------------------------------|------------|------------|------|
|                               |                                              | DBQ (SSOP) | RGE (VQFN) |      |
|                               |                                              | 24 PINS    | 24 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 87.2       | 35.6       | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 42.3       | 34.7       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 41.4       | 15.2       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 9.2        | 0.7        | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 41         | 15.2       | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | N/A        | 5          | °C/W |

(1) For more information about traditional and new thermalmetrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

$V_{CC} = 3\text{ V}$  to  $5.5\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ; typical values are at  $V_{CC} = V_{LED} = 3.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , over recommended operating conditions (unless otherwise noted)

| PARAMETER           |                                                            | TEST CONDITIONS                                                                                                                                                                    | MIN                   | TYP | MAX             | UNIT |
|---------------------|------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----|-----------------|------|
| V <sub>OH</sub>     | High-level output voltage                                  | I <sub>OH</sub> = −2 mA at SOUT                                                                                                                                                    | V <sub>CC</sub> − 0.4 |     | V <sub>CC</sub> | V    |
| V <sub>OL</sub>     | Low-level output voltage                                   | I <sub>OL</sub> = 2 mA at SOUT                                                                                                                                                     |                       |     | 0.4             | V    |
| V <sub>IREF</sub>   | Reference voltage                                          | BC = 00h, R <sub>IREF</sub> = 10.7 kΩ (I <sub>OUTn</sub> = 0.3-mA target)                                                                                                          | 0.8                   |     |                 | V    |
| V <sub>(LOD)</sub>  | LED open-detection threshold                               | All OUTn = on, LODVTH = 00b                                                                                                                                                        | 0.12                  | 0.2 | 0.28            | V    |
|                     |                                                            | All OUTn = on, LODVTH = 01b                                                                                                                                                        | 0.42                  | 0.5 | 0.58            | V    |
|                     |                                                            | All OUTn = on, LODVTH = 10b                                                                                                                                                        | 0.82                  | 0.9 | 0.98            | V    |
|                     |                                                            | All OUTn = on, LODVTH = 11b                                                                                                                                                        | 1.12                  | 1.2 | 1.28            | V    |
| V <sub>(KNEE)</sub> | Knee voltage (OUT0 to OUT15)                               | All OUTn = on, BC = 36h, R <sub>IREF</sub> = 1.27 kΩ (I <sub>OUTn</sub> = 10-mA target)                                                                                            | 0.3                   |     |                 | V    |
| ΔIOLC0              | Constant-current error (channel-to-channel) <sup>(1)</sup> | All OUTn = on, BC = 00h, V <sub>OUTn</sub> = 1 V, R <sub>IREF</sub> = 10.7 kΩ (I <sub>OUTn</sub> = 0.3-mA target), T <sub>A</sub> = 25°C, includes the V <sub>IREF</sub> tolerance | ±1%                   |     | ±3.5%           |      |

(1) The deviation of each output from average of all channels constant current. The deviation is calculated by the formula.

$$\Delta(\%) = \left[ \frac{I_{OUTn}}{I_{OUT0} + I_{OUT1} + \dots + I_{OUT14} + I_{OUT15}} - 1 \right] \times 100$$

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## Electrical Characteristics (continued)

$V_{CC} = 3\text{ V}$  to  $5.5\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ; typical values are at  $V_{CC} = V_{LED} = 3.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , over recommended operating conditions (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS                                                                                                                                                                                                                                     | MIN  | TYP       | MAX         | UNIT             |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------|-------------|------------------|
| $\Delta I_{OLC1}$ | Constant-current error (device-to-device) <sup>(2)</sup><br>All OUTn = on, BC = 00h, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 10.7\text{ k}\Omega$ ( $I_{OUTn} = 0.3\text{-mA}$ target), $T_A = 25^\circ\text{C}$ , includes the $V_{IREF}$ tolerance  |      | $\pm 1\%$ | $\pm 2\%$   |                  |
| $\Delta I_{OLC2}$ | Constant-current error (channel-to-channel) <sup>(1)</sup><br>All OUTn = on, BC = 2Ah, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 10.7\text{ k}\Omega$ ( $I_{OUTn} = 1\text{-mA}$ target), $T_A = 25^\circ\text{C}$ , includes the $V_{IREF}$ tolerance  |      | $\pm 1\%$ | $\pm 3\%$   |                  |
| $\Delta I_{OLC3}$ | Constant-current error (device-to-device) <sup>(2)</sup><br>All OUTn = on, BC = 2Ah, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 10.7\text{ k}\Omega$ ( $I_{OUTn} = 1\text{-mA}$ target), $T_A = 25^\circ\text{C}$ , includes the $V_{IREF}$ tolerance    |      | $\pm 1\%$ | $\pm 2.5\%$ |                  |
| $\Delta I_{OLC4}$ | Constant-current error (channel-to-channel) <sup>(1)</sup><br>All OUTn = on, BC = 36h, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 1.27\text{ k}\Omega$ ( $I_{OUTn} = 10\text{-mA}$ target), $T_A = 25^\circ\text{C}$ , includes the $V_{IREF}$ tolerance |      | $\pm 1\%$ | $\pm 2.5\%$ |                  |
| $\Delta I_{OLC5}$ | Constant-current error (device-to-device) <sup>(2)</sup><br>All OUTn = on, BC = 36h, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 1.27\text{ k}\Omega$ ( $I_{OUTn} = 10\text{-mA}$ target), $T_A = 25^\circ\text{C}$ , includes the $V_{IREF}$ tolerance   |      | $\pm 1\%$ | $\pm 2.5\%$ |                  |
| $\Delta I_{OLC6}$ | Constant-current error (channel-to-channel) <sup>(1)</sup><br>All OUTn = on, BC = 7Eh, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 1.02\text{ k}\Omega$ ( $I_{OUTn} = 25\text{-mA}$ target), $T_A = 25^\circ\text{C}$ , includes the $V_{IREF}$ tolerance |      | $\pm 1\%$ | $\pm 2\%$   |                  |
| $\Delta I_{OLC7}$ | Constant-current error (device-to-device) <sup>(2)</sup><br>All OUTn = on, BC = 7Eh, $V_{OUTn} = 1\text{ V}$ , $R_{IREF} = 1.02\text{ k}\Omega$ ( $I_{OUTn} = 25\text{-mA}$ target), $T_A = 25^\circ\text{C}$ , includes the $V_{IREF}$ tolerance   |      | $\pm 1\%$ | $\pm 2\%$   |                  |
| $\Delta I_{OLC8}$ | Line regulation <sup>(3)</sup><br>All OUTn = on, $V_{CC} = 3\text{ V}$ to $5.5\text{ V}$ , $V_{OUTn} = 1\text{ V}$                                                                                                                                  |      | $\pm 1$   | $\pm 2$     | %/V              |
| $\Delta I_{OLC9}$ | Load regulation <sup>(4)</sup><br>All OUTn = on, $V_{OUTn} = 1\text{ V}$ to $3\text{ V}$                                                                                                                                                            |      | $\pm 1$   | $\pm 2$     | %/V              |
| $V_{IL(ISP)}$     | IREF resistor short-protection enter threshold                                                                                                                                                                                                      | 0.15 | 0.195     |             | V                |
| $V_{IH(ISP)}$     | IREF resistor short-protection release threshold                                                                                                                                                                                                    |      | 0.325     | 0.4         | V                |
| $T_{(TSD)}$       | Thermal shutdown threshold <sup>(5)</sup>                                                                                                                                                                                                           |      | 170       |             | $^\circ\text{C}$ |
| $T_{(HYS)}$       | Thermal shutdown hysteresis <sup>(5)</sup>                                                                                                                                                                                                          |      | 15        |             | $^\circ\text{C}$ |
| $I_I$             | SCLK or SIN Input current<br>$V_I = V_{CC}$ or GND at SCLK or SIN                                                                                                                                                                                   | -1   |           | 1           | $\mu\text{A}$    |

(2) The deviation of the average of constant current from the ideal constant current value.

$$\Delta(\%) = \left[ \frac{\frac{I_{OUT0} + I_{OUT1} + \dots + I_{OUT14} + I_{OUT15}}{16} - \text{Ideal Output Current}}{\text{Ideal Output Current}} \right] \times 100$$

, Ideal current is calculated by the

$$\text{Ideal Output (mA)} = \text{Gain} \times \left( \frac{V_{IREF}}{R_{IREF(\Omega)}} \right) \times \left( \frac{1}{8} + \frac{BC}{144} \right)$$

following equation

(3) Line regulation is calculated by the following equation

$$\Delta(\%V) = \left[ \frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\text{V}) - (I_{OUTn} \text{ at } V_{CC} = 3\text{V})}{(I_{OUTn} \text{ at } V_{CC} = 3\text{V})} \right] \times \frac{100}{5.5\text{V} - 3\text{V}}$$

(4) Load regulation is calculated by the following equation

$$\Delta(\%V) = \left[ \frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\text{V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1\text{V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1\text{V})} \right] \times \frac{100}{3\text{V} - 1\text{V}}$$

(5) Specified by design

## Electrical Characteristics (continued)

$V_{CC} = 3\text{ V}$  to  $5.5\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ; typical values are at  $V_{CC} = V_{LED} = 3.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , over recommended operating conditions (unless otherwise noted)

| PARAMETER          |                               | TEST CONDITIONS                                                                                                                                                                | MIN | TYP | MAX | UNIT |
|--------------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| I <sub>CC(0)</sub> | Supply current <sup>(5)</sup> | GCLK = LAT = SCLK = SIN = GND, GS <sub>n</sub> = 0000h, BC = 00h, PCHG_EN = 0, V <sub>OUTn</sub> = V <sub>CC</sub> , R <sub>IREF</sub> = open                                  | 3   | 4.5 | 6   | mA   |
| I <sub>CC(1)</sub> |                               | GCLK = LAT = SCLK = SIN = GND, GS <sub>n</sub> = 0000h, BC = 36h, PCHG_EN = 0, V <sub>OUTn</sub> is floating, R <sub>IREF</sub> = 1.27 kΩ (I <sub>OUTn</sub> = 10-mA target)   | 4   | 6.5 | 8   | mA   |
| I <sub>CC(2)</sub> |                               | GCLK = LAT = SCLK = SIN = GND, GS <sub>n</sub> = 0000h, BC = 7Eh, PCHG_EN = 0, V <sub>OUTn</sub> is floating, R <sub>IREF</sub> = 1.27 kΩ (I <sub>OUTn</sub> = 20-mA target)   | 4   | 7.5 | 9   | mA   |
| I <sub>CC(3)</sub> |                               | LAT = SCLK = SIN = GND, GCLK = 33 MHz, GS <sub>n</sub> = FFFFh, BC = 36h, PCHG_EN = 0, V <sub>OUTn</sub> = 1 V, R <sub>IREF</sub> = 1.27 kΩ (I <sub>OUTn</sub> = 10-mA target) | 4.7 | 7   | 10  | mA   |
| I <sub>CC(4)</sub> |                               | LAT = SCLK = SIN = GND, GCLK = 33 MHz, GS <sub>n</sub> = FFFFh, BC = 7Eh, PCHG_EN = 0, V <sub>OUTn</sub> = 1 V, R <sub>IREF</sub> = 1.27 kΩ (I <sub>OUTn</sub> = 20-mA target) | 4.7 | 7.7 | 10  | mA   |
| I <sub>CC(6)</sub> |                               | In power-save mode, PCHG_EN = 0, R <sub>IREF</sub> = 1.60 kΩ                                                                                                                   |     | 1   | 1.5 | mA   |
| R <sub>DW</sub>    | Pulldown resistor             | LAT                                                                                                                                                                            | 250 | 480 | 750 | kΩ   |
|                    |                               | GCLK                                                                                                                                                                           | 250 | 480 | 750 |      |

## 7.6 Switching Characteristics

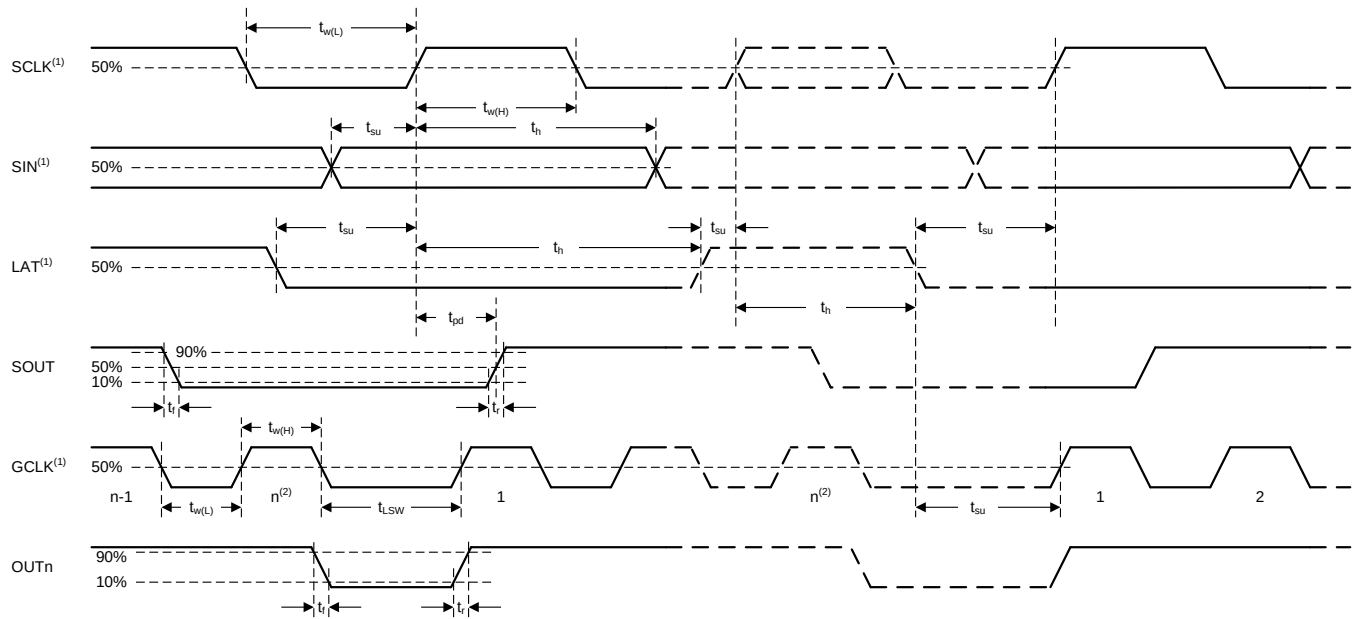
$V_{CC} = 3\text{ V}$  to  $5.5\text{ V}$  and  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ; Typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{LED} = 5\text{ V}$ , over recommended operating conditions (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS                                                                                                                                                                                                | MIN | TYP | MAX | UNIT |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $t_{r(0)}$  | SOUT                                                                                                                                                                                                           |     | 2   |     | ns   |
| $t_{r(1)}$  | Rise time <sup>(1)</sup><br>OUT <sub>n</sub> , BC = 7Eh, V <sub>OUTn</sub> = 1 V, R <sub>IREF</sub> = 1.02 k $\Omega$ (I <sub>OUTn</sub> = 25-mA target), T <sub>A</sub> = 25°C, R <sub>L</sub> = 160 $\Omega$ |     | 20  |     | ns   |
| $t_{f(0)}$  | SOUT                                                                                                                                                                                                           |     | 2   |     | ns   |
| $t_{f(1)}$  | Fall time <sup>(1)</sup><br>OUT <sub>n</sub> , BC = 7Eh, V <sub>OUTn</sub> = 1 V, R <sub>IREF</sub> = 1.02 k $\Omega$ (I <sub>OUTn</sub> = 25-mA target), T <sub>A</sub> = 25°C, R <sub>L</sub> = 160 $\Omega$ |     | 15  |     | ns   |
| $t_{pd(0)}$ | Propagation delay <sup>(1)</sup><br>SCLK $\uparrow$ to SOUT $\uparrow\downarrow$ , SEL_TD0 = 00b                                                                                                               |     | 5   |     | ns   |
|             | SCLK $\uparrow$ to SOUT $\uparrow\downarrow$ , SEL_TD0 = 01b                                                                                                                                                   |     | 10  |     | ns   |
|             | SCLK $\uparrow$ to SOUT $\uparrow\downarrow$ , SEL_TD0 = 10b                                                                                                                                                   |     | 20  |     | ns   |
|             | SCLK $\downarrow$ to SOUT $\uparrow\downarrow$ , SEL_TD0 = 11b                                                                                                                                                 |     | 5   |     | ns   |
| $t_{pd(1)}$ | LAT $\downarrow$ to SOUT, read LOD information                                                                                                                                                                 |     | 25  | 50  | ns   |

(1) Specified by design

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(1) Pulse rise and fall times are 1 ns–3 ns

(2) The last GCLK of each display segment in the sub period

**图 1. Timing Diagram**

## 7.7 Typical Characteristics

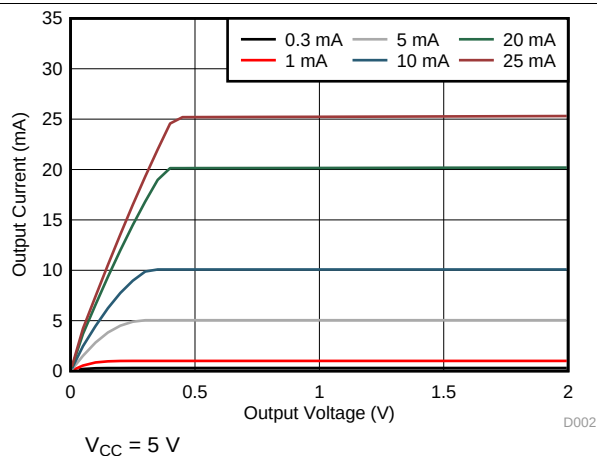


图 2. Channel Sink Current vs OUTn Voltage

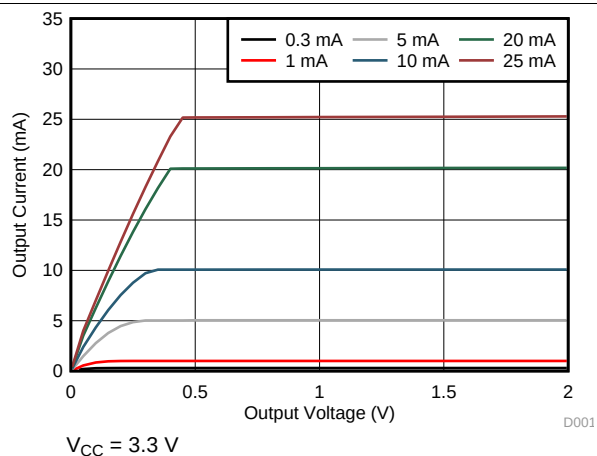


图 3. Channel Sink Current vs OUTn Voltage

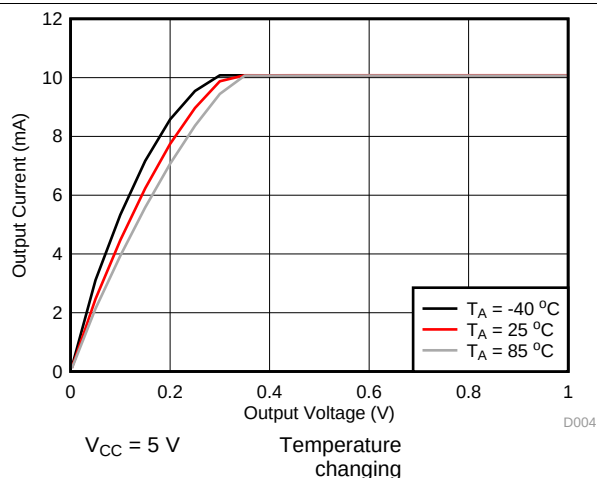


图 4. Channel Sink Current vs OUTn Voltage

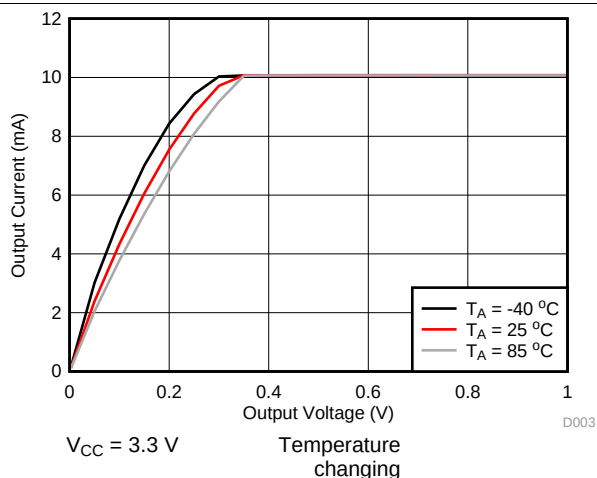


图 5. Channel Sink Current vs OUTn Current

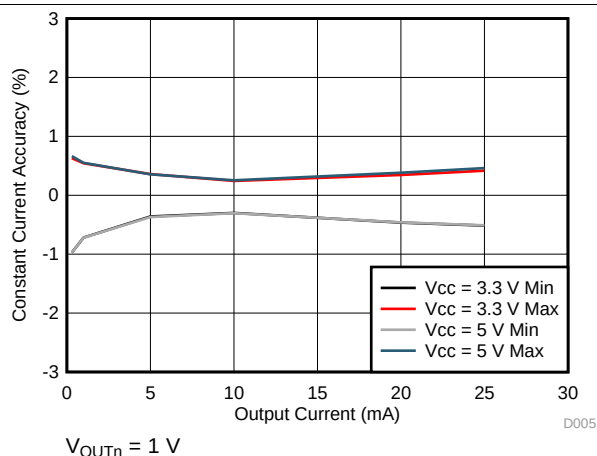


图 6. Channel to Channel Accuracy vs OUTn Current

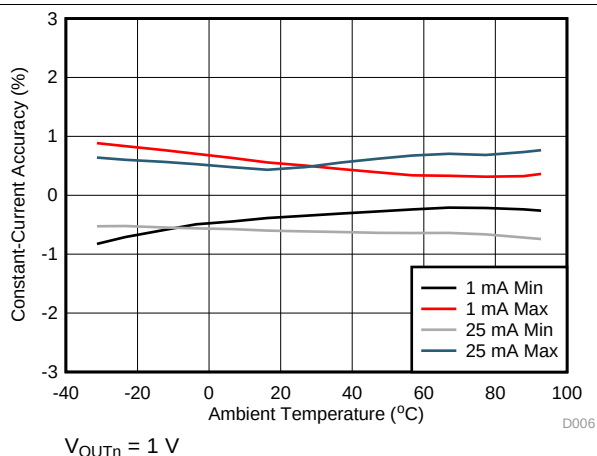


图 7. Channel to Channel Accuracy vs Temperature

## Typical Characteristics (接下页)

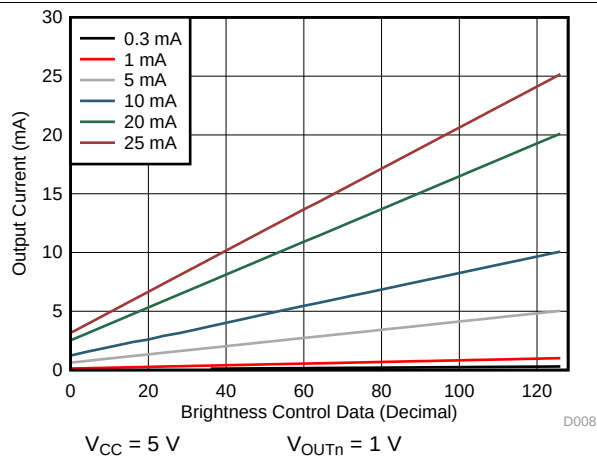


图 8. Channel Sink Current vs Brightness Control (BC)

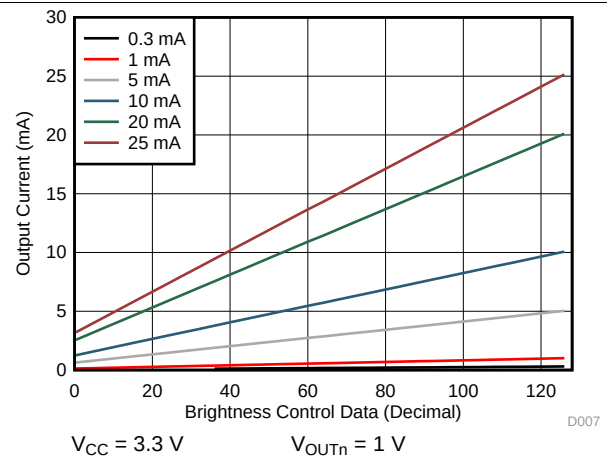


图 9. Channel Sink Current vs Brightness Control (BC)

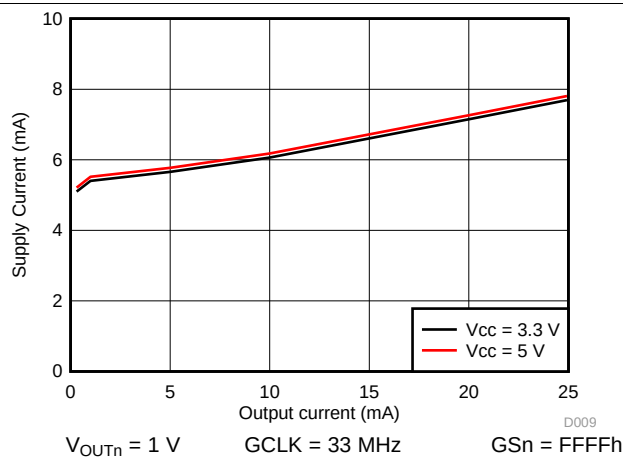


图 10. Supply Current ( $I_{CC}$ ) vs Channel Sink Current

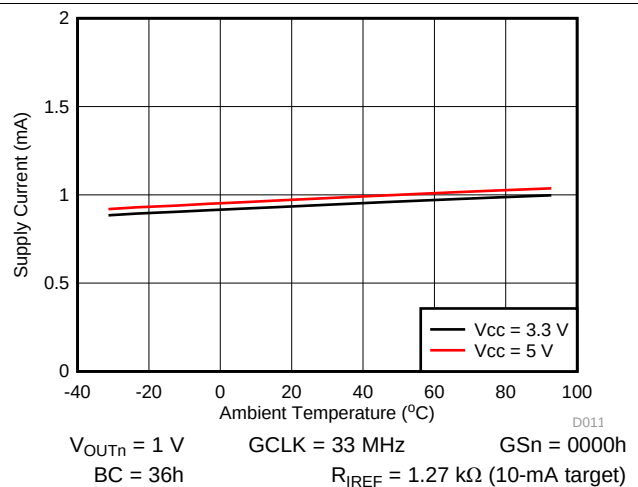
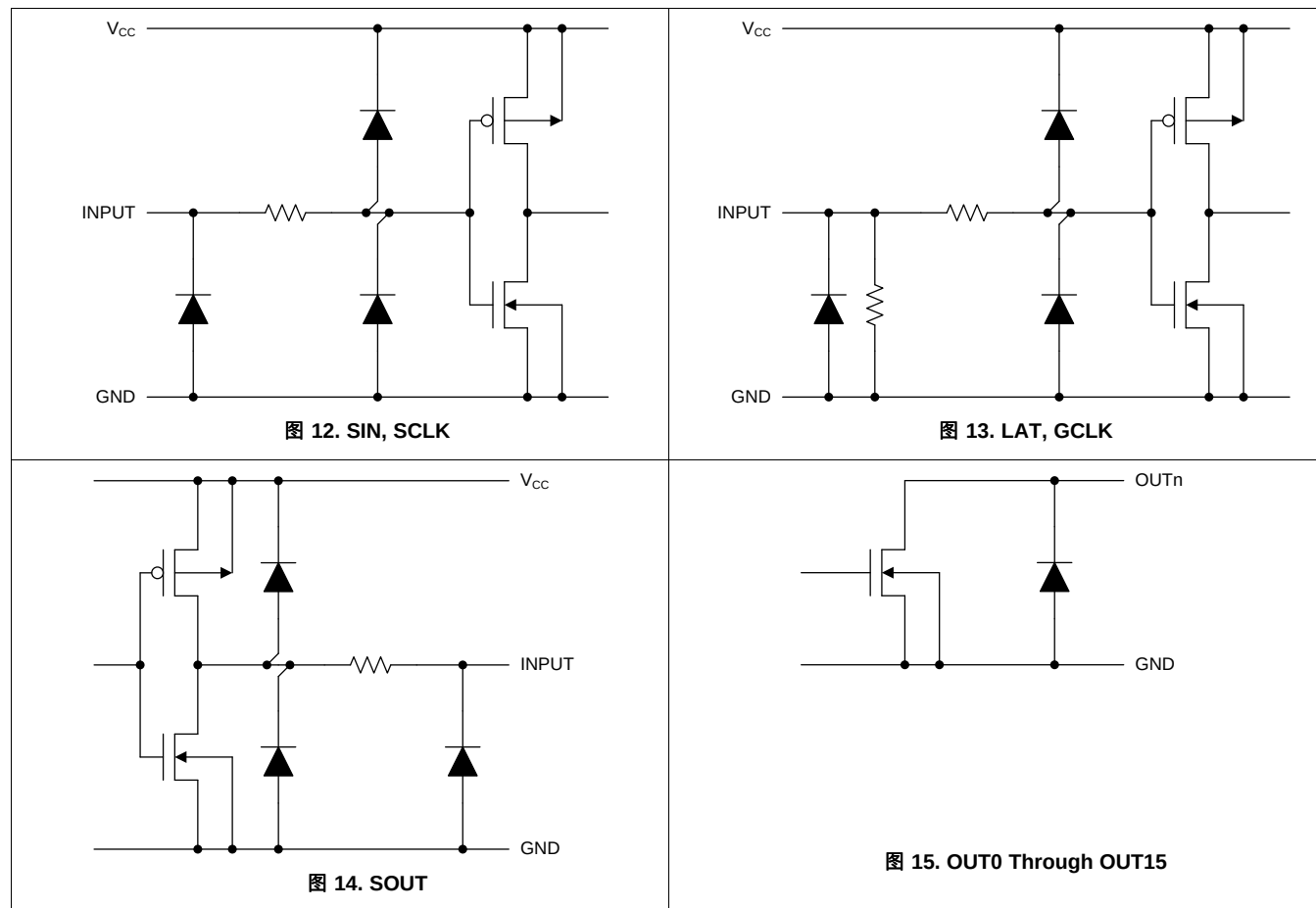


图 11. Supply Current ( $I_{CC}$ ) in Power-Save Mode vs Temperature

## 8 Parameter Measurement Information

### 8.1 Pin Equivalent Input and Output Schematic Diagrams



## 9 Detailed Description

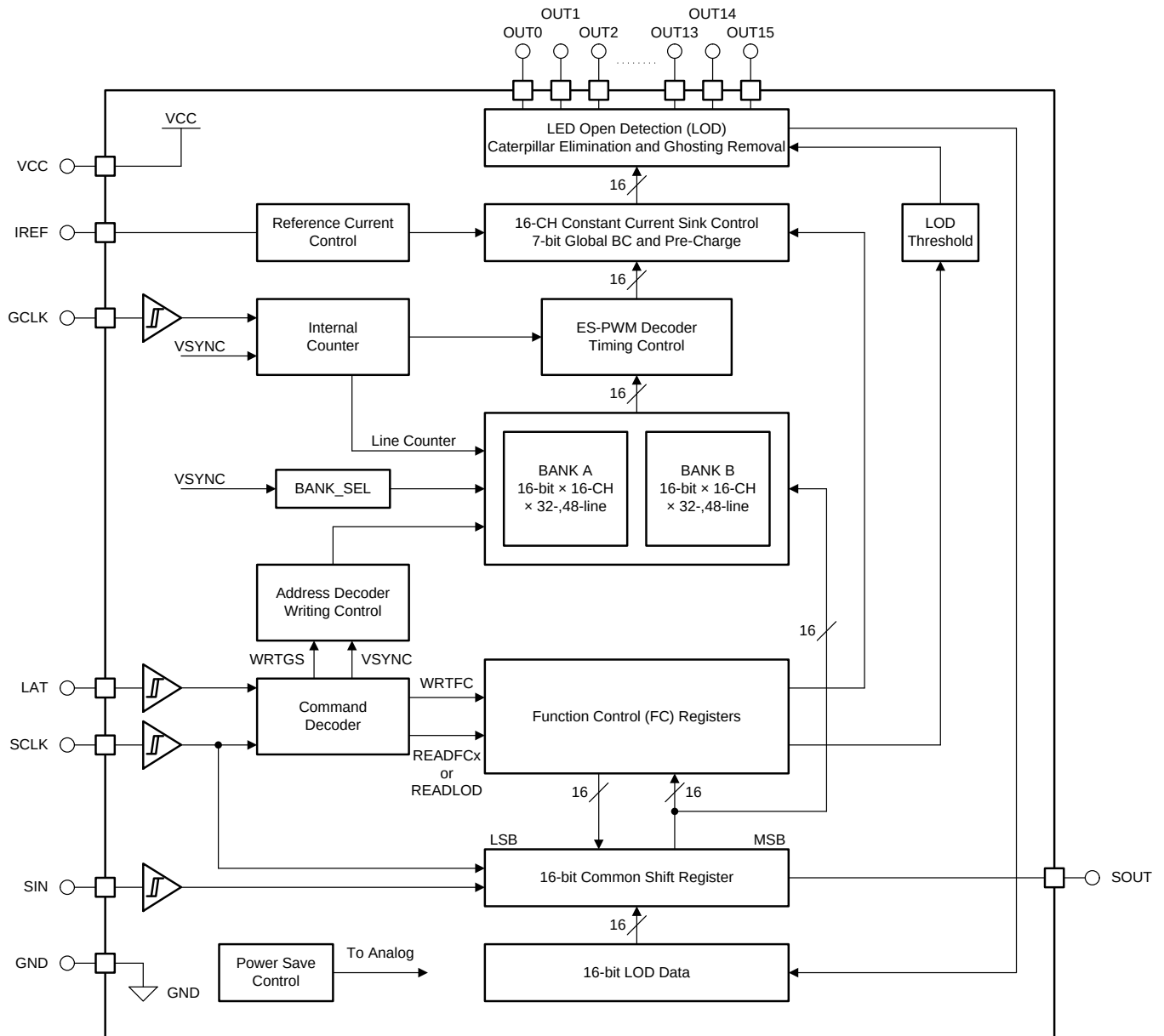
### 9.1 Overview

The TLC694x device is a 16-channel constant-current-sink LED driver supporting 1- to 32-, 48-multiplexing. Each channel has an individually adjustable 65,536-step pulse-width modulation (PWM) grayscale (GS) control. The TLC6946 device implements 16-Kbit display memory and the TLC6948 device implements 24-Kbit display memory to increase the visual refresh rate and to decrease the grayscale data-writing frequency.

The TLC694x device supports current from 0.3 mA to 25 mA for each channel, with typical 1% channel-to-channel current deviation and typical 1% device-to-device current deviation. The maximum current value of all 16 channels is set by an external IREF resistor and can be adjusted by the 128-step global brightness control (BC). The device also implements low-grayscale enhancement technology to solve the coupling issue and improve the display quality in low-grayscale conditions. These features make the TLC694x device a candidate for high-density-multiplexing LED-matrix-display and LED-panel applications.

The TLC694x device integrates enhanced circuits to solve the various display issues in fine-pitch LED display applications: the low-grayscale uniformity issue, coupling issue, ghosting issue, and caterpillar issue. The TLC694x device features an LED-open detection function, and the error detection results can be read via a serial data-interface port. Thermal shutdown and  $I_{REF}$ -resistor short protection ensure a higher system reliability. The TLC694x device also has a smart power-save mode that sets the total current consumption to 1 mA (typical) when all outputs are off.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Built-In 16Kb Display Memory (SRAM)

The TLC6946 device integrates 16K bits of SRAM to support 1- to 32-multiplexing and the TLC6948 device integrates 24K bits of SRAM to support 1- to 48-multiplexing. SRAM is divided into two BANKs: BANK A and BANK B. While BANK A is displaying, BANK B is ready to receive the data of the next frame. While BANK B is displaying, BANK A is ready to receive the data of next frame.

### 9.3.2 GCLK Dual-Edge Operation

The TLC694x device uses the rising edge or both edges of GCLK. The selection is made by setting the GCLK\_EDGE bit in the function control register. By default, the TLC6946 device uses the GCLK rising edge, and the maximum input GCLK frequency is 33 MHz. By setting GCLK\_EDGE = 1, the TLC694x device operates at both GCLK edges (rising and falling), and the maximum internal GCLK frequency is 50 MHz with external 25MHz input.

### 9.3.3 Programmable Constant-Sink Channel Current

#### 9.3.3.1 Global Brightness Control (BC)

The TLC694x device is able to adjust the output current of all constant-current outputs simultaneously. This function is called global brightness control (BC). The global BC for all outputs is programmed with a 7-bit word, thus all output currents can be adjusted in 128 steps from 12.5% to 100.69% for a given current-programming resistor,  $R_{IREF}$  (See 表 1). BC data can be set through the serial interface. When the BC data changes, the output current also changes immediately. When the device is powered on, the BC data in the function control register is set to 36h as the default value.

**表 1. Global BC Data vs Constant-Current Ratio and Set Current Value**

| BC DATA                       |                     |                     | GAIN      | RATIO OF GAIN /<br>GAIN_MAX (AT<br>MAX BC) | $I_{OUT}$ (mA) ( $I_{OLCmax}$ = 25<br>mA, TYP) | $I_{OUT}$ (mA) ( $I_{OLCmax}$ =<br>2.4 mA, TYP) |
|-------------------------------|---------------------|---------------------|-----------|--------------------------------------------|------------------------------------------------|-------------------------------------------------|
| BINARY                        | DECIMAL             | HEX                 |           |                                            |                                                |                                                 |
| 000 0000                      | 0                   | 00                  | 4         | 12.5%                                      | 3.13                                           | 0.3                                             |
| 000 0001                      | 1                   | 01                  | 4.22      | 13.19%                                     | 3.3                                            | 0.32                                            |
| 000 0010                      | 2                   | 02                  | 4.44      | 13.88%                                     | 3.47                                           | 0.33                                            |
| ...                           | ...                 | ...                 | ...       | ...                                        | ...                                            | ...                                             |
| 011 0101                      | 53                  | 35                  | 15.78     | 49.31%                                     | 12.33                                          | 1.18                                            |
| <b>011 0110<br/>(Default)</b> | <b>54 (Default)</b> | <b>36 (Default)</b> | <b>16</b> | <b>50%</b>                                 | <b>12.5</b>                                    | <b>1.2</b>                                      |
| 011 0111                      | 55                  | 37                  | 16.22     | 50.69%                                     | 12.67                                          | 1.22                                            |
| ...                           | ...                 | ...                 | ...       | ...                                        | ...                                            | ...                                             |
| 111 1101                      | 125                 | 7D                  | 31.78     | 99.31%                                     | 24.83                                          | 2.38                                            |
| 111 1110                      | 126                 | 7E                  | 32        | 100%                                       | 25                                             | 2.4                                             |
| 111 1111                      | 127                 | 7F                  | 32.22     | 100.69%                                    | 25.17                                          | 2.42                                            |

#### 9.3.3.2 Select $R_{IREF}$ for a Given BC

The maximum current per channel,  $I_{OLCmax}$ , is determined by resistor  $R_{IREF}$ , placed between the IREF and GND pins. The voltage on IREF is typically 0.8 V.  $R_{IREF}$  can be calculated by 公式 1.

$$R_{IREF} (k\Omega) = \frac{V_{IREF} (V)}{I_{OLCmax} (mA)} \times \text{Gain} = \frac{V_{IREF} (V)}{I_{OLCmax} (mA)} \times 32 \times \left( \frac{1}{8} + \frac{BC}{144} \right)$$

where

- $V_{IREF}$  is the internal reference voltage on  $I_{REF}$  (0.8 V)
- $I_{OLCmax}$  is the maximum current for each channel
- Gain is the current gain at BC = 7E (See 表 1)

(1)

$R_{IREF}$  must be between 1.02 k $\Omega$  and 10.7 k $\Omega$  in order to hold the channel sink current  $I_{OLC}$  between 25 mA (typical) and 0.3 mA (typical). Otherwise, the output may be unstable.

**表 2. Maximum Constant Current vs External Resistor  $R_{IREF}$**

| $I_{OLCmax}$ (mA) | $R_{IREF}$ (k $\Omega$ , typical) |
|-------------------|-----------------------------------|
| 25                | 1.02                              |
| 20                | 1.28                              |
| 15                | 1.71                              |
| 10                | 2.56                              |
| 5                 | 5.12                              |
| 2.4               | 10.7                              |

### 9.3.4 Grayscale (GS) Function (PWM Control)

The TLC694x device can adjust the brightness of each output channel using a pulse-width-modulation (PWM) control scheme. The architecture of 16 bits per channel results in 65536 brightness steps, from 0% up to 100% brightness. The on-time ( $t_{OUT\_ON}$ ) of each output (OUTn) can be calculated by [公式 2](#).

$$t_{OUT\_ON} = t_{GCLK} \times GS_n$$

where  $GS_n$  is the grayscale of channel OUTn (2)

The TLC694x device implements an enhanced spectrum (ES) PWM control. The ES-PWM control can be selected with two different modes: 8-bit MSB + 8-bit LSB (8+8) mode, and 9-bit MSB + 7-bit LSB (9+7) mode. See [TLC6946 Technical Reference Manual](#) for more details.

### 9.3.5 Serial Data Interface

The TLC6948 has a flexible serial interface that can be connected to microcontrollers or digital signal processors in various ways. Only three pins are needed to input data into the device. More than two TLC6948s can be connected in series by connecting an SOUT pin from one device to the SIN pin of the next device. The SOUT pin can also be connected to the controller to read back data from the TLC6948 device.

### 9.3.6 LED-Open Detection (LOD)

The LED-open detection (LOD) function detects faults caused by an open circuit in any LED string or a short from OUTn to ground with low impedance. It does this by comparing the OUTn voltage to the LOD-detection threshold-voltage level set by LODVTH in the function control register. If the OUTn voltage is lower than the programmed voltage, the corresponding output LOD bit is set to 1 to indicate an open LED. Otherwise, the output of that LOD bit is 0. LOD data output by the detection circuit are valid only during the *on* period of that OUTn output channel.

### 9.3.7 Caterpillar Removal

The TLC694x device implements an internal circuit that can eliminate the caterpillar issue caused by an open LED. The caterpillar effect is a common issue for LED panels. The caterpillar removal function is enabled by setting LODRM\_EN to 1 (default value after device powered on) in the function control register. When this function is enabled, the device automatically detects the open LED, and the corresponding channel does not turn on until device reset.

### 9.3.8 Precharge FET

The TLC694x internal precharge FET can prevent ghosting of multiplexed LED modules. One cause of this phenomenon is the charging current from parasitic capacitance on OUTn through the LED when the supply voltage switches from one common line to the next common line. To prevent this unwanted charging current, the TLC694x device uses an internal FET to pull up OUTn during the common-line switching period. As a result, no charging current flows through LED and ghosting is eliminated.

### 9.3.9 Thermal Shutdown

The thermal shutdown (TSD) function turns off all device constant-current outputs when the junction temperature ( $T_J$ ) exceeds 170°C (typical). It resumes normal operation when  $T_J$  falls below 155°C (typical).

### 9.3.10 IREF Resistor Short Protection (ISP)

The IREF resistor short protection (ISP) function prevents unwanted large currents from flowing through the constant-current output when the IREF resistor is shorted accidentally. The TLC694x device turns off all output channels when the IREF pin voltage is lower than 0.19 V (typical). When the IREF pin voltage goes higher than 0.325 V (typical), the TLC694x device resumes normal operation.

## 9.4 Device Functional Modes

### 9.4.1 Normal Operating Mode

The TLC694x device is fully functional when  $V_{CC}$  reaches 3 V and is below 5.5 V. After power on, all OUTn of the TLC694x device are turned off. All the internal counters and function control registers are initialized. Write the proper grayscale data and function control data to enable normal device operation.

### 9.4.2 Power-Save Mode (PSM)

The power-save mode (PSM) is enabled by setting PSM\_EN to 1 in the function control register.

When powered on, the default value of this bit is 0. When this function is enabled, if all the GS data received for the next frame are 0, then device enters power-save mode during the display of the next frame. When the device is in power-save mode, it resumes normal mode when it detects non-zero GS data input. In power-save mode, part of analog circuits are not operational; the device total current consumption,  $I_{CC}$ , is 1 mA(typical).

## 10 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The TLC6948 device is a 16-channel constant-current sink LED driver supporting 1- to 48-multiplexing. Each channel has an individually adjustable 65,536-step pulse-width-modulation (PWM) grayscale (GS) control. The TLC6948 device implements 24 Kbits of display memory to increase the visual refresh rate and to decrease the grayscale data writing frequency. This integrated memory makes TLC6948 a potential for high-density, fine-pitch LED matrix applications.

### 10.2 Typical Application

The TLC6948 is typically connected in series to drive the LED matrix with only a few controller ports. 图 16 shows a typical application diagram with TLC6948 devices connected in cascade for an LED matrix.

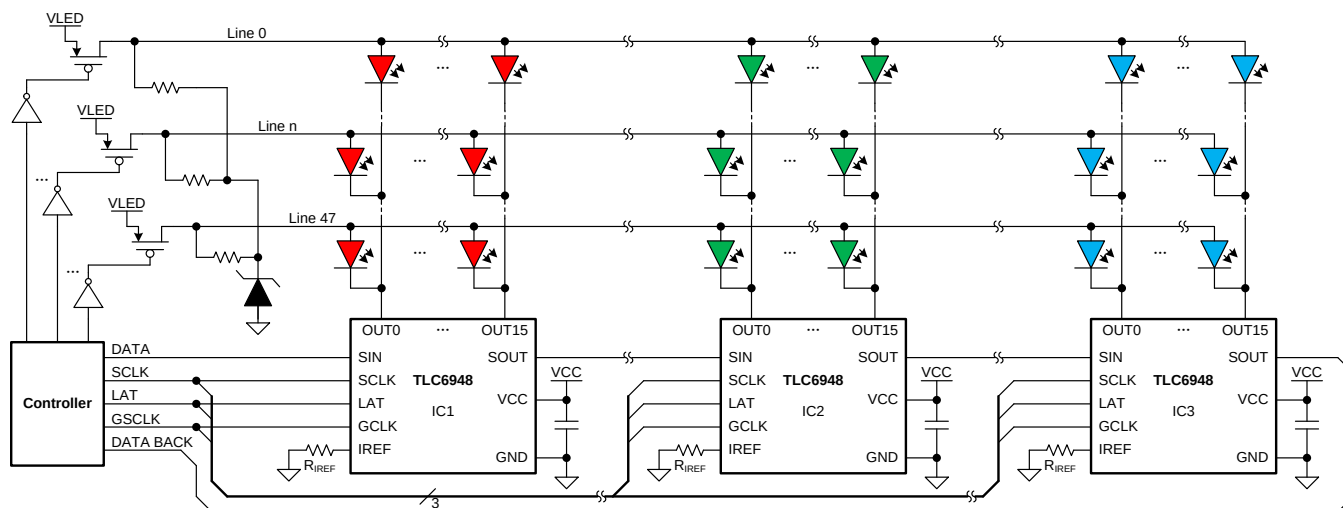


图 16. Cascading Three TLC6948 Devices

#### 10.2.1 Design Requirements

For this design example, use the following as the input parameters.

表 3. Design Parameters

| DESIGN PARAMETER                                     | EXAMPLE VALUE                              |
|------------------------------------------------------|--------------------------------------------|
| $V_{CC}$ and $V_{LED}$ voltage                       | 3 V to 5.5 V                               |
| SIN, SCLK, LAT, and GCLK voltage range               | Low level = GND, high level = $V_{CC}$     |
| The maximum LED forward voltage, $V_{(F)}$           | Red LED 2V, green and blue LED 3V          |
| The maximum current for each color LED, $I_{OLCmax}$ | Red LED 10mA, green LED 6mA, blue LED 4mA. |

## 10.2.2 Detailed Design Procedures

### 10.2.2.1 Power Supply Voltage

The LED power supply voltage  $V_{LED}$  must be higher than  $V_{(F)} + V_{(KNEE)}$ . The device power supply voltage,  $V_{CC}$  should be equal or higher than  $V_{LED}$ . One example value is  $V_{LED} = V_{CC} = 3.8\text{ V}$ . See [TLC6946 Technical Reference Manual](#) for more details.

### 10.2.2.2 Channel Current and Brightness Control

See [Global Brightness Control \(BC\)](#) and [Select  \$R\_{IREF}\$  for a Given BC](#). Select the reference-current-setting resistor  $R_{IREF}$  to set the maximum channel current for each color LED. Select the BC data for the best white balance of the red, green, and blue LED lamp. See [TLC6946 Technical Reference Manual](#) for more details.

### 10.2.2.3 SCLK and GCLK Frequency

SCLK is the serial data shift-in clock signal; and GCLK is the PWM-control reference-clock signal. [公式 3](#) shows the minimum frequency requirement for GCLK and SCLK. See [TLC6946 Technical Reference Manual](#) for more details.

$$f_{GCLK} = m \times n \times f_{VR}$$

$$f_{SCLK} = N \times n \times 256 \times f_{FPS}$$

where

- $f_{GCLK}$  is the minimum GCLK frequency for single-edge operating mode
- $f_{SCLK}$  is the minimum SCLK frequency
- $m$  is the GCLK number of each sub-period, determined by the PWM mode selected
- $f_{VR}$  is the visual refresh rate of the entire cascading series
- $N$  is the number of cascaded TLC6948 devices
- $n$  is the number of scan lines
- $f_{FPS}$  is the frame rate

(3)

### 10.2.3 Application Curves

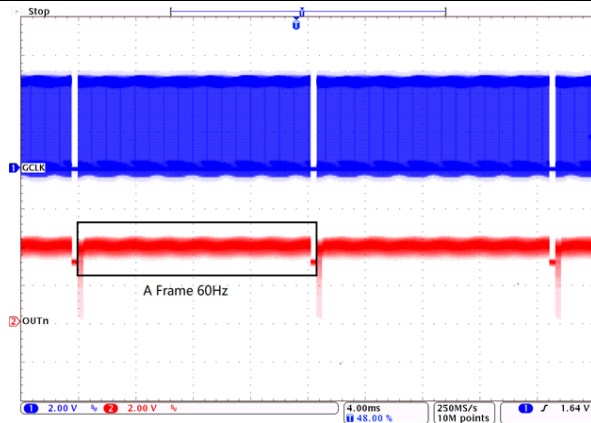


图 17. OUTn Waveform for ES-PWM Mode (GSn = 0001h)

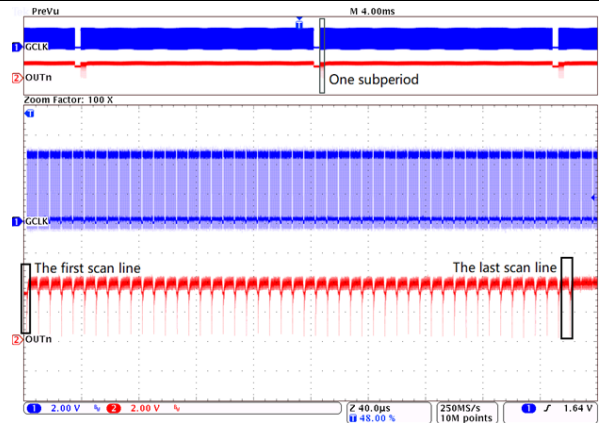


图 18. OUTn Waveform for ES-PWM Mode Zooming in One Sub-period (GSn = 0001h)

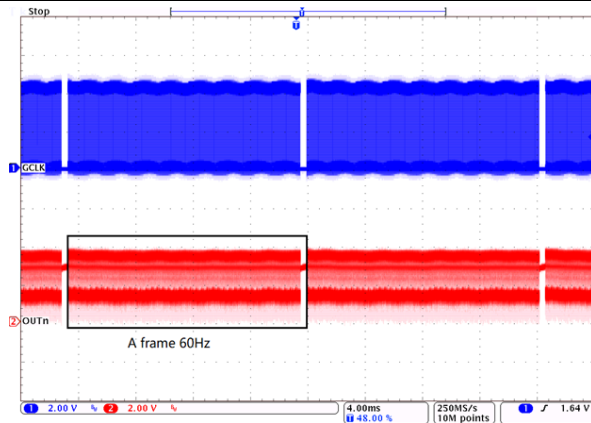


图 19. OUTn Waveform for ES-PWM Mode (GSn = FFFFh)

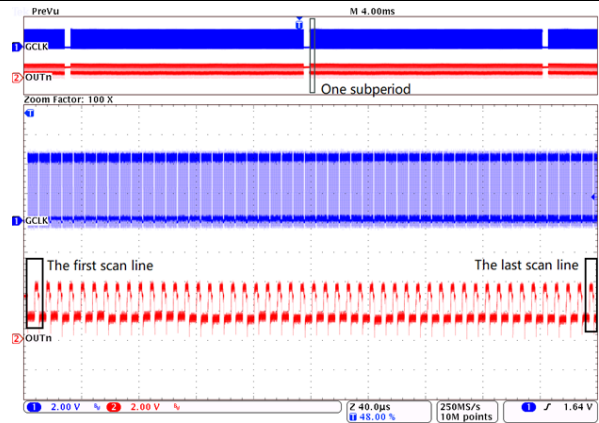


图 20. OUTn Waveform for ES-PWM Mode Zooming in One Sub-period (GSn = FFFFh)

## 11 Power Supply Recommendations

Decouple the  $V_{CC}$  power supply voltage by placing a 0.1- $\mu$ F ceramic capacitor close to the  $V_{CC}$  pin and GND plane. Depending on panel size, several equally distributed electrolytic capacitors must be placed on the board for a well-regulated LED supply voltage  $V_{LED}$ .  $V_{LED}$  voltage ripple must be less than 5% of its nominal value.

## 12 Layout

### 12.1 Layout Guidelines

Place the decoupling capacitor near the  $V_{CC}$  pin and GND plane.

Place the current-programming resistor,  $R_{IREF}$ , close to the IREF pin and the GND pin.

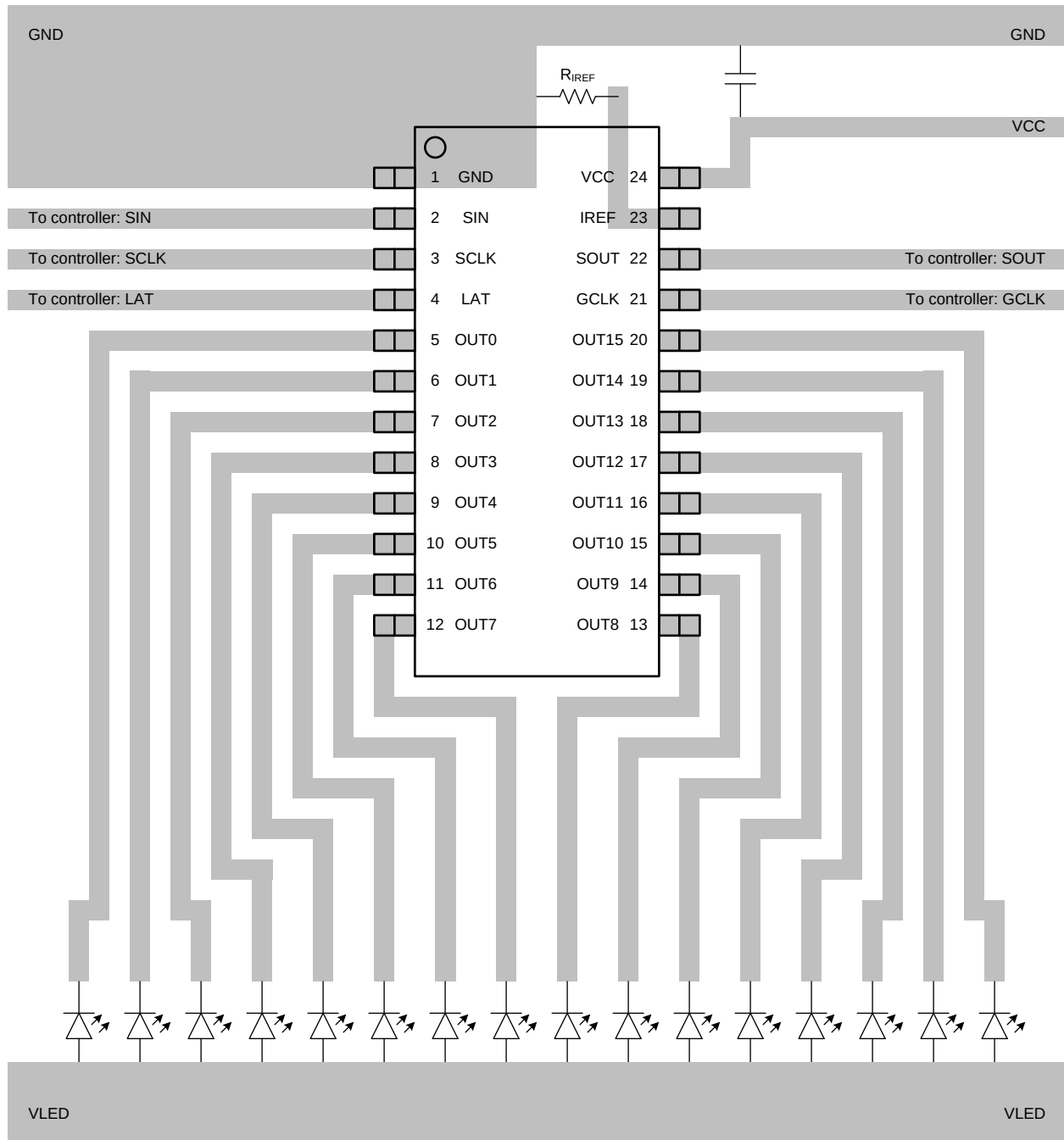
Make the GND trace as wide as possible for large GND currents.

Routing between the LED cathode and the device OUTn pin must be as short and straight as possible to reduce wire inductance.

The thermal pad (QFN package) must be connected to the GND plane. Because the thermal pad is used as a power ground pin internally, there is a large current flow through this pad when all channels turn on. Furthermore, connect the thermal pad to a heat sink layer by thermal vias to reduce device temperature. One suggested thermal via pattern is shown in [Layout Examples](#). For more information about suggested thermal via pattern and via size, see [PowerPAD Thermally Enhanced Package](#).

MOSFETs must be placed in the middle of the board, which should be laid out as symmetrically as possible.

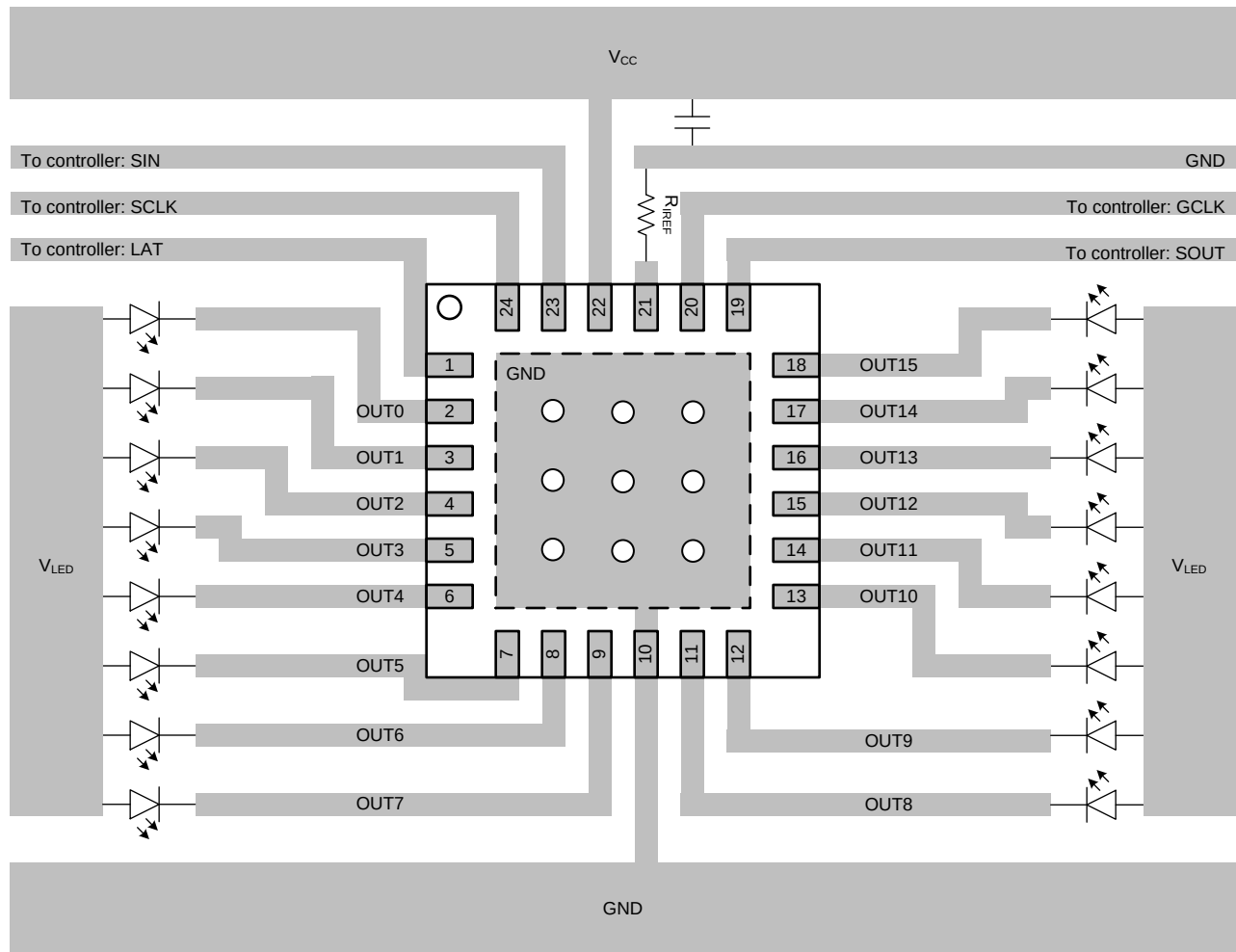
## 12.2 Layout Examples



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**图 21. SSOP-24 Package Layout Example**

## Layout Examples (接下页)



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**图 22. VQFN-24 Package Layout Example**

## 13 器件和文档支持

### 13.1 文档支持

#### 13.1.1 相关文档

请参阅如下相关文档：

- [《TLC694x 16 通道 LED 驱动器技术参考手册》](#)
- [《半导体和 IC 封装热指标》](#)

### 13.2 相关链接

[表 4](#) 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具与软件，以及立即订购快速访问。

**表 4. 相关链接**

| 器件      | 产品文件夹                 | 立即订购                  | 技术文档                  | 工具与软件                 | 支持和社区                 |
|---------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| TLC6946 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| TLC6948 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |

### 13.3 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](#) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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**设计支持** [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.7 术语表

[SLYZ022](#) — [TI 术语表](#)。

这份术语表列出并解释术语、缩写和定义。

## 14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是适用于指定器件的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TLC6946DBQR</a> | Active        | Production           | SSOP (DBQ)   24 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | TLC6946             |
| TLC6946DBQR.A               | Active        | Production           | SSOP (DBQ)   24 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | TLC6946             |
| <a href="#">TLC6946RGER</a> | Active        | Production           | VQFN (RGE)   24 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | TLC<br>6946         |
| TLC6946RGER.A               | Active        | Production           | VQFN (RGE)   24 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | TLC<br>6946         |
| <a href="#">TLC6948DBQR</a> | Active        | Production           | SSOP (DBQ)   24 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | TLC6948             |
| TLC6948DBQR.A               | Active        | Production           | SSOP (DBQ)   24 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | TLC6948             |
| <a href="#">TLC6948RGER</a> | Active        | Production           | VQFN (RGE)   24 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | TLC<br>6948         |
| TLC6948RGER.A               | Active        | Production           | VQFN (RGE)   24 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | TLC<br>6948         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

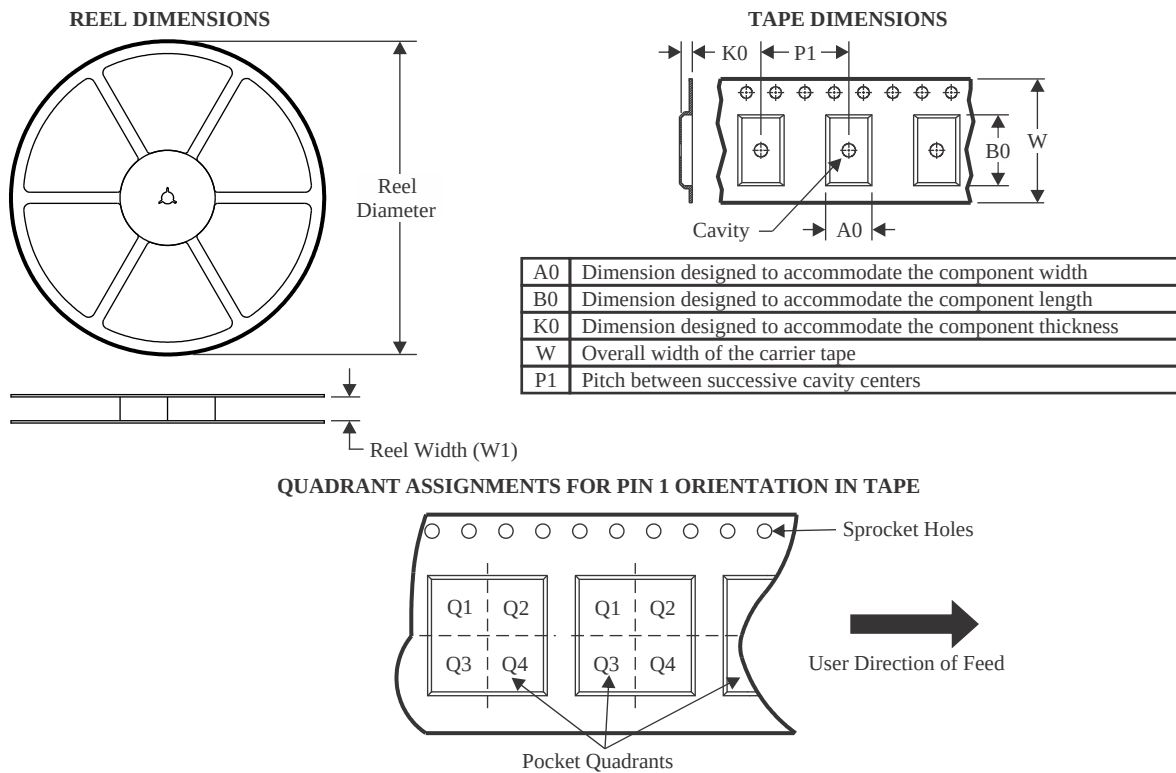
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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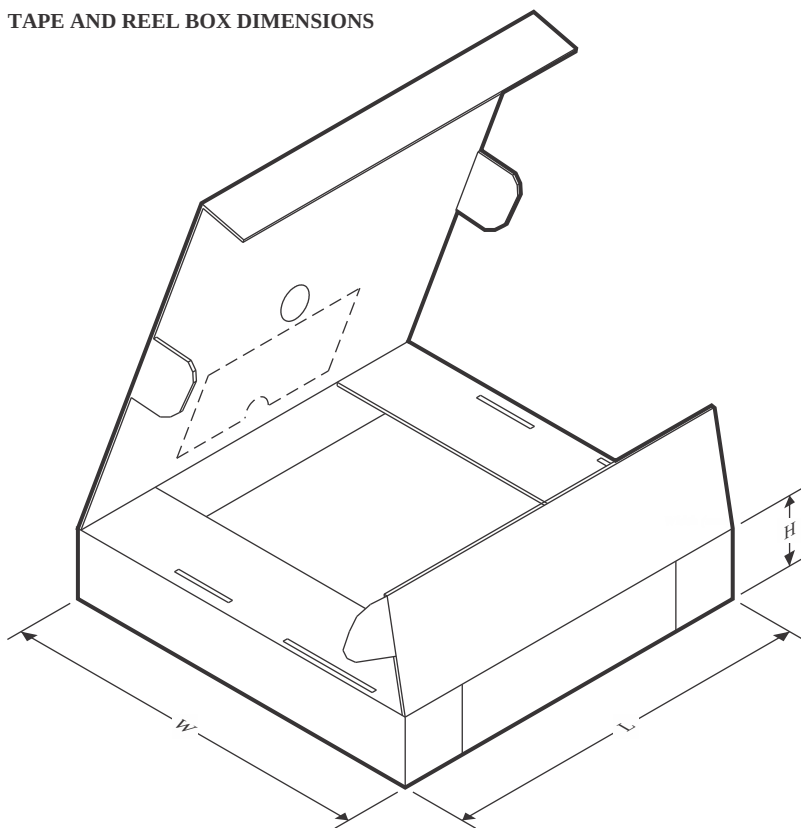
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC6946DBQR | SSOP         | DBQ             | 24   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLC6946RGER | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TLC6948DBQR | SSOP         | DBQ             | 24   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLC6948RGER | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

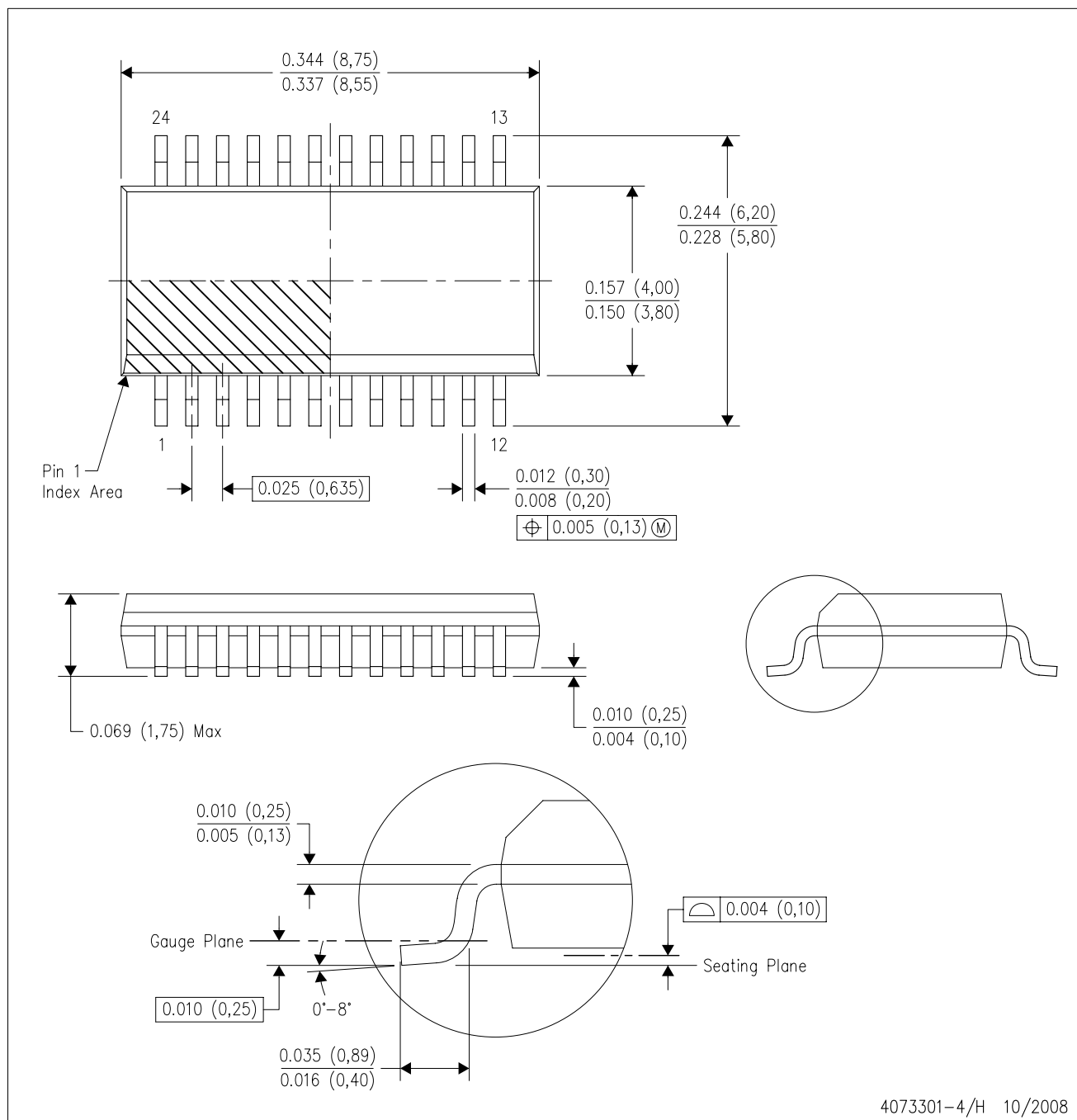


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC6946DBQR | SSOP         | DBQ             | 24   | 2500 | 353.0       | 353.0      | 32.0        |
| TLC6946RGER | VQFN         | RGE             | 24   | 3000 | 360.0       | 360.0      | 36.0        |
| TLC6948DBQR | SSOP         | DBQ             | 24   | 2500 | 353.0       | 353.0      | 32.0        |
| TLC6948RGER | VQFN         | RGE             | 24   | 3000 | 360.0       | 360.0      | 36.0        |

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



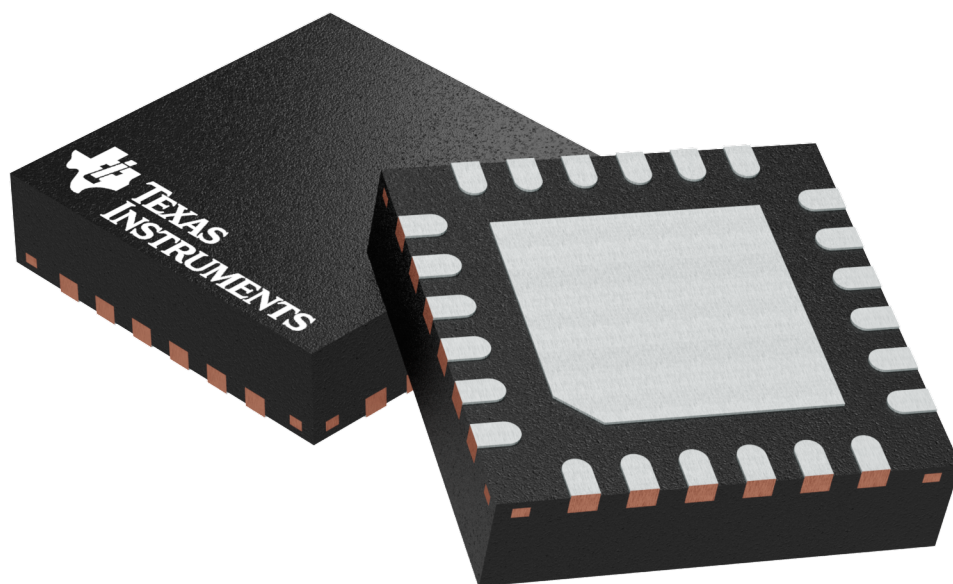
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AE.

**RGE 24**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H

**VQFN - 1 mm max height**

**Top View:**

- Overall width: 4.1 (3.9)
- Overall height: 4.1 (3.9)
- PIN 1 INDEX AREA (hatched square)
- Feature B (top left corner)
- Feature A (top right corner)

**Side View:**

- Height: 1 MAX
- Seating Plane (indicated by a triangle)
- Feature C (top right corner)
- Radius: 0.05 (0.00)
- Radius: 0.08 (C)

**End View:**

- Width: 24
- Pin pitch: 2.5 (2X)
- Pin 1 ID (OPTIONAL)
- Pin 19 (bottom center)
- Pin 13 (right center)
- Pin 25 (center)
- Pin 7 (top left)
- Pin 12 (top right)
- Pin 24 (bottom left)
- Pin 18 (bottom right)
- Pin 6 (top left)
- Pin 1 (bottom left)
- Pin 2 (bottom left)
- Pin 3 (bottom left)
- Pin 4 (bottom left)
- Pin 5 (bottom left)
- Pin 16 (bottom right)
- Pin 17 (bottom right)
- Pin 20 (bottom right)
- Pin 21 (bottom right)
- Pin 22 (bottom right)
- Pin 23 (bottom right)

**Dimensions and Tolerances:**

- 2.7 ± 0.1
- 2X 2.5
- 20X 0.5
- 2X 2.5
- 24X 0.30 / 0.18
- 24X 0.48 / 0.28
- 0.1 (M) C A B
- 0.05 (M) C
- (0.2) TYP

**Feature Callouts:**

- PIN 1 INDEX AREA
- PIN 1 ID (OPTIONAL)
- SEATING PLANE
- SYMM

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**VQFN - 1 mm max height**

Mechanical drawing of a 19-pin connector. The drawing shows a central rectangular area with a dashed line indicating symmetry (SYMM). Dimensions include:
 

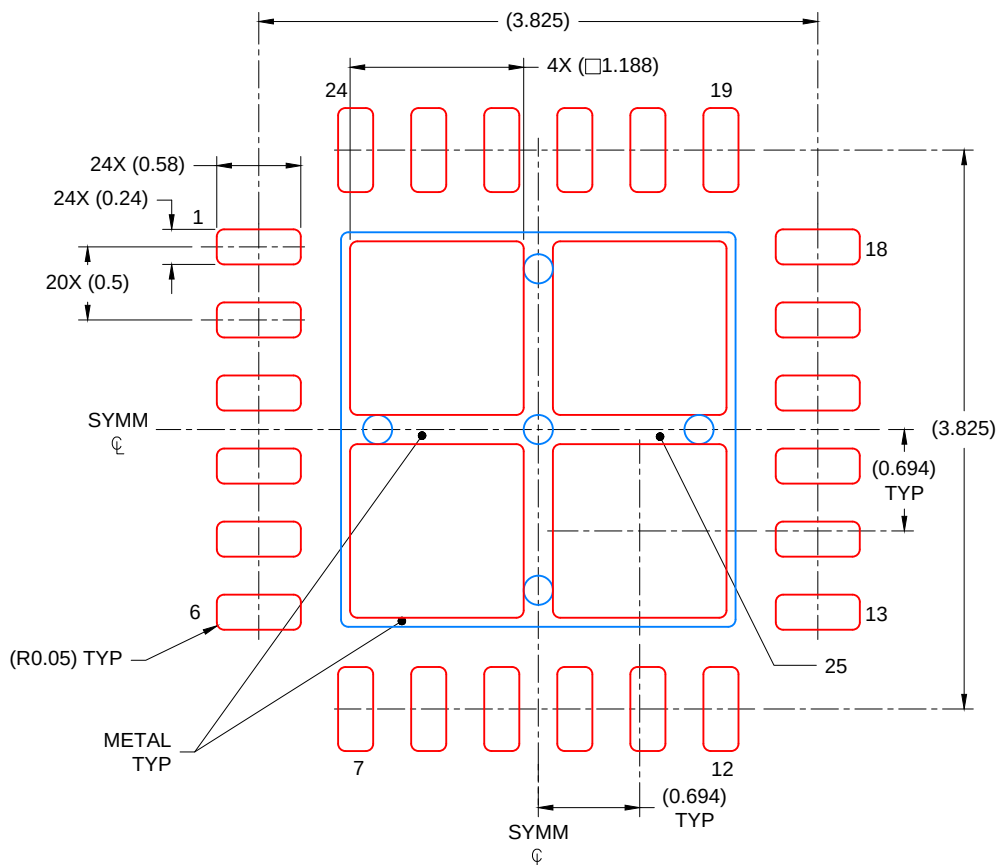
- Overall width: (3.825)
- Pin pitch: (2.7)
- Pin diameter: 24
- Pin spacing: 19
- Pin diameter: 18
- Pin diameter: 13
- Pin diameter: 7
- Pin diameter: 12
- Pin diameter: 25
- Pin diameter: 6
- Pin diameter: 1
- Pin diameter: 20X (0.5)
- Pin diameter: 24X (0.58)
- Pin diameter: 24X (0.24)
- Pin diameter: 2X (1.1)
- Pin diameter: (R0.05)
- Pin diameter: (Ø0.2) VIA TYP
- Pin diameter: SYMM
- Pin diameter: SYMM

The diagram illustrates two types of solder mask openings on a metal pad:

- NON SOLDER MASK DEFINED (PREFERRED):** This type shows a metal pad with a solder mask opening. The dimensions are specified as 0.07 MAX ALL AROUND. The labels include METAL, SOLDER MASK OPENING, and a dimension line indicating the maximum width of the opening.
- SOLDER MASK DEFINED:** This type shows a metal pad with a solder mask opening. The dimensions are specified as 0.07 MIN ALL AROUND. The labels include SOLDER MASK OPENING, METAL UNDER SOLDER MASK, and a dimension line indicating the minimum width of the opening.

**SOLDER MASK DETAILS**

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 78% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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最后更新日期：2025 年 10 月