# TCA6408A-Q1 具有中断输出的低电压 8 位 I²C 和 SMBus I/O 扩展器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C 至 +125°C，$T_A$
- 功能安全型
  - 可提供用于功能安全系统设计的文档
- I²C 至并行端口扩展器
- 工作电源电压范围为 1.65 V 至 3.6 V
- 支持 1.8V、2.5V、3.3V I²C 总线和 P 端口之间进行双向电平转换和 GPIO 扩展
- 低待机电流消耗
- 400kHz 快速 I²C 总线
- 硬件地址引脚，允许在同一 I²C/SMBus 总线上支持两个 TCA6408A-Q1 器件
- 低电平有效复位 ($\overline{RESET}$) 输入
- 开漏低电平有效中断 ($\overline{INT}$) 输出
- 输入和输出配置寄存器
- 极性反转寄存器
- 内部上电复位
- 加电时所有通道均被配置为输入
- 加电时无干扰
- SCL 和 SDA 输入端装有噪声滤波器
- 具有最大高电流驱动能力的锁存输出，适用于直接驱动 LED
- 锁断性能达 100mA，符合 AEC Q100-004
- 施密特触发操作支持在 SCL 和 SDA 输入端实现缓慢输入转换并提升开关噪声抗扰度
- ESD 保护
  - 2000V 人体放电模型 (Q100-002)
  - 1000V 带电器件模型 (Q100-011)

## 2 应用

- 汽车信息娱乐系统
- 高级驾驶员辅助系统 (ADAS)
- 汽车车身电子设备
- HEV、EV 和动力总成
- 工业、工厂和楼宇自动化
- 测试与测量
- EPOS

## 3 说明

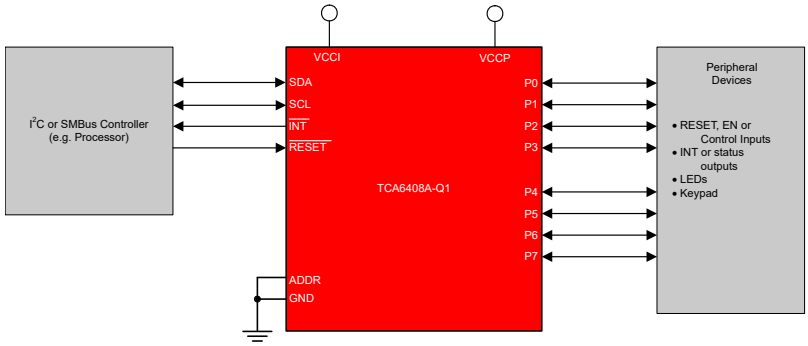
TCA6408A-Q1 是一款 16 引脚器件，可为两线双向 I²C 总线（或 SMBus）协议提供 8 位通用并行输入/输出 (I/O) 扩展。在器件运行过程中，I²C 总线侧 ($V_{CCI}$) 和 P 端口侧 ($V_{CCP}$) 均可由电压介于 1.65V 至 3.6V 之间的电源供电。这使得 TCA6408A-Q1 能够在 SDA/SCL 侧（电源电平在此逐渐降低以节省功率）与下一代微处理器和微控制器相连。与微处理器和微控制器的降压电源相比，部分 PCB 组件（例如 LED）仍由高电压电源供电。

该器件支持 100kHz（标准模式）和 400kHz（快速模式）时钟频率。当开关、传感器、按钮、LED、风扇等设备需要额外使用 I/O 时，I/O 扩展器（如 TCA6408A-Q1）可提供简易解决方案。

**封装信息**

| 器件型号 | 封装(1) | 封装尺寸（标称值） |
|---|---|---|
| TCA6408A-Q1 | TSSOP (16) | 5.00mm × 4.40mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




简化版原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

# Table of Contents

**1 特性** ... 1
**2 应用** ... 1
**3 说明** ... 1
**4 Revision History** ... 2
**5 Pin Configuration and Functions** ... 3
**6 Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 I²C Interface Timing Requirements ... 6
6.7 Reset Timing Requirements ... 7
6.8 Switching Characteristics ... 8
6.9 Typical Characteristics ... 9
**7 Parameter Measurement Information** ... 12
**8 Detailed Description** ... 16
8.1 Overview ... 16
8.2 Functional Block Diagrams ... 17
8.3 Feature Description ... 19
8.4 Device Functional Modes ... 20
8.5 Programming ... 20
8.6 Register Map ... 24
**9 Application and Implementation** ... 26
9.1 Application Information ... 26
9.2 Typical Application ... 27
9.3 Power Supply Recommendations ... 30
9.4 Layout ... 31
**10 Device and Documentation Support** ... 33
10.1 Receiving Notification of Documentation Updates ... 33
10.2 商标 ... 33
10.3 静电放电警告 ... 33
10.4 术语表 ... 33
**11 支持资源** ... 33
**12 Mechanical, Packaging, and Orderable Information** ... 33

## 4 Revision History

| Changes from Revision * (September 2016) to Revision A (February 2023) | Page |
|---|---|
| • 将提到 I²C 的旧术语实例通篇更改为控制器和目标 | 1 |
| • 添加了特性：符合面向汽车应用的 AEC-Q100 标准 | 1 |
| • Added the HBM and CDM ESD classification levels | 4 |
| • Added paragraph: "Ramping up the device $V_{CCP}$" to *Power-On Reset Requirements* | 30 |


Copyright © 2023 Texas Instruments Incorporated

# 5 Pin Configuration and Functions

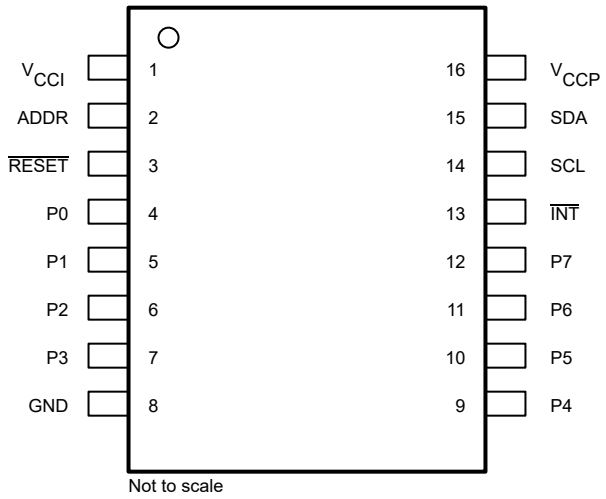



**图 5-1. PW Package, 16-Pin TSSOP (Top View)**

**表 5-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ADDR | 2 | I | Address input. Connect directly to $V_{CCP}$ or ground |
| GND | 8 | — | Ground |
| $\overline{INT}$ | 13 | O | Interrupt output. Connect to $V_{CCI}$ through a pull-up resistor |
| P0 | 4 | I/O | P-port input-output (push-pull design structure). At power on, P0 is configured as an input |
| P1 | 5 | I/O | P-port input-output (push-pull design structure). At power on, P1 is configured as an input |
| P2 | 6 | I/O | P-port input-output (push-pull design structure). At power on, P2 is configured as an input |
| P3 | 7 | I/O | P-port input-output (push-pull design structure). At power on, P3 is configured as an input |
| P4 | 9 | I/O | P-port input-output (push-pull design structure). At power on, P4 is configured as an input |
| P5 | 10 | I/O | P-port input-output (push-pull design structure). At power on, P5 is configured as an input |
| P6 | 11 | I/O | P-port input-output (push-pull design structure). At power on, P6 is configured as an input |
| P7 | 12 | I/O | P-port input-output (push-pull design structure). At power on, P7 is configured as an input |
| $\overline{RESET}$ | 3 | I | Active-low reset input. Connect to $V_{CCI}$ through a pull-up resistor, if no active connection is used |
| SCL | 14 | I | Serial clock bus. Connect to $V_{CCI}$ through a pull-up resistor |
| SDA | 15 | I/O | Serial data bus. Connect to $V_{CCI}$ through a pull-up resistor |
| $V_{CCI}$ | 1 | — | Supply voltage of $I^2C$ bus. Connect directly to the $V_{CC}$ of the external $I^2C$ controller. Provides voltage level translation |
| $V_{CCP}$ | 16 | — | Supply voltage of TCA6408A-Q1 for P-ports |

Copyright © 2023 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (see (1))

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCI}$ | Supply voltage for $I^2C$ pins | | | –0.5 | 3.6 | V |
| $V_{CCP}$ | Supply voltage for P-ports | | | –0.5 | 3.6 | V |
| $V_I$ | Input voltage(2) | | | –0.5 | 3.6 | V |
| $V_O$ | Output voltage(2) | | | –0.5 | 3.6 | V |
| $I_{IK}$ | Input clamp current | ADDR, $\overline{RESET}$, SCL | $V_I$ < 0 | | ±20 | mA |
| $I_{OK}$ | Output clamp current | $\overline{INT}$ | $V_O$ < 0 | | ±20 | mA |
| $I_{IOK}$ | Input/output clamp current | P-port | $V_O$ < 0 or $V_O$ > $V_{CCP}$ | | ±20 | mA |
| | | SDA | $V_O$ < 0 or $V_O$ > $V_{CCI}$ | | ±20 | |
| $I_{OL}$ | Continuous output low current | P-port | $V_O$ = 0 to $V_{CCP}$ | | 50 | mA |
| | Continuous output low current | SDA, $\overline{INT}$ | $V_O$ = 0 to $V_{CCI}$ | | 25 | |
| $I_{OH}$ | Continuous output high current | P-port | $V_O$ = 0 to $V_{CCP}$ | | 50 | mA |
| $I_{CC}$ | Continuous current through GND | | | | 200 | mA |
| | Continuous current through $V_{CCP}$ | | | | 160 | |
| | Continuous current through $V_{CCI}$ | | | | 10 | |
| $T_{j(MAX)}$ | Maximum junction temperature | | | | 135 | °C |
| $T_{stg}$ | Storage temperature | | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1)<br>HBM ESD classification level 1C | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011<br>CDM ESD classification level C6 | ±1000 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCI}$ (1) | Supply voltage for $I^2C$ pins | SCL, SDA, $\overline{INT}$ | 1.65 | 3.6 | V |
| $V_{CCP}$ | Supply voltage for P-ports | P-ports, ADDR, $\overline{RESET}$ | 1.65 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | SCL, SDA | 0.7 × $V_{CCI}$ | $V_{CCI}$ | V |
| | | $\overline{RESET}$ | 0.7 × $V_{CCI}$ | 3.6 | |
| | | ADDR, P7 – P0 | 0.7 × $V_{CCP}$ | 3.6 | |
| $V_{IL}$ | Low-level input voltage | SCL, SDA, $\overline{RESET}$ | –0.5 | 0.3 × $V_{CCI}$ | V |
| | | ADDR, P7 – P0 | –0.5 | 0.3 × $V_{CCP}$ | |
| $I_{OH}$ | High-level output current | P00-P07 | | 10 | mA |


Copyright © 2023 Texas Instruments Incorporated

## 6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OL}$ (2) | Low-level output current | P00-P07 | $T_j$ = 65°C | | 25 | mA |
| | | | $T_j$ = 85°C | | 18 | |
| | | | $T_j$ = 105°C | | 9 | |
| | | | $T_j$ = 125°C | | 4.5 | |
| | | | $T_j$ = 135°C | | 3.5 | |
| | | $\overline{INT}$, SDA | $T_j$ = 85°C | | 6 | |
| | | | $T_j$ = 105°C | | 3 | |
| | | | $T_j$ = 125°C | | 1.8 | |
| | | | $T_j$ = 135°C | | 1.5 | |
| $T_A$ | Operating free-air temperature | | | – 40 | 125 | °C |

(1) For voltages applied above $V_{CCI}$, and increase in $I_{CC}$ will result.
(2) The values shown apply to specific junction temperature. See the 节 9.2.1.1 section on how to calculate the junction temperature.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TCA6408A-Q1 PW (TSSOP) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 122 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 56.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 67.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 10.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 66.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range, $V_{CCI}$ = 1.65 V to 3.6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CCP}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input diode clamp voltage | $I_I$ = – 18 mA | 1.65 V to 3.6 V | – 1.2 | | | V |
| $V_{PORR}$ | Power-on reset voltage, $V_{CCP}$ rising(2) | $V_I$ = $V_{CCP}$ or GND, $I_O$ = 0 | 1.65 V to 3.6 V | | 1.2 | 1.5 | V |
| $V_{PORF}$ | Power-on reset voltage, $V_{CCP}$ falling(2) | $V_I$ = $V_{CCP}$ or GND, $I_O$ = 0 | 1.65 V to 3.6 V | 0.6 | 1 | | V |
| $V_{OH}$ | P-port high-level output voltage | $I_{OH}$ = – 8 mA | 1.65 V | 1.2 | | | V |
| | | | 2.3 V | 1.8 | | | |
| | | | 3 V | 2.6 | | | |
| | | | 3.6 V | 3.3 | | | |
| | | $I_{OH}$ = – 10 mA | 1.65 V | 1.0 | | | |
| | | | 2.3 V | 1.7 | | | |
| | | | 3 V | 2.5 | | | |
| | | | 3.6 V | 3.2 | | | |

Copyright © 2023 Texas Instruments Incorporated

## 6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range, $V_{CCI}$ = 1.65 V to 3.6 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | $V_{CCP}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | P-port low-level output voltage | | $I_{OL}$ = 8 mA | 1.65 V | | | 0.45 | V |
| | | | | 2.3 V | | | 0.25 | |
| | | | | 3 V | | | 0.25 | |
| | | | | 3.6 V | | | 0.23 | |
| | | | $I_{OL}$ = 10 mA | 1.65 V | | | 0.6 | |
| | | | | 2.3 V | | | 0.3 | |
| | | | | 3 V | | | 0.25 | |
| | | | | 3.6 V | | | 0.23 | |
| $I_{OL}$ | SDA | | $V_{OL}$ = 0.4 V | 1.65 V to 3.6 V | 3 | | | mA |
| | $\overline{INT}$ | | | | 3 | 15 | | |
| $I_I$ | SCL, SDA, $\overline{RESET}$ | | $V_I = V_{CCI}$ or GND | 1.65 V to 3.6 V | | | ±0.1 | µA |
| | ADDR | | $V_I = V_{CCP}$ or GND | | | | ±0.1 | |
| $I_{IH}$ | P-port | | $V_I = V_{CCP}$ | 1.65 V to 3.6 V | | | 1 | µA |
| $I_{IL}$ | P-port | | $V_I$ = GND | 1.65 V to 3.6 V | | | 1 | µA |
| $I_{CC}$ ($I_{CCI}$ + $I_{CCP}$) | Operating mode | SDA, P-port, ADDR, $\overline{RESET}$ | $V_I = V_{CC}$ or GND, I/O = inputs, $f_{SCL}$ = 400 kHz, No load | 2.3 V to 3.6 V | | 9 | 36 | µA |
| | | | | 1.65 V to 2.3 V | | 5 | 33 | |
| | Standby mode | SCL, SDA, P-port, ADDR, $\overline{RESET}$ | $V_I = V_{CC}$ or GND, I/O = inputs, $f_{SCL}$ = 0 kHz, No load | 2.3 V to 3.6 V | | 1.2 | 10 | |
| | | | | 1.65 V to 2.3 V | | 0.6 | 7 | |
| $\Delta I_{CCI}$ | Additional current in standby mode | SCL, SDA | One input at $V_{CCI}$ – 0.6 V, Other inputs at $V_{CCI}$ or GND | 1.65 V to 3.6 V | | 6 | 10 | µA |
| | | $\overline{RESET}$ | $\overline{RESET}$ at $V_{CCI}$ – 0.6 V, Other inputs at $V_{CCI}$ or GND | | | 6 | 55 | |
| $\Delta I_{CCP}$ | | P-port, ADDR | One input at $V_{CCP}$ – 0.6 V, Other inputs at $V_{CCP}$ or GND | 1.65 V to 3.6 V | | 6 | 80 | µA |
| $C_i$ | SCL | | $V_I = V_{CCI}$ or GND | 1.65 V to 3.6 V | | 7 | 9 | pF |
| $C_{io}$ | SDA | | $V_{IO} = V_{CCI}$ or GND | 1.65 V to 3.6 V | | 8 | 10.5 | pF |
| | P-port | | $V_{IO} = V_{CCP}$ or GND | | | 7 | 8 | |

(1) All typical values are at nominal supply voltage (1.8-V, 2.5-V, or 3.3-V $V_{CC}$) and $T_A$ = 25°C.
(2) When power (from 0 V) is applied to $V_{CCP}$, an internal power-on reset holds the TCA6408A-Q1 in a reset condition until $V_{CCP}$ has reached $V_{PORR}$. At that time, the reset condition is released, and the TCA6408A-Q1 registers and I²C/SMBus state machine initialize to their default states. After that, $V_{CCP}$ must be lowered to below $V_{PORF}$ and back up to the operating voltage for a power-reset cycle.

## 6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **I²C BUS—STANDARD MODE** | | | | |
| $f_{scl}$ | I²C clock frequency | 0 | 100 | kHz |
| $t_{sch}$ | I²C clock high time | 4 | | µs |
| $t_{scl}$ | I²C clock low time | 4.7 | | µs |
| $t_{sp}$ | I²C spike time | 0 | 50 | ns |
| $t_{sds}$ | I²C serial data setup time | 250 | | ns |
| $t_{sdh}$ | I²C serial data hold time | 0 | | ns |
| $t_{icr}$ | I²C input rise time | | 1000 | ns |


Copyright © 2023 Texas Instruments Incorporated

## 6.6 I²C Interface Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{icf}$ | I²C input fall time | | 300 | ns |
| $t_{ocf}$ | I²C output fall time, 10-pF to 400-pF bus | | 300 | ns |
| $t_{buf}$ | I²C bus free time between Stop and Start | 4.7 | | µs |
| $t_{sts}$ | I²C Start or repeater Start condition setup time | 4.7 | | µs |
| $t_{sth}$ | I²C Start or repeater Start condition hold time | 4 | | µs |
| $t_{sps}$ | I²C Stop condition setup time | 4 | | µs |
| $t_{vd(data)}$ | Valid data time, SCL low to SDA output valid | | 1 | µs |
| $t_{vd(ack)}$ | Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low | | 1 | µs |
| **I²C BUS—FAST MODE** | | | | |
| $f_{scl}$ | I²C clock frequency | 0 | 400 | kHz |
| $t_{sch}$ | I²C clock high time | 0.6 | | µs |
| $t_{scl}$ | I²C clock low time | 1.3 | | µs |
| $t_{sp}$ | I²C spike time | 0 | 50 | ns |
| $t_{sds}$ | I²C serial data setup time | 100 | | ns |
| $t_{sdh}$ | I²C serial data hold time | 0 | | ns |
| $t_{icr}$ | I²C input rise time | 20 | 300 | ns |
| $t_{icf}$ | I²C input fall time | 20 x (Vcc/ 5.5 V) | 300 | ns |
| $t_{ocf}$ | I²C output fall time, 10-pF to 400-pF bus | 20 x (Vcc/ 5.5 V) | 300 | ns |
| $t_{buf}$ | I²C bus free time between Stop and Start | 1.3 | | µs |
| $t_{sts}$ | I²C Start or repeater Start condition setup time | 0.6 | | µs |
| $t_{sth}$ | I²C Start or repeater Start condition hold time | 0.6 | | µs |
| $t_{sps}$ | I²C Stop condition setup time | 0.6 | | µs |
| $t_{vd(data)}$ | Valid data time, SCL low to SDA output valid | | 1 | µs |
| $t_{vd(ack)}$ | Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low | | 1 | µs |

## 6.7 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-4)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **I²C BUS—STANDARD and FAST MODE** | | | | |
| $t_W$ | Reset pulse duration | 40 | | ns |
| $t_{REC}$ | Reset recovery time | 0 | | ns |
| $t_{RESET}$ | Time to reset | 600 | | ns |

Copyright © 2023 Texas Instruments Incorporated

## 6.8 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see 图 7-1)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| **I²C BUS—STANDARD and FAST MODE** | | | | | | |
| $t_{iv}$ | Interrupt valid time | P-Port | $\overline{INT}$ | | 4 | μs |
| $t_{ir}$ | Interrupt reset delay time | SCL | $\overline{INT}$ | | 4 | μs |
| $t_{pv}$ | Output data valid | SCL | P7 – P0 | | 400 | ns |
| $t_{ps}$ | Input data setup time | P-Port | SCL | 0 | | ns |
| $t_{ph}$ | Input data hold time | P-Port | SCL | 300 | | ns |


Copyright © 2023 Texas Instruments Incorporated

## 6.9 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

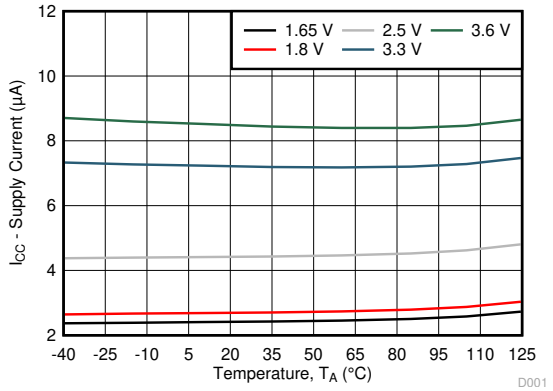



图 6-1. Supply Current vs Temperature

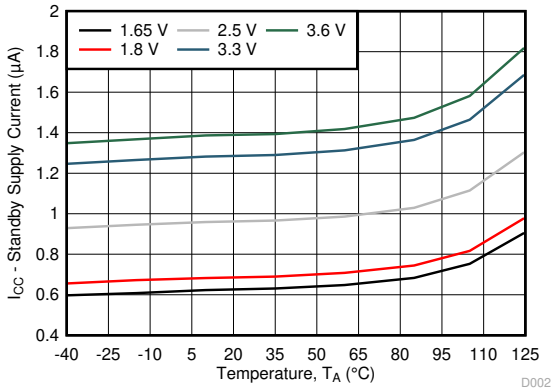



图 6-2. Standby Supply Current vs Temperature

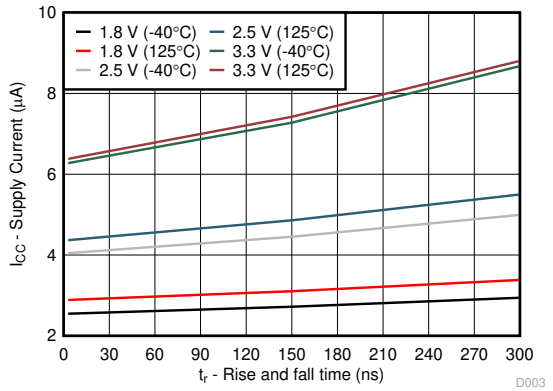



图 6-3. Supply Current vs Rise and Fall Times ($t_r$)

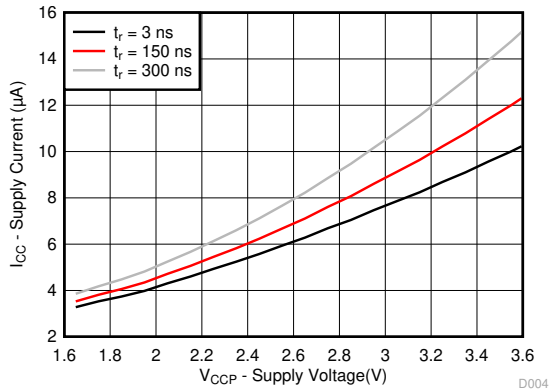



图 6-4. Supply Current vs Supply Voltage

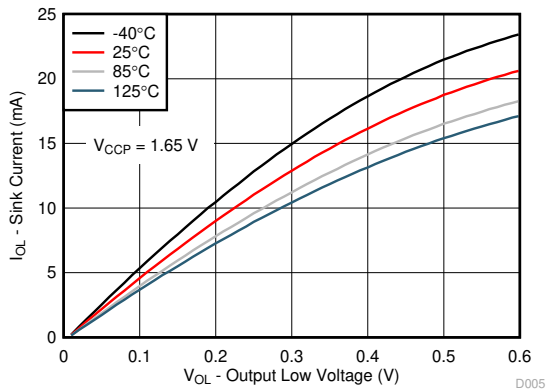



图 6-5. I/O Sink Current vs Output Low Voltage ($V_{CCP}$ = 1.65 V)

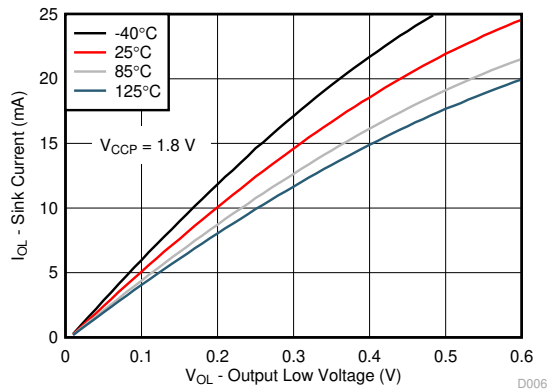



图 6-6. I/O Sink Current vs Output Low Voltage ($V_{CCP}$ = 1.8 V)

Copyright © 2023 Texas Instruments Incorporated

## 6.9 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

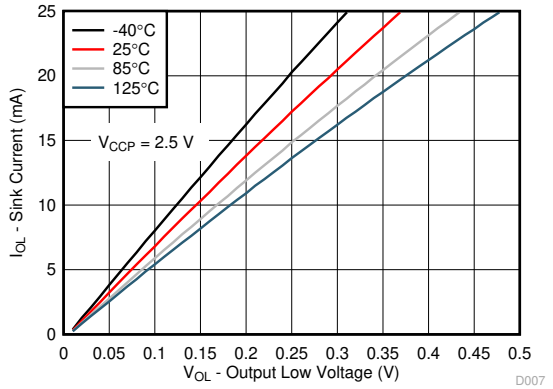



图 6-7. I/O Sink Current vs Output Low Voltage ($V_{CCP}$ = 2.5 V)

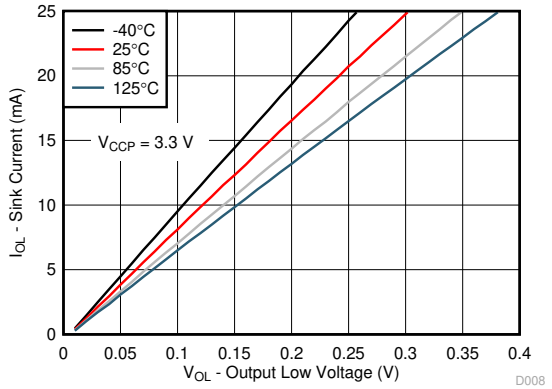



图 6-8. I/O Sink Current vs Output Low Voltage ($V_{CCP}$ = 3.3 V)

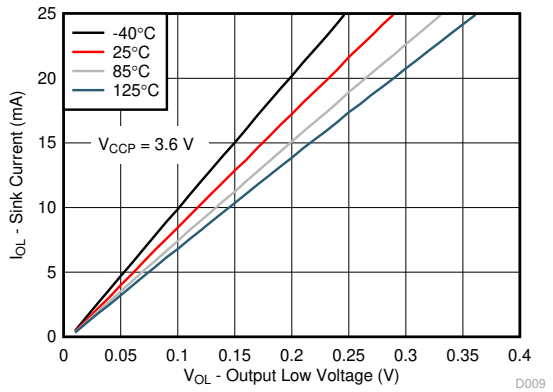



图 6-9. I/O Sink Current vs Temperature ($V_{CCP}$ = 3.6 V)

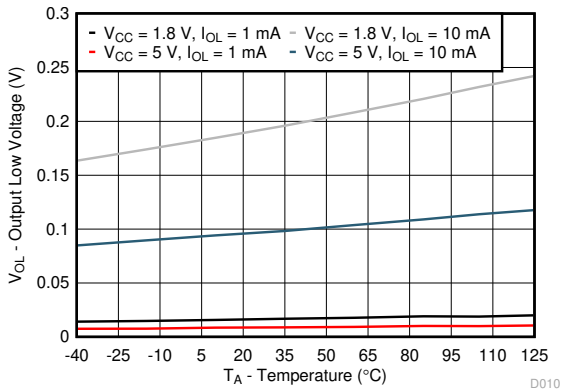



图 6-10. I/O Low Voltage vs Temperature

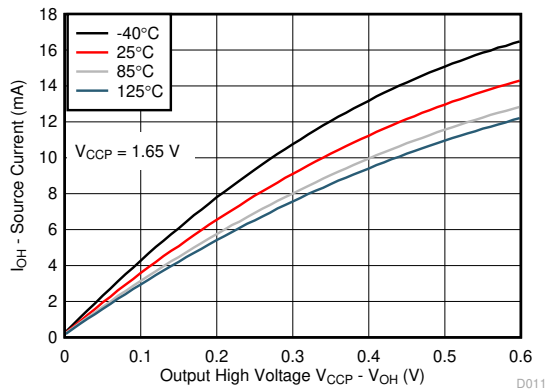



图 6-11. I/O Source Current vs Output High Voltage ($V_{CCP}$ = 1.65 V)

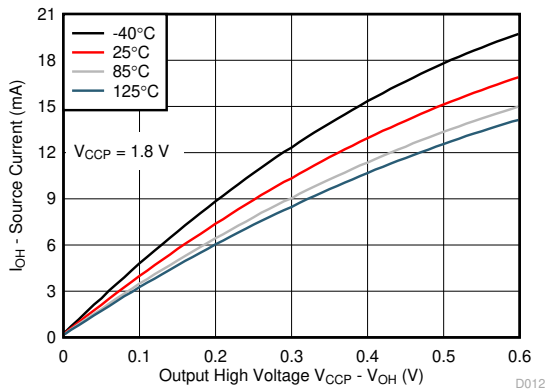



图 6-12. I/O Source Current vs Output High Voltage ($V_{CCP}$ = 1.8 V)


Copyright © 2023 Texas Instruments Incorporated

## 6.9 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

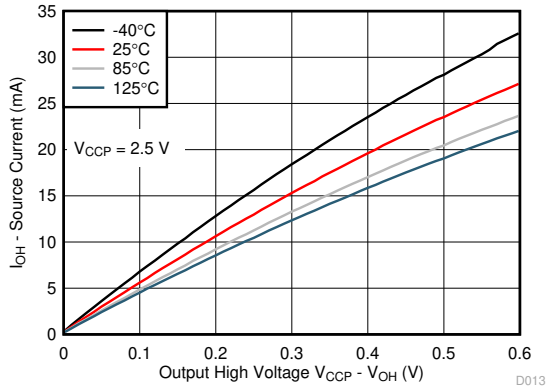



图 6-13. I/O Source Current vs Output High Voltage ($V_{CCP}$ = 2.5 V)

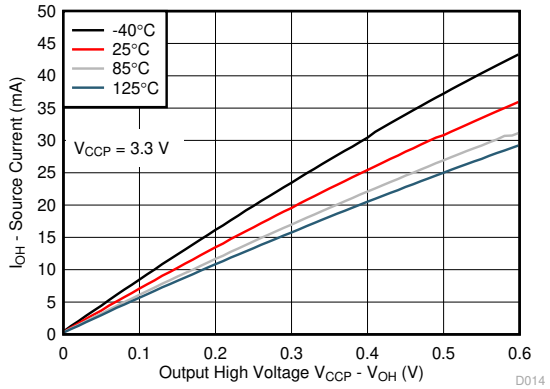



图 6-14. I/O Source Current vs Output High Voltage ($V_{CCP}$ = 3.3 V)

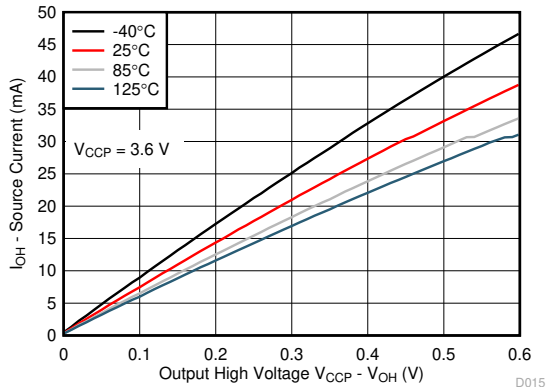



图 6-15. I/O Source Current vs Output High Voltage ($V_{CCP}$ = 3.6 V)

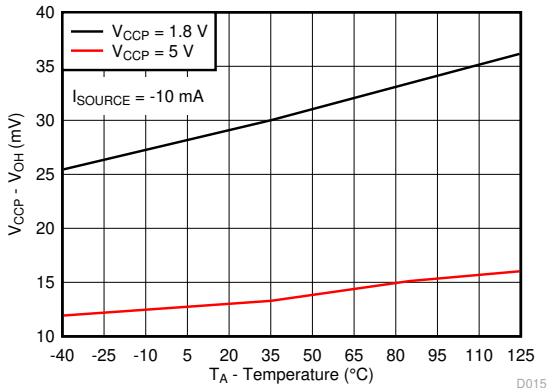
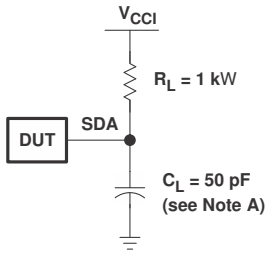
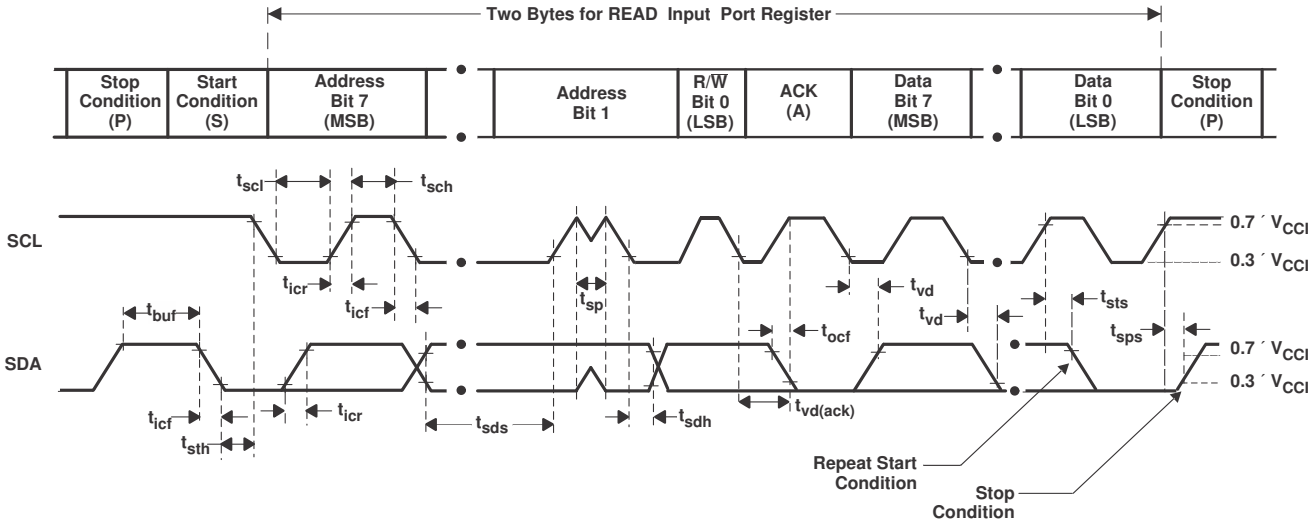



图 6-16. I/O High Voltage vs Temperature

# 7 Parameter Measurement Information




SDA LOAD CONFIGURATION




VOLTAGE WAVEFORMS

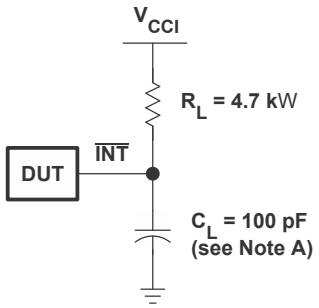
| BYTE | DESCRIPTION |
|---|---|
| 1 | $I^2C$ address |
| 2 | Input register port data |

A. $C_L$ includes probe and jig capacitance. $t_{ocf}$ is measured with $C_L$ of 10 pF or 400 pF.

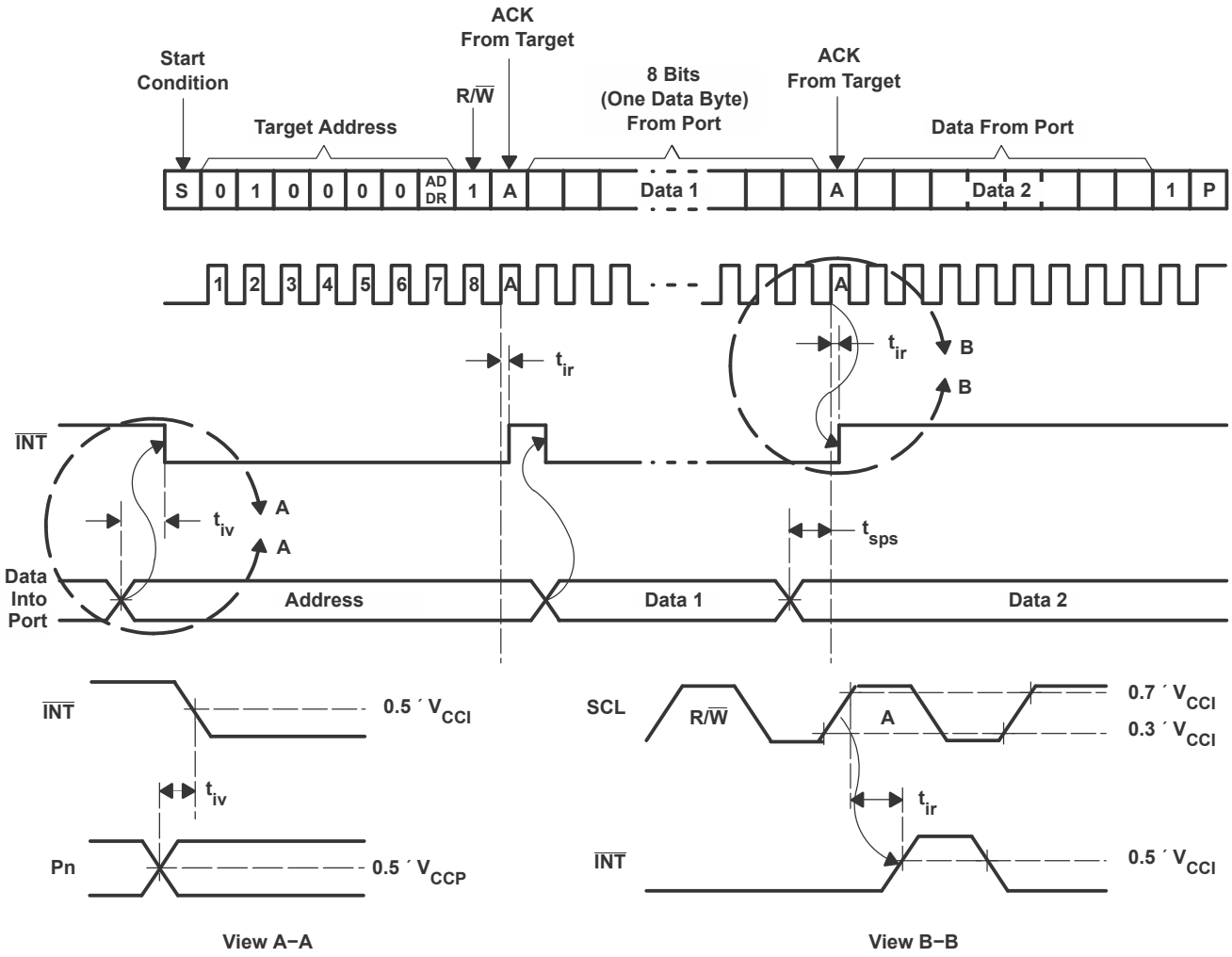
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ ≤ 30 ns.

**图 7-1. $I^2C$ Interface Load Circuit and Voltage Waveforms**


Copyright © 2023 Texas Instruments Incorporated




INTERRUPT LOAD CONFIGURATION



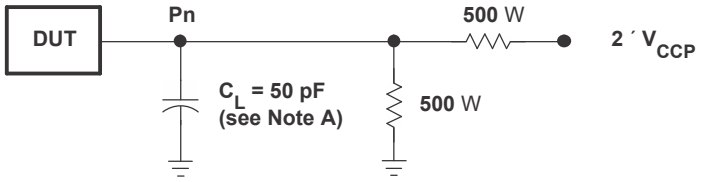

View A−A View B−B

A. $C_L$ includes probe and jig capacitance.

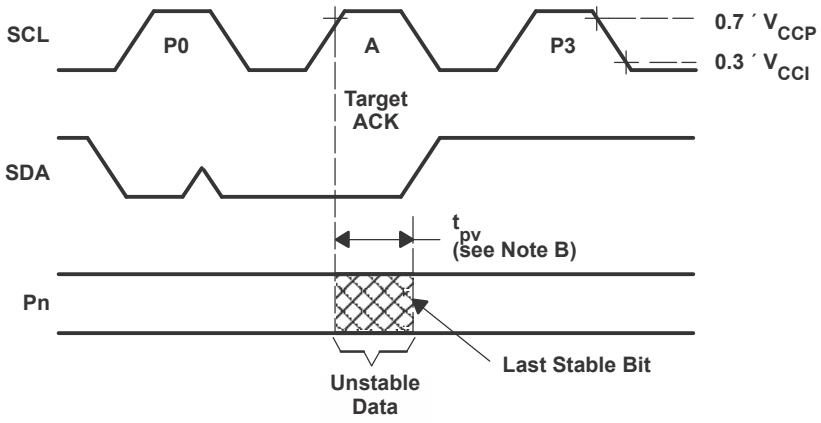
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ ≤ 30 ns.

**图 7-2. Interrupt Load Circuit and Voltage Waveforms**

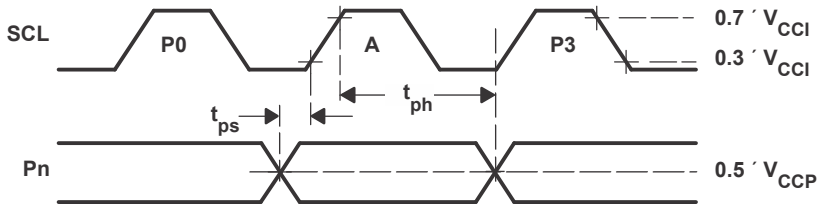
Copyright © 2023 Texas Instruments Incorporated




P-PORT LOAD CONFIGURATION




WRITE MODE (R/$\overline{W}$ = 0)

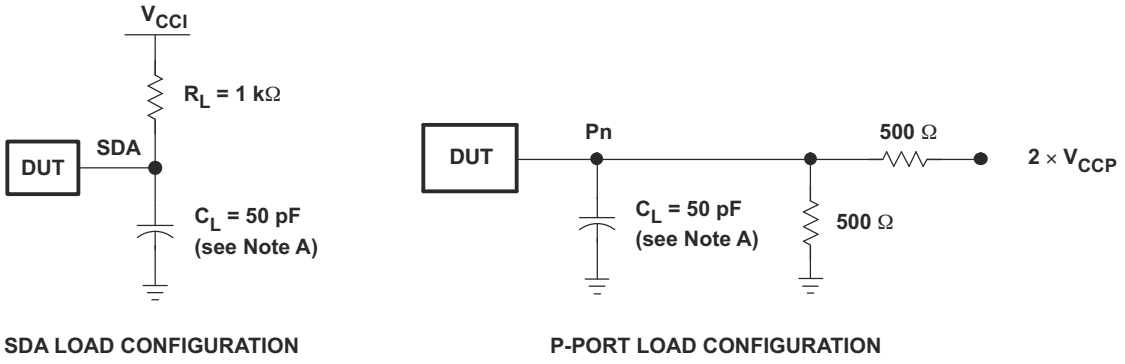



READ MODE (R/$\overline{W}$ = 1)

A. $C_L$ includes probe and jig capacitance.
B. $t_{pv}$ is measured from 0.7 × $V_{CC}$ on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ ⩽ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.

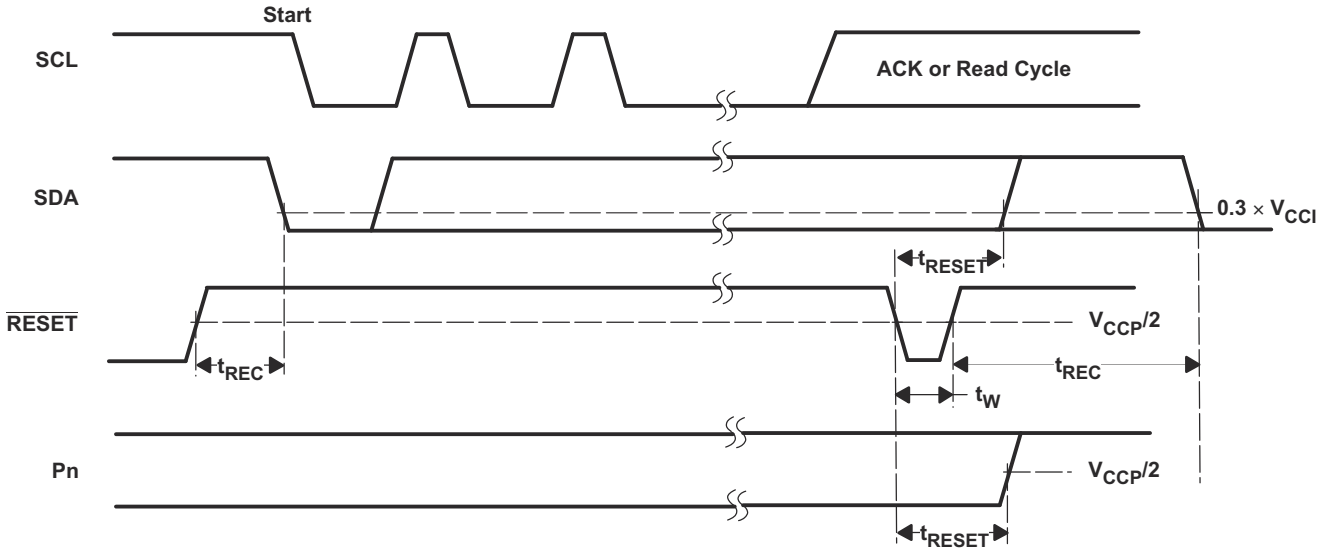
**图 7-3. P-Port Load Circuit and Timing Waveforms**


Copyright © 2023 Texas Instruments Incorporated




SDA LOAD CONFIGURATION

P-PORT LOAD CONFIGURATION




A. $C_L$ includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ ⩽ 30 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. I/Os are configured as inputs.

**图 7-4. Reset Load Circuits and Voltage Waveforms**

Copyright © 2023 Texas Instruments Incorporated

# 8 Detailed Description

## 8.1 Overview

The bidirectional voltage-level translation in the TCA6408A-Q1 is provided through $V_{CCI}$. $V_{CCI}$ must be connected to the $V_{CC}$ of the external SCL/SDA lines. This indicates the $V_{CC}$ level of the $I^2C$ bus to the TCA6408A-Q1. The voltage level on the P-port of the TCA6408A-Q1 is determined by $V_{CCP}$.

The TCA6408A-Q1 consists of one 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high) Register. At power on, the I/Os are configured as inputs. However, the system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output Register. The polarity of the Input Port Register can be inverted with the Polarity Inversion Register. All registers can be read by the system controller.

The system controller can reset the TCA6408A-Q1 in the event of a timeout or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the $I^2C$/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part.

The TCA6408A-Q1 open-drain interrupt ( $\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port Register state and is used to indicate to the system controller that an input state has changed.

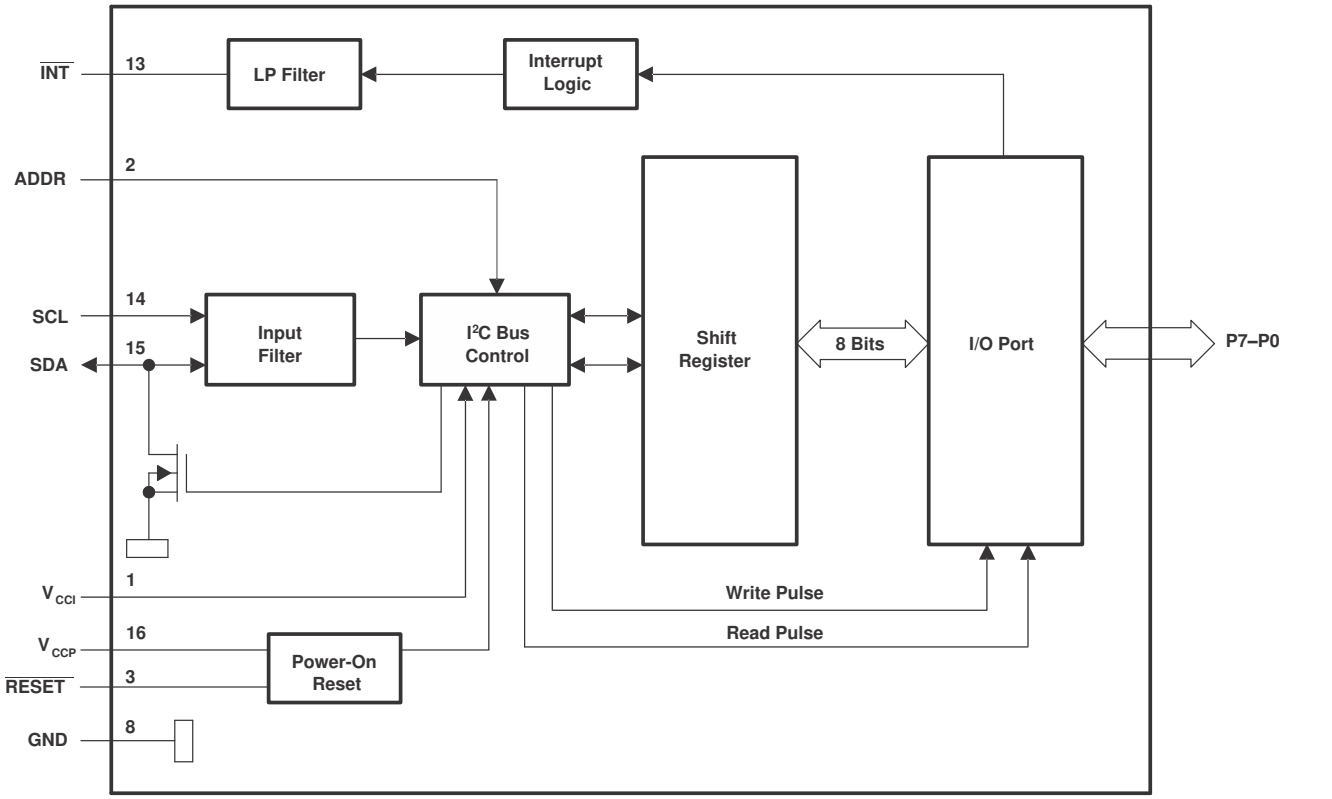
$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the $I^2C$ bus. Thus, the TCA6408A-Q1 can remain a simple target device.

The device P-port outputs have high-current sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed $I^2C$ address and allow up to two devices to share the same $I^2C$ bus or SMBus.


Copyright © 2023 Texas Instruments Incorporated

## 8.2 Functional Block Diagrams

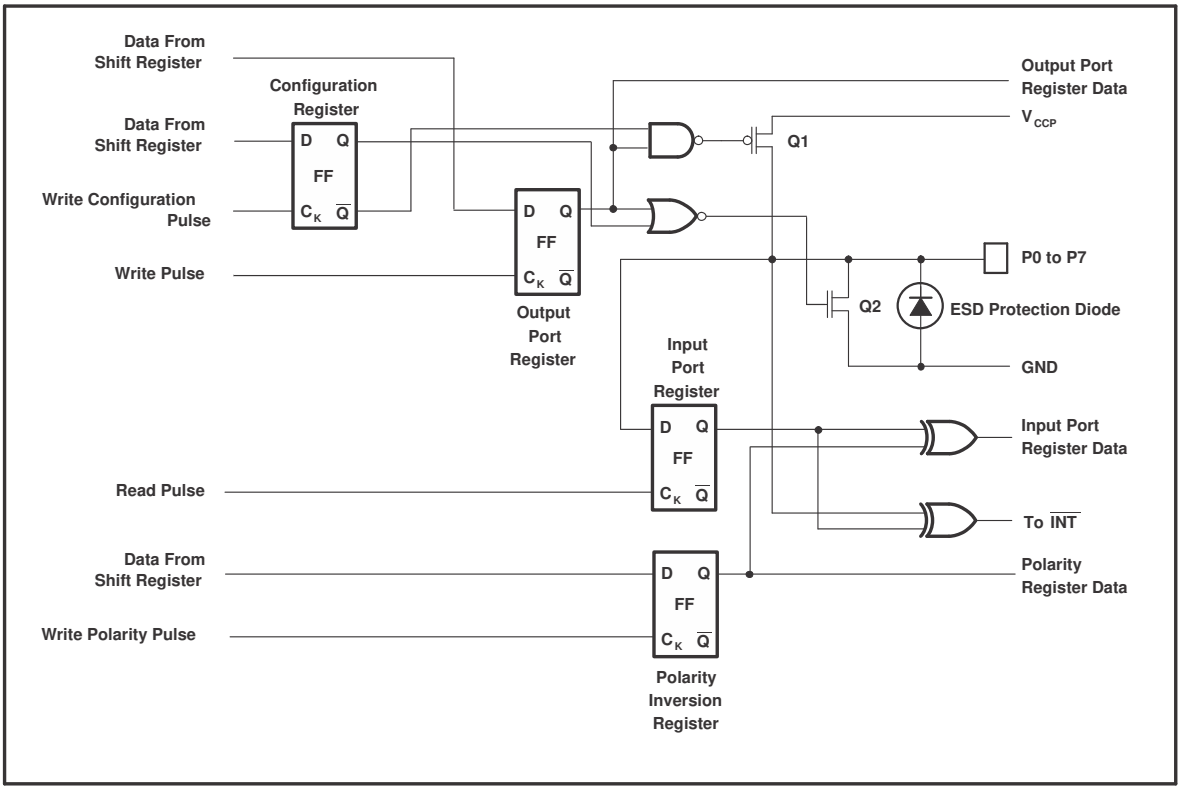



Copyright © 2016, Texas Instruments Incorporated

All pin numbers shown are for the PW package.

All I/Os are set to inputs at reset.

**图 8-1. Logic Diagram (Positive Logic)**




Copyright © 2016, Texas Instruments Incorporated

On power up or reset, all registers return to default values.

**图 8-2. Simplified Schematic of P0 to P7**


Copyright © 2023 Texas Instruments Incorporated

## 8.3 Feature Description

### 8.3.1 Voltage Translation

表 8-1 shows some common supply voltage options for voltage translation between the $I^2C$ bus and the P-ports of the TCA6408A-Q1.

**表 8-1. Voltage Translation**

| $V_{CCI}$ (SCL AND SDA OF $I^2C$ CONTROLLER) (V) | $V_{CCP}$ (P-PORT) (V) |
|---|---|
| 1.8 | 1.8 |
| 1.8 | 2.5 |
| 1.8 | 3.3 |
| 2.5 | 1.8 |
| 2.5 | 2.5 |
| 2.5 | 3.3 |
| 3.3 | 1.8 |
| 3.3 | 2.5 |
| 3.3 | 3.3 |

### 8.3.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above $V_{CC}$ to a maximum of 3.6 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either $V_{CC}$ or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

### 8.3.3 Interrupt Output ( $\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time $t_{iv}$, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to $V_{CCP}$ or $V_{CCI}$, depending on the application. $\overline{INT}$ must be connected to the voltage source of the device that requires the interrupt information.

### 8.3.4 Reset Input ( $\overline{RESET}$)

The $\overline{RESET}$ input can be asserted to initialize the system while keeping the $V_{CCP}$ at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin low for a minimum of $t_W$. The TCA6408A-Q1 registers and $I^2C$/SMBus state machine are changed to their default state when $\overline{RESET}$ is low (0). When $\overline{RESET}$ is high (1), the I/O levels at the P-port can be changed externally or through the controller. This input requires a pull-up resistor to $V_{CCI}$, if no active connection is used. It is not recommended to assert the $\overline{RESET}$ pin during communication with the TCA6408A-Q1. Assertion of $\overline{RESET}$ during communication can result in data corruption.

Copyright © 2023 Texas Instruments Incorporated

## 8.4 Device Functional Modes

### 8.4.1 Power-On Reset (POR)

When power (from 0 V) is applied to $V_{CCP}$, an internal power-on reset holds the TCA6408A-Q1 in a reset condition until $V_{CCP}$ has reached $V_{PORR}$. At that time, the reset condition is released, and the TCA6408A-Q1 registers and $I^2C$/SMBus state machine initialize to their default states. After that, $V_{CCP}$ must be lowered to below $V_{PORF}$ and back up to the operating voltage for a power-reset cycle.

### 8.4.2 Powered-Up

When power has been applied to both $V_{CCP}$ and $V_{CCI}$ and a POR has taken place, the device is in a functioning mode. The device is always ready to receive new requests via the $I^2C$ bus.

## 8.5 Programming

### 8.5.1 $I^2C$ Interface

The TCA6408A-Q1 has a standard bidirectional $I^2C$ interface that is controlled by a controller device in order to be configured or read the status of this device. Each target on the $I^2C$ bus has a specific device address to differentiate between other target devices that are on the same $I^2C$ bus. Many target devices require configuration upon startup to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.

The physical $I^2C$ interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to $V_{CC}$ through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the $I^2C$ lines. (For further details, see the application report, *$I^2C$ Pull-up Resistor Calculation* (SLVA689)). Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition. See 图 8-3 and 图 8-4.

The following is the general procedure for a controller to access a target device:

1. If a controller wants to send data to a target:
   - Controller-transmitter sends a START condition and addresses the target-receiver.
   - Controller-transmitter sends data to target-receiver.
   - Controller-transmitter terminates the transfer with a STOP condition.
2. If a controller wants to receive or read data from a target:
   - Controller-receiver sends a START condition and addresses the target-transmitter.
   - Controller-receiver sends the requested register to read to target-transmitter.
   - Controller-receiver receives data from the target-transmitter.
   - Controller-receiver terminates the transfer with a STOP condition.

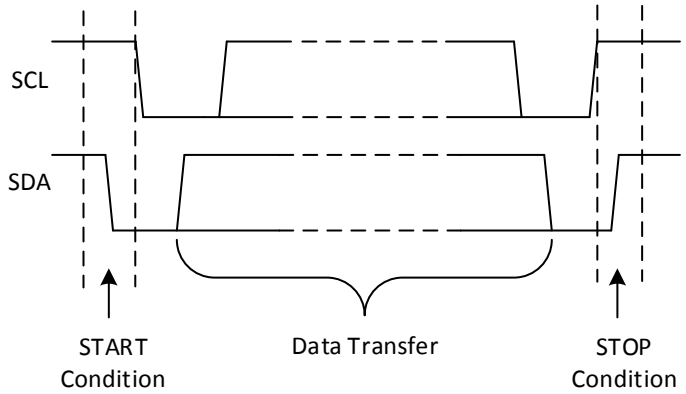



**图 8-3. Definition of Start and Stop Conditions**


Copyright © 2023 Texas Instruments Incorporated

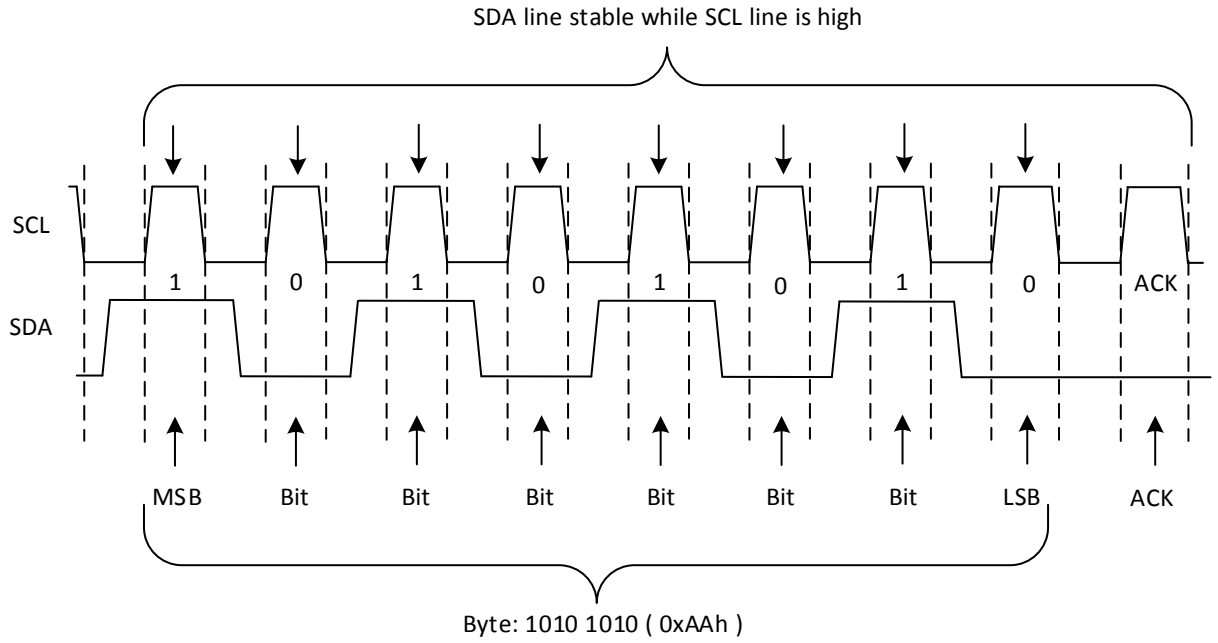



**图 8-4. Bit Transfer**

表 8-2 shows the interface definition for the TCA6408A-Q1 device.

**表 8-2. Interface Definition**

| BYTE | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
| $I^2C$ target address | L | H | L | L | L | L | ADDR | R/ $\overline{W}$ |
| I/O data bus | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

### 8.5.2 Bus Transactions

Data must be sent to and received from the target devices, and this is accomplished by reading from or writing to registers in the target device.

Registers are locations in the memory of the target which contain information, whether it be the configuration information or some sampled data to send back to the controller. The controller must write information to these registers in order to instruct the target device to perform a task.

While it is common to have registers in $I^2C$ targets, note that not all target devices will have registers. Some devices are simple and contain only 1 register, which may be written to directly by sending the register data immediately after the target address, instead of addressing a register. An example of a single-register device is an 8-bit $I^2C$ switch, which is controlled via $I^2C$ commands. Since it has 1 bit to enable or disable a channel, there is only 1 register needed, and the controller merely writes the register data after the target address, skipping the register number.

#### *8.5.2.1 Writes*

To write on the $I^2C$ bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/ $\overline{W}$ bit) set to 0, which signifies a write. After the target sends the acknowledge bit, the controller then sends the register address of the register to which it wishes to write. The target will acknowledge again, letting the controller know it is ready. After this, the controller starts sending the register data to the target until the controller has sent all the data necessary (which is sometimes only a single byte), and the controller terminates the transmission with a STOP condition.

图 8-5 and 图 8-6 show an example of writing a single byte to a target register.

Copyright © 2023 Texas Instruments Incorporated

Controller controls SDA line

Target controls SDA line

Write to one register in a device

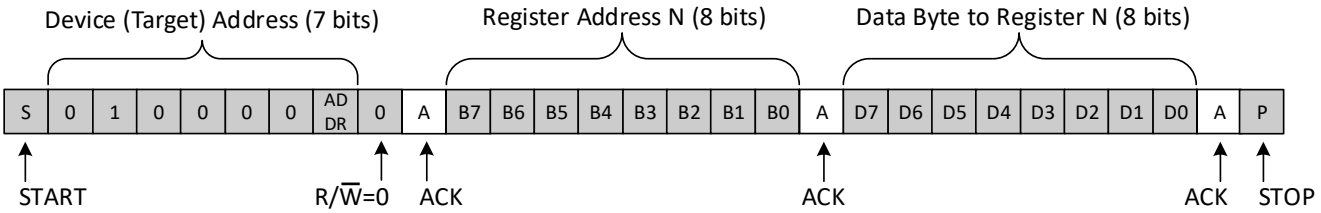



**图 8-5. Write to Register**

Controller controls SDA line

Target controls SDA line

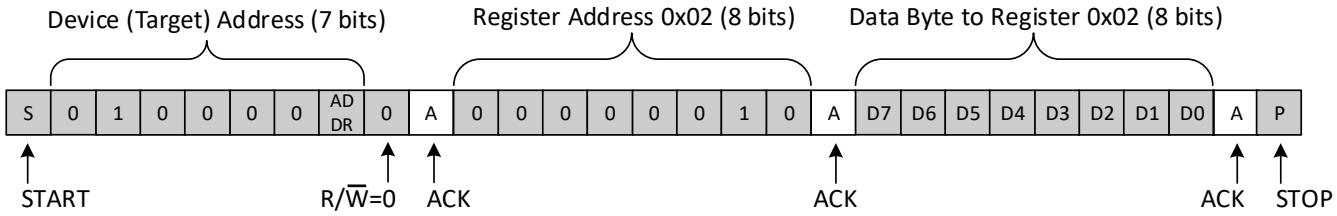



**图 8-6. Write to the Polarity Inversion Register**


Copyright © 2023 Texas Instruments Incorporated

### 8.5.2.2 Reads

Reading from a target is very similar to writing, but requires some additional steps. In order to read from a target, the controller must first instruct the target which register it wishes to read from. This is done by the controller starting off the transmission in a similar fashion as the write, by sending the address with the R/ $\overline{W}$ bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the target acknowledges this register address, the controller sends a START condition again, followed by the target address with the R/ $\overline{W}$ bit set to 1 (signifying a read). This time, the target acknowledges the read request, and the controller releases the SDA bus but continues supplying the clock to the target. During this part of the transaction, the controller becomes the controller-receiver, and the target becomes the target-transmitter.

The controller continues to send out the clock pulses, but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that it is ready for more data. When the controller has received the number of bytes it is expecting, it sends a NACK, signaling to the target to halt communications and release the bus. The controller follows this up with a STOP condition.

Read transactions that are performed without writing to the address of the device and simply supply the command byte will result in a NACK.

图 8-7 and 图 8-8 show an example of reading a single byte from a target register.

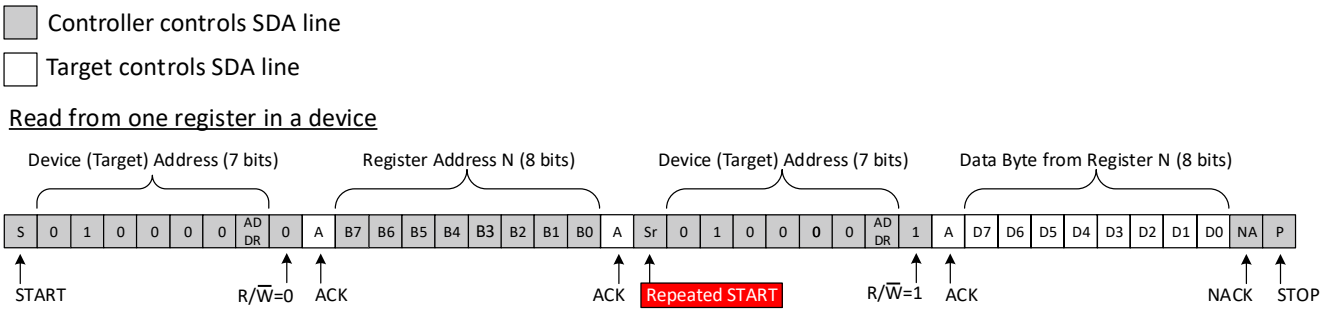
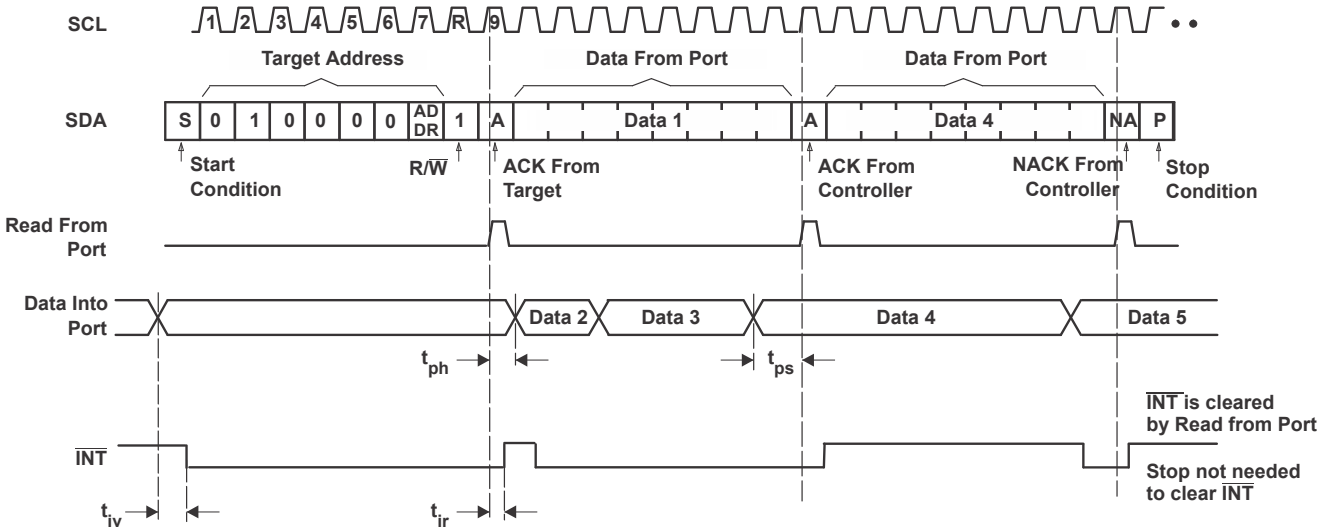



**图 8-7. Read from Register**




A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port Register).

B. This figure eliminates the command byte transfer, a restart, and target address call between the initial target address call and actual data transfer from P-port (see 图 8-7).

**图 8-8. Read from Input Port Register**

Copyright © 2023 Texas Instruments Incorporated

## 8.6 Register Map

### 8.6.1 Device Address

The address of the TCA6408A-Q1 is shown in 图 8-9.

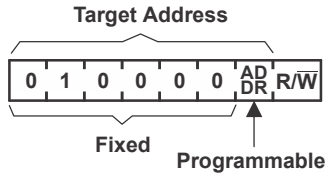



**图 8-9. TCA6408A-Q1 Address**

表 8-3 shows the TCA6408A-Q1 address reference.

**表 8-3. Address Reference**

| ADDR | I²C BUS TARGET ADDRESS |
|---|---|
| L | 32 (decimal), 20 (hexadecimal) |
| H | 33 (decimal), 21 (hexadecimal) |

The last bit of the target address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

### 8.6.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte (see 表 8-4), which is stored in the Control Register in the TCA6408A-Q1. Two bits of this data byte state both the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that is affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission. See 图 8-10.

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|

**图 8-10. Control Register Bits**

**表 8-4. Command Byte**

| CONTROL REGISTER BITS | | | | | | | | COMMAND BYTE (HEX) | REGISTER | PROTOCOL | POWER-UP DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | Input Port | Read byte | xxxx xxxx |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | Output Port | Read/write byte | 1111 1111 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 | Polarity Inversion | Read/write byte | 0000 0000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 | Configuration | Read/write byte | 1111 1111 |


Copyright © 2023 Texas Instruments Incorporated

### 8.6.3 Register Descriptions

The Input Port Register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. They act only on read operation. Writes to this register have no effect. The default value (X) is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the $I^2C$ device that the Input Port Register will be accessed next. See 表 8-5.

**表 8-5. Register 0 (Input Port Register)**

| BIT | I-7 | I-6 | I-5 | I-4 | I-3 | I-2 | I-1 | I-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | X | X | X | X | X | X | X | X |

The Output Port Register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration Register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See 表 8-6.

**表 8-6. Register 1 (Output Port Register)**

| BIT | O-7 | O-6 | O-5 | O-4 | O-3 | O-2 | O-1 | O-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The Polarity Inversion Register (register 2) allows polarity inversion of pins defined as inputs by the Configuration Register. If a bit in this register is set (written with 1), the polarity of the corresponding port pin is inverted. If a bit in this register is cleared (written with a 0), the original polarity of the corresponding port pin is retained. See 表 8-7.

**表 8-7. Register 2 (Polarity Inversion Register)**

| BIT | N-7 | N-6 | N-5 | N-4 | N-3 | N-2 | N-1 | N-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The Configuration Register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See 表 8-8.

**表 8-8. Register 3 (Configuration Register)**

| BIT | C-7 | C-6 | C-5 | C-4 | C-3 | C-2 | C-1 | C-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Copyright © 2023 Texas Instruments Incorporated

# 9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

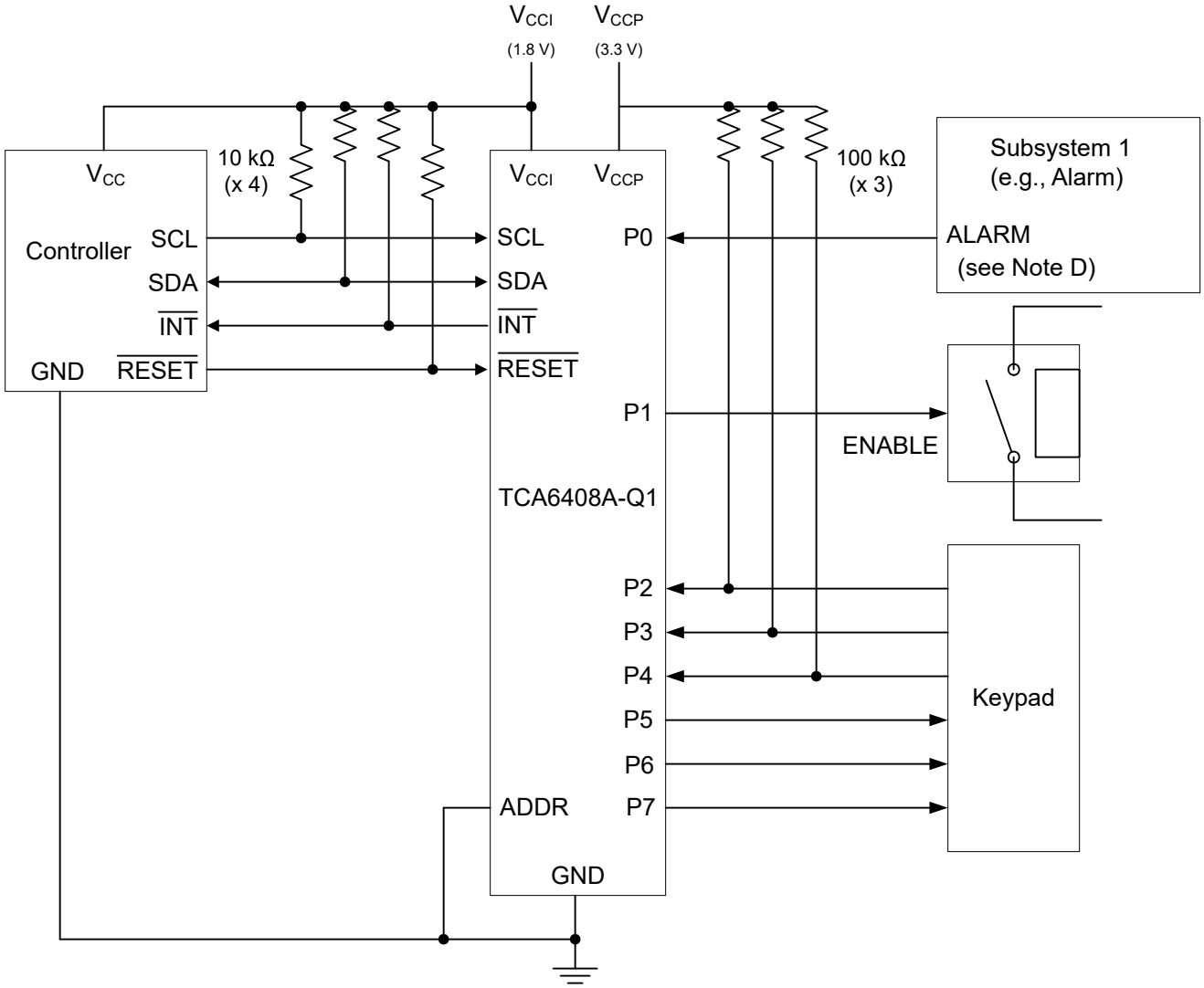
Applications of the TCA6408A-Q1 has this device connected as a target to an $I^2C$ controller (processor), and the $I^2C$ bus may contain any number of other target devices. The TCA6408A-Q1 is in a remote location from the controller, placed close to the GPIOs to which the controller needs to monitor or control.

A typical application of the TCA6408A-Q1 operates with a lower voltage on the controller side ($V_{CCI}$), and a higher voltage on the P-port side ($V_{CCP}$). The P-ports can be configured as outputs connected to inputs of devices such as enable, reset, power select, the gate of a switch, and LEDs. The P-ports can also be configured as inputs to receive data from interrupts, alarms, status outputs, or push buttons.


Copyright © 2023 Texas Instruments Incorporated

## 9.2 Typical Application

图 9-1 shows an application in which the TCA6408A-Q1 can be used.




A. Device address configured as 0100000 for this example.
B. P0 and P2 – P4 are configured as inputs.
C. P1 and P5 – P7 are configured as outputs.
D. Resistors are required for inputs (on P-port) that may float. If a driver to an input will never let the input float, a resistor is not needed. Outputs (in the P-port) do not need pull-up resistors.

**图 9-1. Typical Application Schematic**

### 9.2.1 Design Requirements

#### *9.2.1.1 Calculating Junction Temperature and Power Dissipation*

When designing with the TCA6408A-Q1, it is important that the *节 6.3* not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in 方程式 1.

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (1)$$

$\theta_{JA}$ is the standard junction to ambient thermal resistance measurement of the package, as seen in 节 6.4 table. $P_d$ is the total power dissipation of the device, and the approximation is shown in 方程式 2.

$$P_d \approx \left(I_{CC_STATIC} \times V_{CC}\right) + \sum P_{d_PORT_L} + \sum P_{d_PORT_H} \quad (2)$$

方程式 2 is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the $\overline{INT}$ and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using 方程式 3 to calculate the power dissipation in $\overline{INT}$ or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d_PORT_L} = \left(I_{OL} \times V_{OL}\right) \quad (3)$$

方程式 3 shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the $V_{OL}$ of the port multiplied by the current it is sinking.

$$P_{d_PORT_H} = \left(I_{OH} \times \left(V_{CC} - V_{OH}\right)\right) \quad (4)$$

方程式 4 shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between $V_{CC}$ and the output voltage).

#### 9.2.1.2 Minimizing $I_{CC}$ When I/O is Used to Control LEDs

When the I/Os are used to control LEDs, normally they are connected to $V_{CC}$ through a resistor as shown in 图 9-1. The LED acts as a diode, so when the LED is off, the I/O $V_{IN}$ is about 1.2 V less than $V_{CC}$. The $\Delta I_{CC}$ parameter in the 节 6.5 table shows how $I_{CC}$ increases as $V_{IN}$ becomes lower than $V_{CC}$. Designs that must minimize current consumption, such as battery power applications, must consider maintaining the I/O pins greater than or equal to $V_{CC}$ when the LED is off.

图 9-2 shows a high-value resistor in parallel with the LED. 图 9-3 shows $V_{CC}$ less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O $V_{IN}$ at or above $V_{CC}$ and prevent additional supply current consumption when the LED is off.

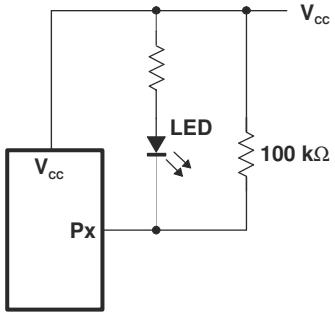



**图 9-2. High-Value Resistor in Parallel With LED**


Copyright © 2023 Texas Instruments Incorporated

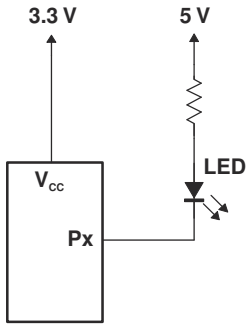



**图 9-3. Device Supplied by a Low Voltage**

### 9.2.2 Detailed Design Procedure

The pull-up resistors, $R_P$, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the $I^2C$ bus. The minimum pull-up resistance is a function of $V_{CC}$, $V_{OL,(max)}$, and $I_{OL}$ as shown in 方程式 5.

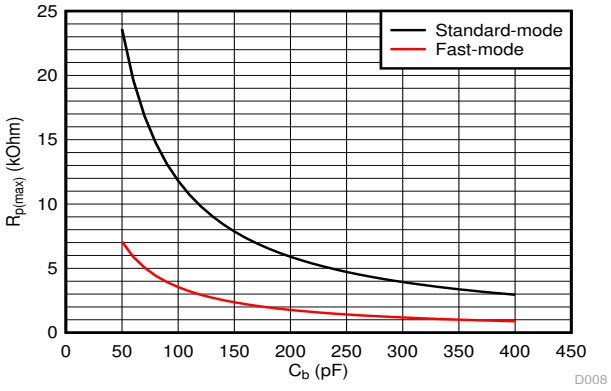
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \tag{5}$$

The maximum pull-up resistance is a function of the maximum rise time, $t_r$ (300 ns for fast-mode operation, $f_{SCL}$ = 400 kHz) and bus capacitance, $C_b$ as shown in 方程式 6.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \tag{6}$$

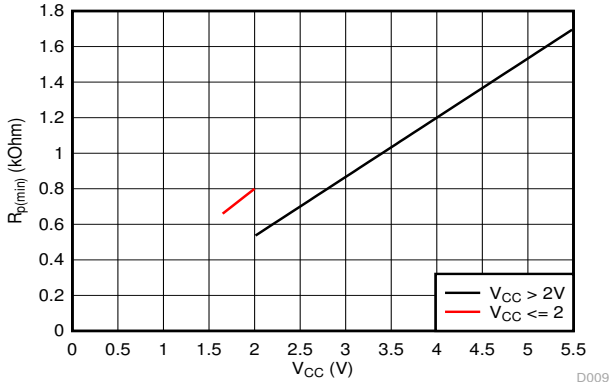
The maximum bus capacitance for an $I^2C$ bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA6408A-Q1, $C_i$ for SCL or $C_{IO}$ for SDA, the capacitance of wires, connections, traces, and the capacitance of additional targets on the bus.

### 9.2.3 Application Curves




Standard-mode: $f_{SCL}$= 100 kHz, $t_r$ = 1 µs
Fast-mode: $f_{SCL}$= 400 kHz, $t_r$= 300 ns$_b$

**图 9-4. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C)**




$V_{OL}$ = 0.2 × $V_{CC}$, $I_{OL}$ = 2 mA when $V_{CC} \leqslant$ 2 V
$V_{OL}$ = 0.4 V, $I_{OL}$ = 3 mA when $V_{CC}$ > 2 V

**图 9-5. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage ($V_{CCI}$)**

Copyright © 2023 Texas Instruments Incorporated

## 9.3 Power Supply Recommendations

### 9.3.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA6408A-Q1 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

Ramping up the device $V_{CCP}$ before $V_{CCI}$ is recommended to prevent SDA from potentially being stuck LOW.

The two types of power-on reset are shown in 图 9-6 and 图 9-7.

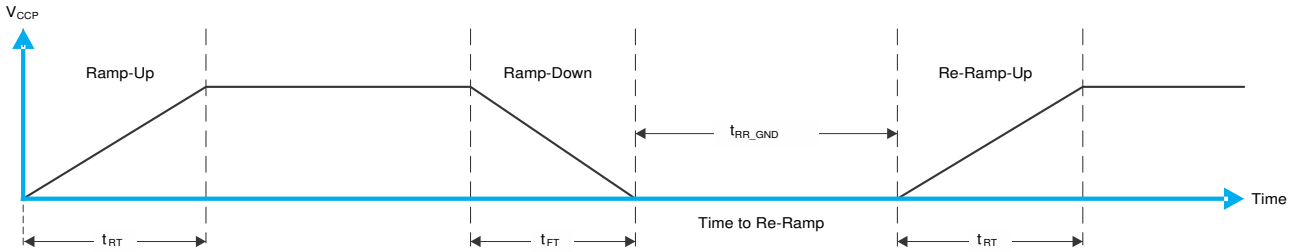



**图 9-6. $V_{CCP}$ is Lowered Below 0.2 V and then Ramped Up to $V_{CCP}$**

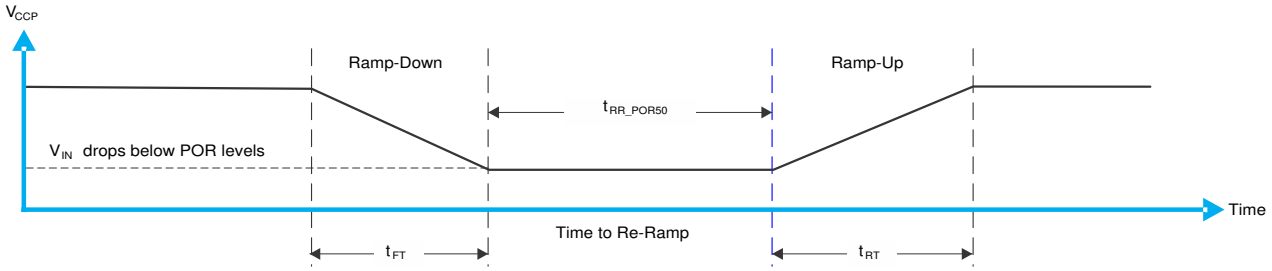



**图 9-7. $V_{CCP}$ is Lowered Below the POR Threshold, then Ramped Back Up to $V_{CCP}$**

表 9-1 specifies the performance of the power-on reset feature for TCA6408A-Q1 for both types of power-on reset.

**表 9-1. Recommended Supply Sequencing and Ramp Rates at $T_A$ = 25°C(1)**

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{FT}$ | Fall rate | See 图 9-6 | 0.1 | | 2000 | ms |
| $t_{RT}$ | Rise rate | See 图 9-6 | 0.1 | | 2000 | ms |
| $t_{RR_GND}$ | Time to re-ramp (when $V_{CCP}$ drops to GND) | See 图 9-6 | 1 | | | µs |
| $t_{RR_POR50}$ | Time to re-ramp (when $V_{CCP}$ drops to $V_{POR_MIN}$ – 50 mV) | See 图 9-7 | 1 | | | µs |
| $V_{CCP_GH}$ | Level that $V_{CCP}$ can glitch down from $V_{CCP}$, but not cause a functional disruption when $t_{VCCP_GW}$ = 1 µs | See 图 9-8 | | | 1.2 | V |
| $V_{CCP_MV}$ | The minimum voltage that VCC can glitch down to without causing a reset ($V_{CC_GH}$ must not be violated) | See 图 9-8 | 1.5 | | | V |
| $t_{VCCP_GW}$ | Glitch width that does not cause a functional disruption when $t_{VCCP_GH}$ = 0.5 × $V_{CCx}$ | See 图 9-8 | | | 10 | µs |
| $V_{PORF}$ | Voltage trip point of POR on falling $V_{CCP}$ | | 0.6 | 1 | | V |
| $V_{PORR}$ | Voltage trip point of POR on rising $V_{CCP}$ | | | 1.2 | 1.5 | V |

(1) Not tested. Specified by design.


Copyright © 2023 Texas Instruments Incorporated

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{VCCP_GW}$) and height ($V_{CCP_GH}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. 图 9-8 and 表 9-1 provide more information on how to measure these specifications.

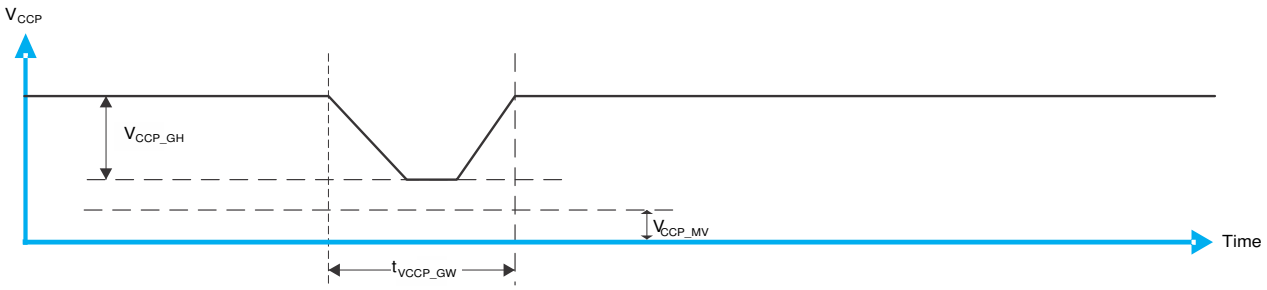



**图 9-8. Glitch Width and Glitch Height**

$V_{POR}$ is critical to the power-on reset. $V_{PORR}$ / $V_{PORF}$ is the voltage level at which the reset condition is released/ asserted and all the registers and the $I^2C$/SMBus state machine are initialized to the default states (upon a release of a reset condition). The voltage that the device has a reset condition asserted or released differs based on whether $V_{CCP}$ is being lowered to or from 0. 图 9-9 and 表 9-1 provide more details on this specification.

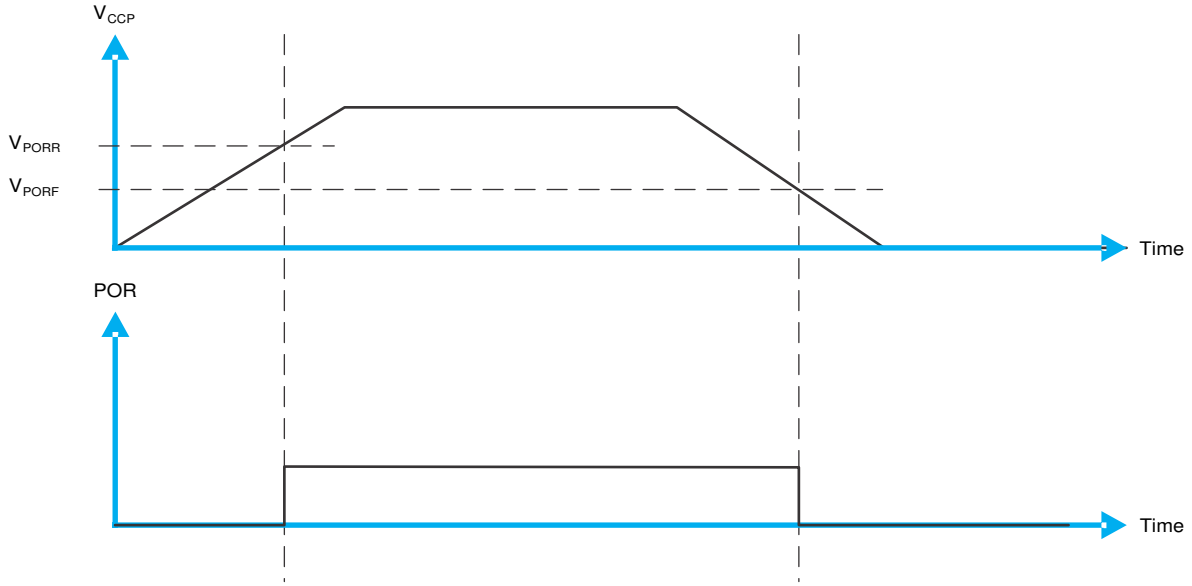



**图 9-9. Power On Reset**

## 9.4 Layout

### 9.4.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA6408A-Q1, common PCB layout practices must be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for $I^2C$ signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the $V_{CCI}$ and $V_{CCP}$ pins, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency

Copyright © 2023 Texas Instruments Incorporated

ripple. These capacitors must be placed as close to the TCA6408A-Q1 as possible. These best practices are shown in 节 9.4.2.

For the layout example provided in 节 9.4.2, it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power ($V_{CCI}$ and $V_{CCP}$) and ground (GND). However, a 4-layer board is preferable for boards with higher density signal routing. On a 4-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to $V_{CCI}$, $V_{CCP}$, or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in 节 9.4.2.

### 9.4.2 Layout Example

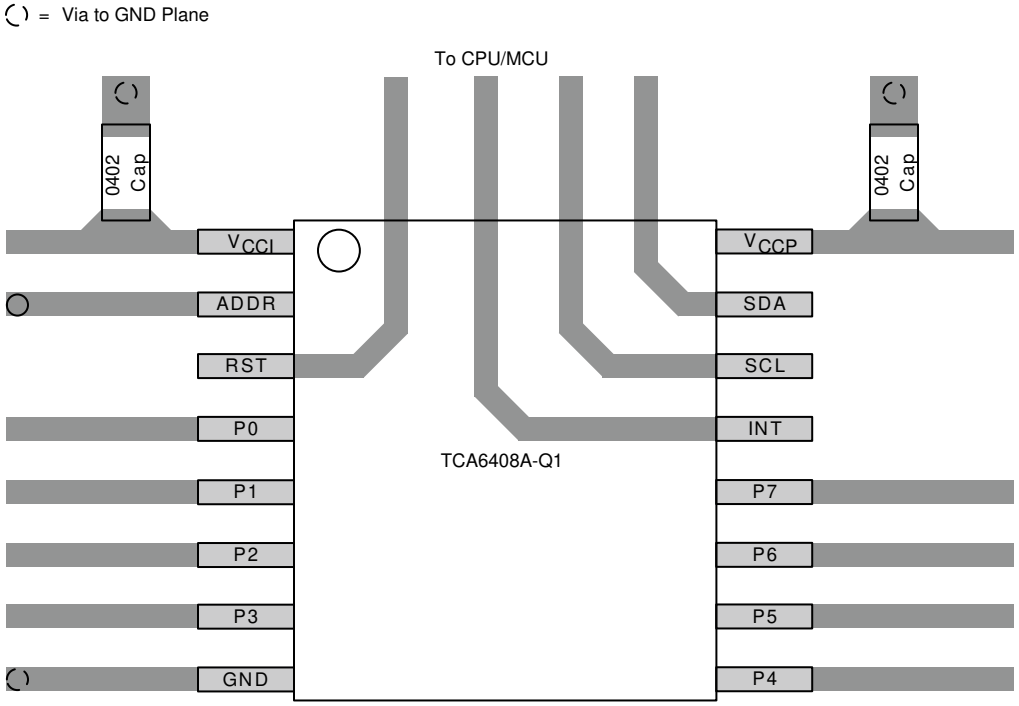



**图 9-10. Example Layout (PW Package)**


Copyright © 2023 Texas Instruments Incorporated

# 10 Device and Documentation Support

## 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.2 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 10.3 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 10.4 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |

# 11 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TCA6408AQPWRQ1 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 6408AQ |
| TCA6408AQPWRQ1.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 6408AQ |
| TCA6408AQPWRQ1.B | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 6408AQ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TCA6408A-Q1 :**

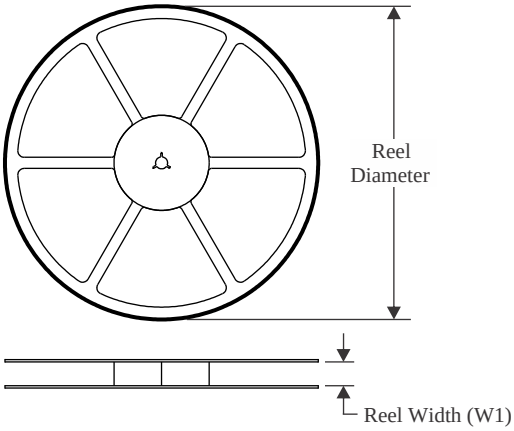
- Catalog : TCA6408A

NOTE: Qualified Version Definitions:

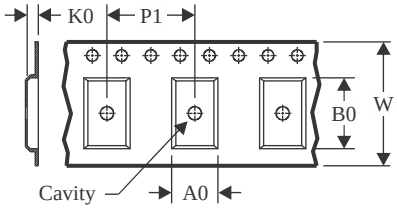
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

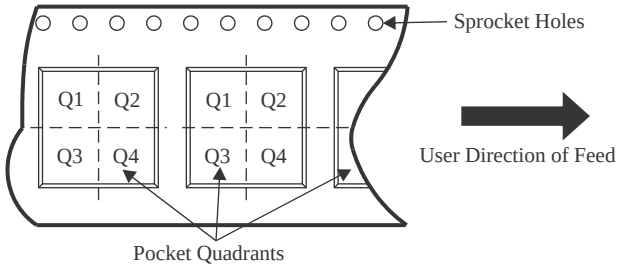



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

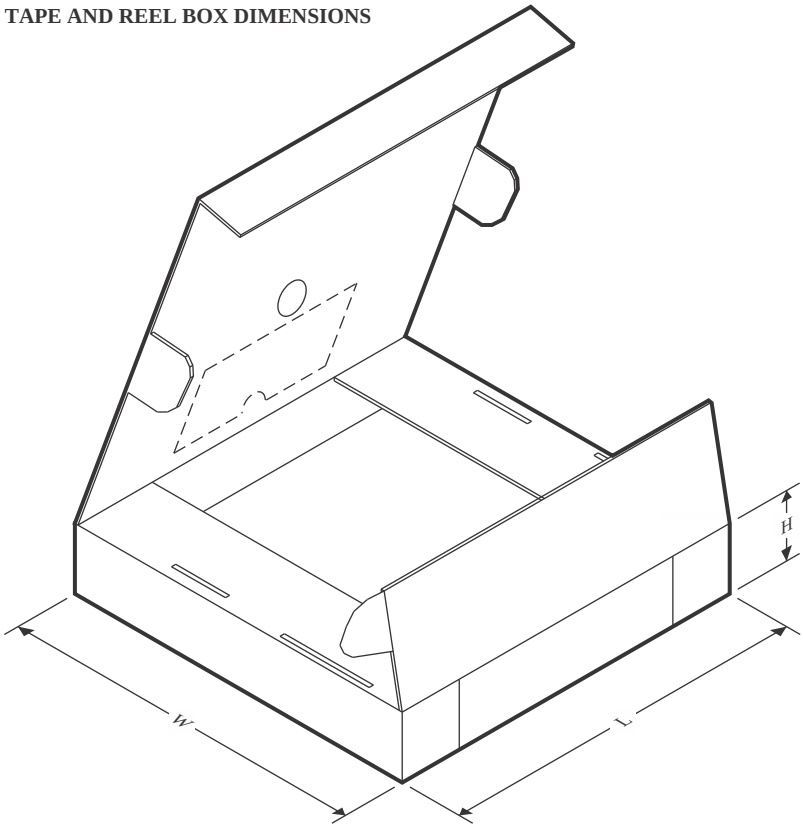
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TCA6408AQPWRQ1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

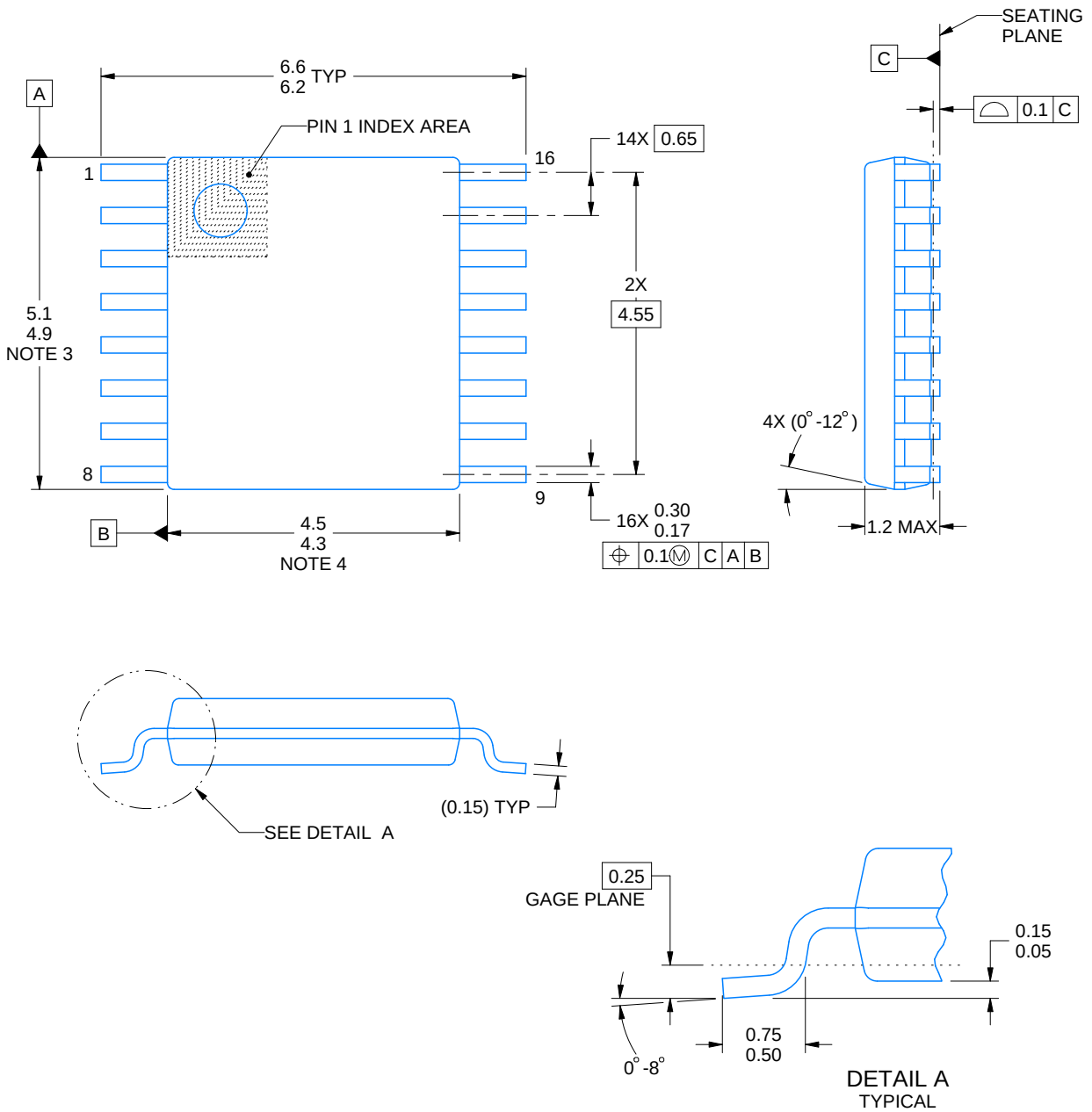
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TCA6408AQPWRQ1 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |

# PACKAGE OUTLINE

## PW0016A

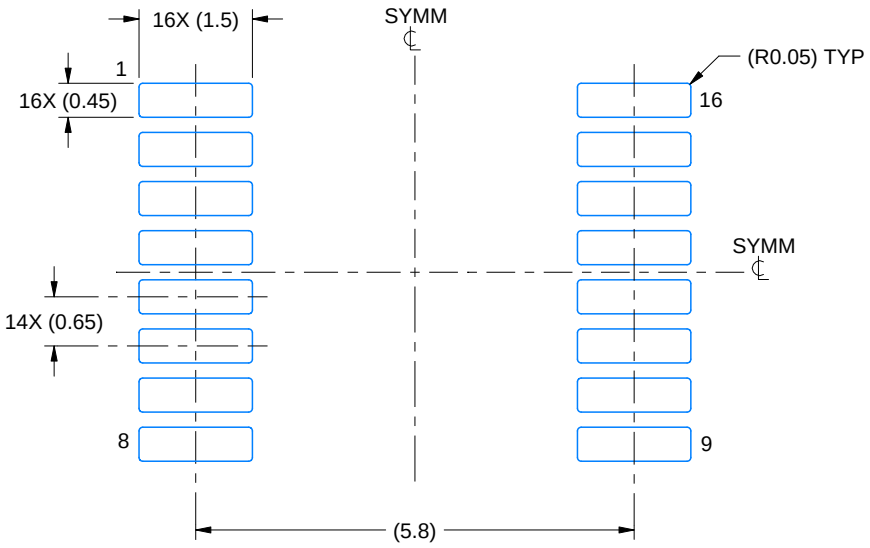
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

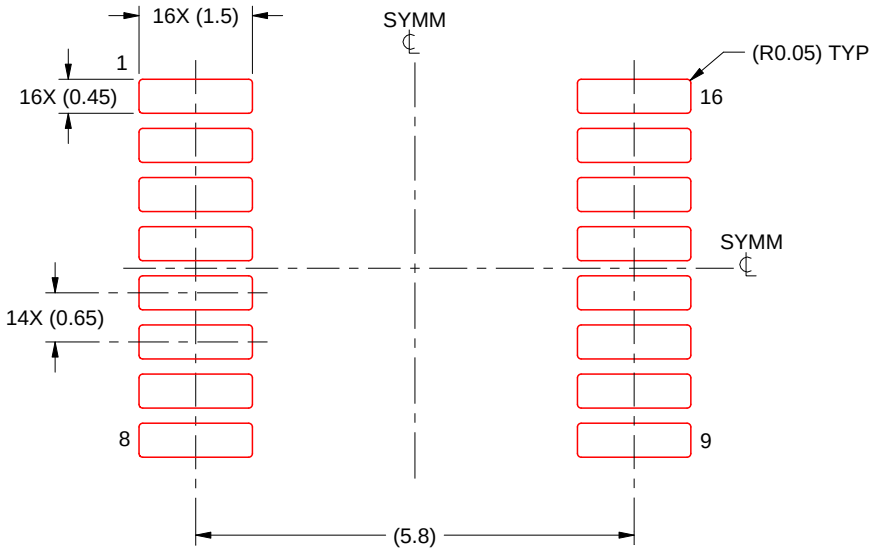



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月