1.5/3.0/6.0 Gbps SATA/SAS 再驱动器

查询样品: SN75LVCP600S

特性

- **3.3-V** 单电源
- 适用于为达 **40** 英寸（**1.0** 米）以上的各种尺寸 **FR4 PC** 电路板接收 **6.0 Gbps** 数据。
- 与**TX** 的两级均衡**RX**
  - **RX→ 7, 15 dB**
  - **TX→ 0, –1.3 dB**
- 引脚可选 **SATA/SAS** 信号发送
- 可编程长通道静噪阈值
- 低有效功率及局部工作 / 睡眠状态支持
  - 典型值（**6Gbps** 时的工作模式）**106 mW**
  - **11 mW**（局部工作 / 睡眠状态下的链路）低于
- 支持布局优化的超小型封装
  - 焊盘**2.5** 毫米**x 2.5** 毫米**QFN10**
- 高 **ESD** 瞬态保护
  - **HBM: 9,000 V**
  - **CDM: 1,500 V**
  - **MM: 200 V**

应用

- 笔记本与桌面电脑、扩展基座、有源线缆、服务器以及工作站

说明

SN75LVCP600S 是一款支持高达 6.0Gbps 数据速率的单通道 SATA/SAS 信号调节器。 该器件符合 SATA 物理规范 rev 3.0 与 SAS 电子规范 2.0。SN75LVCP600S 采用 3.3 V 单电源供电，提供具有自偏压特性的 100 Ω 线路端接，是 AC 耦合的理想选择。 各种输入整合了带外 (OOB) 检测器，可在保持稳定共模电压与 SATA/SAS 链路一致的同时，自动消除输出噪声。

SN75LVCP600S 可通过可选均衡设置处理其输入的互连损耗，能够通过编程来匹配通道中的信号损耗。 对于 3Gbps 及以下的数据速率，LVCP600S 可为达 50 英寸径距的 FR4 电路板材料均衡信号。 对于 6Gbps 数据速率而言，该器件可针对 40 英寸以上的 FR4 材料进行补偿。 通过设置信号控制引脚 EQ 与 DE，可对 Rx/Tx 均衡级别进行控制。

该器件支持热插拔功能(1)，可在非同步信号插拔、无供电插拔、带电插拔或异常插拔等器件热插入过程中防止器件损坏。

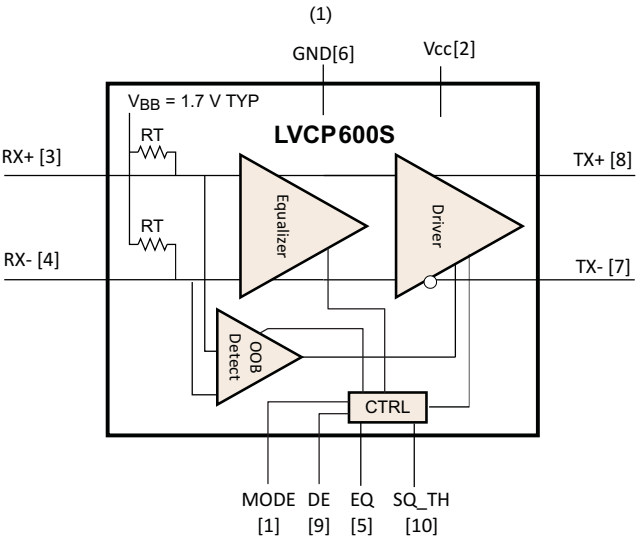


图 **1.** 数据流方框图

(1) 在不同输入输出中均需使用 AC 耦合电容器。

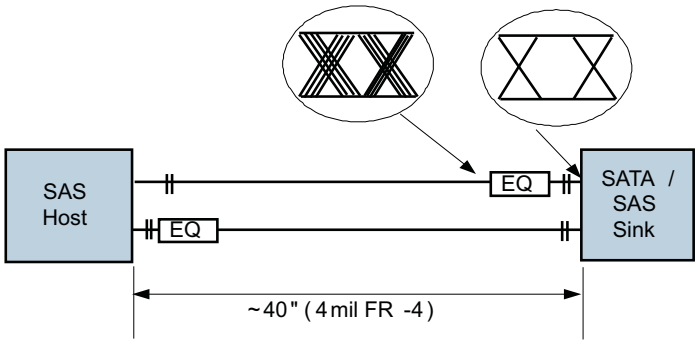
Table 1. ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN75LVCP600SDSKR	600S	10-pin DSK Reel (large)
SN75LVCP600SDSKT	600S	10-pin DSK Reel (small)

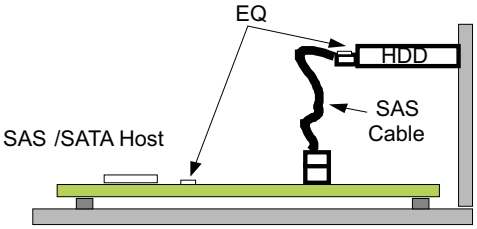
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



EQ = LVCP600S



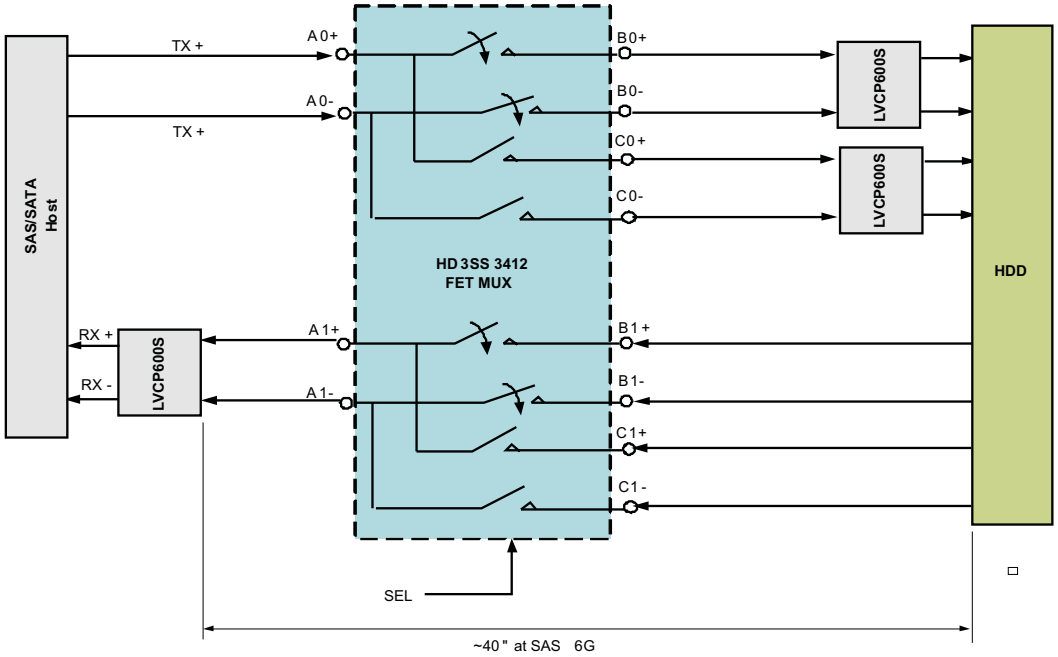
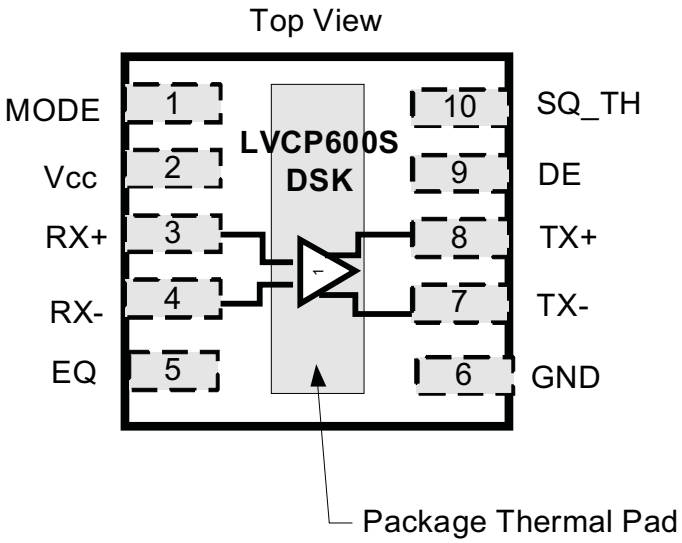


Figure 2. Typical Application

PIN ASSIGNMENTS



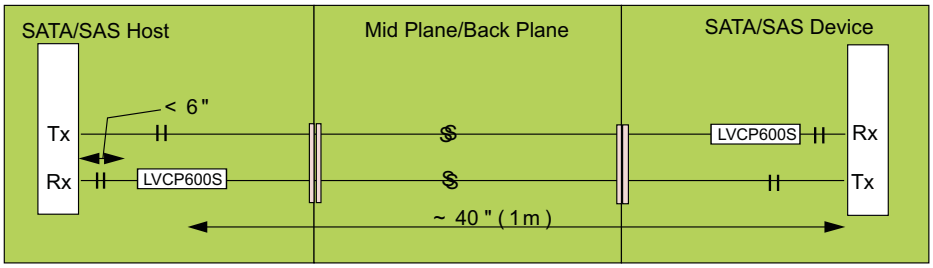
It is recomended to solder the package thermal pad to the ground plane for maximum thermal performance.

PIN FUNCTIONS

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
HIGH SPEED DIFFERENTIAL I/O			
3	RX+	I, CML	Non-inverting and inverting CML differential inputs. These pins are tied to an internal voltage bias by dual termination-resistor circuit.
4	RX–	I, CML	
8	TX+	I, CML	Non-inverting and inverting CML differential outputs. These pins are tied to an internal voltage bias by dual termination-resistor circuit.
7	TX–	I, CML	
CONTROL PINS			
5	EQ	I, LVCMOS	Selects equalization settings per Table 2. Internally tied to GND.
9	DE	I, LVCMOS	Selects de-emphasis settings per Table 2. Internally tied to GND.
1	MODE	I, LVCMOS	Selects SATA or SAS output levels per Table 2. Internally tied to GND
10	SQ_TH	I, LVCMOS	Selects squelch threshold settings per Table 2. Internally tied to GND
POWER			
2	V_{CC}	Power	Positive supply should be 3.3V ±10%
6	GND	Power	Supply ground

Table 2. EQ and DE Settings

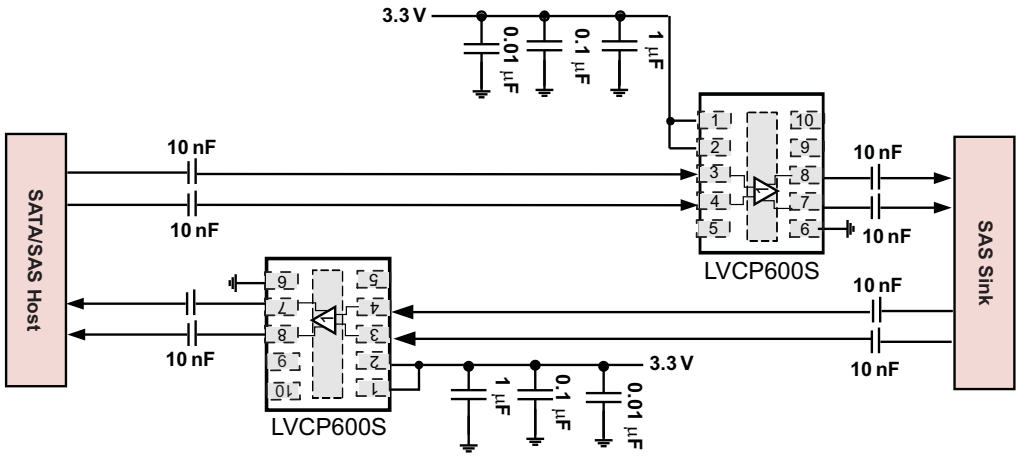
Level	CONTROL PINS			
	EQ (typ) dB at 6Gbps	DE (typ) dB at 6Gbps	SQ_TH (see V_{OOB} spec)	MODE
0 (***default***)	7	0	Full Level (normal)	SATA
1	14	–1.3	Reduced Level (long channel)	SAS



Trace lengths are suggested values based on TI spice simulations (done over programmable limits of input EQ) to meet SATA/SAS loss and jitter spec.

Actual trace length supported by the LVCP600S may be more or less than suggested values and will depend on board layout, trace widths and number of connectors used in the high speed signal path. See eye diagrams at end of datasheet for more placement guidance.

Figure 3. Trace Length Example



A. Place supply capacitors close to device pin

B. EQ selection is set at 7db, device is set in SAS mode, DE and SQ_TH at default settings

C. Actual EQ settings depend on device placement relative to host and SATA/SAS device

Figure 4. Typical Device Implementation

OPERATION DESCRIPTION

INPUT EQUALIZATION

The SN75LVCP600S supports programmable equalization in its front stage; the equalization settings are shown in Table 2. The input equalizer is designed to recover a signal even when no eye is present at the receiver and will affectively support FR4 trace at the input anywhere from 4" to 40" at SATA 6G speed. In SAS mode, the device meets compliance point IR in a TXRX connection.

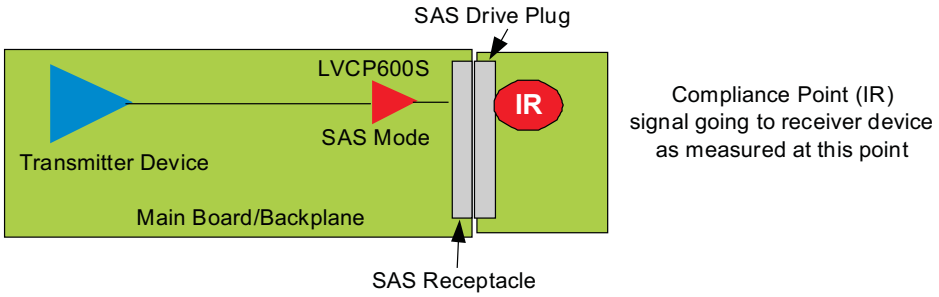


Figure 5. Compliance Point In SAS Mode

AUTO LOW POWER (ALP) MODE (see Figure 10)

As a redriver, the SN75LVCP600S does not participate in SATA or SAS link power management (PM) states. However, the redriver tracks link-power management mode (Partial and Slumber) by relying on the link differential voltage, V_{IDp-p}. The SATA/SAS link is continuously sending and receiving data even in long periods of disk inactivity by sending SYNC primitives (logical idle), except when the link enters Partial or Slumber mode. In these modes the link is in an electrical-idle state (EID). The device input squelch detector tracks EID status. When the input signal is in the electrical idle state, i.e. V_{IDp-p} <VOOB_SATA/VOOB_SAS and stays in this state for > 10µS, the device automatically enters the low power state. In this state, the output is driven to V_{CM} and the device selectively shuts off internal circuitry to lower power consumption by ~90% of its normal operating power. While in ALP mode, the device continues to actively monitor input signal levels; when the input signal exceeds the SATA/SAS OOB upper threshold level, the device reverts to active state. Exit time from auto low power mode is <50ns (MAX).

OUT-OF-BAND (OOB) SUPPORT

The squelch detector circuit within the device enables full detection of OOB signaling as specified in the SATA and SAS specifications. Selection of squelch threshold level is made automatically based on the state of MODE pin, SATA or SAS. Squelch circuit ON/OFF time is 8ns max. While in squelch mode, outputs are held to V_{CM}.

DEVICE POWER

The SN75LVCP600S is designed to operate from a single 3.3V supply. Always practice proper power supply sequencing procedure. Apply V_{CC} *first* before any input signals are applied to the device. The power down sequence is in reverse order.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range(2)	V_{CC}	–0.5 to 4	V
Voltage range	Differential I/O	–0.5 to 4	V
	Control I/O	–0.5 to V_{CC} + 0.5	V
Electrostatic discharge	Human body model(3)	±9000	V
	Charged-device model(4)	±1500	V
	Machine model(5)	±200	V
Continuous power dissipation		See Dissipation Rating Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

THERMAL INFORMATION

THERMAL METRIC(1)		SN75LVCP600S DSK (10) PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	55.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	61.9	
θ_{JB}	Junction-to-board thermal resistance	29.2	
ψ_{JT}	Junction-to-top characterization parameter	1.0	
ψ_{JB}	Junction-to-board characterization parameter	29.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	9.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

typical values for all parameters are at V_{CC} = 3.3 V and T_A = 25°C; all temperature limits are specified by design

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage		3	3.3	3.6	V
$C_{COUPLING}$	Coupling capacitor			12		nF
T_A	Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
ICC_{Max}	Active mode supply current	MODE/EQ/DE/SQ_TH = NC, K28.5 pattern at 6Gbps, V_{ID} = 700mV_{pp}, (SATA mode)		29	41	mA
		MODE/EQ/DE/SQ_TH = V_{CC}, K28.5 pattern at 6Gbps, V_{ID} = 700mV_{pp}, (SAS mode)		32	45	
I_{CCPS}	Auto power save mode I_{CC}	When auto low power conditions are met		3.3	5.0	mA
	Maximum data rate				6.0	Gbps
t_{PDelay}	Propagation delay	Measured using K28.5 pattern, See Figure 8		280	330	ps
$AutoLP_{ENTRY}$	Auto low power entry time	Electrical idle at input, See Figure 10		11	20	µs
$AutoLP_{EXIT}$	Auto low power exit time	After first signal activity, See Figure 10		30	40	ns

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
OOB						
V_{OOB_SAS}	Input OOB threshold (output squelched below this level)	F = 750MHz; SQ_TH=0, MODE = 1 Measured at receiver pin	88	112	131	mV_{pp}
		F = 750MHz; SQ_TH=1, MODE = 1 Measured at receiver pin	67	85	100	
V_{OOB_SATA}	Input OOB threshold (output squelched below this level)	F = 750MHz; SQ_TH=0, MODE = 0 Measured at receiver pin	40	66	86	
		F = 750MHz; SQ_TH=1, MODE = 0 Measured at receiver pin	35	56	72	
$D_{VdiffOOB}$	OOB differential delta				25	mV
D_{VCMOOB}	OOB common-mode delta				50	mV
t_{OOB1}	OOB mode enter	See Figure 9		3	8	ns
t_{OOB2}	OOB mode exit	See Figure 9		3	8	ns
CONTROL LOGIC						
V_{IH}	High-level input voltage	For all control pins	1.4			V
V_{IL}	Low-level input voltage				0.5	V
VIN_{HYS}	Input hysteresis			115		mV
I_{IH}	High-level input current	MODE, SQ_TH = V_{CC}			30	µA
		EQ, DE = V_{CC}			20	
I_{IL}	Low-level input current	MODE, SQ_TH = GND	–30			
		EQ, DE = GND	–10			
RECEIVER AC/DC						
Z_{DIFFRX}	Differential input impedance		85	100	115	Ω
Z_{SERX}	Single-ended input impedance		40			Ω
VCM_{RX}	Common-mode voltage			1.7		V
RL_{DiffRX}	Differential mode return loss (RL)	f = 150MHz–300MHz	18	26		dB
		f = 300MHz–600MHz	14	23		
		f = 600MHz–1.2GHz	10	17		
		f = 1.2GHz–2.4GHz	8	14		
		f = 2.4GHz–3.0GHz	3	13		
$RX_{DiffRLSlope}$	Differential mode RL slope	f = 300MHz–6.0GHz		–13		dB/dec
RL_{CMRX}	Common-mode return loss	f = 150MHz–300MHz	5	10		dB
		f = 300MHz–600MHz	5	18		
		f = 600MHz–1.2GHz	2	16		
		f = 1.2GHz–2.4GHz	1	12		
		f = 2.4GHz–3.0GHz	1	12		
V_{diffRX}	Differential input voltage PP	MODE = 1, f = 1.5GHz and 3.0GHz	275		1600	mV/ppd
		MODE = 0, f = 1.5GHz and 3.0GHz	225		1600	
IB_{RX}	Impedance balance	f = 150MHz–300MHz	30	47		dB
		f = 300MHz–600MHz	30	40		
		f = 600MHz–1.2GHz	20	34		
		f = 1.2GHz–2.4GHz	10	28		
		f = 2.4GHz–3.0GHz	10	24		
		f = 3.0GHz–5.0GHz	4	22		
		f = 5.0GHz–6.5GHz	4	22		
$T_{20\text{-}80RX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. SATA/SAS 6 Gbps speed measured 1" from device pin	62		75	ps

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
T_{skewRX}	Differential skew	Difference between the single-ended mid-point of the RX+ signal rising/falling edge, and the single-ended mid-point of the RX– signal falling/rising edge			30	ps
TRANSMITTER AC/DC						
Z_{diffTX}	Pair differential impedance		85	100	122	Ω
Z_{SETX}	Single-ended input impedance		40			Ω
$V_{TXtrans}$	Sequencing transient voltage	Transient voltages on the serial data bus during power sequencing (lab load)	–1.2	0	1.2	V
RL_{DiffTX}	Differential mode return loss	f = 150MHz–300MHz	13	22		dB
		f = 300MHz–600MHz	8	21		
		f = 600MHz–1.2GHz	6	20		
		f = 1.2GHz–2.4GHz	6	17		
		f = 2.4GHz–3.0GHz	3	17		
$TX_{DiffRLSlope}$	Differential mode RL slope	f = 300MHz – 3.0GHz		–13		dB/dec
RL_{CMTX}	Common-mode return loss	f = 150MHz–300MHz	5	19		dB
		f = 300MHz–600MHz	5	16		
		f = 600MHz–1.2GHz	2	11		
		f = 1.2GHz–2.4GHz	1	9		
		f = 2.4GHz–3.0GHz	1	10		
IB_{TX}	Impedance balance	f = 150MHz–300MHz	30	43		dB
		f = 300MHz–600MHz	30	40		
		f = 600MHz–1.2GHz	20	32		
		f = 1.2GHz–2.4GHz	10	25		
		f = 2.4GHz–3.0GHz	10	27		
		f = 3.0GHz–5.0GHz	4	25		
		f = 5.0GHz–6.5GHz	4	26		
$Diff_{VppTX}$	Differential output voltage swing	DE = 1, MODE = 1→(SAS), f = 3.0GHz (under no interconnect loss)	385	850	1300	mV/ppd
		DE = 0, MODE = 0→(SATA), f = 3.0GHz (under no interconnect loss)	400	600	800	
DE	De-Emphasis Level	DE = 1		–1.3		dB
		DE = 0		0		
VCM_{AC_TX}	TX AC CM voltage	At 1.5GHz		20	50	mVppd
		At 3.0GHz		11	26	dBmv (rms)
		At 6.0GHz		13	30	
VCM_{TX}	Common-mode voltage			1.7		V
$T_{20\text{-}80TX}$	Rise/Fall time	Rise times and fall times measured between 20% and 80% of the signal. At 6Gbps SATA or SAS, under no load, measured at the pin	33	50	76	ps
T_{skewTX}	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising/falling edge, and the single-ended mid-point of the TX– signal falling/rising edge, SATA or SAS mode		4	14	ps
TxR/F_{lmb}	TX rise/fall imbalance	At 3 Gbps		3	18	%
$TxAm_{plmb}$	TX amplitude imbalance			1.5	10	

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER JITTER AT CP(1)						
3Gbps SATA mode						
TJ_{TX}	Total jitter(1)			0.26	0.38	UI_{pp}
DJ_{TX}	Deterministic jitter	V_{ID} = 500 mV_{pp}, UI = 333ps, K28.5 control character, EQ/DE=1		0.13	0.24	UI_{pp}
RJ_{TX}	Residual random jitter	V_{ID} = 500 mV_{pp}, UI = 333ps, K28.7 control character, EQ/DE=1		1.16	1.95	ps-rms
6Gbps SATA mode						
TJ_{TX}	Total jitter(1)			0.37	0.61	UI_{pp}
DJ_{TX}	Deterministic jitter	V_{ID} = 500 mV_{pp}, UI = 167ps, K28.5 control character, EQ/DE=1		012	0.32	UI_{pp}
RJ_{TX}	Residual random jitter	V_{ID} = 500 mV_{pp}, UI = 167ps, K28.7 control character, EQ/DE=1		1.15	2.2	ps-rms
3Gbps SAS mode						
TJ_{TX}	Total jitter(1)			0.25	0.37	UI_{pp}
DJ_{TX}	Deterministic jitter	V_{ID} = 500 mV_{pp}, UI = 333ps, K28.5 control character, EQ/DE=1		0.12	0.23	UI_{pp}
RJ_{TX}	Residual random jitter	V_{ID} = 500 mV_{pp}, UI = 333ps, K28.7 control character, EQ/DE=1		1.11	2.0	ps-rms
6Gbps SAS mode						
TJ_{TX}	Total jitter(1)			0.35	0.57	UI_{pp}
DJ_{TX}	Deterministic jitter	V_{ID} = 500 mV_{pp}, UI = 167ps, K28.5 control character, EQ/DE=1		0.10	0.29	UI_{pp}
RJ_{TX}	Residual random jitter	V_{ID} = 500 mV_{pp}, UI = 167ps, K28.7 control character, EQ/DE=1		1.10	2.14	ps-rms

(1) T_J = (14.1×RJ_{SD} + DJ) where RJ_{SD} is one standard deviation value of RJ Gaussian distribution. Jitter measurement is at the CP connector and includes jitter generated at the package connection on the printed circuit board, and at the board interconnect as shown in Figure 6.

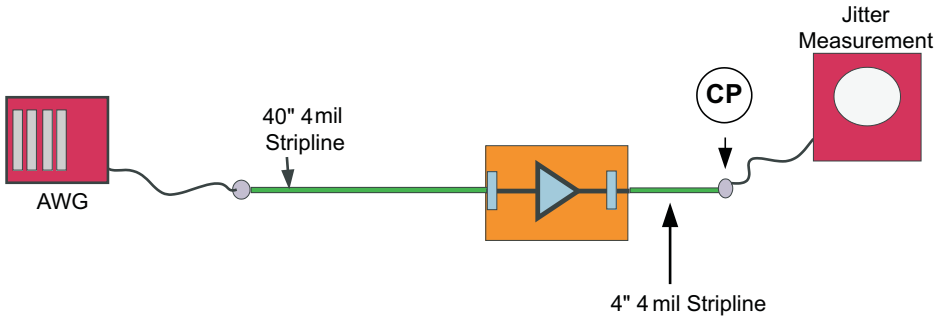


Figure 6. Jitter Measurement Test Condition

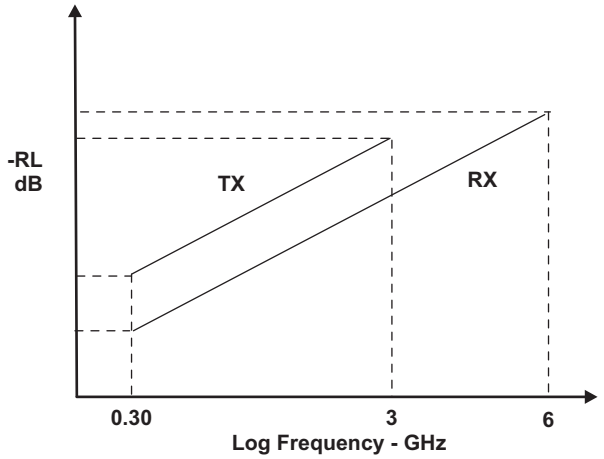


Figure 7. TX, RX Differential Return Loss Limits

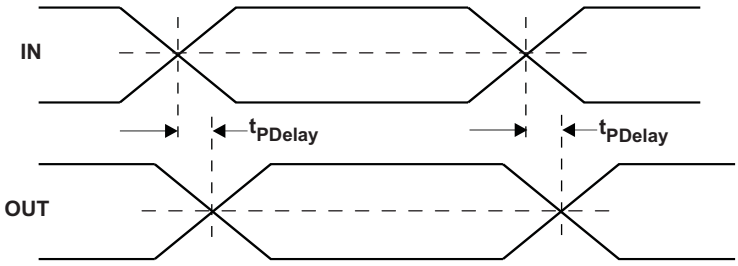


Figure 8. Propagation Delay Timing Diagram

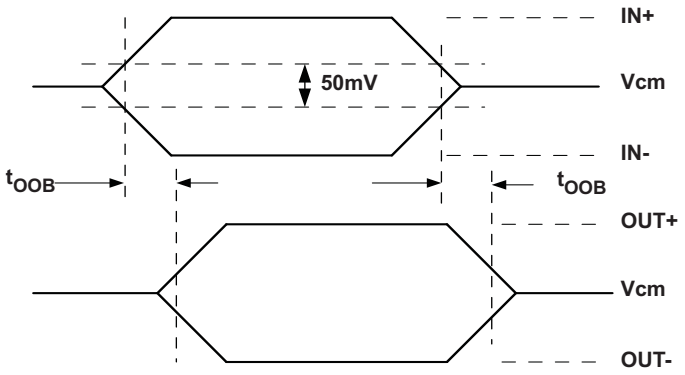


Figure 9. OOB Enter and Exit Timing

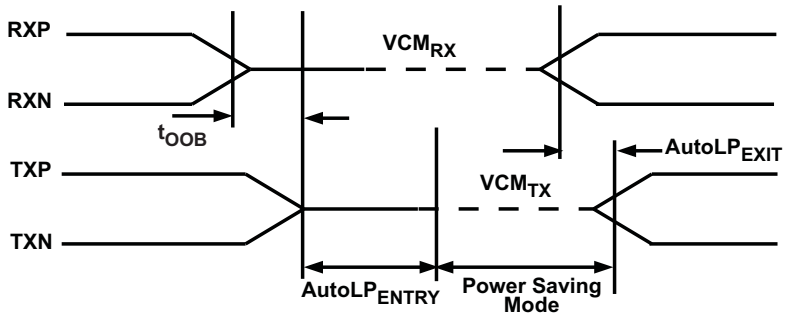
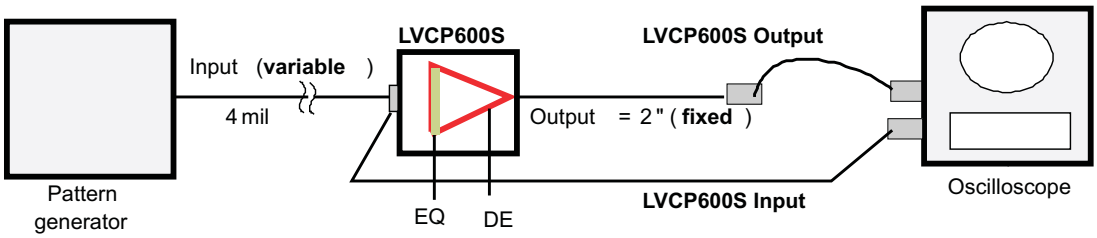


Figure 10. Auto Low Power Mode Entry and Exit Timing

TYPICAL EYE DIAGRAMS AND PERFORMANCE CURVES



A. V_{CC} = 3.3V; INPUT = K28.5 pattern at 1.5Gbps; 3.0Gbps and 6.0 Gbps; V_{ID} = 1000mVpp; TEMP = 25°C; TRACE WIDTH = 4mil

Figure 11. Eye Diagram Measurement Setup for LVCP600S

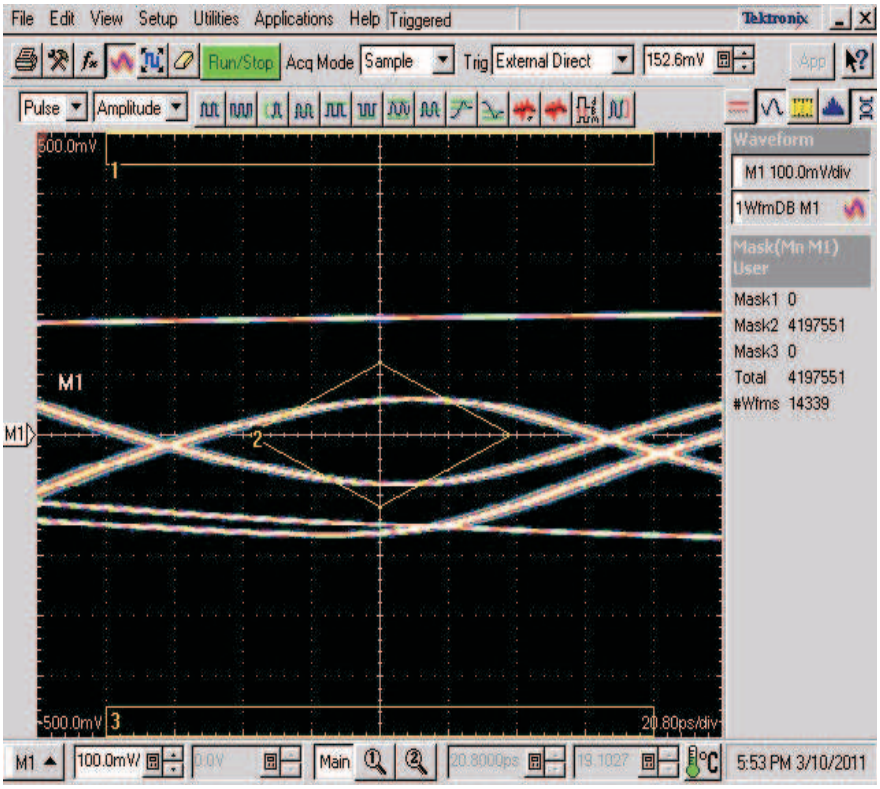


Figure 12. SATA 6.0 Gbps Signal After 16”, Input of LVCP600S (MODE=0)

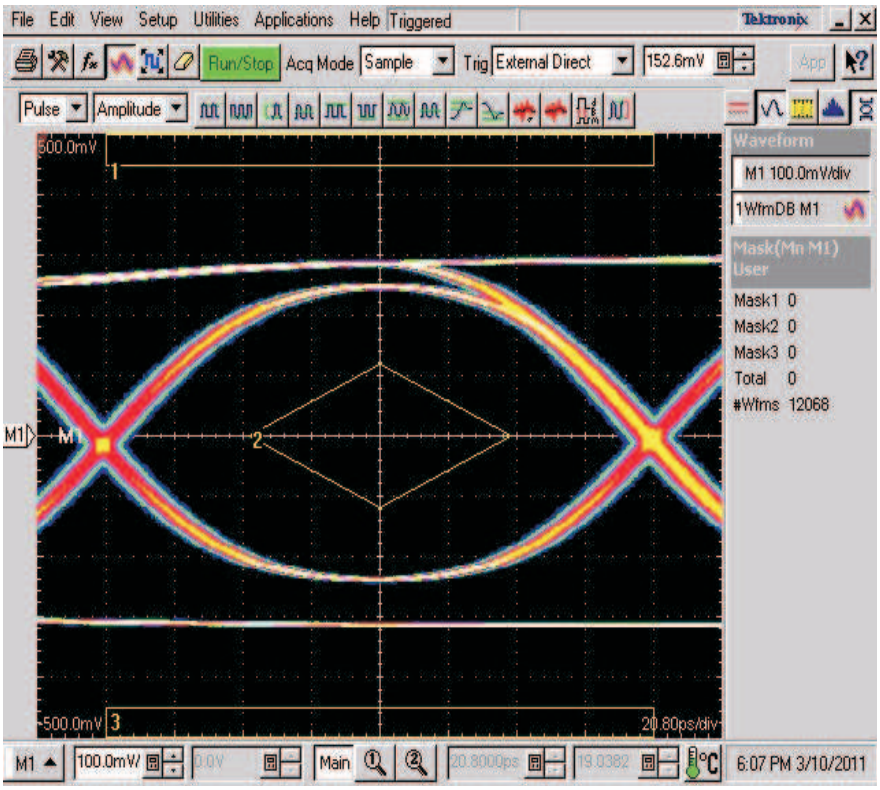


Figure 13. SATA 6.0 Gbps DE= 0, EQ = 1, at Output = 2” after Equalizing (MODE=0)

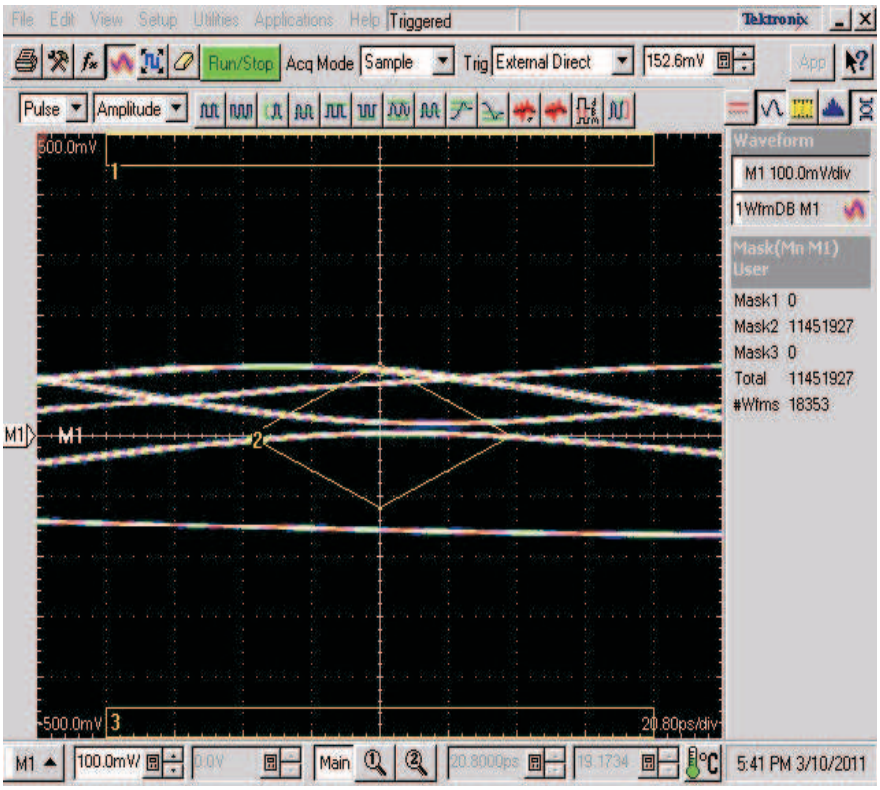


Figure 14. SATA 6.0 Gbps signal after 32” at Input of LVCP600S (MODE=0)

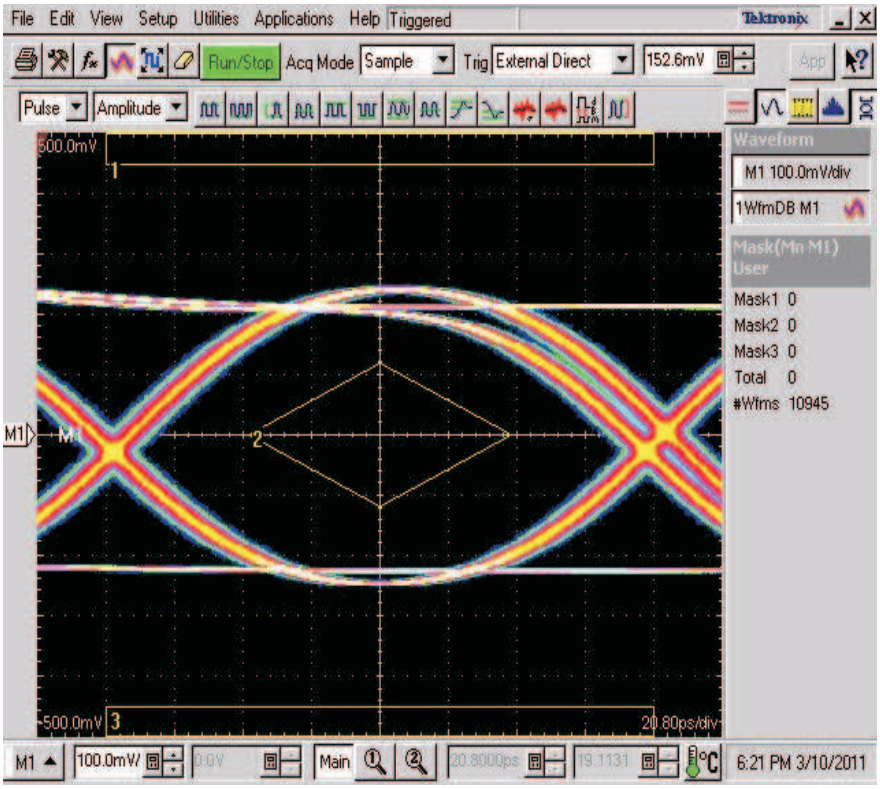


Figure 15. SATA 6.0 Gbps DE= 0, EQ = 1, at Output = 2” after Equalizing (MODE=0)

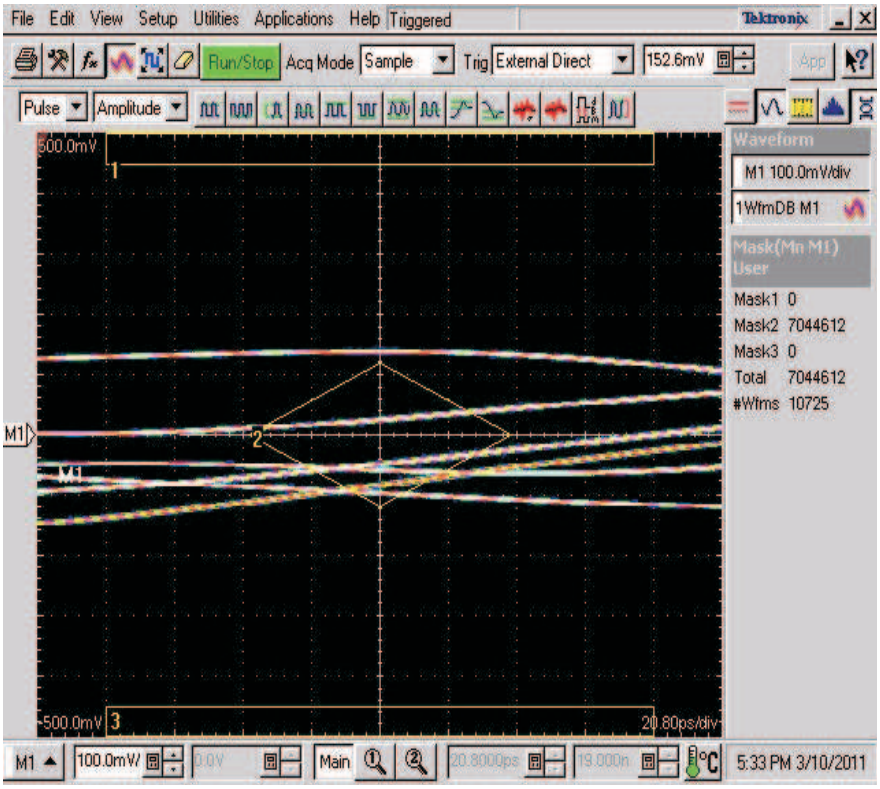


Figure 16. SATA 6.0 Gbps signal after 40” at Input of LVCP600S (MODE=0)

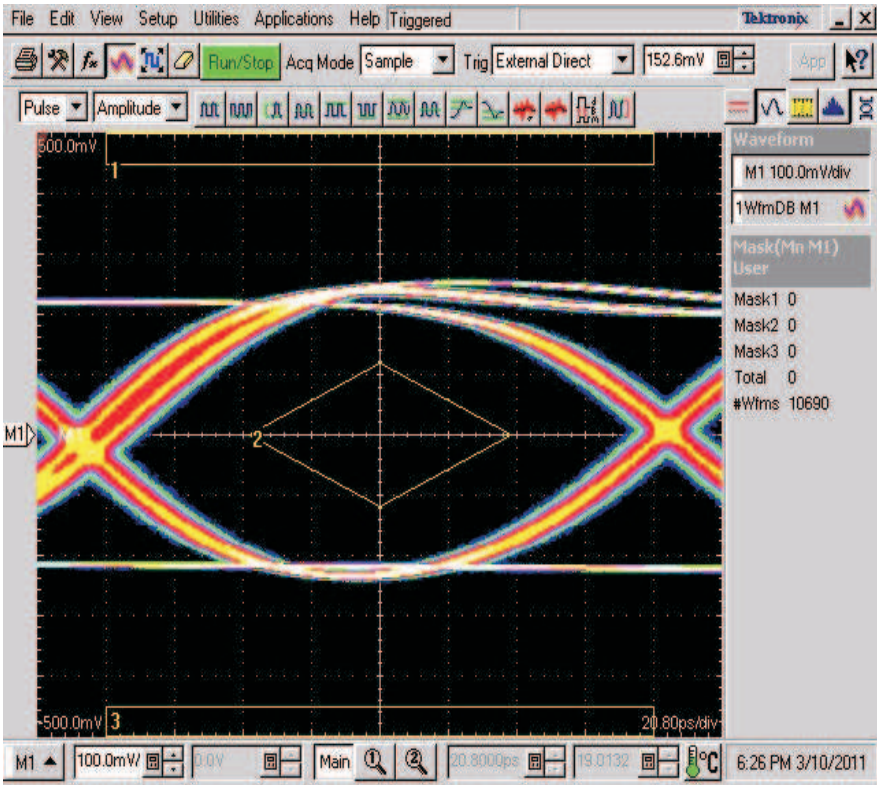


Figure 17. SATA 6.0 Gbps DE= 1, EQ = 1, at Output = 2” after Equalizing (MODE=0)

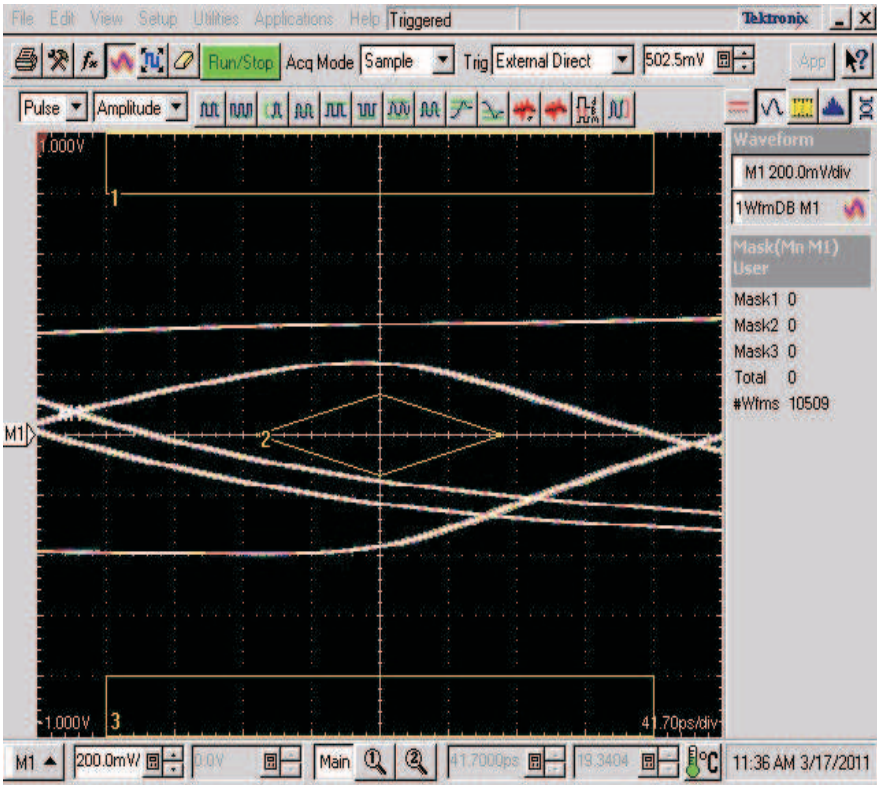


Figure 18. SAS 3.0 Gbps signal after 32” at Input of LVCP600S (MODE=1)

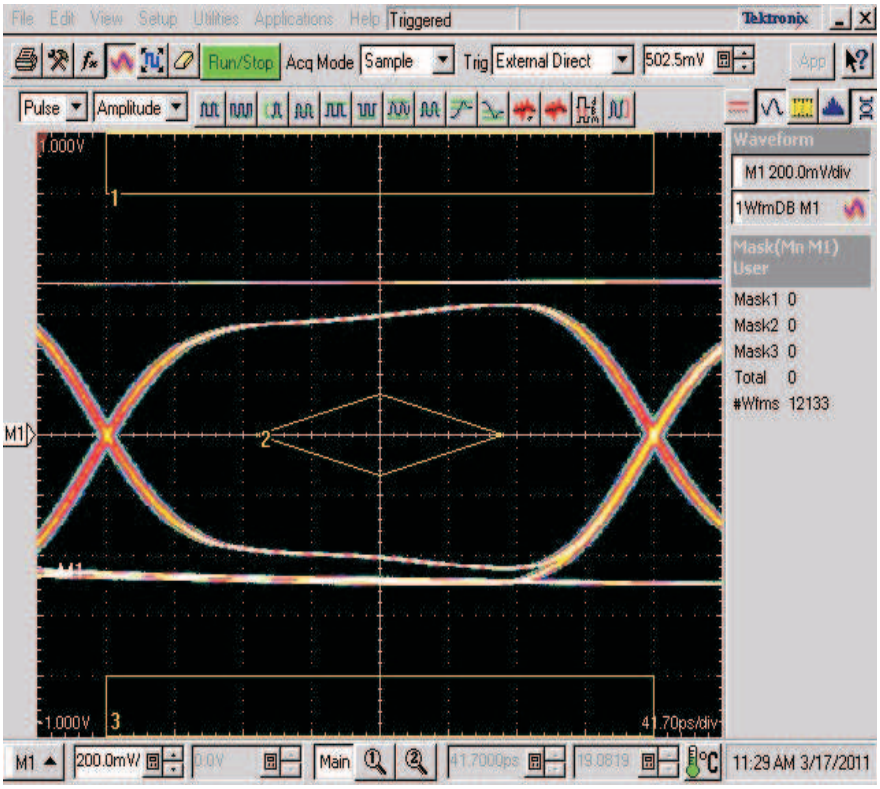


Figure 19. SAS 3.0 Gbps DE= 0, EQ = 1, at Output = 2” after Equalizing (MODE=1)

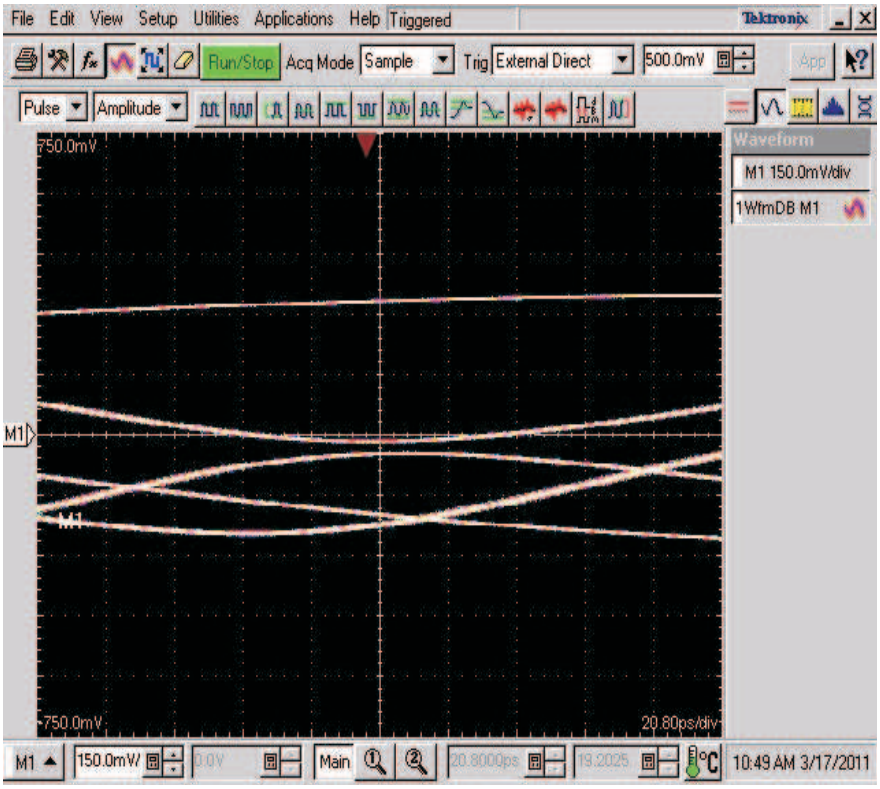


Figure 20. SAS 6.0 Gbps signal after 32" at Input of LVCP600S (MODE=1)

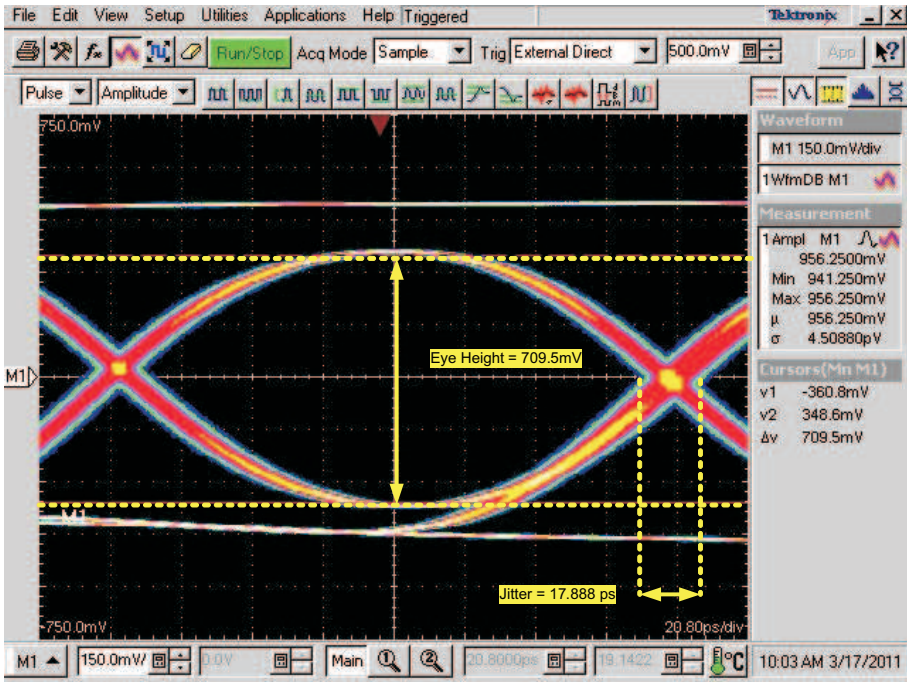


Figure 21. SAS 6.0 Gbps DE= 0, EQ = 1, at Output = 2" after Equalizing (MODE=1)

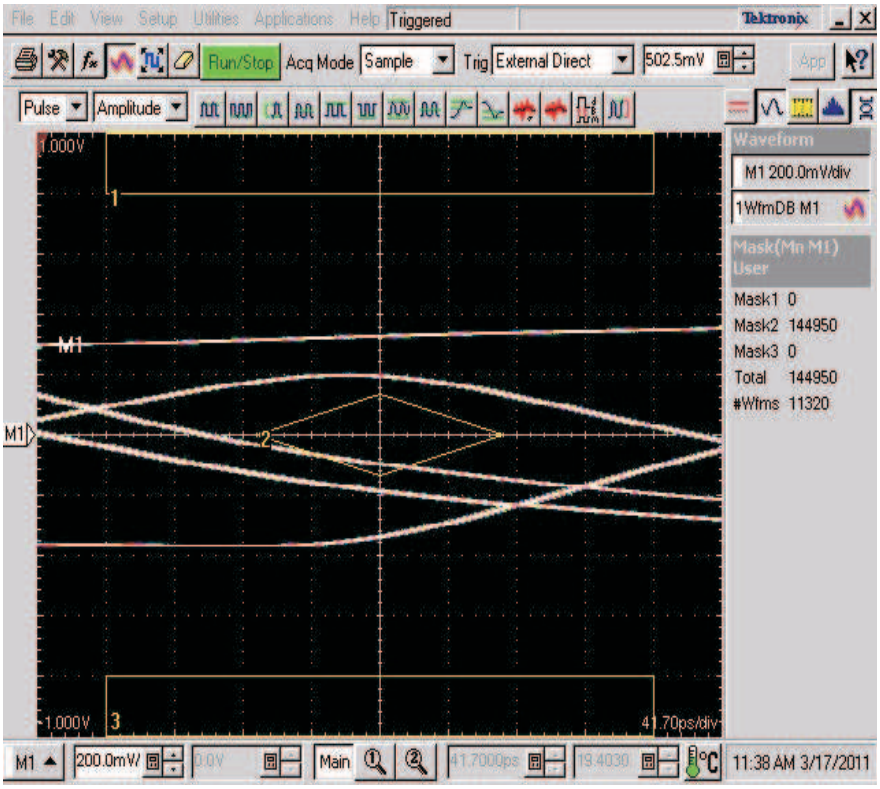


Figure 22. SAS 3.0 Gbps signal after 40” at Input of LVCP600S (MODE=1)

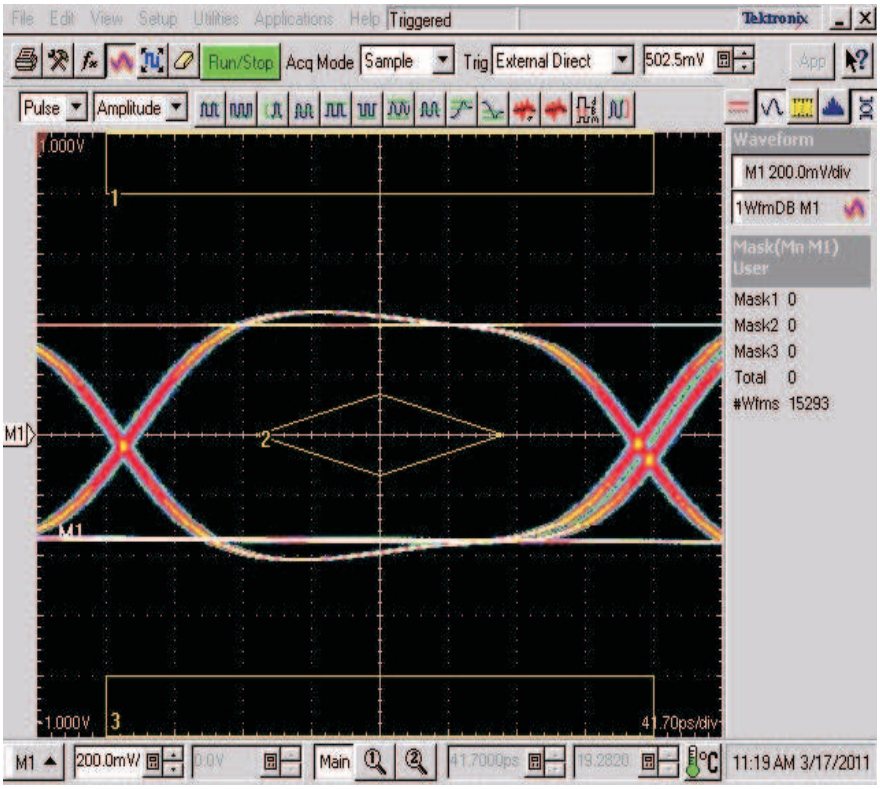


Figure 23. SAS 3.0 Gbps DE= 1, EQ = 1, at Output = 2” after Equalizing (MODE=1)

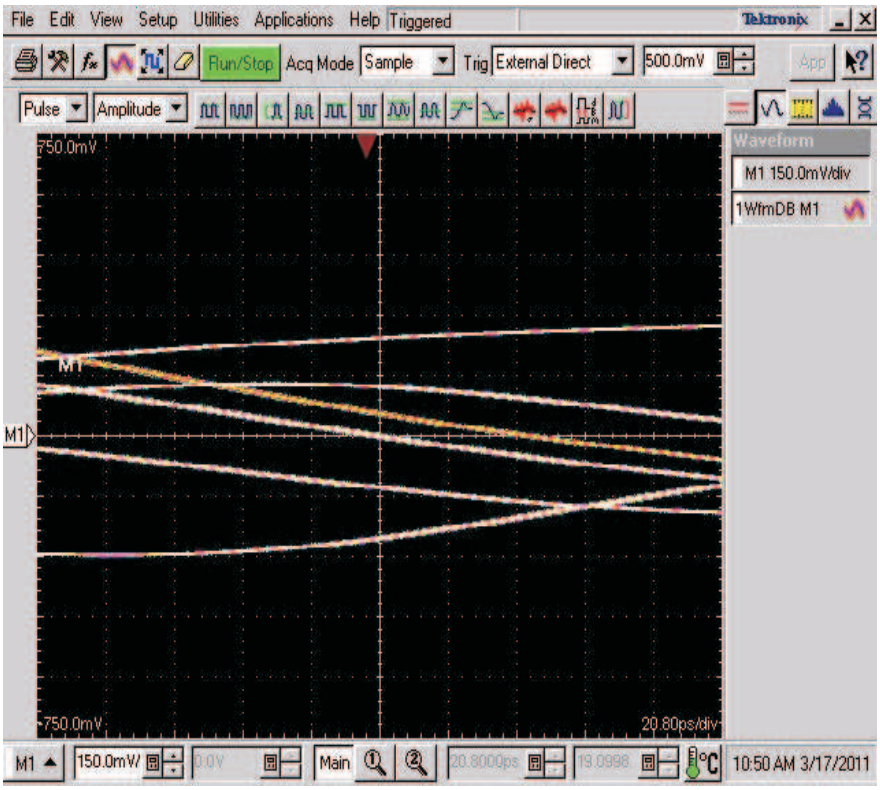


Figure 24. SAS 6.0 Gbps signal after 40” at Input of LVCP600S (MODE=1)

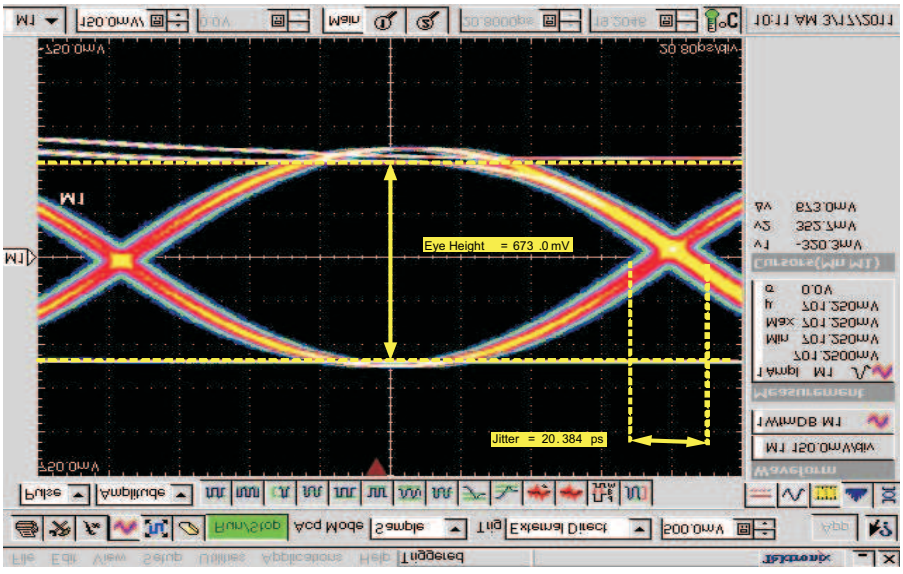


Figure 25. SAS 6.0 Gbps DE= 1, EQ = 1, at Output = 2” after Equalizing (MODE=1)

SATA MODE DETERMINISTIC JITTER vs DATA RATE

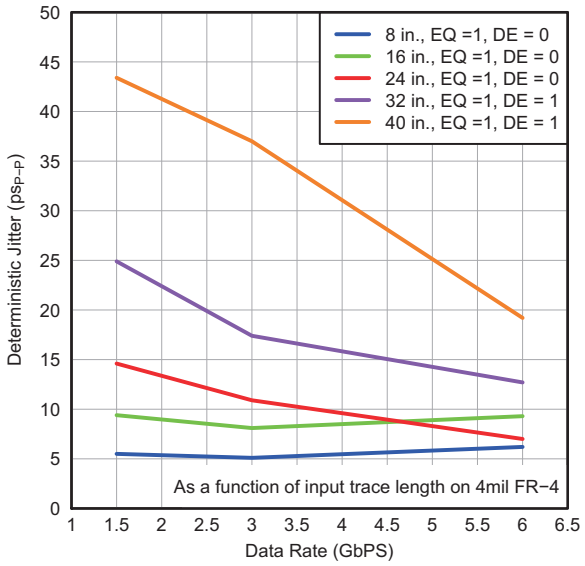


Figure 26.

SATA MODE DETERMINISTIC JITTER vs LAUNCH AMPLITUDE

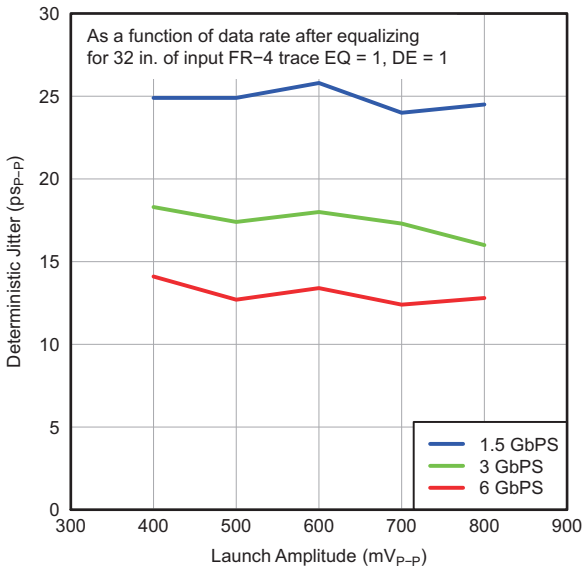


Figure 27.

SAS MODE DETERMINISTIC JITTER vs DATA RATE

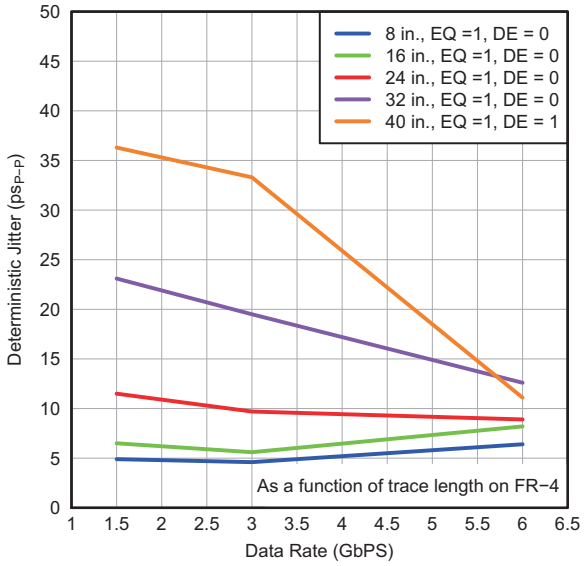


Figure 28.

SAS MODE DETERMINISTIC JITTER vs LAUNCH AMPLITUDE

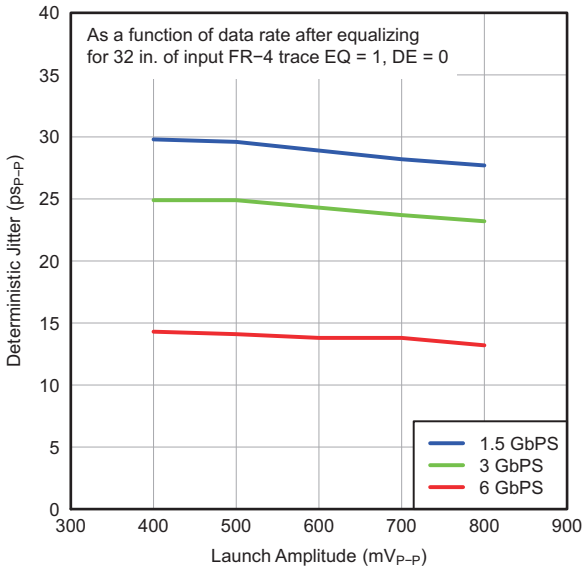


Figure 29.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LVCP600SDSKR	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	600S
SN75LVCP600SDSKR.B	Active	Production	SON (DSK) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	600S
SN75LVCP600SDSKT	Active	Production	SON (DSK) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	600S
SN75LVCP600SDSKT.B	Active	Production	SON (DSK) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	600S
SN75LVCP600SDSKTG4	Active	Production	SON (DSK) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	600S
SN75LVCP600SDSKTG4.B	Active	Production	SON (DSK) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	600S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

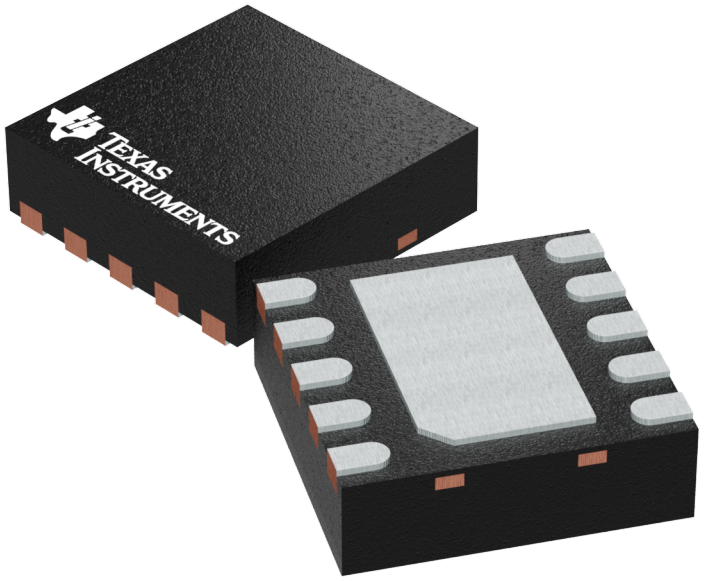
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

DSK 10 WSON - 0.8 mm max height

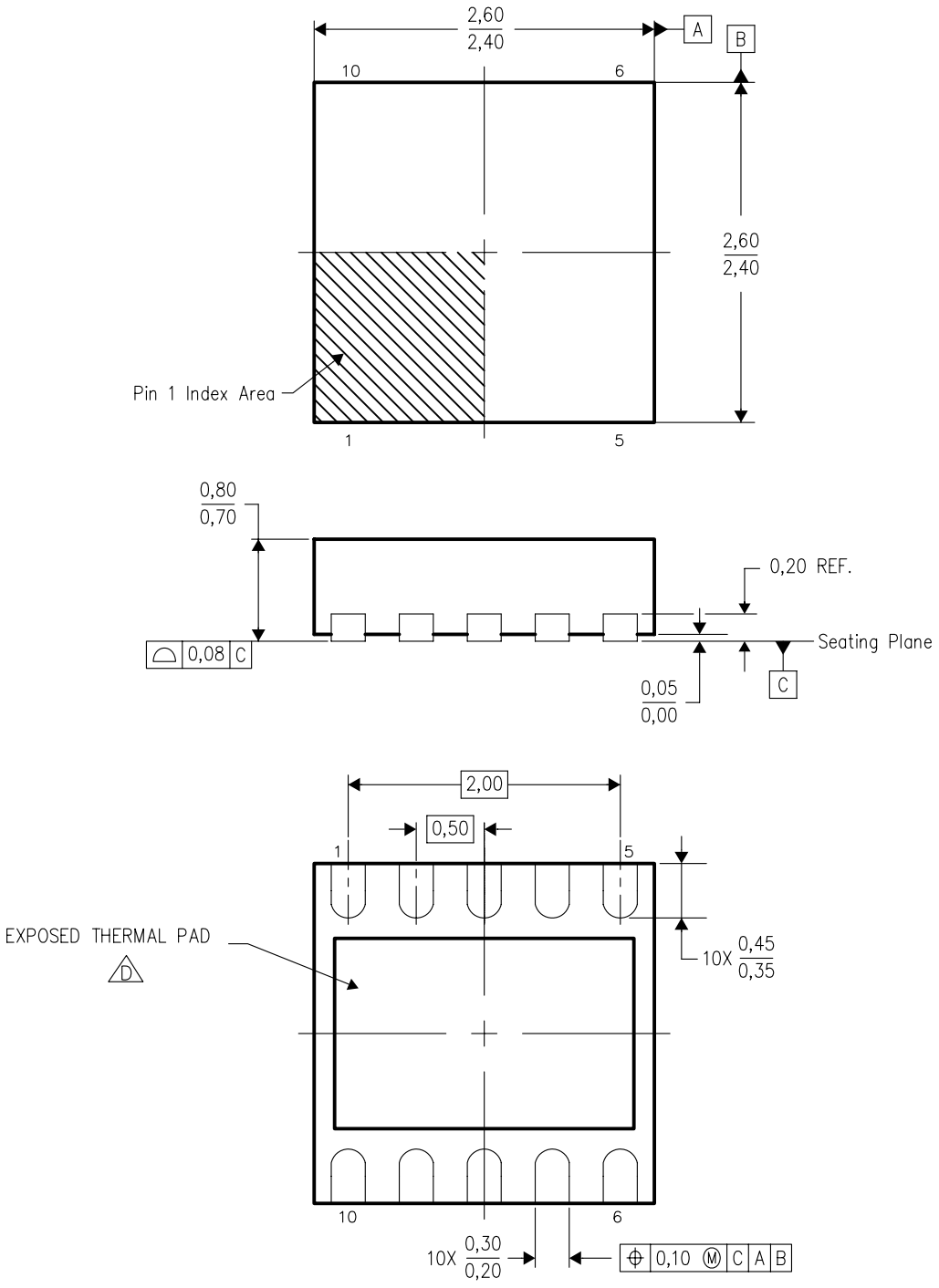
2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DSK (S–PDSO–N10) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

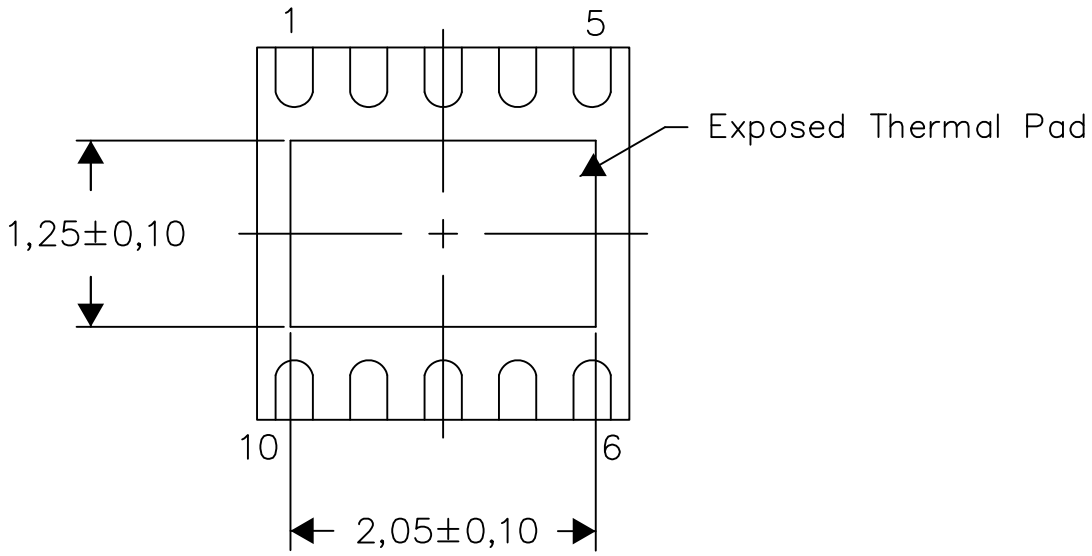
DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



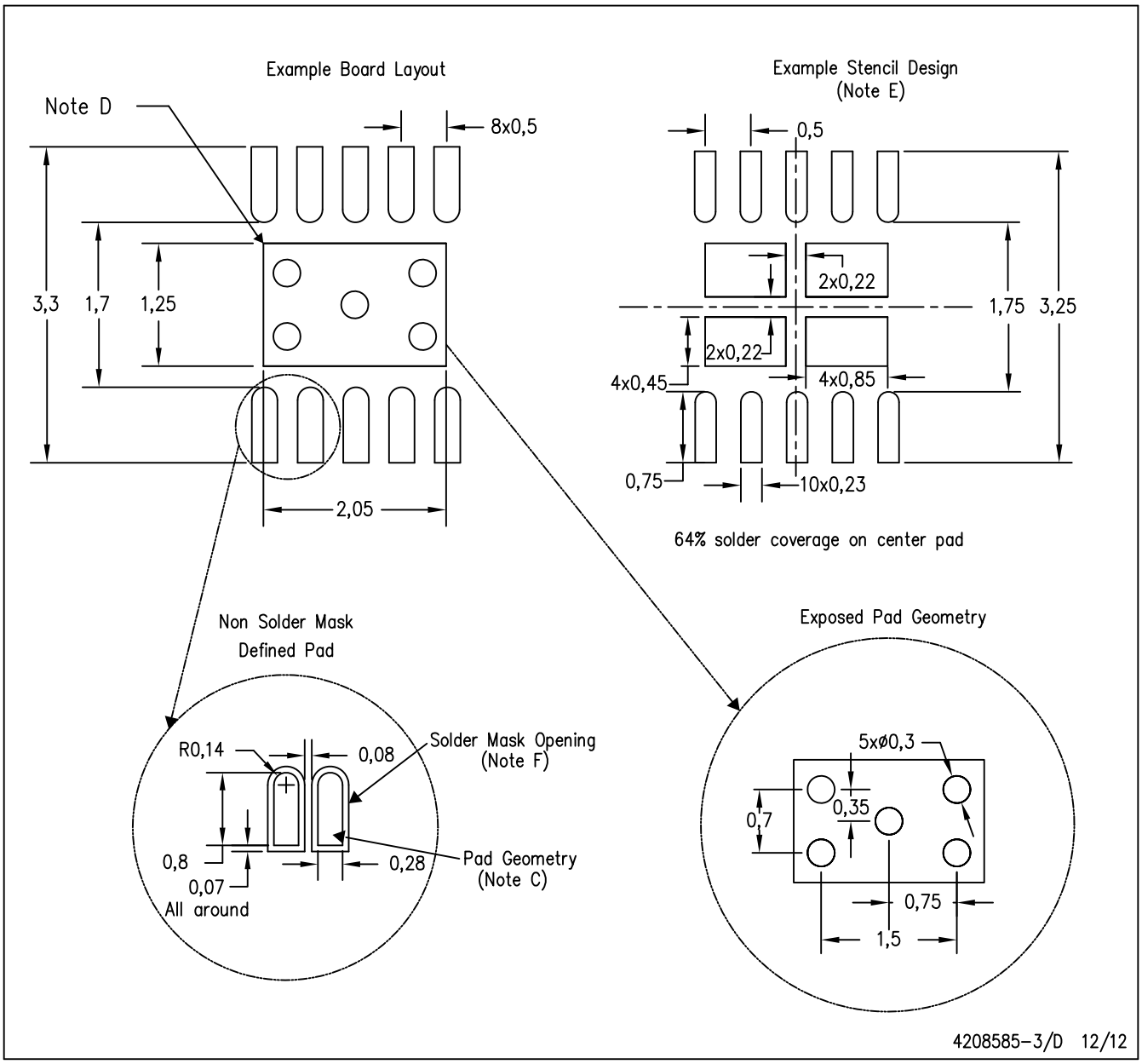
Bottom View

Exposed Thermal Pad Dimensions

4208579–3/E 12/12

NOTE: All linear dimensions are in millimeters

DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

最后更新日期：2025 年 10 月