SN75ALS193 四路差分线路接收器

1 特性

- 符合或超出 ANSI 标准 EIA/TIA-422-B 和 EIA/TIA-423-A 以及 ITU 建议 V.10 和 V.11 的要求
- 适用于嘈杂环境中长总线上的多点总线传输
- 三态输出
- 共模输入电压范围：-7V 至 7V
- 输入灵敏度：±200mV
- 输入迟滞：120mV（典型值）
- 高输入阻抗：12kΩ（最小值）
- 由 5V 单电源供电
- 低电源电流要求（最高 35mA）
- 较 AM26LS32A 版本改善了速度和功耗

2 应用

- 电机驱动器
- 工厂自动化和控制

3 说明

SN75ALS193 是一款采用高级低功耗肖特基技术、具有三态输出的单片四路线路接收器。该技术在 bar 设计、加工生产和晶圆制造方面实现了综合改进，因此，与其他设计相比，显著降低了功耗要求并允许高得多的数据吞吐量。此器件符合 ANSI 标准 EIA/TIA-422-B 和 EIA/TIA-423-A 以及 ITU 建议 V.10 和 V.11 的规范要求。它具有三态输出，允许直接连接到总线式系统，并且采用失效防护设计，可确保在输入处于开路状态时输出始终处于高电平状态。

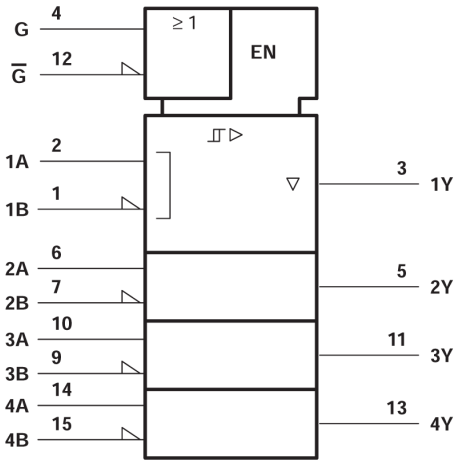
该器件经优化，能够以高达 20 兆位/秒的速率实现平衡多点总线传输。该输入具有高输入阻抗、用于提高抗噪性的输入迟滞、以及在 –7V 至 7V 共模输入电压范围内 ±200mV 的输入灵敏度。该器件还具有四个通道所共用的高电平有效和低电平有效使能功能。SN75ALS193 与 ’ ALS192 四路差分线路驱动器配合使用时，可实现卓越性能。

SN75ALS193 的额定工作温度范围为 0°C 至 70°C。

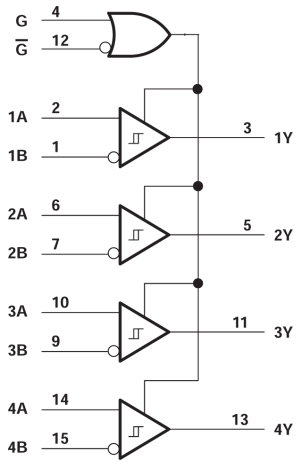
封装信息

器件型号	封装(1)	封装尺寸(2)
SN75ALS193	N（PDIP，16）	19.3mm × 9.4mm
	D（SOIC，16）	9.9mm × 6mm

(1) 如需更多信息，请参阅 节 10。
(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。



逻辑符号†



逻辑图（正逻辑）

† 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

Table of Contents

4 Pin Configuration and Functions

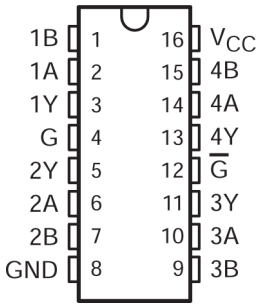


图 4-1. D or N Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
G	4	I	Active High Enable
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
$\overline{G}$	12	I	Active Low Enable
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
V_{CC}	16	PWR	Device VCC (4.75V to 5.25V)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage, see (2)		7	V
V_I	Input voltage, A or B		±15	V
V_{ID}	Differential input voltage, see (3)		±15	V
V_I	Enable input voltage		7	V
I_{OL}	Low-level output current		50	mA
	Continuous total dissipation	See *Dissipation Rating* table		
T_A	Operating free-air temperature range	0	70	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds		300	°C
T_{stg}	Storage temperature range	– 65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to network ground terminal.
(3) Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Rating

PACKAGE	$T_A \leqslant 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
N	1150 mW	9.2 mW/°C	736 mW

5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 400	µA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0	70		°C

5.4 Thermal Information

THERMAL METRIC(1)		SN75ALS193		UNIT
		N (PDIP)	D (SOIC)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	43.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	43.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	42.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					200	mV
V_{IT-}	Negative-going input threshold voltage			−200(3)			mV
V_{hys}	Hysteresis voltage (V_{IT+} -V_{IT-})				120		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −400 μA,	V_{ID} = 200 mV, See Figure 1	2.5	1.6		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = MAX	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	
I_I	Line input current	Other input at 0, See (4)	V_{CC} = MIN, V_I = 15 V		0.7	1.2	mA
			V_{CC} = MIN, V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current	V_{CC} = MAX	V_{IH} = 2.7 V			20	μA
			V_{IH} = MAX			100	
I_{IL}	Low-level enable-input current	V_{CC} = MAX,	V_{IL} = 0.4 V			−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_O = 0,	V_{ID} = 3 V, See (5)	−15	−78	−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	Outputs disabled		22	35	mA

(1) For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
(4) Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-A for exact conditions.
(5) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

5.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V			15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF	See 图 6-1		15	22	
t_{PZH}	Output enable time to high level	C_L =15 pF	See 图 6-2		13	25	
					11	25	
t_{PHZ}	Output disable time from high level	C_L = 5 pF	See 图 6-2		13	25	
					15	22	

5.7 Typical Characteristics

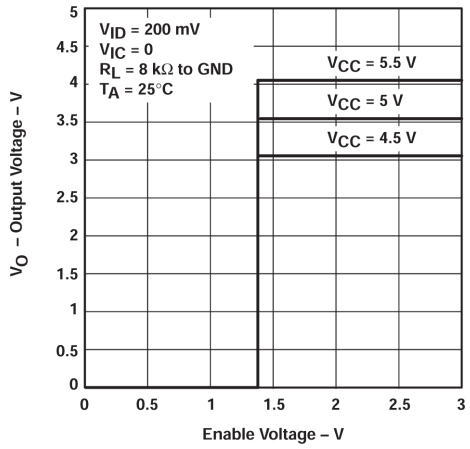


图 5-1. Output Voltage vs Enable Voltage

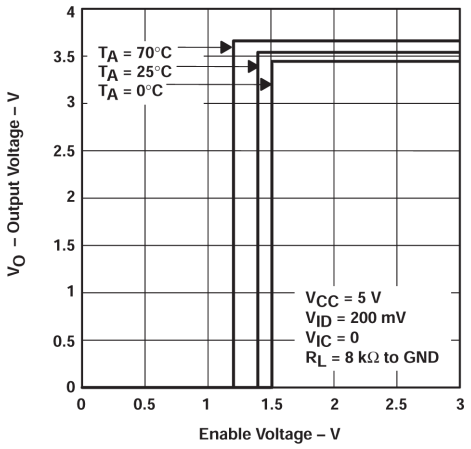


图 5-2. Output Voltage vs Enable Voltage

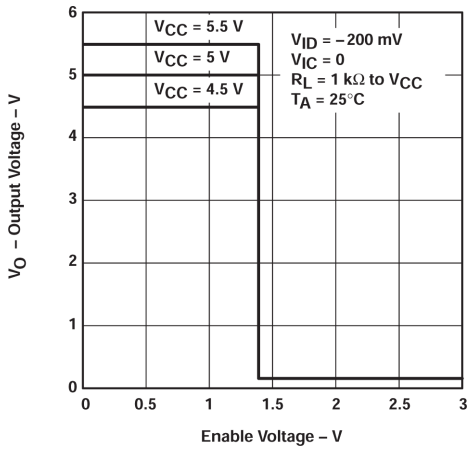


图 5-3. Output Voltage vs Enable Voltage

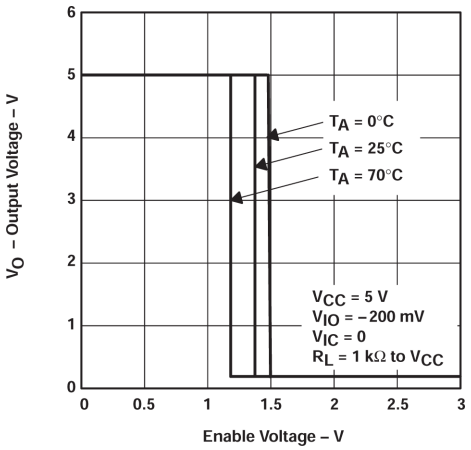


图 5-4. Output Voltage vs Enable Voltage

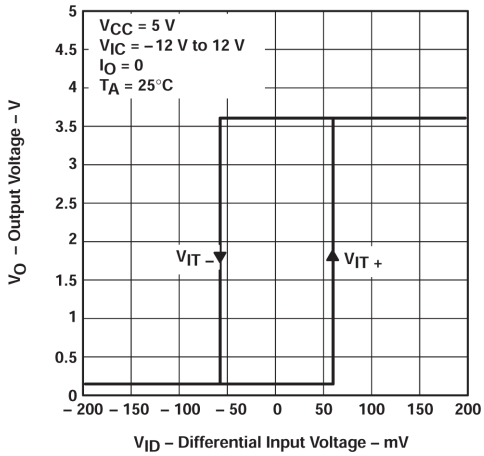


图 5-5. Output Voltage vs Differential Input Voltage

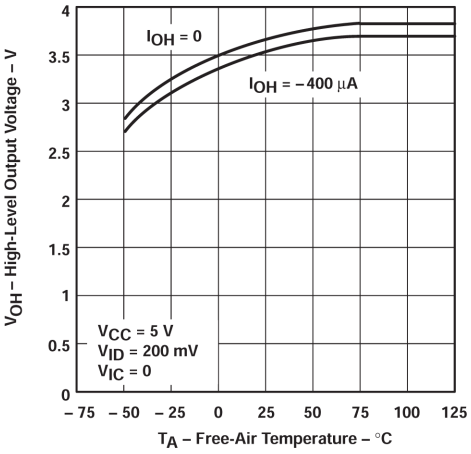


图 5-6. High-level Output Voltage vs Free-air Temperature

5.7 Typical Characteristics (continued)

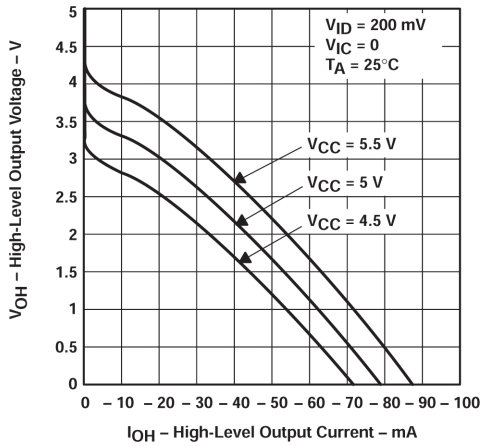


图 5-7. High-level Output Voltage vs High-level Output Current

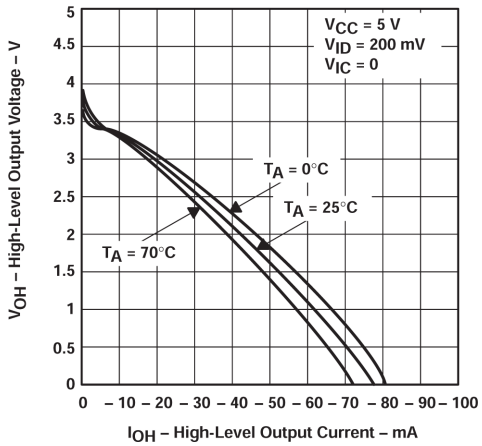


图 5-8. High-level Output Voltage vs High-level Output Current

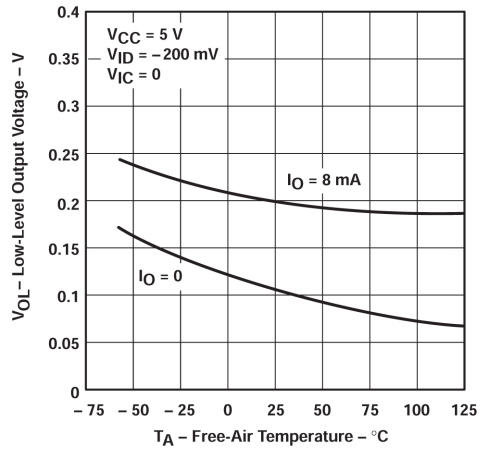


图 5-9. Low-level Output Voltage vs Free-air Temperature

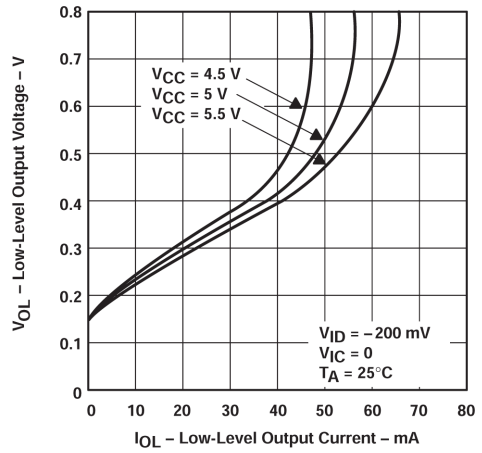


图 5-10. Low-level Output Voltage vs Low-level Output Current

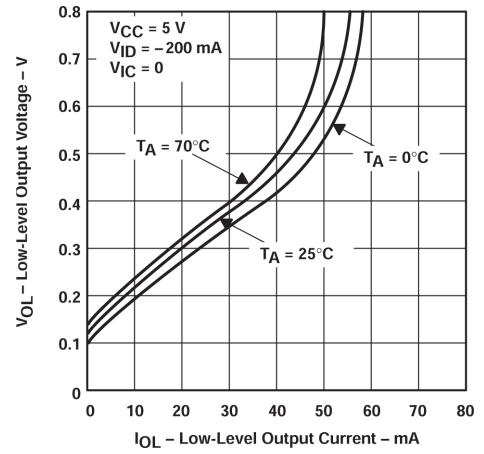


图 5-11. Low-level Output Voltage vs Low-level Output Current

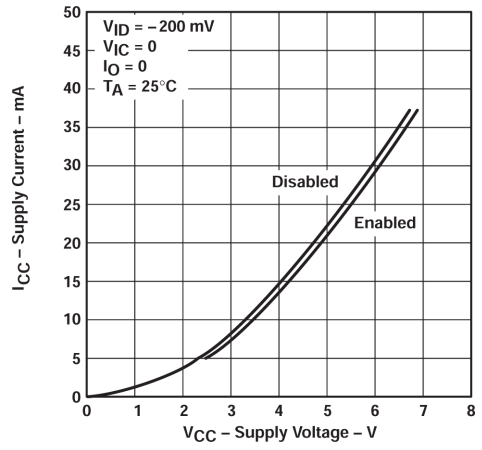


图 5-12. Supply Current vs Supply Voltage

5.7 Typical Characteristics (continued)

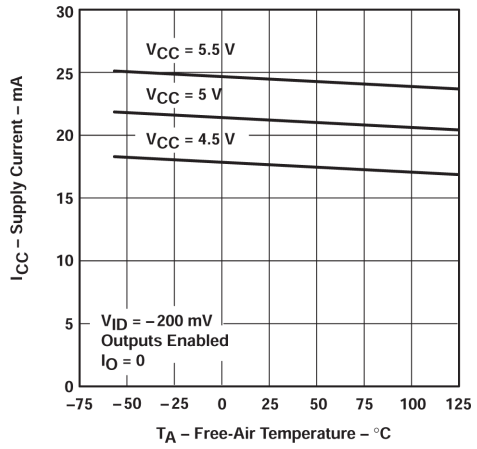


图 5-13. Supply Current vs Free-air Temperature

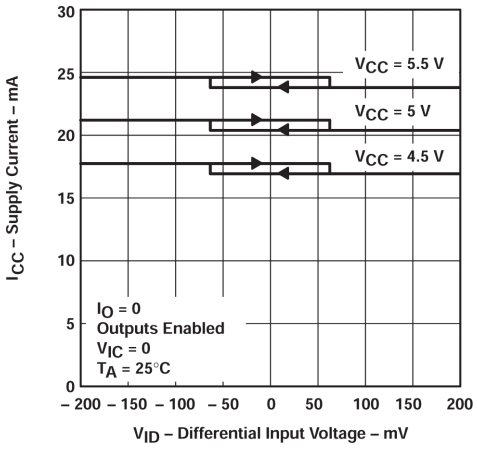


图 5-14. Supply Current vs Differential Input Voltage

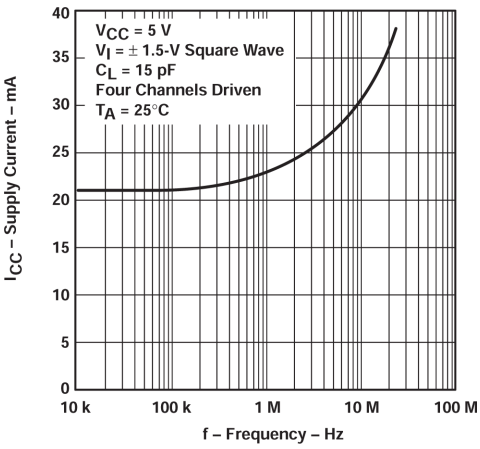


图 5-15. Supply Current vs Frequency

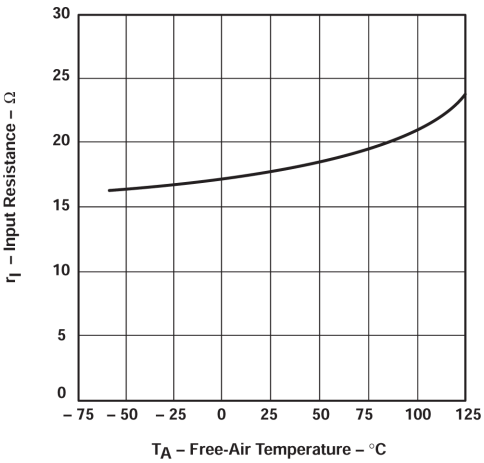


图 5-16. Input Resistance vs Free-air Temperature

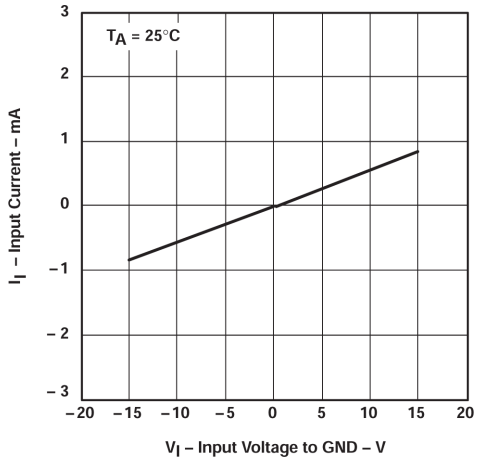


图 5-17. Input Current vs Input Voltage to GND

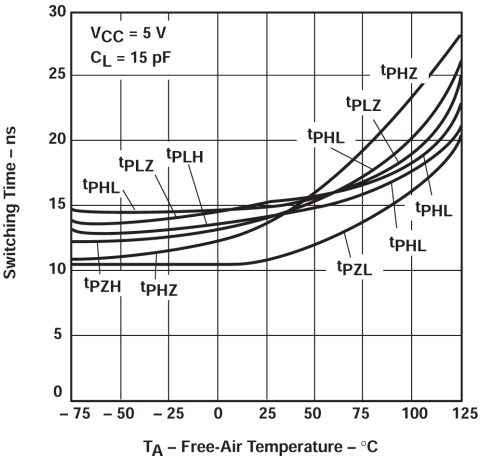


图 5-18. Switching Time vs Free-air Temperature

5.7 Typical Characteristics (continued)

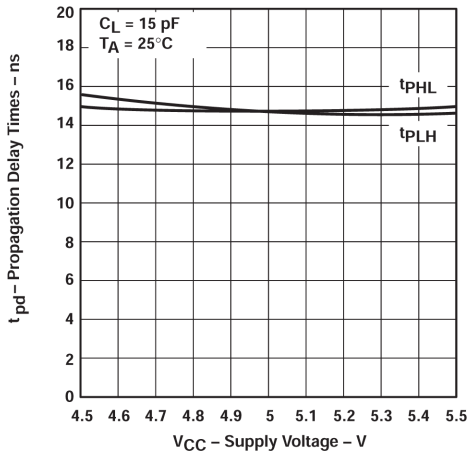


图 5-19. Propagation Delay Time vs Supply Voltage

6 Parameter Measurement Information

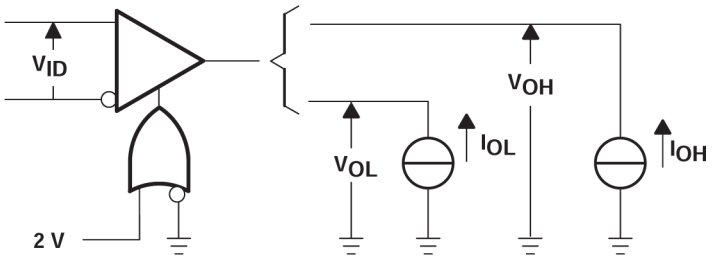
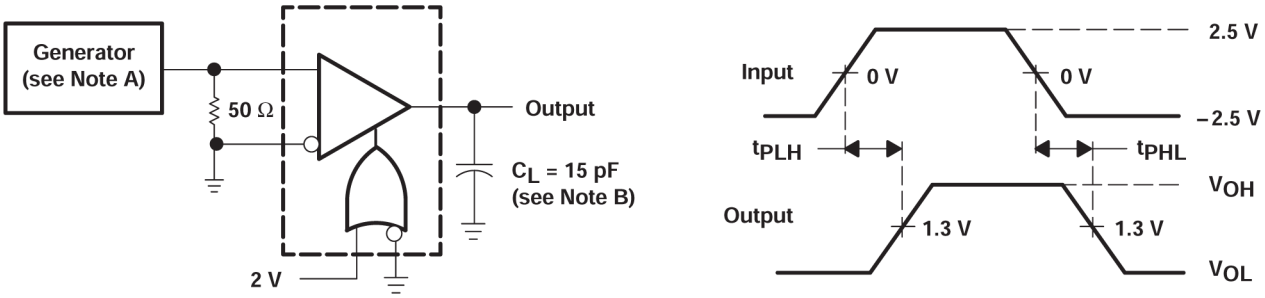


图 6-1. V_{OH}, V_{OL}

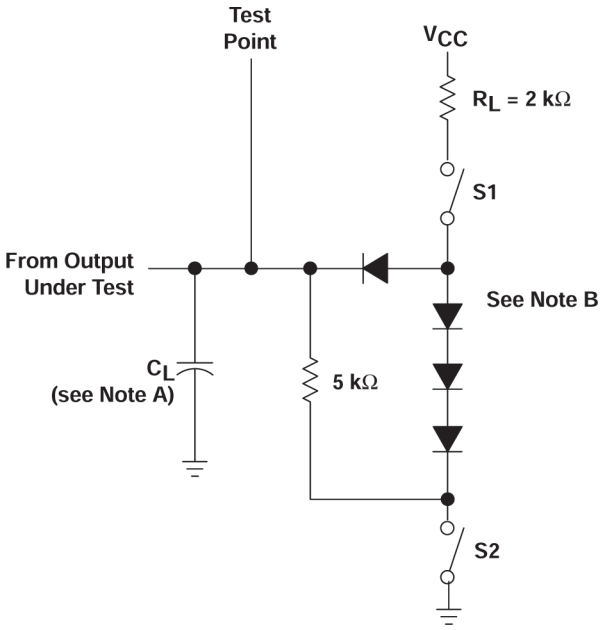


TEST CIRCUIT　　VOLTAGE WAVEFORMS

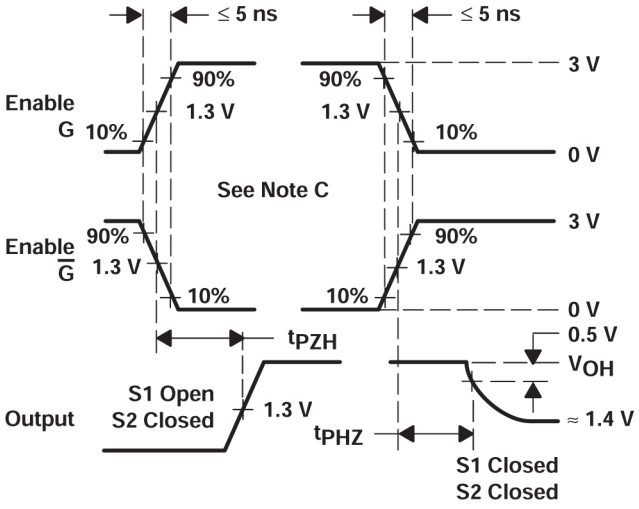
A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, duty cycle ⩽ 50%, Z_O = 50 Ω, t_r ⩽ 6 ns, t_f ⩽ 6 ns.

B. C_L includes probe and jig capacitance.

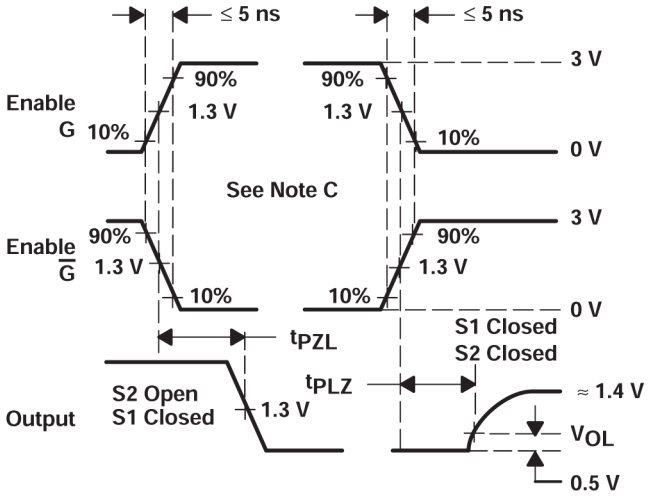
图 6-2. Test Circuit and Voltage Waveforms



LOAD CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

图 6-3. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

DIFFERENTIAL INPUTS A – B(1)	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

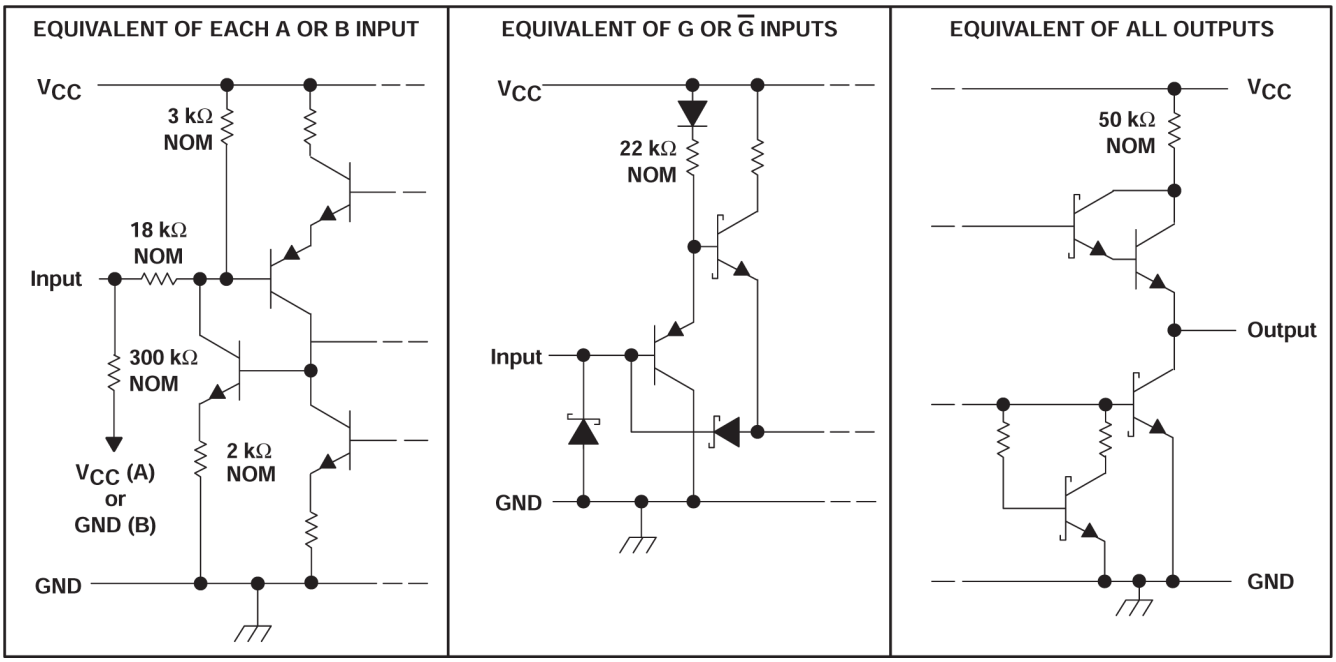


图 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (May 1995) to Revision E (October 2023)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS193D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	75ALS193
SN75ALS193DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193
SN75ALS193DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193
SN75ALS193DRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193
SN75ALS193DRG4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193
SN75ALS193N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	(SN75ALS193N, SN7ALS193N)
SN75ALS193N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	(SN75ALS193N, SN7ALS193N)
SN75ALS193NE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	(SN75ALS193N, SN7ALS193N)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

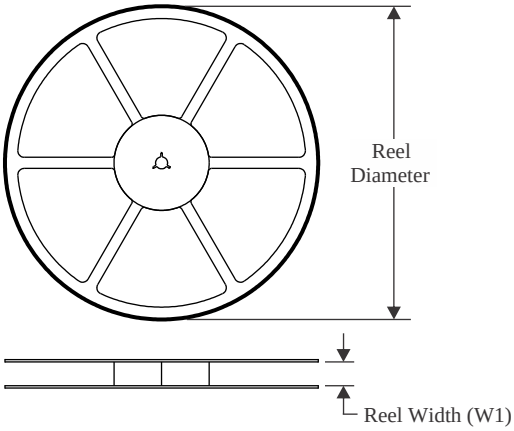
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

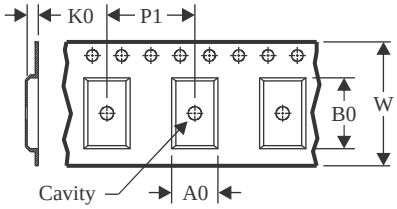
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

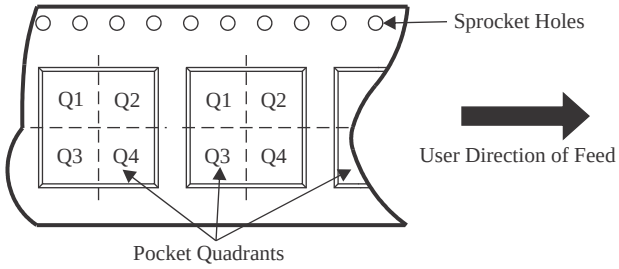


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

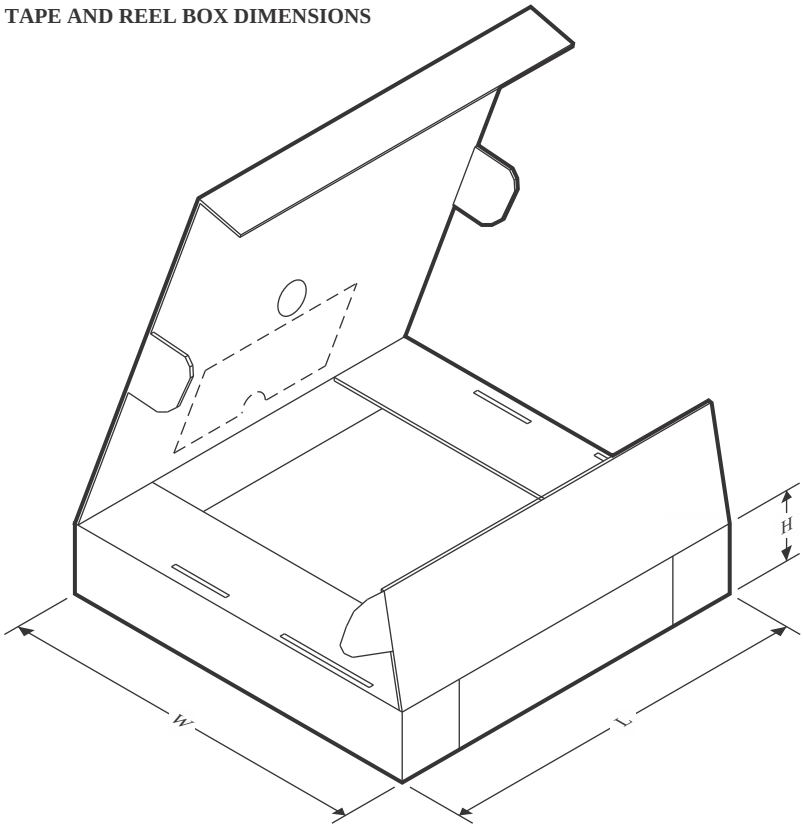
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS193DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75ALS193DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

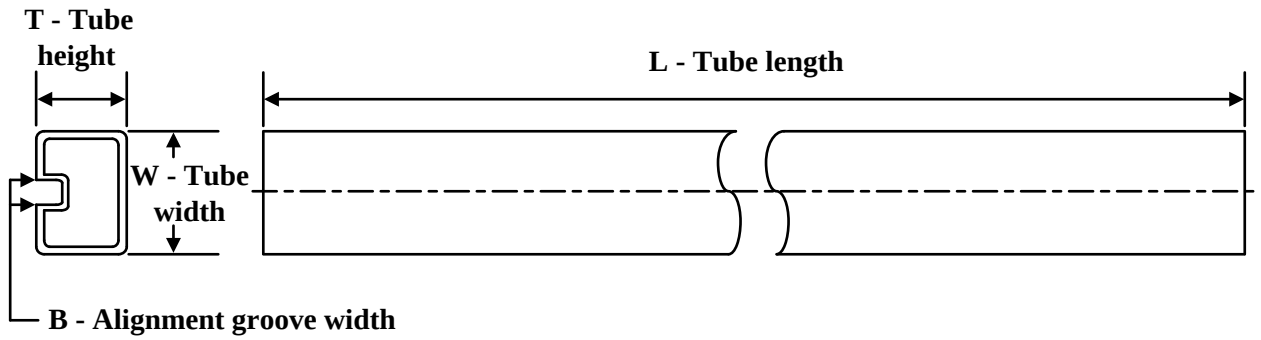
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS193DR	SOIC	D	16	2500	340.5	336.1	32.0
SN75ALS193DRG4	SOIC	D	16	2500	353.0	353.0	32.0

TUBE



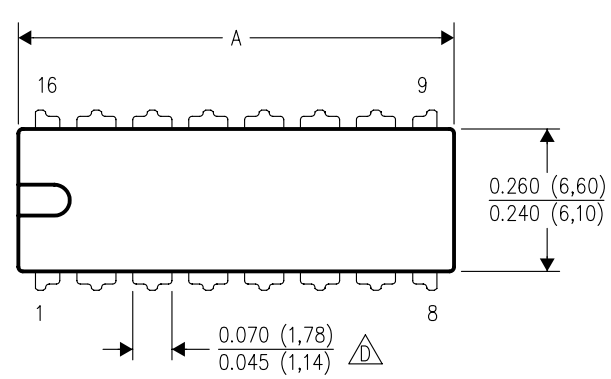
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS193N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS193N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS193NE4	N	PDIP	16	25	506	13.97	11230	4.32

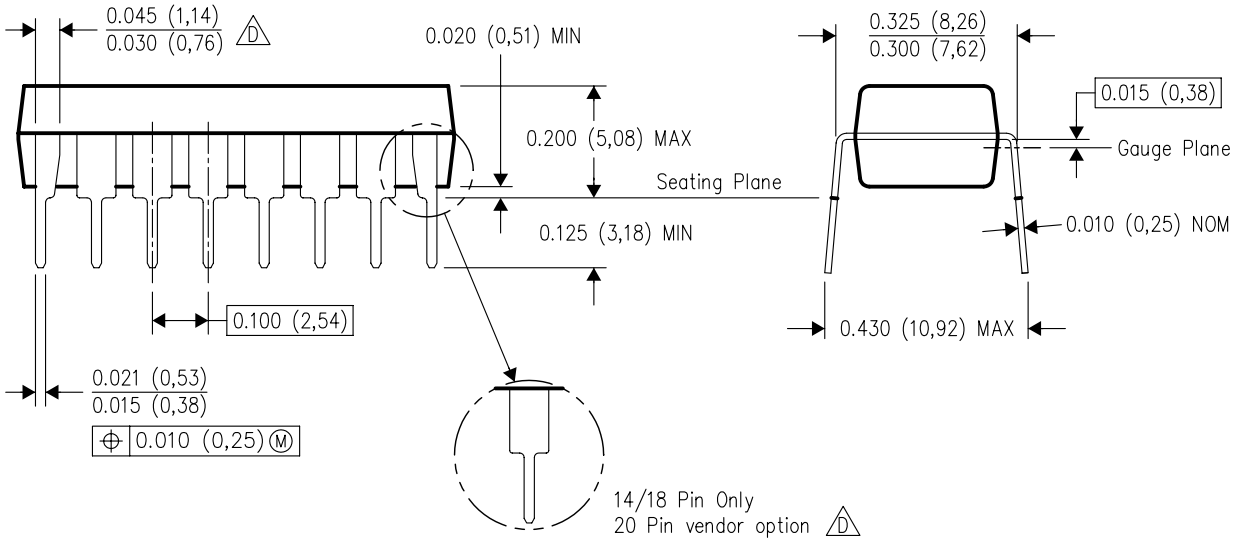
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



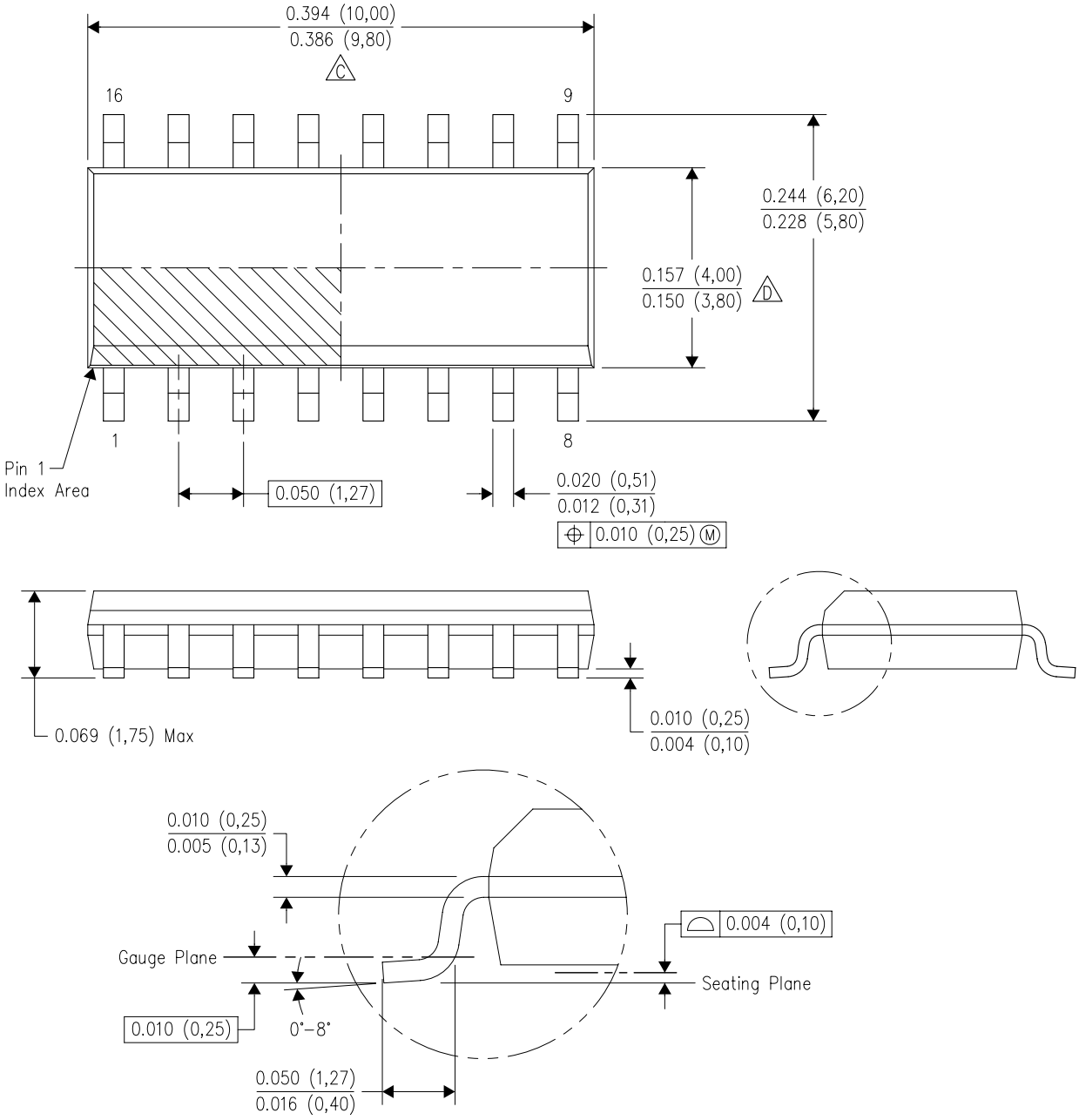
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

最后更新日期：2025 年 10 月