

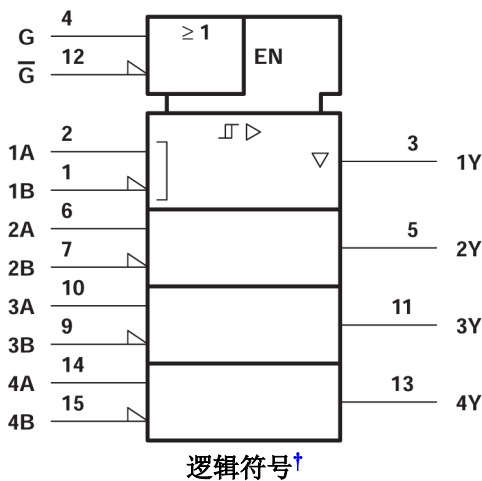
SN75ALS173 四路差分线路接收器

1 特性

- 符合或超出 ANSI EIA/TIA-422-B、EIA/TIA-423-B 和 RS-485 的要求
- 符合或超出 ITU 建议 V.10、V.11、X.26 和 X.27 的要求
- 适用于嘈杂环境中长总线上的多点总线传输
- 三态输出
- 12V 至 12V 的共模输入电压范围
- 输入灵敏度： $\pm 200\text{mV}$
- 输入迟滞：50mV (典型值)
- 高输入阻抗：12k Ω (最小值)
- 由 5V 单电源供电
- 低电源电流要求 (最高 27mA)

2 应用

- 电机驱动器
- 工厂自动化和控制



3 说明

SN75ALS173 是一款具有三态输出的单片四路差分线路接收器，满足 ANSI 标准 EIA/TIA-422-B、EIA/TIA-423-B、RS-485 以及数项 ITU 建议的要求。先进的低功耗肖特基技术可提供高速度，但不会导致常见的功率损耗。四个接收器共用一对进行了“或”运算的使能端。G 高电平或 $\overline{G}$ 低电平可启用所有接收器。该器件具有高输入阻抗、用于提高抗噪性的输入迟滞、以及在 -12V 至 12V 共模输入电压范围内 $\pm 200\text{mV}$ 的输入灵敏度。

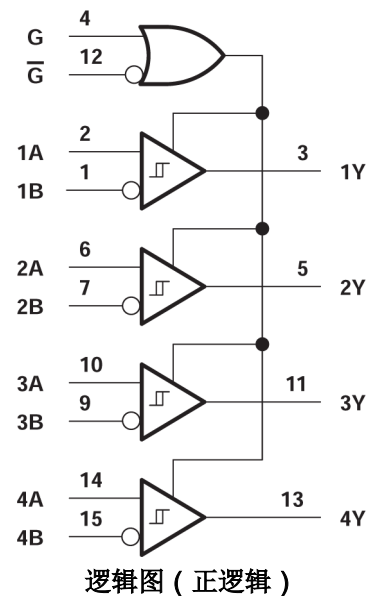
SN75ALS173 的额定工作温度范围为 0°C 至 70°C。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
SN75ALS173	N (PDIP, 16)	19.3mm × 9.4mm
	NS (SOP, 16)	10.2mm × 7.8mm

(1) 如需更多信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



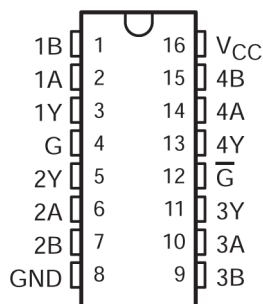
[†] 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。



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4 Pin Configuration and Functions



A. The NS package is only available left-end taped and reeled (order device SN75ALS173 NSLE).

图 4-1. N or NS Package (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
G	4	I	Active High Enable
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
G	12	I	Active Low Enable
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
V _{CC}	16	PWR	Device VCC (4.75 V to 5.25 V)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage, (see ⁽²⁾)		7	V
V_I	Input voltage, (A or B inputs)		± 14	V
V_{ID}	Differential input voltage, (see ⁽³⁾)		± 14	V
V_I	Enable input voltage		7	V
I_{OL}	Low-level output current		50	mA
	Continuous total dissipation	See Dissipation Rating Table		
T_A	Operating free-air temperature range	0	70	°C
T_{stg}	Storage temperature range	– 65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential input voltage, are with respect to network ground terminal.
- (3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Rating Table

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				± 12	V
Differential input voltage, V_{ID}				± 12	V
High-level input voltage, V_{IH}	G, $\overline{G}$	2			V
Low-level input voltage, V_{IL}	G, $\overline{G}$			0.8	V
High-level output current, I_{OH}				– 400	μA
Low-level output current, I_{OL}				8	mA
Operating free-air temperature, T_A		0		70	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN75ALS173		UNIT
		N (PDIP)	NS (SOP)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	13.5	°C/W

5.4 Thermal Information (续)

THERMAL METRIC ⁽¹⁾		SN75ALS173		UNIT
		N (PDIP)	NS (SOP)	
		16 Pins	16 Pins	
ψ_{JB}	Junction-to-board characterization parameter	40.3	50.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted) (see [Note 3](#))

PARAMETER			TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage							200	mV
V _{IT-}	Negative-going input threshold voltage					-200 ⁽²⁾			mV
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})					50			mV
V _{IK}	Input clamp voltage	G, $\overline{G}$	I _I = -18 mA					-1.5	V
V _{OH}	High-level output voltage		V _{ID} = 200 mV,	I _{OH} = -400 μA,	See 图 6-1	2.7			v
V _{OL}	Low-level output voltage		V _{ID} = -200 mV,	I _{OL} = 8 mA,	See 图 6-1			0.45	v
I _{OZ}	High-impedance-state output current		V _O = 0.4 V to 2.4 V					-20	μA
I _I	Line input current		Other input at 0 V		V _I = 12 V			1	mA
					V _I = -7 V			-0.8	
I _{IH}	High-level input current	G, $\overline{G}$	V _{IH} = 2.7 V					20	μA
I _{IL}	Low-level input current	G, $\overline{G}$	V _{IL} = 0.4 V					-100	μA
r _i	Input resistance					12			kΩ
I _{OS}	Short-circuit output current		See Note 4			-15		-85	mA
I _{CC}	Supply current (total package)		No load,	Outputs enabled		16		24	mA
			No load,	Outputs disabled		18		27	

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

(3) Refer to ANSI Standard RS-485 for exact conditions.

(4) The duration of the short circuit should not cause the maximum package power dissipation to be exceeded.

5.6 Switching Characteristics

$V_{CC} = 5 \text{ V}, C_L = 15 \text{ pF}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	$V_{ID} = -2.5 \text{ V to } 2.5 \text{ V},$ See 图 6-2	9	18	27	ns
t_{PLH}	Propagation delay time, low- to high-level output		9	18	27	ns
t_{PZH}	Output enable time to high level	See 图 6-3	4	12	18	ns
t_{PZL}	Output enable time to low level	See 图 6-4	6	13	21	ns
t_{PHZ}	Output disable time from high level	See 图 6-3	10	21	27	ns
t_{PLZ}	Output disable time from low level	See 图 6-4	8	15	25	ns

6 Parameter Measurement Information

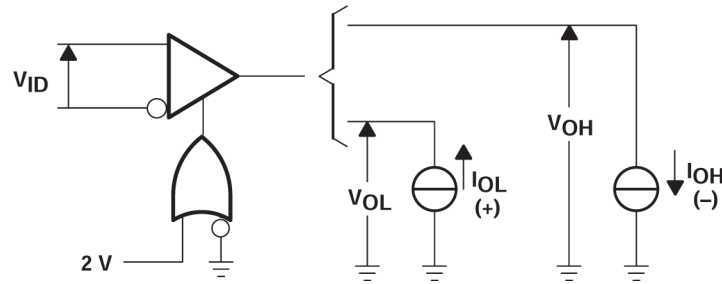


图 6-1. V_{OH} , V_{OL}

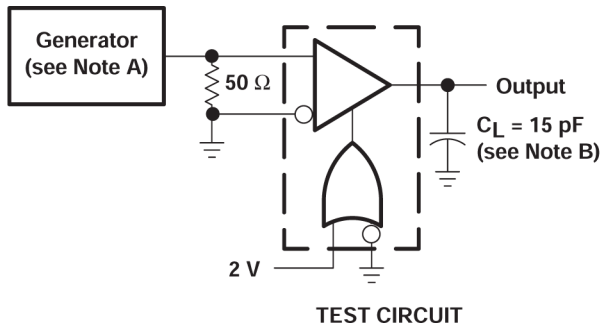
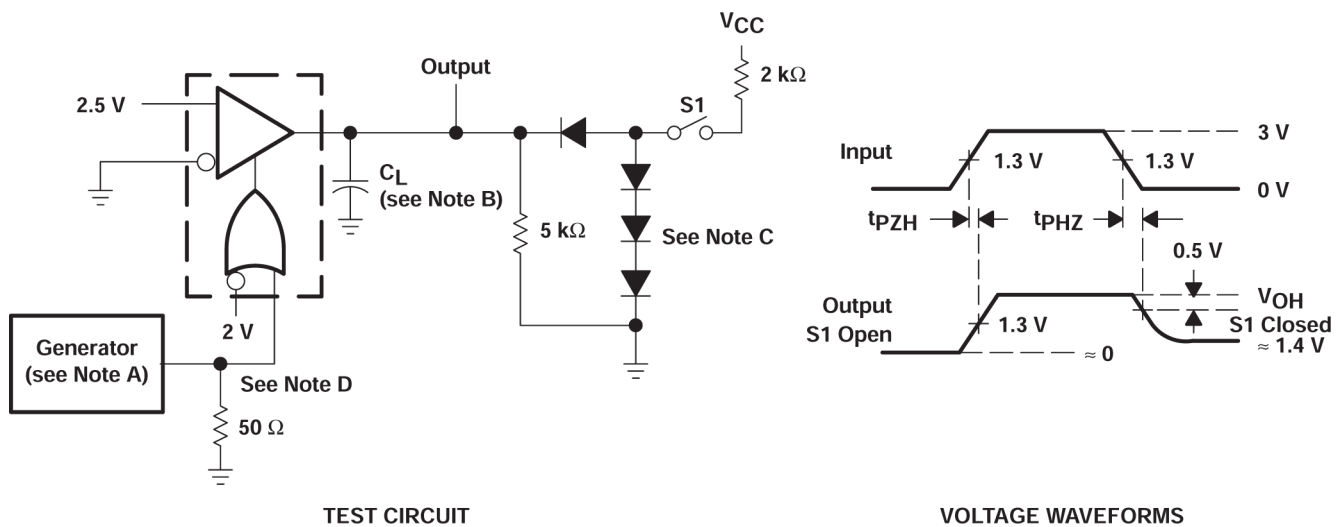
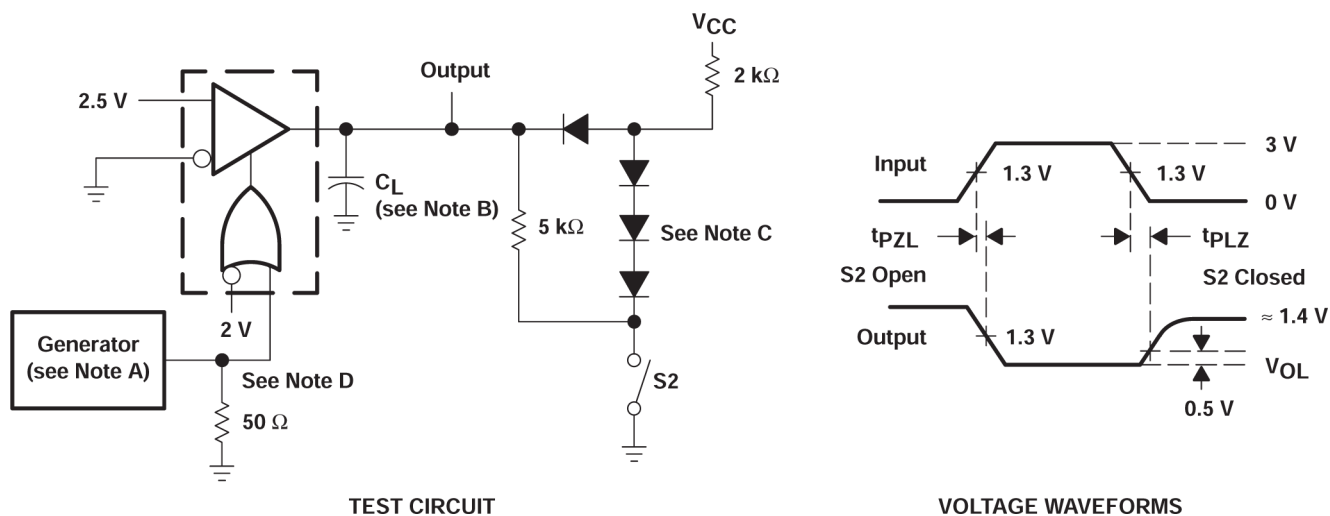


图 6-2. Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.
- D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

图 6-3. Test Circuit and Voltage Waveforms



- The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- C_L includes probe and jig capacitance.
- All diodes are 1N916 or equivalent.
- To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

图 6-4. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

DIFFERENTIAL A - B	ENABLES ⁽¹⁾		OUTPUT Y
	G	G	
$V_{ID} \geq 0.2 \text{ V}$	H	X	H
	X	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	H	X	?
	X	L	?
$V_{ID} < -0.2 \text{ V}$	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

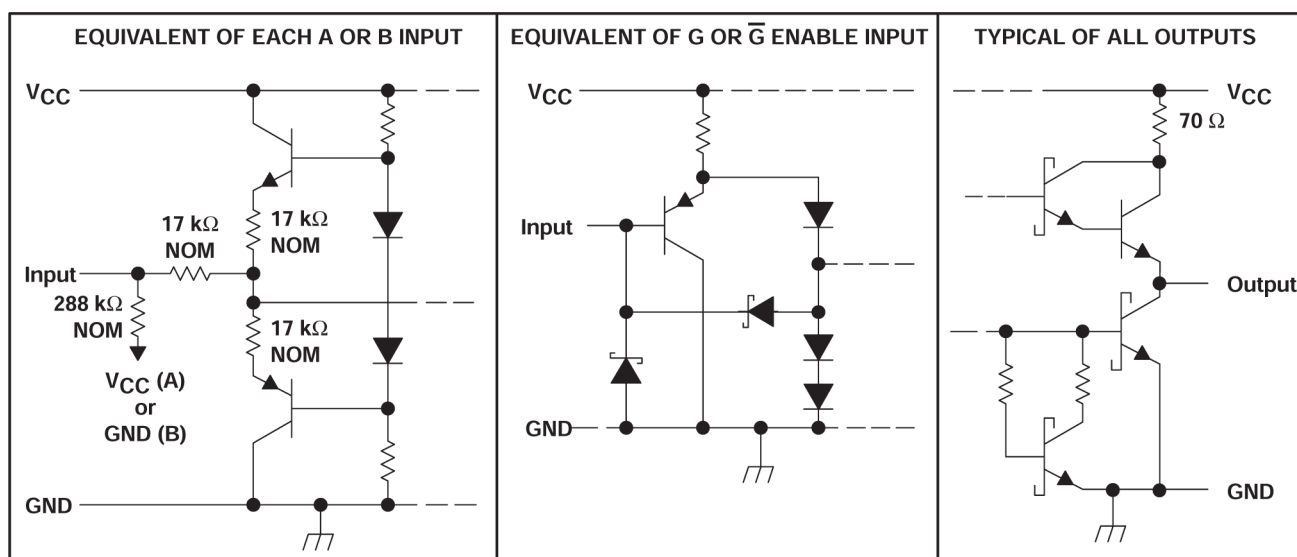


图 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (May 1995) to Revision D (October 2023)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS173N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS173N
SN75ALS173N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS173N
SN75ALS173NS	Obsolete	Production	SOP (NS) 16	-	-	Call TI	Call TI	0 to 70	75ALS173
SN75ALS173NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS173
SN75ALS173NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS173
SN75ALS173NSRG4	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS173

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

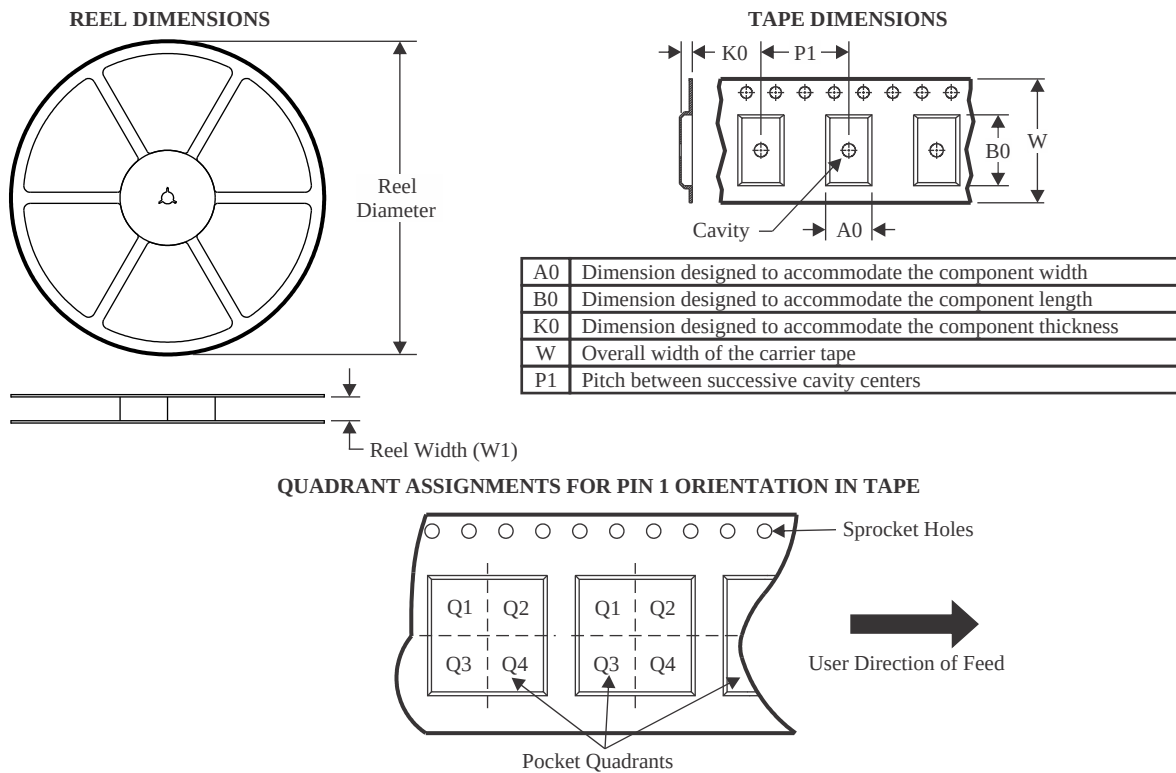
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

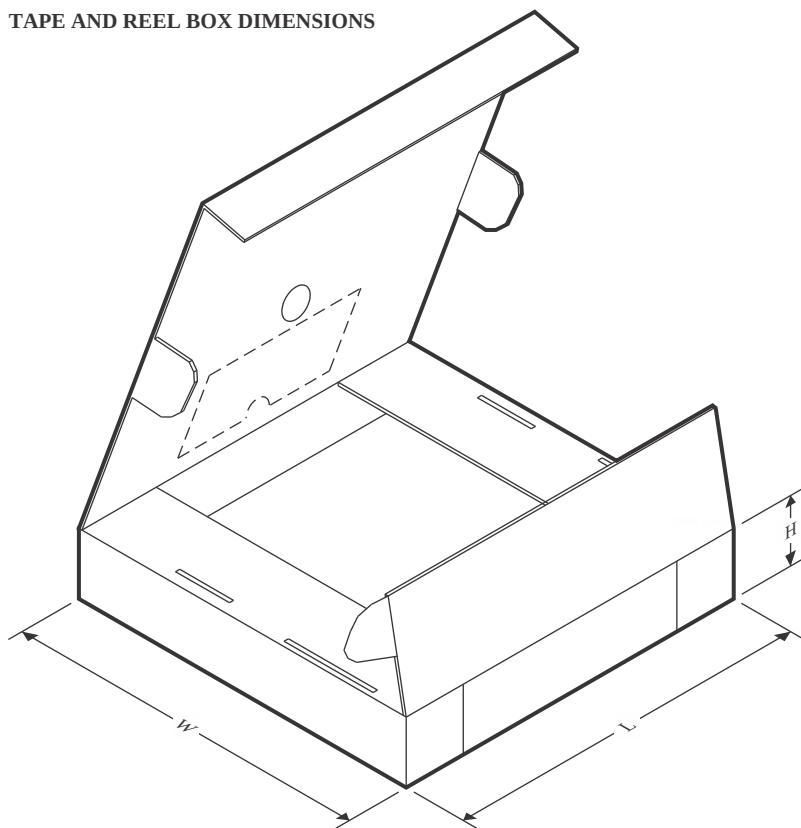
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS173NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

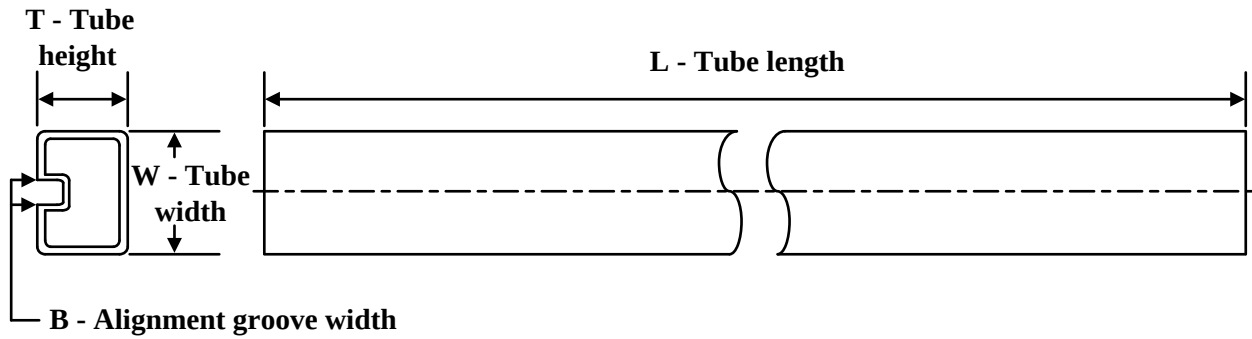
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS173NSR	SOP	NS	16	2000	353.0	353.0	32.0

TUBE



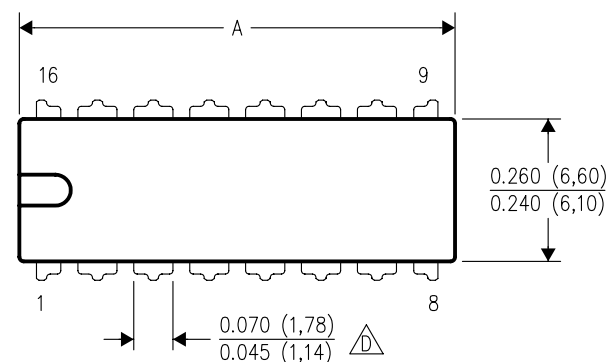
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS173N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS173N.A	N	PDIP	16	25	506	13.97	11230	4.32

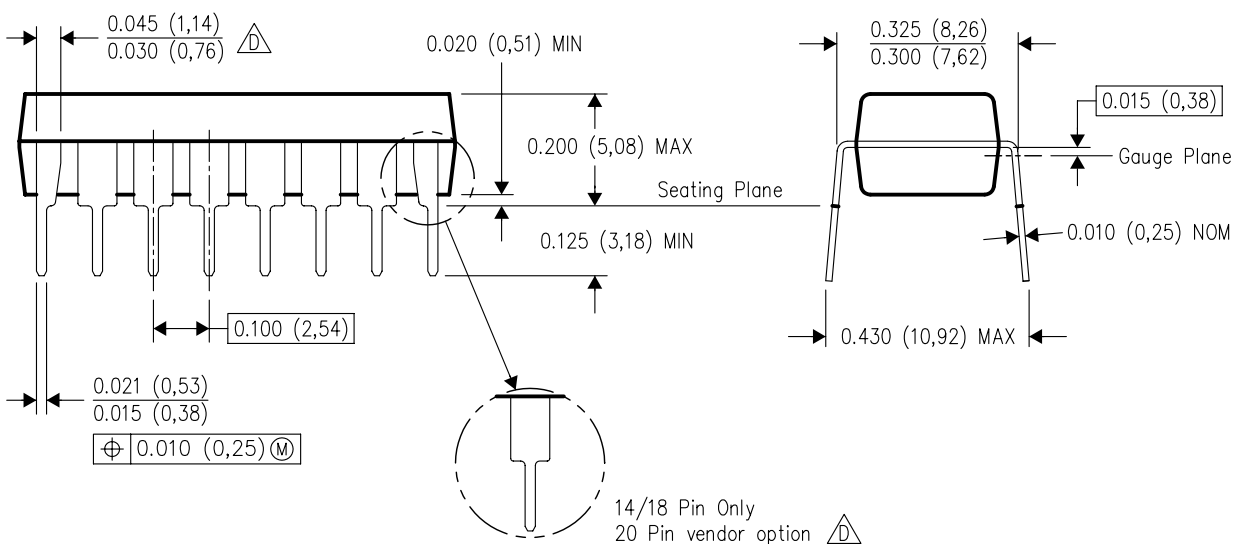
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



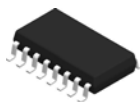
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

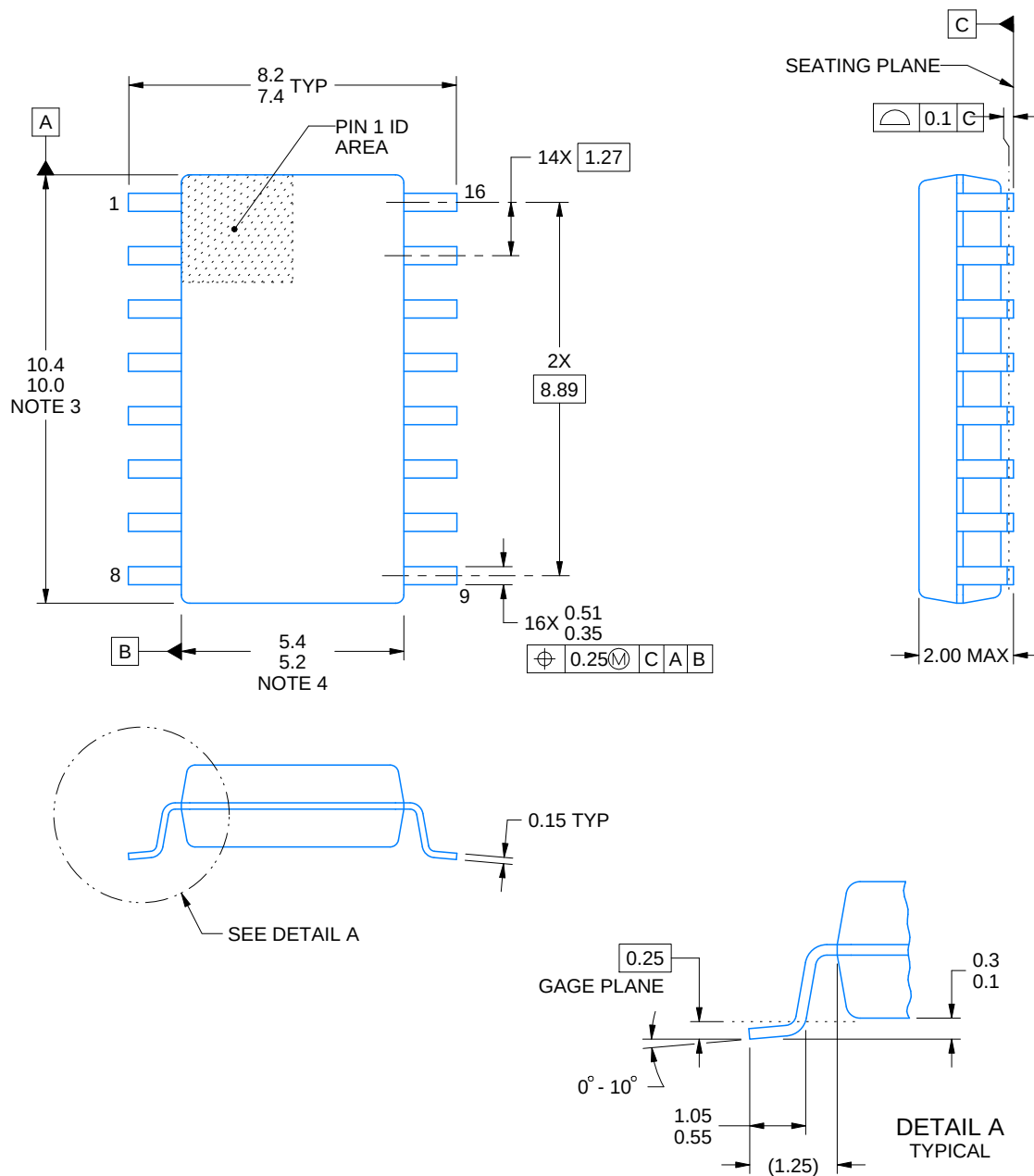


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

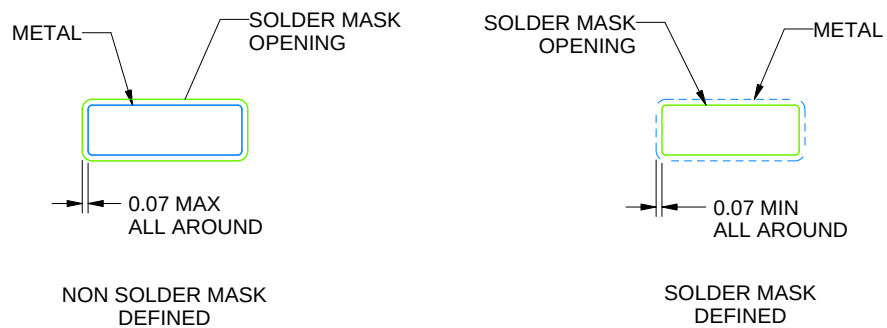
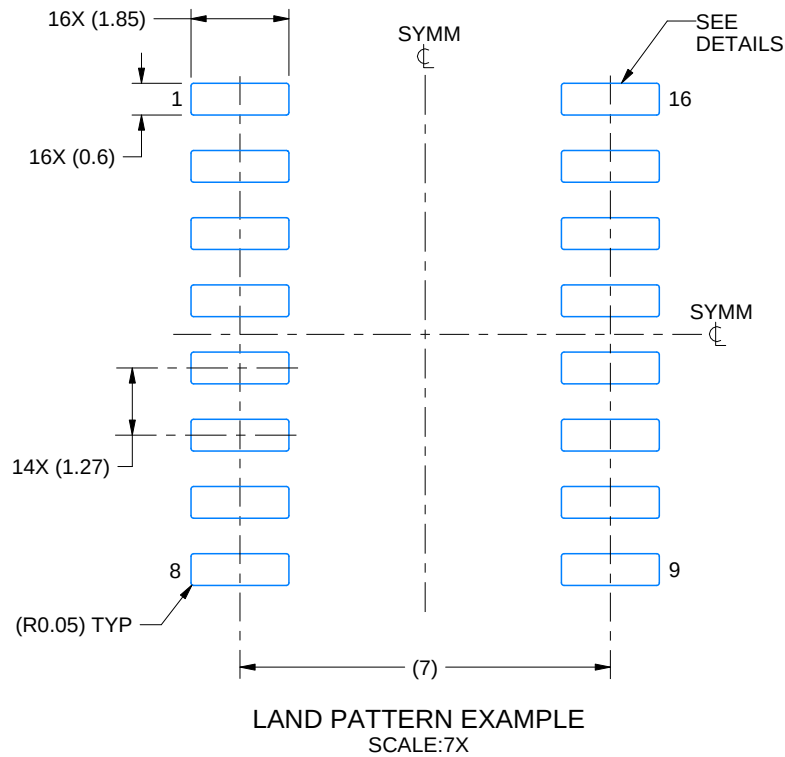
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



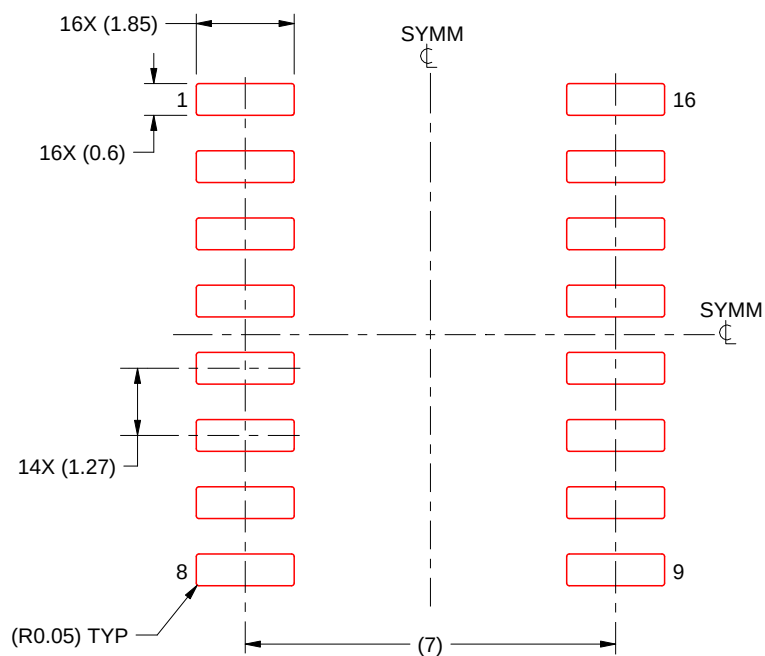
SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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