SN75179B 差分驱动器和接收器对

1 特性

- 符合或超出 TIA/EIA-422-B、TIA/EIA-485-A 和 ITU Recommendation V.11 的要求
- 总线电压范围：-7V 至 12V
- 正负电流限制
- 驱动器输出能力：60mA（最大值）
- 驱动器热关断保护
- 接收器输入阻抗：12kΩ（最小值）
- 接收器输入灵敏度：±200mV
- 接收器输入迟滞：50mV（典型值）
- 由 5V 单电源供电
- 低功耗要求

2 说明

SN75179B 是一款差分驱动器和接收器对，专为平衡传输线路应用而设计，符合 TIA/EIA-422-B、TIA/EIA-485-A 和 ITU Recommendation V.11 的要求。该器件旨在提高长总线线路上全双工数据通信的性能。

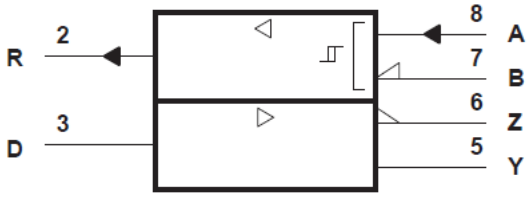
SN75179B 驱动器输出可限制正电流和负电流。该接收器具有高输入阻抗、用于提高抗噪性的输入迟滞，以及在 –7V 至 12V 共模输入电压范围内 ±200mV 的输入灵敏度。该驱动器还提供热关断功能，避免出现线路故障状况。热关断设计为在约 150°C 的结温下发生。SN75179B 旨在驱动高达 60mA 的电流负载。

SN75179B 的工作温度范围是 0°C 至 70°C。

封装信息

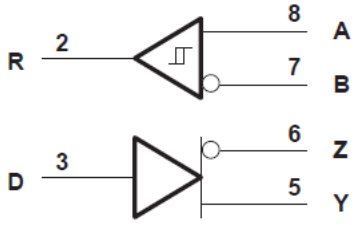
器件型号	封装(1)	封装尺寸(2)
SN75179B	D (SOIC)	4.9mm x 6mm
	P (PDIP)	9.81mm x 9.43mm
	PS (SOP)	6.2mm x 7.8mm

(1) 有关所有可用封装，请参阅 节 9。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



A. 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

逻辑符号



逻辑图（正逻辑）

Table of Contents

3 Pin Configuration and Functions

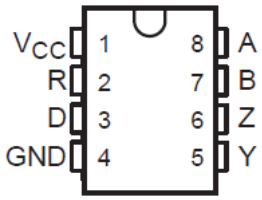


图 3-1. D, PS, or P Package
Top View

表 3-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1	V_{CC}	P	5V Voltage Supply
2	R	O	RS485 Logic Output
3	D	I	RS485 Logic Input
4	GND	G	Ground
5	Y	O	Non-Inverting RS485 Bus Output
6	Z	O	Inverted RS485 Bus Output
7	B	I	Inverted RS485 Bus Input
8	A	I	Non-Inverting RS485 Bus Input

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	–10	15	V
V_{ID}	Differential input voltage (3)		±25	V
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	Driver	2			V
V_{IL}	Low-level input voltage	Driver			0.8	V
V_{IC}	Common-mode input voltage		–7(1)		12	V
V_{ID}	Differential input voltage,				±12	V
I_{OH}	High level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low level output current	Driver			60	mA
		Receiver			8	mA
T_A	Operating free-air temperature		0		70	°C

(1) The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

4.3 Thermal Information

THERMAL METRIC(1)		SOIC (D)	PDIP (P)	SOP (PS)	UNIT
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	109.5	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	53.9	65.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	65.7	62.1	
ψ_{JT}	Junction-to-top characterization parameter	8.8	11.6	31.3	
ψ_{JB}	Junction-to-board characterization parameter	62.6	64.5	60.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

4.4 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See 图 5-1	1/2 V_{OD1}			V
				2(2)			
		R_L = 54 Ω	See 图 5-1	1.5	2.5	5	V
$\|V_{OD3}\|$	Differential output voltage	See (4)		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage					±0.2	V
V_{OC}	Common mode output voltage	R_L = 54 Ω or 100 Ω,	See 图 5-1			3	V
						–1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(3)					±0.2	V
I_O	Output current	V_{CC} = 0	V_O = -7V to 12V			±100	µA
I_{IH}	High-level input current	V_{IH} = 2.4V				20	µA
I_{IL}	Low-level input current	V_{IL} = 0.4V				–200	µA
I_{OS}	Short circuit output current	V_O = –7V				–250	mA
		V_O = V_{CC}				250	
		V_O = 12V				250	
I_{CC}	Supply current (total package)	No load			57	70	mA

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The minimum V_{OD2} with 100Ω load is either 1/2 VOD2 or 2V, whichever is greater
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) See TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.

4.5 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω	See 图 5-3		15	22	ns
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω	See 图 5-3		20	30	ns

4.6 Symbol Equivalent

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t(R_L = 100 Ω)	V_t(R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
D $\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
D $\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

4.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7V	I_O = –0.4mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5V	I_O = 8mA		–0.2(2)			V
$\|V_{hys}\|$	Hysteresis voltage (V_{IT+} – V_{IT-})					50		mV
V_{OH}	High-level output voltage	V_{ID} = 200mV	I_{OH} = -400µA	See 图 5-2	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = -200mV	I_{OL} = 8mA	See 图 5-2			0.45	V
I_I	Line input current	Other input at 0V	See (3)	V_I = 12V			1	mA
				V_I = –7V			–0.8	mA
r_I	Input resistance				12			kΩ
I_{OS}	Short-circuit output current				–15		–85	mA
I_{OS}	Supply current (total package)	No load				57	70	mA

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) See TIA/EIA-422-B for exact conditions.

4.8 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5V to 1.5V			19	35	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 15pF	See 图 5-4		30	40	ns

4.9 Typical Characteristics

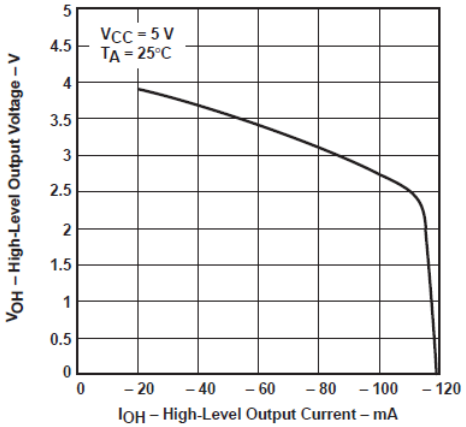


图 4-1. Driver High-Level Output Voltage vs High-Level Output Current

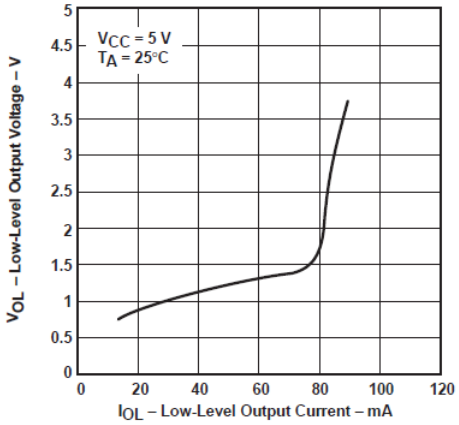


图 4-2. Driver Low-Level Output Voltage vs Low-Level Output Current

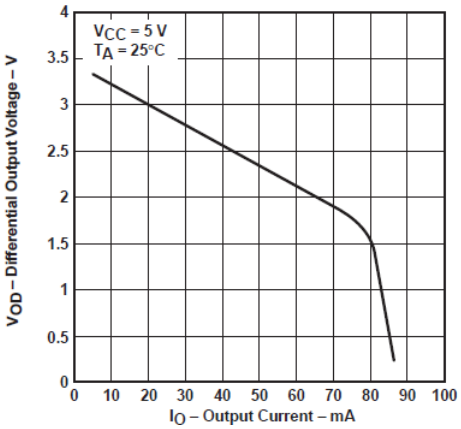


图 4-3. Driver Differential Output Voltage vs Output Current

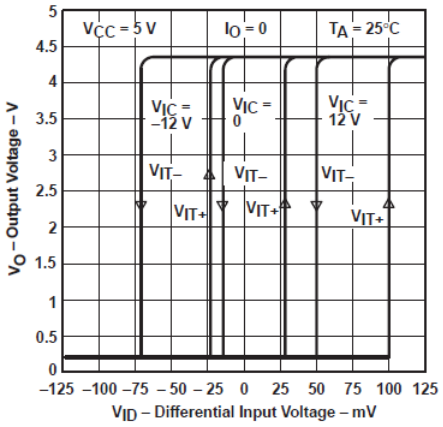


图 4-4. Receiver Output Voltage vs Differential Input Voltage

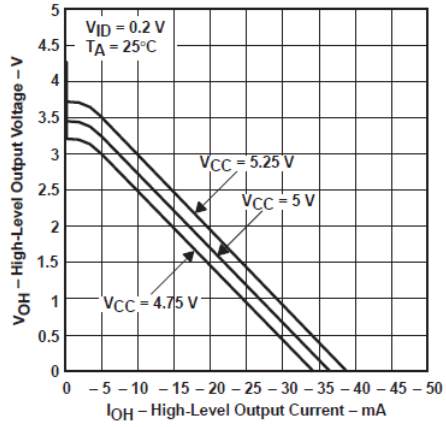


图 4-5. High-Level Output Voltage vs High-Level Output Current

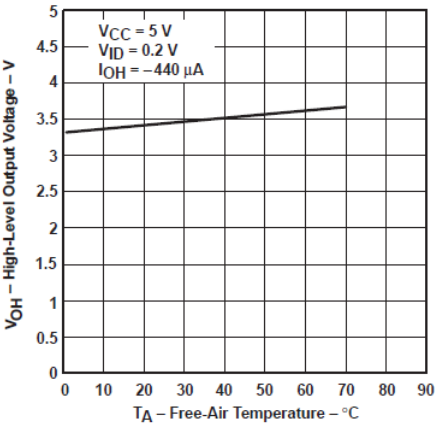


图 4-6. High-Level Output Voltage vs Free-Air Temperature

4.9 Typical Characteristics (continued)

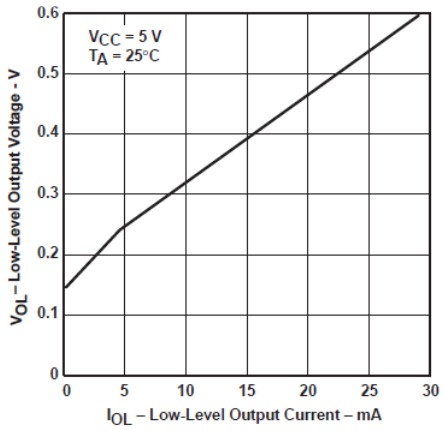


图 4-7. Receiver Low-Level Output Voltage vs Low-Level Output Current

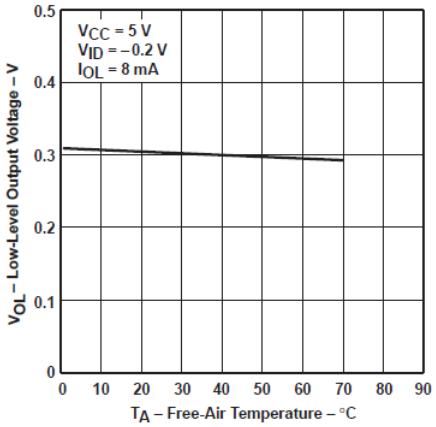


图 4-8. Receiver Low-Level Output Voltage vs Free-Air Temperature

5 Parameter Measurement Information

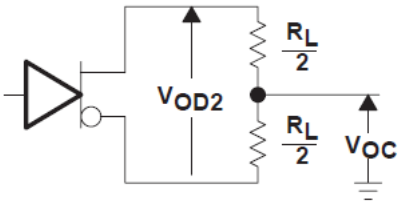


图 5-1. Driver V_{DD} and V_{OC}

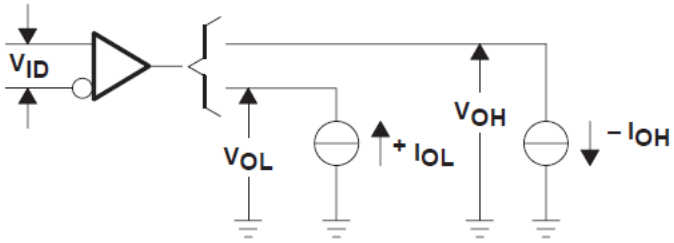
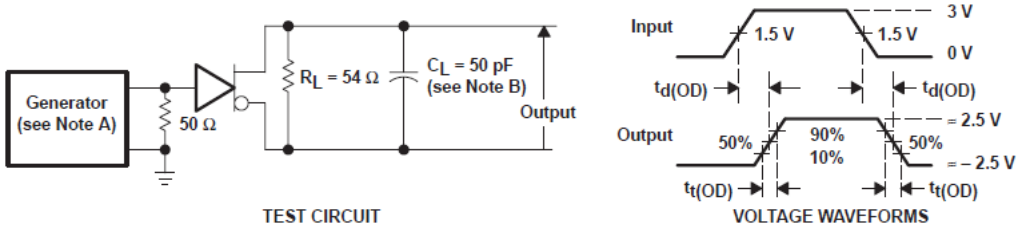


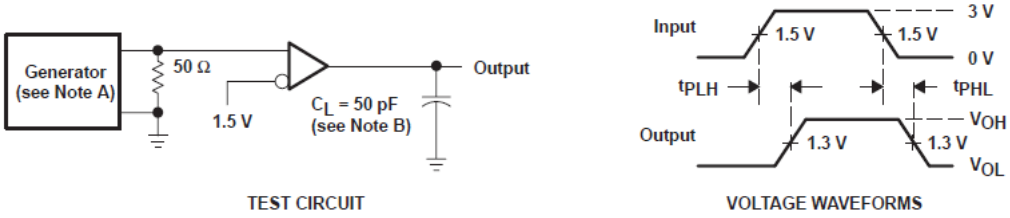
图 5-2. Receiver V_{OH} and V_{OL}



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1MHz, 50% duty cycle, t_r ⩽ 6ns, t_f ⩽ 6ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

图 5-3. Driver Test Circuit and Voltage Waveforms



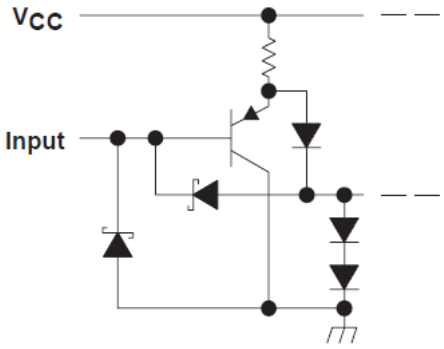
A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1MHz, 50% duty cycle, t_r ⩽ 6ns, t_f ⩽ 6ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

图 5-4. Receiver Test Circuit and Voltage Waveforms

6 Detailed Description

6.1 Functional Block Diagram



A. Driver input: $R_{(eq)}$ = 3k Ω NOM$R_{(eq)}$ = equivalent resistor

图 6-1. Equivalent of Driver Input

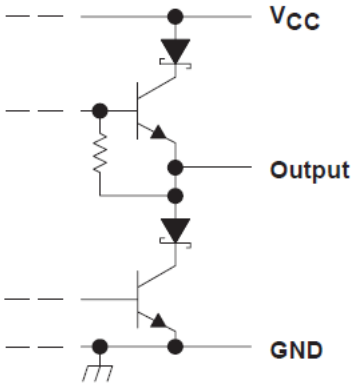


图 6-2. Typical of All Driver Outputs

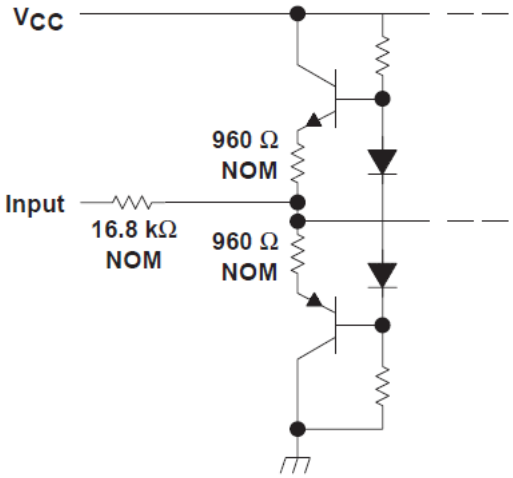


图 6-3. Equivalent of Each Receiver Input

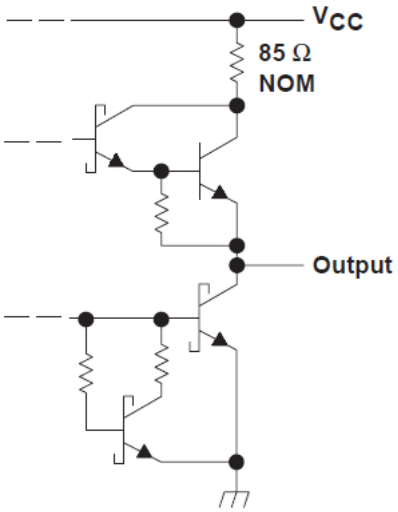


图 6-4. Typical of All Receiver Outputs

6.2 Device Functional Modes

表 6-1. Driver (1)

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H

(1) H = high level, L = low level, ? = indeterminate

表 6-2. Receiver

DIFFERENTIAL INPUTS A – B	OUTPUT(1) R
$V_{ID} \geq 0.2V$	H
$-0.2V < V_{ID} < 0.2V$	?
$V_{ID} \leq -0.2V$	L
Open	?

(1) H = high level, L = low level, ? = indeterminate

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

7.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

7.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (October 2022) to Revision G (April 2025)	Page
• 更新了*封装信息* 表	1
• Changed the I_{OH} driver max value from −602mA to −60mA in the *Recommended Operating Conditions*	4

Changes from Revision E (June 2008) to Revision F (October 2022)	Page
• 将数据表格式更改为最新的数据表格式	1
• Changed the *Thermal Information* table	4

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75179BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75179B
SN75179BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75179B
SN75179BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75179B
SN75179BP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75179BP
SN75179BP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75179BP
SN75179BPE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75179BP
SN75179BPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A179B
SN75179BPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A179B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

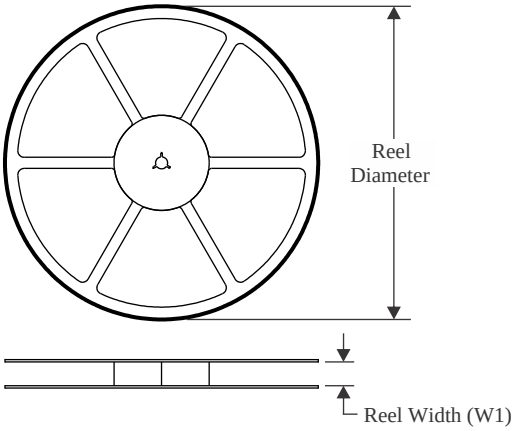
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

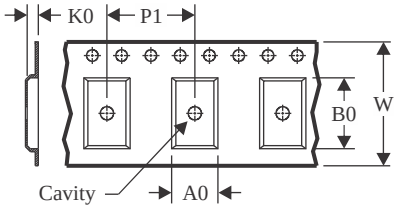
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

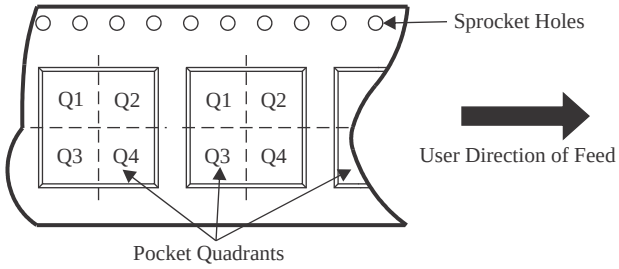


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

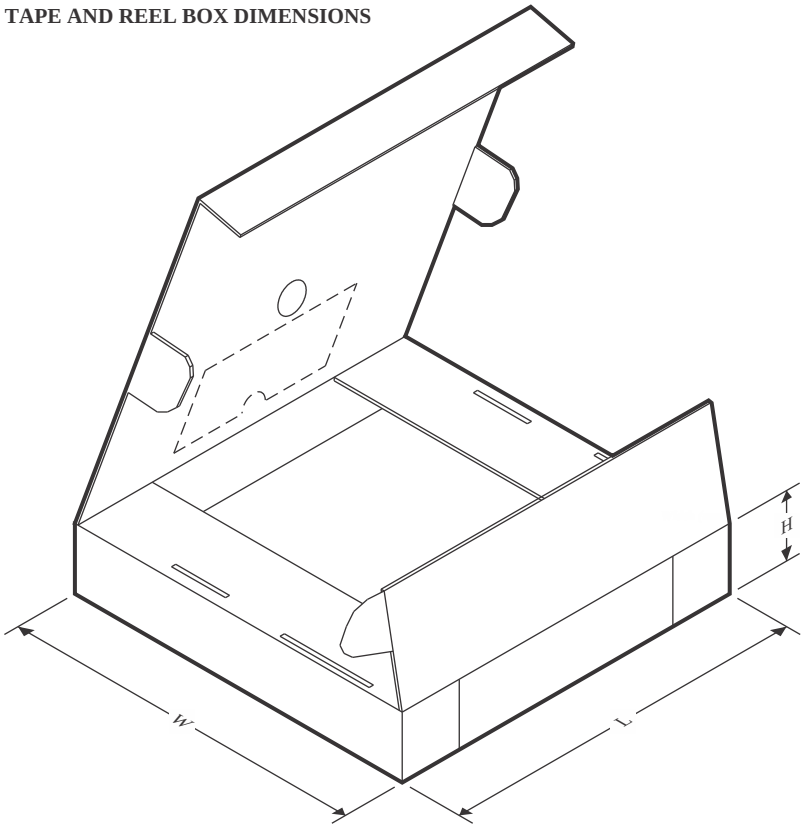
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75179BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75179BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

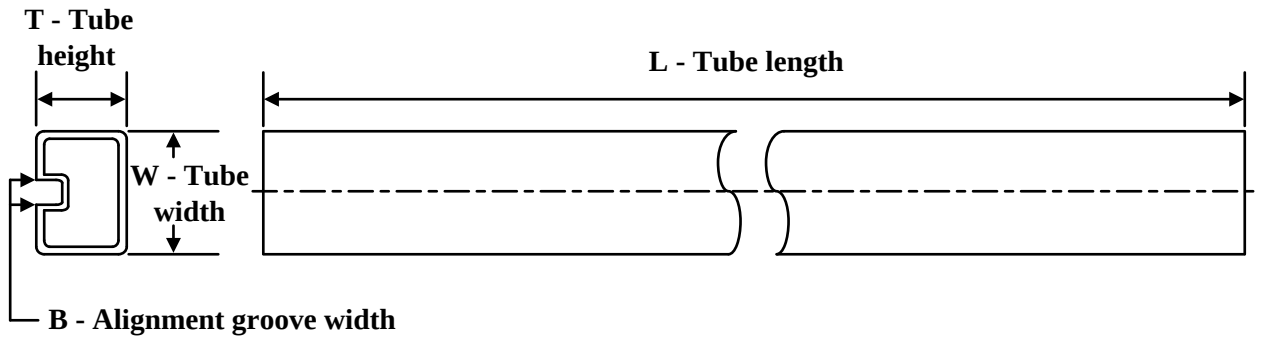
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

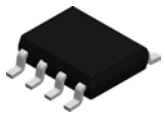
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75179BDR	SOIC	D	8	2500	353.0	353.0	32.0
SN75179BPSR	SO	PS	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75179BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75179BP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75179BPE4	P	PDIP	8	50	506	13.97	11230	4.32

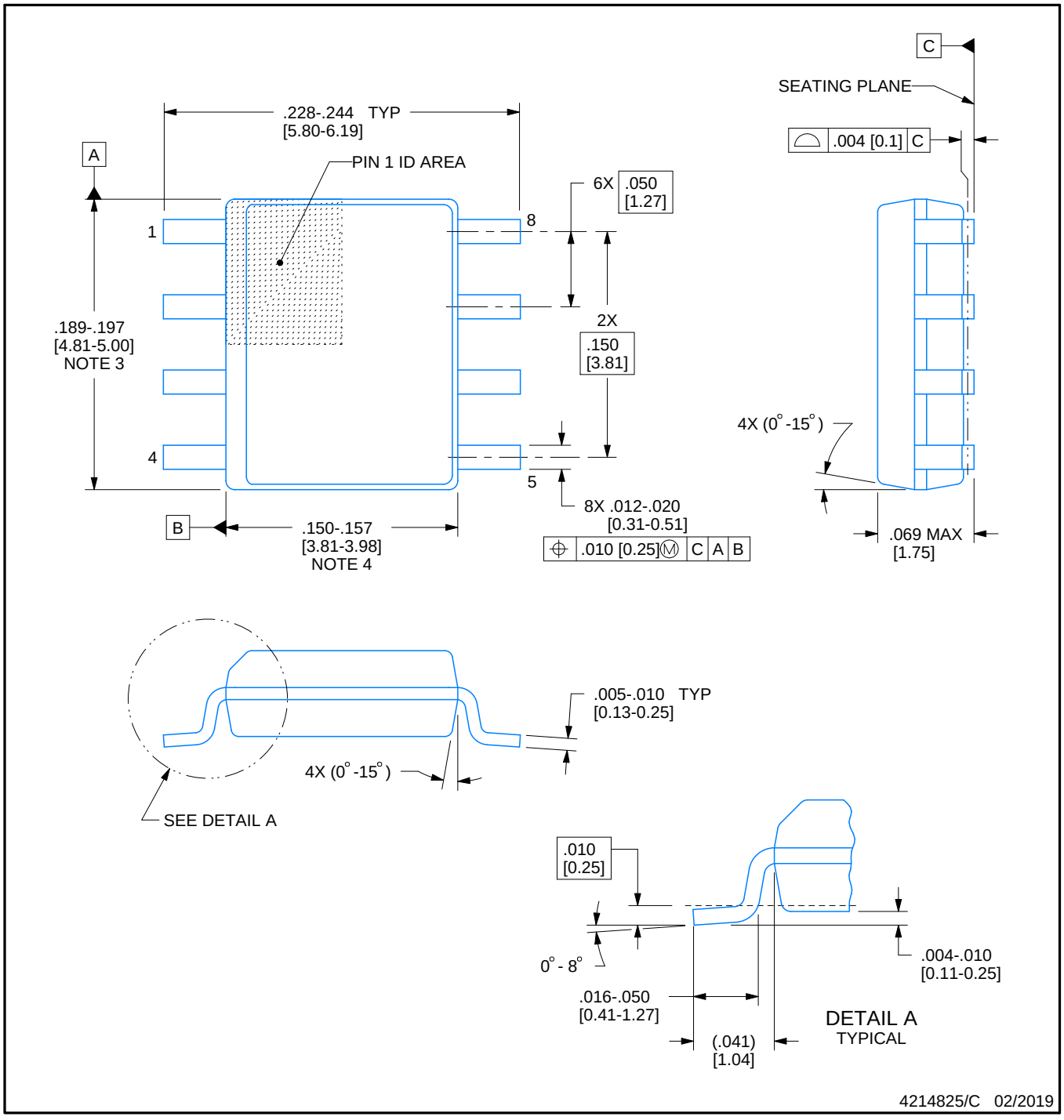


PACKAGE OUTLINE

D0008A

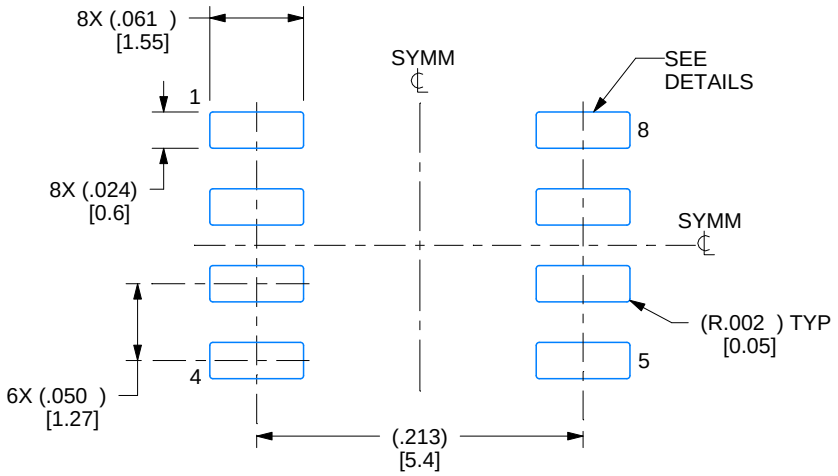
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

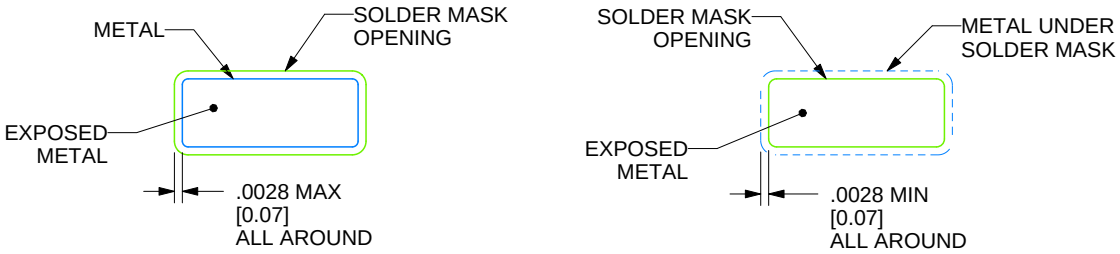


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

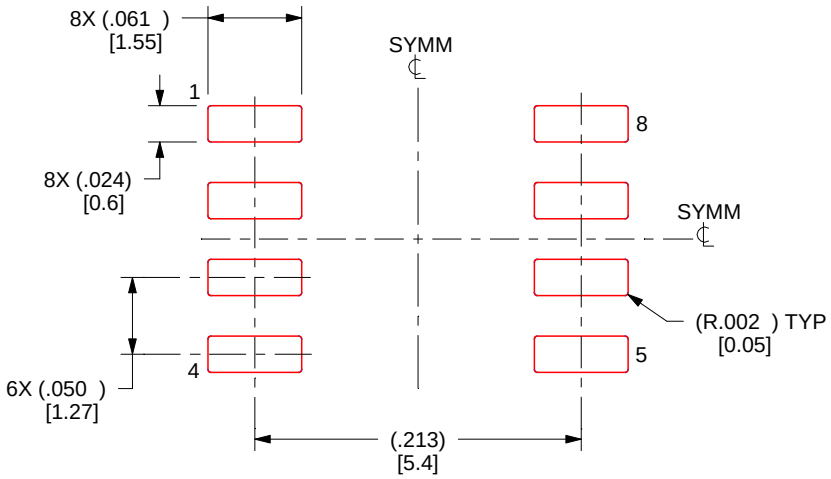
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

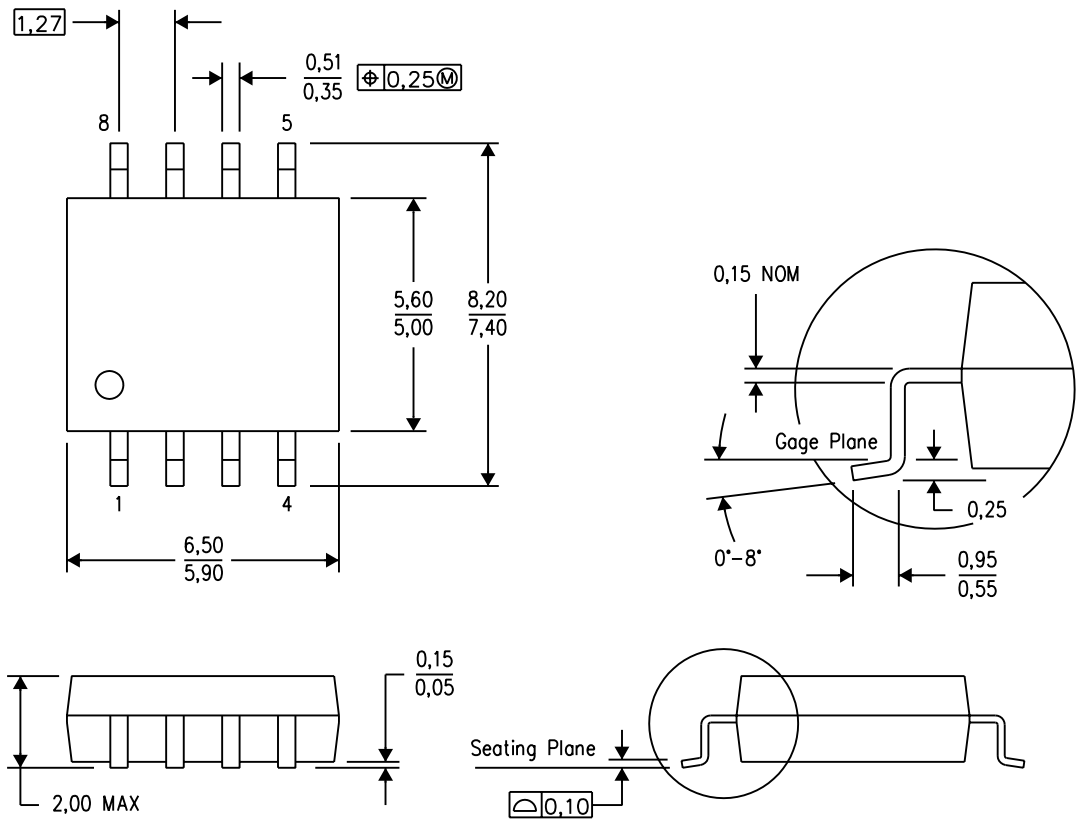
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

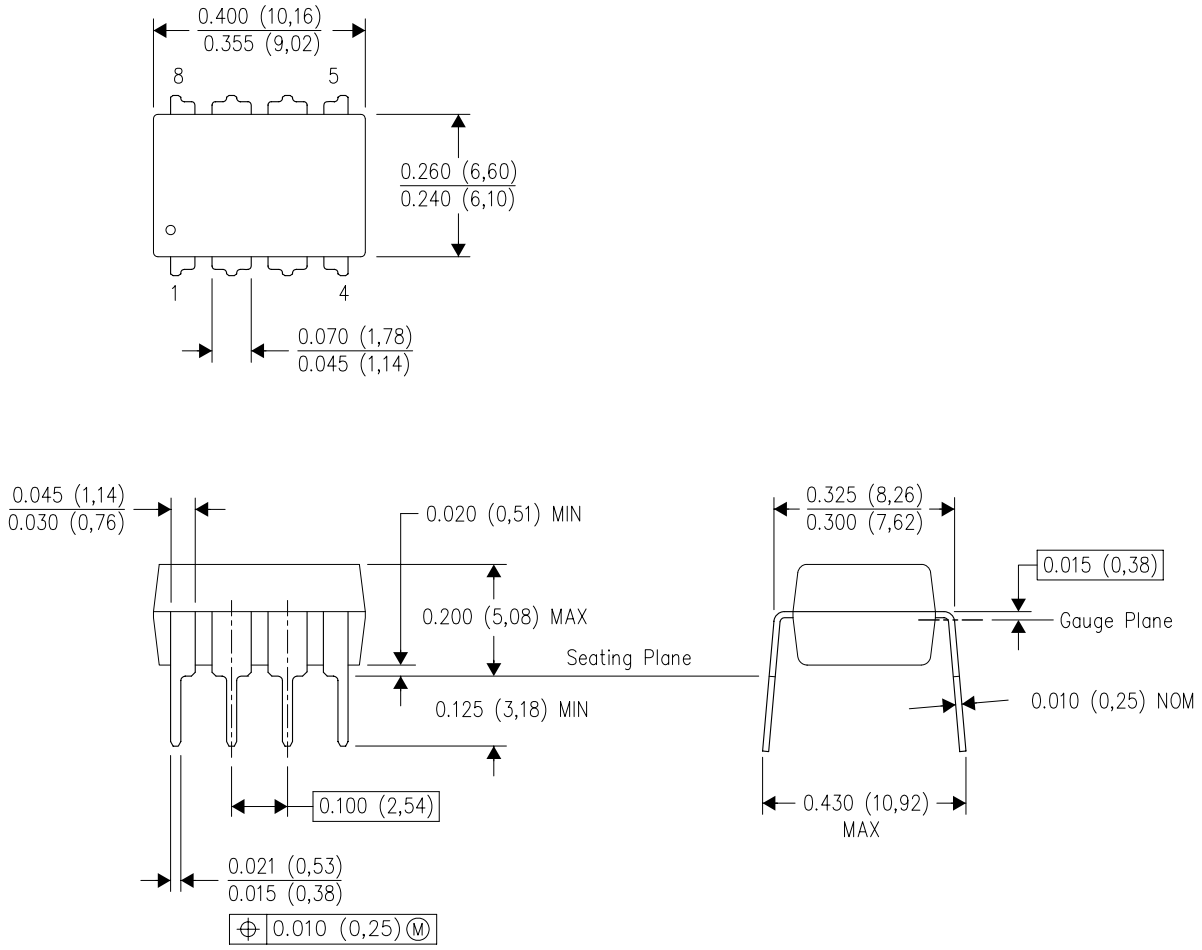
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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最后更新日期：2025 年 10 月