SN74LXC1T14-Q1 具有施密特触发输入的汽车类双电源反相转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
- 完全可配置的双电源轨设计可允许各个端口在 1.1V 至 5.5V 范围内运行
- 稳健、无干扰供电时序
- 在 3.3V 至 5.0V 范围内，支持高达 420Mbps 的速率
- 施密特触发输入可实现慢速或高噪声输入
- 带有集成动态下拉电阻器的输入有助于减少外部元件数量
- 高驱动强度（在 5V 时最高达 32 mA）
- 低功耗
  - 最大值 3 μA (25°C)
  - 最大值 6 μA（–40°C 至 125°C）
- V_{CC} 隔离和 V_{CC} 断开 ($I_{off-float}$) 特性
  - 如果任何一个 V_{CC} 电源电压 < 100 mV 或已断开，则所有 I/O 都被下拉，然后成为高阻抗状态
- 过压容差输入支持最高 5.5V 的电压，而与电源电压无关。
- I_{off} 支持局部断电模式运行
- 工作温度范围为 –40°C 至 +125°C
- 闩锁性能超过 100 mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
  - 4000V 人体放电模型
  - 1000V 充电器件模型

2 应用

- 消除缓慢或嘈杂输入信号
- 驱动指示 LED 或蜂鸣器
- 机械开关去抖
- 通用 I/O (GPIO) 电平转换

3 说明

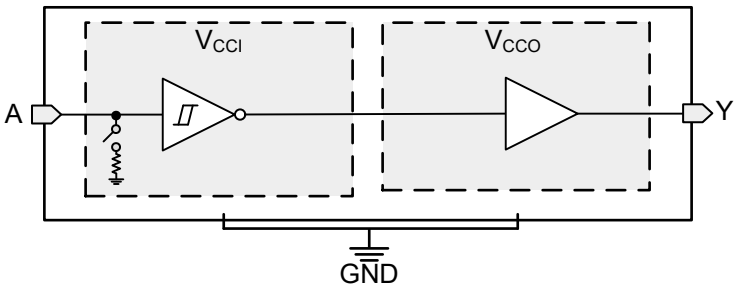
SN74LXC1T14-Q1 是一款具有施密特触发输入的一位双电源反相电压电平转换器件。输入引脚 A 以 V_{CCI} 逻辑电平为基准，输出引脚 Y 以 V_{CCO} 逻辑电平为基准。输入引脚 A 能够接受 1.1V 至 5.5V 的电压，并且可以直接连接到 V_{CCI} 或 GND。请参阅*器件功能模式*，简要了解逻辑的运行方式。

该器件可确保低功耗，并且完全符合使用 I_{off} 的部分断电应用的规范要求。当器件断电时，I_{off} 电路将会禁用输出。这会抑制电流反流到器件中，从而防止损坏器件。

封装信息 (1)

器件型号	封装	封装尺寸（标称值）
SN74LXC1T14-Q1	SC70 (5) (DCK)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

DATE	REVISION	NOTES
August 2022	*	Initial Release

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5 Pin Configuration and Functions

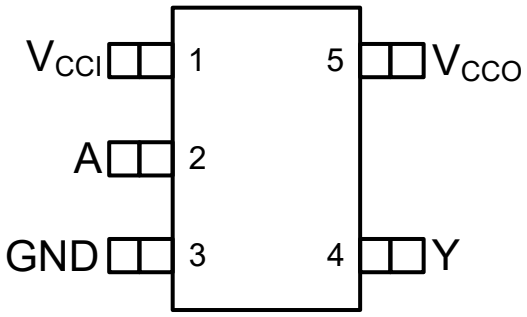


图 5-1. DCK Package, 5-Pin SC70 (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DCK		
V_{CCI}	1	—	Input supply voltage. 1.1 V ⩽ V_{CCI} ⩽ 5.5 V.
A	2	I	Input A. Referenced to V_{CCI}
GND	3	—	Ground.
Y	4	O	Output Y. Referenced to V_{CCO}.
V_{CCO}	5	—	Output supply voltage. 1.1 V ⩽ V_{CCO} ⩽ 5.5 V.

(1) I = input, O = output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCI}	Input supply voltage A		– 0.5	6.5	V
V_{CCO}	Output supply voltage Y		– 0.5	6.5	V
V_I	Input Voltage(2)		– 0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		– 0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2) (3)		– 0.5	V_{CCB} + 0.5	V
I_{IK}	Input clamp current	V_I < 0	– 50		mA
I_{OK}	Output clamp current	V_O < 0	– 50		mA
I_O	Continuous output current		– 50	50	mA
	Continuous current through V_{CC} or GND		– 200	200	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		– 65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			MIN	MAX	UNIT
V_{CCI}	Input supply voltage		1.1	5.5	V
V_{CCO}	Output Supply voltage		1.1	5.5	V
I_{OH}	High-level output current	V_{CCO} = 1.1 V		–0.1	mA
		V_{CCO} = 1.4 V		–4	
		V_{CCO} = 1.65 V		–8	
		V_{CCO} = 2.3 V		–12	
		V_{CCO} = 3 V		–24	
		V_{CCO} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CCO} = 1.1 V		0.1	mA
		V_{CCO} = 1.4 V		4	
		V_{CCO} = 1.65 V		8	
		V_{CCO} = 2.3 V		12	
		V_{CCO} = 3 V		24	
		V_{CCO} = 4.5 V		32	
V_I	Input voltage (3)		0	5.5	V
V_O	Output voltage	Active State	0	V_{CCO}	V
		Tri-State	0	5.5	
T_A	Operating free-air temperature		–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) Input of this device has a weak pulldown to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LXC1T14 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	222.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	132.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	109.5	°C/W
Y_{JT}	Junction-to-top characterization parameter	48.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	108.9	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCI}	V_{CCO}	Operating free-air temperature (T_A)									UNIT
					25°C			– 40°C to 85°C			– 40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going input-threshold voltage	Data Input (Referenced to V_{CCI})	1.1 V	1.1 V				0.44		0.88	0.44		0.88	V
			1.4 V	1.4 V				0.60		0.98	0.60		0.98	
			1.65 V	1.65 V				0.76		1.13	0.76		1.13	
			2.3 V	2.3 V				1.08		1.56	1.08		1.56	
			3 V	3 V				1.48		1.92	1.48		1.92	
			4.5 V	4.5 V				2.19		2.74	2.19		2.74	
			5.5 V	5.5 V				2.65		3.33	2.65		3.33	
V_{T-}	Negative-going input-threshold voltage	Data Input (Referenced to V_{CCI})	1.1 V	1.1 V				0.17		0.48	0.17		0.48	V
			1.4 V	1.4 V				0.28		0.59	0.28		0.59	
			1.65 V	1.65 V				0.35		0.69	0.35		0.69	
			2.3 V	2.3 V				0.56		0.97	0.56		0.97	
			3 V	3 V				0.89		1.5	0.89		1.5	
			4.5 V	4.5 V				1.51		1.97	1.51		1.97	
			5.5 V	5.5 V				1.88		2.4	1.88		2.4	
ΔV_T	Input-threshold hysteresis (V_{T+} – V_{T-})	Data Input (A) (Referenced to V_{CCI})	1.1 V	1.1 V				0.2		0.4	0.2		0.4	V
			1.4 V	1.4 V				0.25		0.5	0.25		0.5	
			1.65 V	1.65 V				0.3		0.55	0.3		0.55	
			2.3 V	2.3 V				0.38		0.65	0.38		0.65	
			3 V	3 V				0.46		0.72	0.46		0.72	
			4.5 V	4.5 V				0.58		0.93	0.58		0.93	
			5.5 V	5.5 V				0.69		1.06	0.69		1.06	
V_{OH}	High-level output voltage (3)	I_{OH} = – 100 µA	1.1 V – 5.5 V	1.1 V – 5.5 V				V_{CCO} – 0.1			V_{CCO} – 0.1			V
		I_{OH} = – 4 mA	1.4 V	1.4 V				1			1			
		I_{OH} = – 8 mA	1.65 V	1.65 V				1.2			1.2			
		I_{OH} = – 12 mA	2.3 V	2.3 V				1.9			1.9			
		I_{OH} = – 24 mA	3 V	3 V				2.4			2.4			
		I_{OH} = – 32 mA	4.5 V	4.5 V				3.8			3.8			
V_{OL}	Low-level output voltage (4)	I_{OL} = 100 µA	1.1 V – 5.5 V	1.1 V – 5.5 V						0.1			0.1	V
		I_{OL} = 4 mA	1.4 V	1.4 V						0.3			0.3	
		I_{OL} = 8 mA	1.65 V	1.65 V						0.45			0.45	
		I_{OL} = 12 mA	2.3 V	2.3 V						0.3			0.3	
		I_{OL} = 24 mA	3 V	3 V						0.55			0.55	
		I_{OL} = 32 mA	4.5 V	4.5 V						0.55			0.55	
I_I	Input leakage current	Data Input (5) V_I = V_{CCI} or GND	1.1 V – 5.5 V	1.1 V – 5.5 V	– 0.3		1	– 1		1	– 2		2	µA
I_{off}	Partial power down current	Inputs V_I or V_O = 0 V – 5.5 V	0 V	0 V – 5.5 V	– 1		1	– 2		2	– 2.5		2.5	µA
			0 V – 5.5 V	0 V	– 1		1	– 2		2	– 2.5		2.5	

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6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCI}	V_{CCO}	Operating free-air temperature (T_A)									UNIT
					25°C			– 40°C to 85°C			– 40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$I_{off-float}$	Floating supply Partial power down current	Inputs V_I or V_O = GND	Floating (6)	0 V – 5.5 V	– 1.5		1.5	– 2		2	– 2.5		2.5	µA
			0 V – 5.5 V	Floating (6)	– 1.5		1.5	– 2		2	– 2.5		2.5	
I_{CCI}	V_{CCI} supply current	V_I = V_{CCI} or GND I_O = 0	1.1 V – 5.5 V	1.1 V – 5.5 V			2			3			6	µA
			0 V	5.5 V	– 0.2			– 0.5			– 1			
			5.5 V	0 V			1			2			4	
		V_I = GND I_O = 0	5.5 V	Floating (6)			2			3			6	
I_{CCO}	V_{CCO} supply current	V_I = V_{CCI} or GND I_O = 0	1.1 V – 5.5 V	1.1 V – 5.5 V			2			3			6	µA
			0 V	5.5 V			1			2			4	
			5.5 V	0 V	– 0.2			– 0.5			– 1			
I_{CCO}		V_I = GND I_O = 0	Floating (6)	5.5 V			2			3			6	
I_{CCI} + I_{CCO}	Combined supply current	V_I = V_{CCI} or GND I_O = 0	1.1 V – 5.5 V	1.1 V – 5.5 V			3			4			6	µA
ΔI_{CCI}	Additional input supply current	V_I = V_{CCI} – 0.6 V	3.0 V – 5.5 V	3.0 V – 5.5 V						50			75	µA
C_i	Input Capacitance	V_I = 3.3 V or GND	3.3 V	3.3 V		5				10			10	pF
C_o	Output Capacitance	V_{CCO} = 0V V_O = 1.65 V DC +1 MHz -16 dBm sine wave	3.3 V	3.3 V		5				10			10	pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) Tested at V_I = $V_{T+(MAX)}$.
(4) Tested at V_I = $V_{T-(MIN)}$.
(5) For I/O ports, the parameter I_I includes the I_{OZ} current.
(6) Floating is defined as a node that is both not actively driven by an external device and has leakage not exeeding 10 nA.

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6.6 Switching Characteristics: Tpd

Over operating free-air temperature range (T_A). See Figure 7-1 and Table 7-1for test circuit and loading. See Figure 7-2 and Figure 7-3 for measurement waveforms.

PARAMETER		FROM	TO	Output Supply Voltage (V_{CCO})	Input Supply Voltage (V_{CCI})																	UNIT
					1.2 ± 0.1 V			1.5 ± 0.1 V			1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	Y	1.2 ± 0.1 V	10		83	10		70	10		66	9		59	9		58	9		54	ns
				1.5 ± 0.1 V	9		36	8		28	7		26	7		22	7		21	7		20	
				1.8 ± 0.15 V	8		32	7		23	6		21	6		18	6		17	6		16	
				2.5 ± 0.2 V	7		29	6		18	5		15	5		13	4		12	4		11	
				3.3 ± 0.3 V	7		29	6		16	4		13	4		11	3		10	3		9	
				5.0 ± 0.5 V	7		28	5		15	4		12	3		10	2		9	2		8	

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6.7 Switching Characteristics: T_{MAX}

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCI}	V_{CCO}	Operating free-air temperature (T_A)			UNIT
					-40°C to 125°C			
					MIN	TYP	MAX	
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	Up Translation	3.0 V - 3.6 V	4.5 V - 5.5 V	200	420		Mbps
			2.25 V - 2.75 V	4.5 V - 5.5 V	150	300		
			1.65 V - 1.95 V	4.5 V - 5.5 V	100	200		
			1.1 V - 1.3 V	4.5 V - 5.5 V	20	40		
			1.65 V - 1.95 V	3.0 V - 3.6 V	100	210		
			1.1 V - 1.3 V	3.0 V - 3.6 V	10	20		
			1.1 V - 1.3 V	1.65 V - 1.95 V	5	10		
		Down Translation	4.5 V - 5.5 V	3.0 V - 3.6 V	100	210		
			4.5 V - 5.5 V	2.25 V - 2.75 V	75	140		
			4.5 V - 5.5 V	1.65 V - 1.95 V	50	75		
			4.5 V - 5.5 V	1.1 V - 1.3 V	15	30		
			3.0 V - 3.6 V	1.65 V - 1.95 V	40	75		
			3.0 V - 3.6 V	1.1 V - 1.3 V	10	20		
			1.65 V - 1.95 V	1.1 V - 1.3 V	5	10		

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6.8 Typical Characteristics

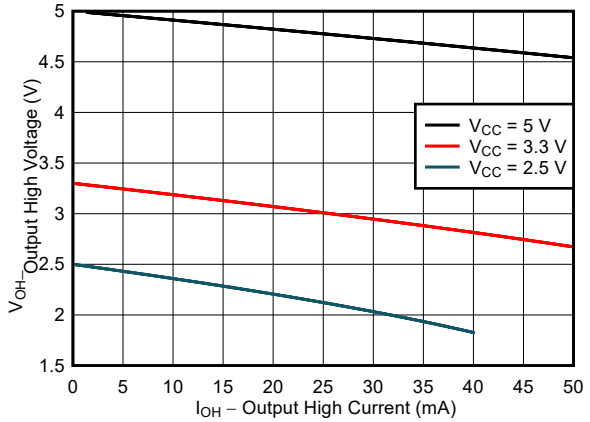


图 6-1. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

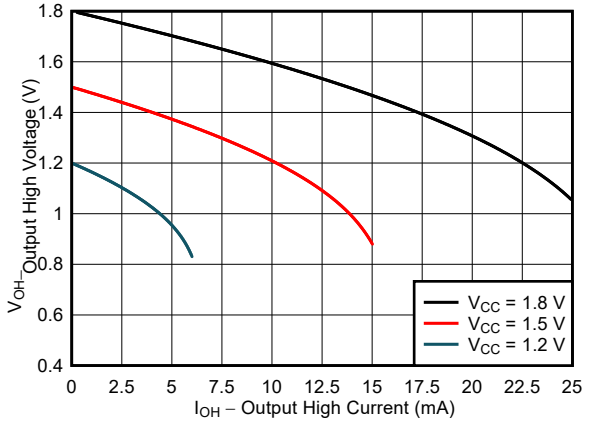


图 6-2. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

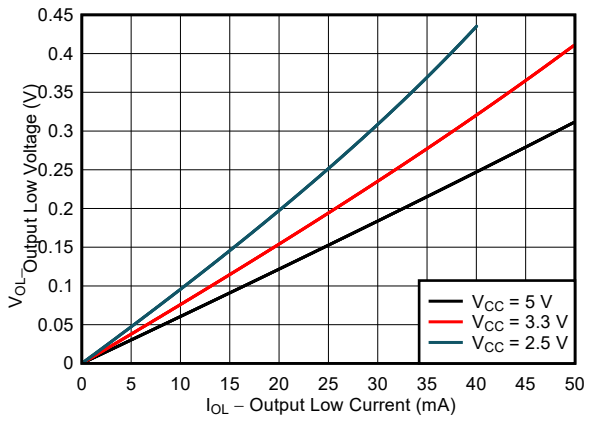


图 6-3. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

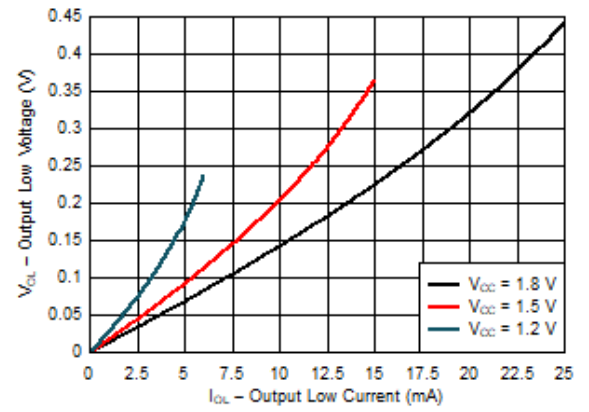


图 6-4. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

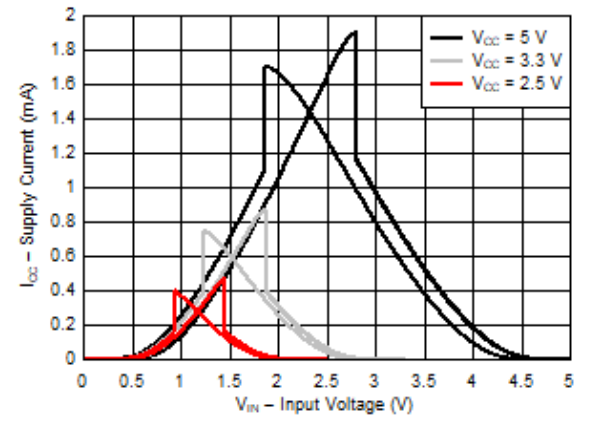


图 6-5. Typical (T_A=25°C) Supply Current (I_{CC}) vs Input Voltage (V_{IN})

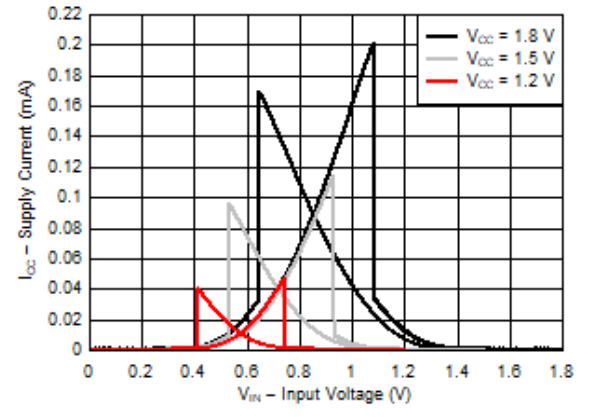


图 6-6. Typical (T_A=25°C) Supply Current (I_{CC}) vs Input Voltage (V_{IN})

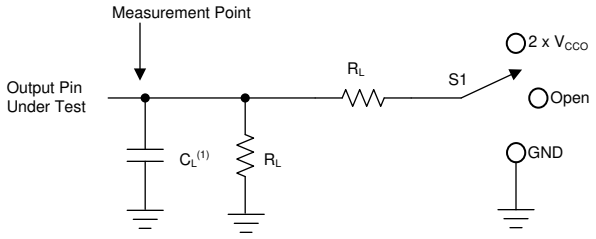
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7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- $\Delta t/\Delta V \leq$ 1 ns/V

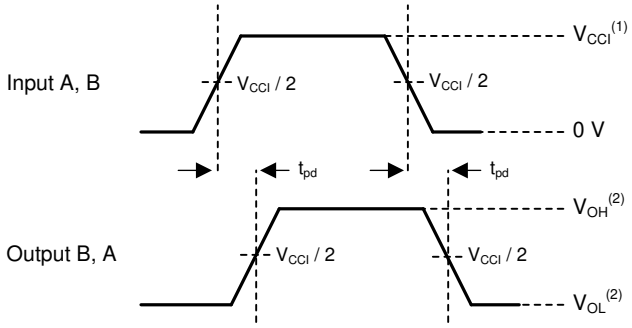


1. C_L includes probe and jig capacitance.

图 7-1. Load Circuit

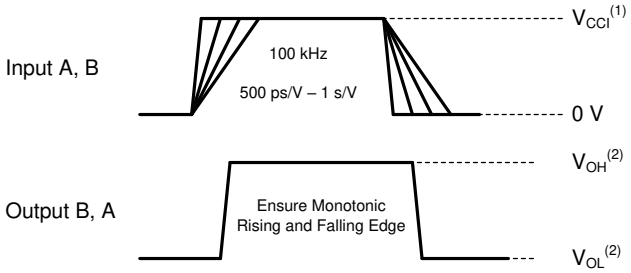
表 7-1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
t_{pd}	Propagation (delay) time	1.1 V – 5.5 V	2 kΩ	15 pF	Open	N/A



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

图 7-2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

图 7-3. Input Transition Rise and Fall Rate

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8 Detailed Description

8.1 Overview

The SN74LXC1T14-Q1 is a single bit translating transceiver that uses two individually configurable power-supply rails. The device is operational with both V_{CCI} and V_{CCO} supplies as low as 1.1 V and as high as 5.5 V. The A input is designed to track V_{CCI}, and the Y output is designed to track V_{CCO}.

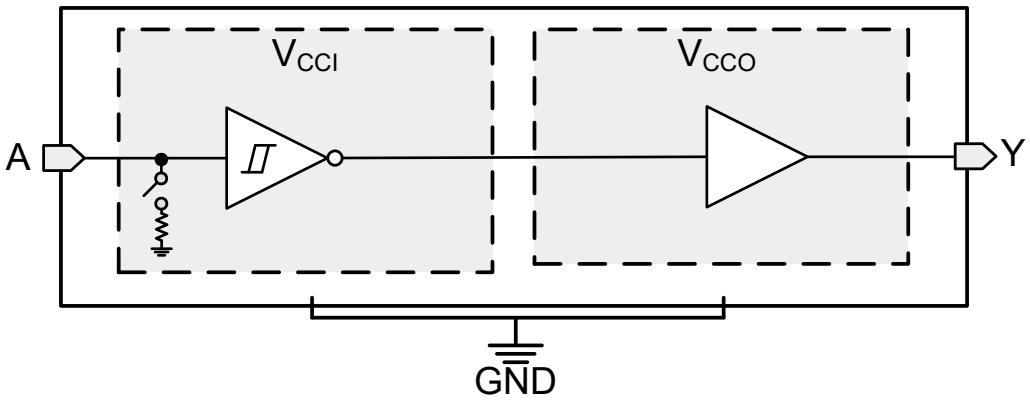
The SN74LXC1T14-Q1 device is designed for asynchronous communication between devices, and transmits data from A to Y. The input circuitry on the A pin is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry ensures that no excessive current is drawn from or sourced into an input or output while the device is powered down.

The V_{CC} isolation or V_{CC} disconnect feature ensures that if either V_{CC} is less than 100 mV or disconnected with the complementary supply within recommended operating conditions, the input is weakly pulled-down and then set to the high-impedance state by disabling their outputs while the supply current is maintained. The $I_{off\text{-}float}$ circuitry ensures that no excess current is drawn from or sourced into an input, or output while the supply is floating.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 CMOS Schmitt-Trigger Inputs with Integrated Pulldowns

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. Driving the inputs slowly will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, see *Understanding Schmitt Triggers*.

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8.3.1.1 Input with Integrated Dynamic Pull-Down Resistors

Input circuitry is always active even when the device is disabled. It is recommended to keep a valid voltage level at the input to avoid high current consumption. To help avoid a floating input during disabling, this device has 100-kΩ typical integrated weak dynamic pull-down at the input. When the device is disabled, the dynamic pull-downs are activated for only a short period of time to help drive and keep the floating input low before the device output becomes high impedance. If the input lines will be floated after the device is disabled, it is recommended to keep them at a valid input voltage level using external pull-downs. This feature is ideal for loads of 30 pF or less. If greater capactive loading is present then external pull-downs are recommended. If an external pull-up is required, it should be no larger than 15 kΩ to avoid contention with the 100 kΩ internal pull-down.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

8.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

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8.3.4 V_{CC} Isolation and V_{CC} Disconnect ($I_{off-float}$)

This device has an *Input with Integrated Dynamic Pull-Down Resistors*. The input will get pulled down and then enter a high-impedance state when either supply is < 100 mV or left floating (disconnected), while the other supply is still connected to the device. It is recommended to not drive the input for this device, but to keep it at a logic low state prior to floating (disconnecting) either supply.

The maximum supply current is specified by I_{CCx}, while V_{CCx} is floating, in the *Electrical Characteristics*. The maximum leakage into or out of any input or output pin on the device is specified by $I_{off(float)}$ in the *Electrical Characteristics*.

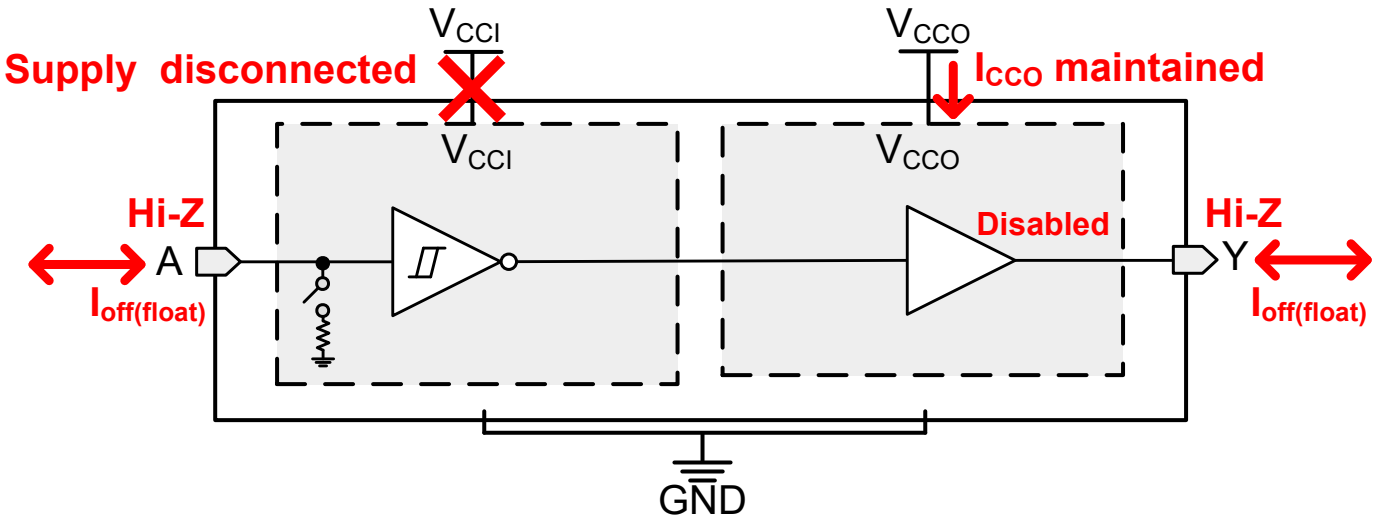


图 8-1. V_{CC} Disconnect Feature

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

8.3.6 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the output (that is, where the output erroneously transitions to VCC when it should be held low or vice versa). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

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8.3.7 Negative Clamping Diodes

As shown in 图 8-2, the inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

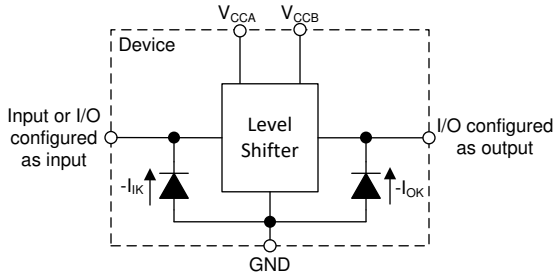


图 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.8 Fully Configurable Dual-Rail Design

Both the V_{CCI} and V_{CCO} pins can be supplied at any voltage from 1.1 V to 5.5 V, making the device suitable for translating between any of the voltage nodes (1.2 V, 1.5 V, 1.8 V, 3.3 V, and 5.0 V).

8.3.9 Supports High-Speed Translation

The SN74LXC1T14-Q1 device can support high data-rate applications. The translated signal data rate can be up to 420 Mbps when the signal is translated from 3.3 V to 5.0 V.

8.4 Device Functional Modes

表 8-1. Function Table

Input A	Output Y
H	L
L	H

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LXC1T14-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74LXC1T14-Q1 device is ideal for use in applications where a push-pull driver is connected to the input. The maximum data rate can be up to 420 Mbps when the device translates a signal from 3.3 V to 5.0 V.

9.2 Typical Application

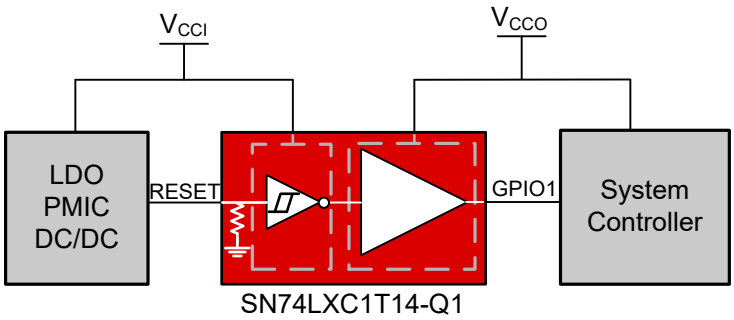


图 9-1. LED Driver Application

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.1 V to 5.5 V
Output voltage range	1.1 V to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74LXC1T14-Q1 device to determine the input voltage range. For a valid logic-high, the value must exceed the positive-going input-threshold voltage (V_{t+}) of the input port. For a valid logic low the value must be less than the negative-going input-threshold voltage (V_{t-}) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74LXC1T14-Q1 device is driving to determine the output voltage range.

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10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices, as described in *Glitch-Free Power Supply Sequencing*.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1 µF capacitor is recommended, but transient performance can be improved by having both 1 µF and 0.1 µF capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

11.2 Layout Example

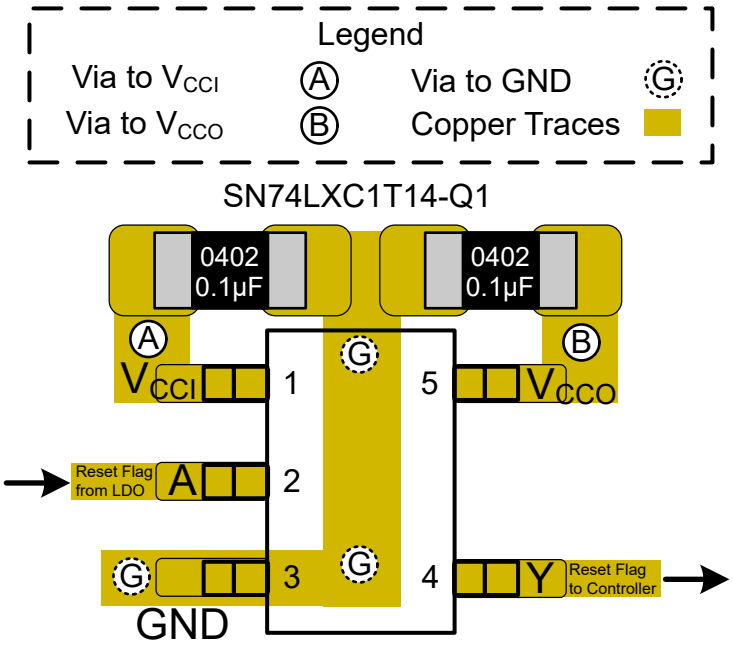


图 11-1. Layout Example – SN74LXC1T14-Q1

12 Device and Documentation Support

12.1 Device Support

12.1.1 Regulatory Requirements

No statutory or regulatory requirements apply to this device.

There are no special characteristics for this product.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Understanding Schmitt Triggers* applicatin report

12.3 接收文档更新通知

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12.4 支持资源

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LXC1T14QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2OAT
SN74LXC1T14QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2OAT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LXC1T14-Q1 :

- Catalog : SN74LXC1T14

NOTE: Qualified Version Definitions:

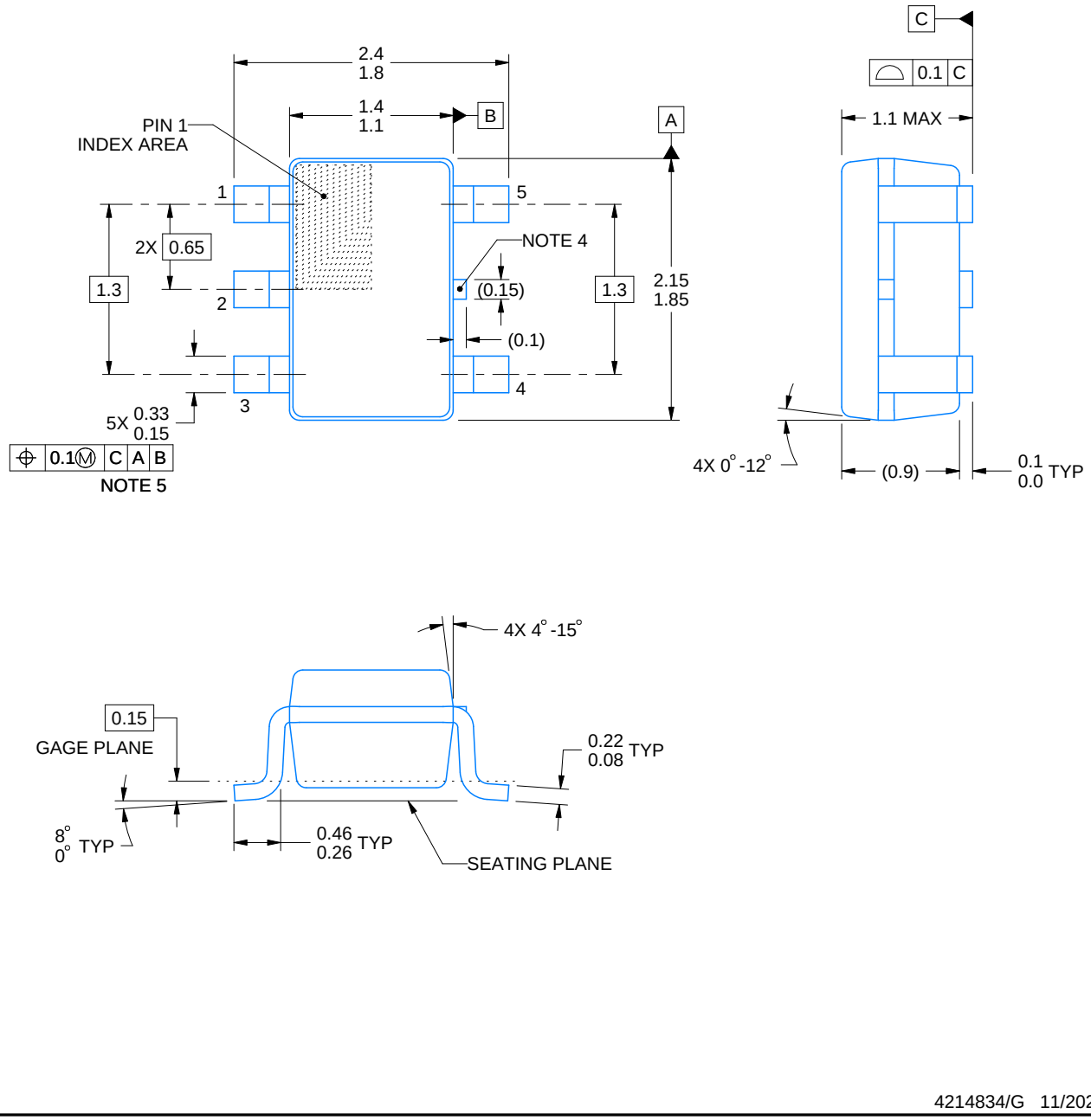
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

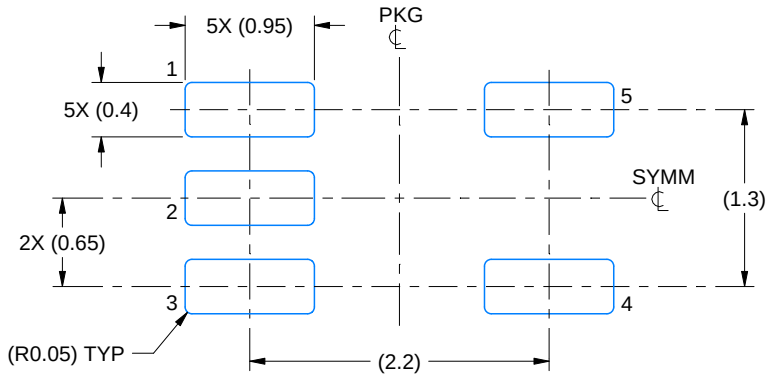
SMALL OUTLINE TRANSISTOR



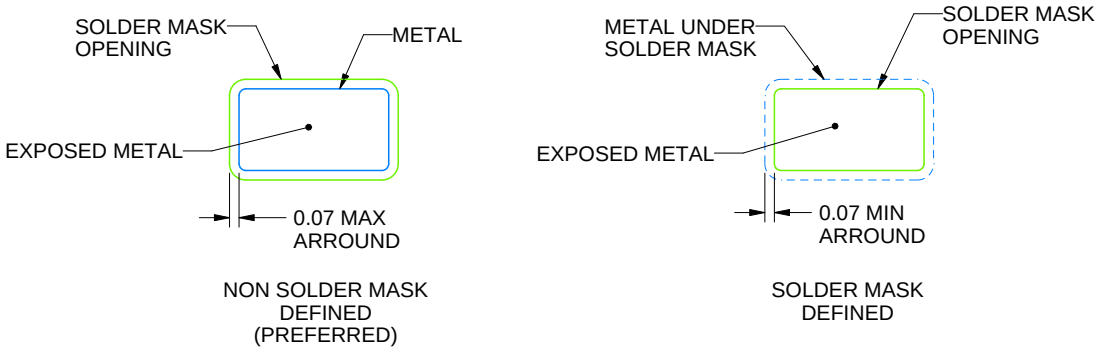
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

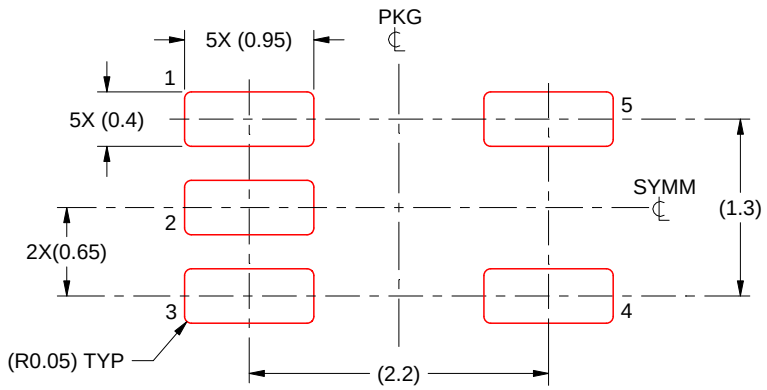


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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