具有漏极开路输出的 SN74LVC1G06 单路反相器缓冲器或驱动器

1 特性

- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)
  - 1000V 充电器件模型 (C101)
- 采用德州仪器 (TI) NanoFree™ 封装
- 支持 5V V_{CC} 运行
- 输入与开漏输出支持最高 5.5V 的电压
- 125°C、3.3V 时，t_{pd} 最大值为 4.5ns
- 低功耗，I_{CC} 最大值为 10μA
- 对于开漏器件，±24mA 输出以 3.3V 驱动
- I_{off} 支持局部关断模式和后驱动保护
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- 可用于上行或下行转换
- 所有端口上的施密特触发操作

2 应用

- AV 接收器
- 蓝光播放器与家庭影院
- DVD 录像机和播放器
- 台式机或笔记本电脑
- 数字音频广播或互联网广播播放器
- 数码摄像机 (DVC)
- 嵌入式个人电脑 (PC)
- GPS：个人导航设备
- 移动互联网设备
- 网络投影仪前端
- 便携式媒体播放器
- 专业音频混合器
- 烟雾探测器
- 固态硬盘 (SSD)：企业级
- 高清 (HDTV)
- 平板电脑：企业级
- 音频接口盒：便携式
- DLP 正投系统
- DVR 和 DVS
- 数码相框 (DPF)
- 数码相机

3 说明

该单路反相器缓冲器和驱动器设计成在 1.65V 至 5.5V V_{CC} 下运行。

NanoFree 封装技术是 IC 封装概念的一项重大突破，它将硅晶片用作封装。

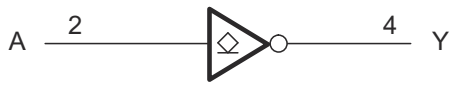
SN74LVC1G06 器件的输出为漏极开路，可连接其它开漏输出，从而实现低电平有效的连线 OR 或高电平有效的连线 AND 功能。最大灌电流为 32mA。

该器件完全适合使用 I_{off} 的局部断电应用。当器件断电时，I_{off} 电路将会禁用输出。这会抑制电流回流到器件中，从而防止损坏器件。

封装信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸（标称值）(3)
SN74LVC1G06	DBV（SOT-23，5）	2.90mm × 2.80mm	2.90mm × 1.60mm
	DCK（SC70，5）	2.00mm × 2.10mm	2.00mm × 1.25mm
	DRL（SOT-5X3，5）	1.60mm × 1.60mm	1.60mm × 1.20mm
	DRY（USON，6）	1.45mm × 1.00mm	1.45mm × 1.00mm
	DSF（X2SON，6）	1.00mm × 1.00mm	1.00mm × 1.00mm
	YZP（DSBGA，5）	1.75mm × 1.25mm	1.40mm × 0.90mm
	YZV（DSBGA，4）	1.25mm × 1.25mm	0.90mm × 0.90mm
	DPW（X2SON，5）	0.80mm × 0.80mm	0.80mm × 0.80mm

(1) 有关更多信息，请参阅 机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 封装尺寸（长 × 宽）为标称值，不包括引脚。



逻辑图（正逻辑）

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4 引脚配置和功能

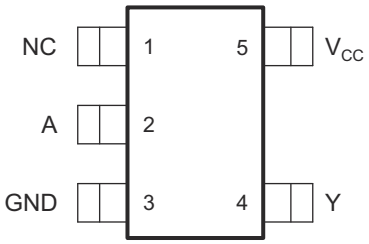

图 4-1. DBV 封装 5 引脚 SOT-23 顶视图

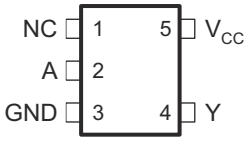

图 4-2. DRL 封装 5 引脚 SOT-5X3 顶视图

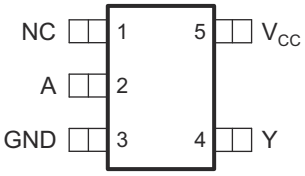

图 4-3. DCK 封装 5 引脚 SC70 顶视图

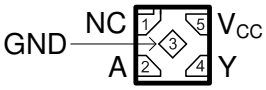

图 4-4. DPW 封装 5 引脚 X2SON 顶视图

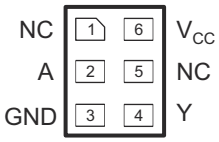

图 4-5. DRY 封装 6 引脚 SON 顶视图

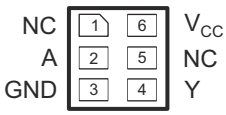

图 4-6. DSF 封装 6 引脚 SON 顶视图

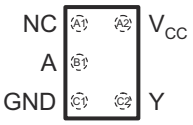

图 4-7. YZP 封装 5 引脚 DSBGA 顶视图

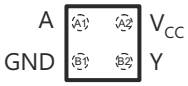

图 4-8. YZV 封装 4 引脚 DSBGA 顶视图

表 4-1. 引脚功能 (2)

引脚					I/O	说明
名称	DBV、DCK、DRL、DPW	DRY、DSF	YZP	YZV		
A	2	2	B1	A1	I	输入
DNU	—	—	A1	—	—	请勿使用
GND	3	3	C1	B1	—	接地
NC(1)	1	1 5	—	—	—	未连接
V_{CC}	5	6	A2	A2	—	电源引脚
Y	4	4	C2	B2	O	输出

(1) NC – 无内部连接
(2) 请参阅机械制图，了解尺寸。

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）[(1)]

			最小值	最大值	单位
V_{CC}	电源电压		-0.5	6.5	V
V_I	输入电压[(2)]		-0.5	6.5	V
V_O	施加到任一处于高阻抗或断电状态输出的电压[(2)]		-0.5	6.5	V
V_O	施加到任一处于高电平或低电平状态输出的电压[(2) (3)]		-0.5	6.5	V
I_{IK}	输入钳位电流	$V_I < 0$		-50	mA
I_{OK}	输出钳位电流	$V_O < 0$		-50	mA
I_O	持续输出电流			±50	mA
	通过 V_{CC} 或 GND 的持续电流			±100	mA
T_j	结温		-65	150	°C
T_{stg}	贮存温度		-65	150	°C

(1) 在*绝对最大额定值*范围外运行可能对器件造成永久损坏。*绝对最大额定值* 并不表示器件在这些条件下或在*建议的工作条件* 以外的任何其他条件下能够正常运行。如果超出*建议运行条件* 但在*绝对最大额定值* 范围内使用，器件可能不会完全正常运行，这可能影响器件的可靠性、功能和性能并缩短器件寿命。
(2) 如果遵守输入和输出电流额定值，则可能会超过输入和输出负电压额定值。
(3) V_{CC} 的值在*建议运行条件* 表中提供。

5.2 ESD 等级

		值	单位
$V_{(ESD)}$ 静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准[(1)]	2000	V
	充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101[(2)]	1000	
	机器放电模型 (MM)，符合 A115-A 标准	200	

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

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5.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）[(1)]

			最小值	最大值	单位
V_{CC}	电源电压	工作	1.65	5.5	V
		仅数据保留	1.5		
V_{IH}	高电平输入电压	V_{CC} = 1.65V 至 1.95V	0.65 × V_{CC}		V
		V_{CC} = 2.3V 至 2.7V	1.7		
		V_{CC} = 3V 至 3.6V	2		
		V_{CC} = 4.5V 至 5.5V	0.7 × V_{CC}		
V_{IL}	低电平输入电压	V_{CC} = 1.65V 至 1.95V		0.35 × V_{CC}	V
		V_{CC} = 2.3V 至 2.7V		0.7	
		V_{CC} = 3V 至 3.6V		0.8	
		V_{CC} = 4.5V 至 5.5V		0.3 × V_{CC}	
V_I	输入电压		0	5.5	V
V_O	输出电压		0	5.5	V
I_{OL}	低电平输出电流	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		32	
Δt/Δv	输入转换上升或下降速率	V_{CC} = 1.8V ± 0.15V，2.5V ± 0.2V		20	ns/V
		V_{CC} = 3.3V ± 0.3V		10	
		V_{CC} = 5V ± 0.5V		5	
T_A	自然通风条件下的工作温度范围		-40	125	°C

(1) 器件的所有未使用输入必须保持在 V_{CC} 或 GND，以保证器件正常运行。请参阅*慢速或悬空 CMOS 输入的影响*应用报告。

5.4 热性能信息

热指标[(1)]		SN74LVC1G06							单位
		DBV (SOT-23)	DCK (SC70)	DRL (SOT-5X3)	DRY (SON)	DPW (X2SON)	YZV (DSBGA)	YZP (DSBGA)	
		5 引脚	5 引脚	5 引脚	5 引脚	5 引脚	4 引脚	5 引脚	
$R_{\theta JA}$	结至环境热阻	357.1	371.0	296.2	369.6	511	168.2	144.4	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	263.7	297.5	137.3	257.6	241.9	2.1	1.3	°C/W
$R_{\theta JB}$	结至电路板热阻	264.4	258.6	145.3	230.8	374.2	55.9	39.9	°C/W
ψ_{JT}	结至顶部特征参数	195.6	195.6	14.7	77.2	45	1.1	0.5	°C/W
ψ_{JB}	结至电路板特征参数	262.2	256.2	145.9	231	373.3	56.3	39.7	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	不适用	不适用	168	不适用	不适用	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用手册。

5.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数		测试条件		V_{CC}	最小值	典型值[1]	最大值	单位
V_{OL}	高电平输出电压	I_{OL} = 100 μA		1.65V 至 5.5V			0.1	V
		I_{OL} = 4mA		1.65V			0.45	
		I_{OL} = 8mA		2.3V			0.3	
		I_{OL} = 16mA		3V			0.4	
		I_{OL} = 24mA					0.55	
		I_{OL} = 32mA		4.5V			0.55	
I_I	拐点电流	V_I = 5.5V 或 GND	A 输入	0 至 5.5V			±1	μA
I_{off}	关断状态电流	V_I 或 V_O = 5.5V		0			±10	μA
I_{CC}		V_I = 5.5V 或 GND，I_O = 0		1.65V 至 5.5V			10	μA
ΔI_{CC}		一个输入电压为 V_{CC} – 0.6V，另一个输入电压为 V_{CC} 或 GND		3V 至 5.5V			500	μA
C_I	输入电容	V_I = V_{CC} 或 GND		3.3V		4		pF
C_O	关断状态电容	V_O = V_{CC} 或 GND		3.3V		5		pF

(1) 所有典型值均在 V_{CC} = 3.3V、T_A = 25°C 下测得。

5.6 开关特性：-40°C 至 +85°C

在推荐的自然通风条件下的工作温度范围内测得，T_A = –40°C 至 +85°C（除非另有说明）（请参阅图 6-1）

参数		从（输入）	至（输出）	V_{CC}	最小值	最大值	单位
t_{pd}	传播延迟	A	Y	1.8V ± 0.15V	2.2	6.5	ns
				2.5V ± 0.2V	1.1	4	
				3.3V ± 0.3V	1.2	4	
				5V ± 0.5V	1	3	

5.7 开关特性：-40°C 至 +125°C

在推荐的自然通风条件下的工作温度范围内测得，T_A = –40°C 至 +125°C（除非另有说明）（请参阅图 6-1）

参数		从（输入）	至（输出）	V_{CC}	最小值	最大值	单位
t_{pd}	传播延迟	A	Y	1.8V ± 0.15V	2.2	7	ns
				2.5V ± 0.2V	1.1	4.5	
				3.3V ± 0.3V	1.2	4.5	
				5V ± 0.5V	1	3.5	

5.8 工作特性

T_A = 25°C

参数		测试条件	V_{CC}	典型值	单位
C_{pd}	功率耗散电容	f = 10MHz	1.8V	3	pF
			2.5V	3	
			3.3V	4	
			5V	6	

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5.9 典型特性

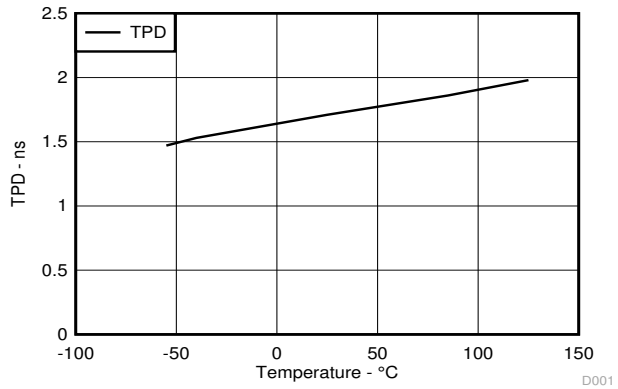


图 5-1. 3.3V V_{CC} 时 TPD 与温度间的关系

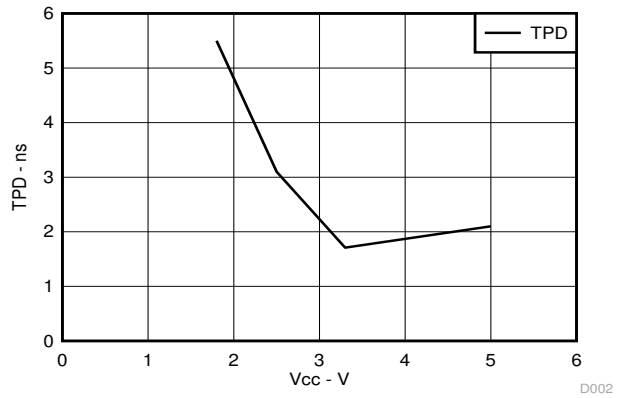
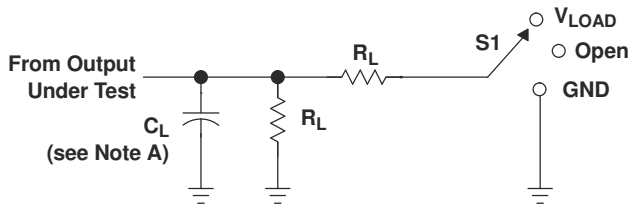


图 5-2. 25°C 时 TPD 与 V_{CC} 间的关系

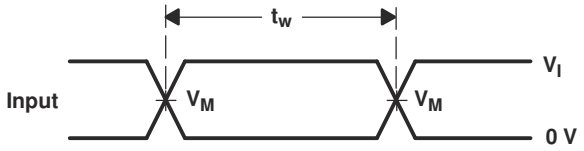
参数测量信息



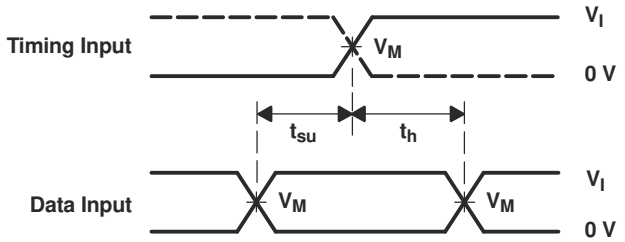
LOAD CIRCUIT

TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

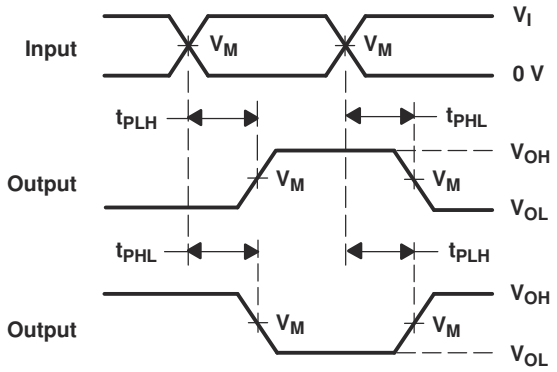
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



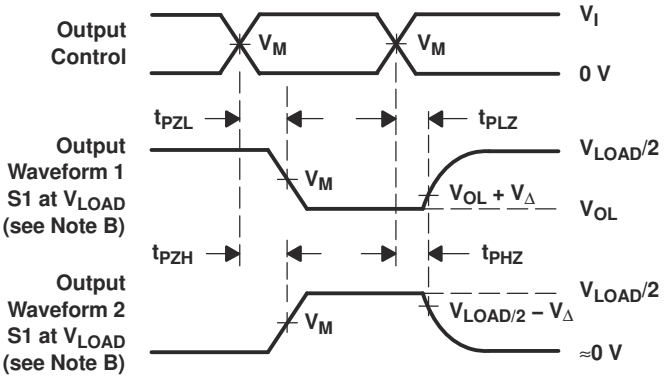
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
F. t_{PZL} is measured at V_M.
G. t_{PLZ} is measured at $V_{OL} + V_\Delta$.
H. All parameters and waveforms are not applicable to all devices.

图 6-1. 负载电路和电压波形（漏极开路）

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6 详细说明

6.1 概述

SN74LVC1G06 器件包含一个最大灌电流为 32mA 的开漏反相器。该器件专用于使用 I_{off} 的局部断电应用。当器件断电时，I_{off} 电路将会禁用输出。这会抑制电流回流到器件中，从而防止损坏器件。

6.2 功能方框图

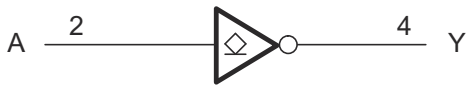

图 6-1. 逻辑图（正逻辑）

6.3 特性说明

6.3.1 CMOS 开漏输出

开漏输出允许器件将电流灌入 GND，但不会从 V_{CC} 拉出电流。当输出没有主动将线路拉至低电平时，它将进入高阻抗状态（三态）。由于输出电压可由外部上拉电阻器确定，因此该器件适用于各种应用，包括上行转换和下行转换。

考虑此器件的驱动能力可能在轻负载时产生快速边沿，因此布线和负载条件应避免振铃。此外，该器件的输出能够驱动的电流比此器件能够承受的电流更大，而不会损坏器件。务必限制器件的功率输出，以避免因过电流而导致热失控和器件损坏。必须始终遵守*绝对最大额定值*中规定的电气和热限值。

6.3.2 标准 CMOS 输入

标准 CMOS 输入的阻抗很高。通常，CMOS 输入被建模为与输入电容并联的电阻器，如*电气特性*中所示。最坏情况下的电阻是根据*绝对最大额定值*中给出的最大输入电压和*电气特性*中给出的最大输入漏电流，使用欧姆定律 (R = V ÷ I) 计算得出的。

施加到输入端的信号需要具有快速的边沿速率（由*建议运行条件*中的 Δt/Δv 定义），以避免过多的电流消耗和振荡。如果需要缓慢或有噪声的输入信号，应使用带有施密特触发输入的器件在标准 CMOS 输入之前调节输入信号。

6.3.3 负钳位二极管

该器件的输入和输出具有负钳位二极管，如图 6-2 所示。

> **小心**
>
> 电压超出*绝对最大额定值* 表中规定的值可能会损坏器件。如果遵守输入和输出钳制电流额定值，有可能超过输入负电压和输出电压额定值。

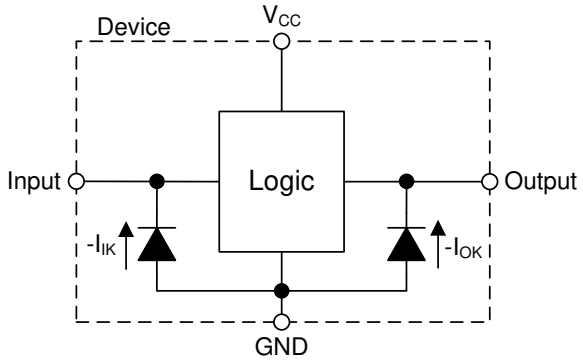

图 6-2. 每个输入和输出的钳位二极管的电气布置

6.3.4 局部断电 (I_{off})

当电源电压为 0V 时，每个输入和输出进入高阻抗状态。进出器件任何输入或输出引脚的最大漏电流由*电气特性*中的 I_{off} 指定。

6.3.5 过压耐受输入

此器件的输入信号只要保持低于*建议运行条件* 中指定的最大输入电压值，就可以驱动到高于电源电压的电压。

6.4 器件功能模式

表 6-1 列出了 SN74LVC1G06 器件的功能模式。

表 6-1. 功能表

输入 A	输出 Y
L	高阻态
H	L

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7 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 应用信息

SN74LVC1G06 是一款高驱动 CMOS 器件，可用于实现高输出驱动缓冲器，例如 LED 应用。它可以在 4.5V 时灌入 32mA 电流，因此非常适合高驱动应用。它非常适合高达 100MHz 的高速应用。输入可耐受 5.5V 电压，从而可将其升压或降压转换至 V_{CC}。下面显示了器件单个通道的简单 LED 驱动器应用。

7.2 典型应用

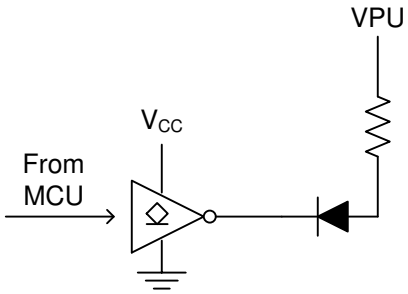

图 7-1. 典型应用图

7.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限值的电流。高驱动也会在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。

7.2.2 详细设计过程

1. 建议的输入条件
   - 上升时间和下降时间规格。请参阅*建议运行条件*表中的 $\Delta t/\Delta V$。
   - 指定的高电平和低电平。请参阅*建议运行条件*表中的 V_{IH} 和 V_{IL}。
   - 输入可耐受过压，允许它们在任何有效 V_{CC} 下高达*建议运行条件*表中的（V_I 最大值）。
2. 建议的输出条件
   - 每路输出的负载电流不应超过（I_O 最大值），且不能超过该器件的总电流（通过 V_{CC} 或 GND 的持续电流）。这些限值位于*绝对最大额定值*表中。
   - 输出不应被拉至高于 5.5V。

7.2.3 应用曲线

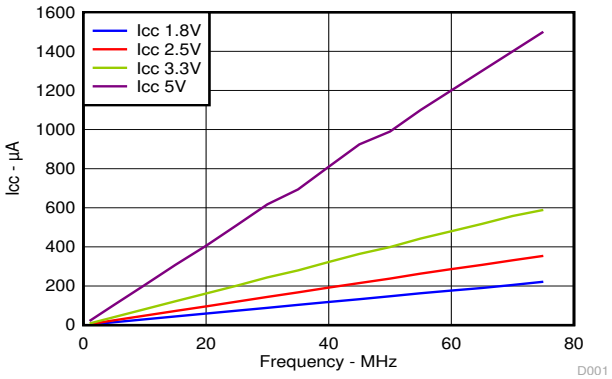

图 7-2. I_{CC} 与频率间的关系

7.3 电源相关建议

电源可以是*建议运行条件*中提供的最小和最大电源电压额定值之间的任何电压。

V_{CC} 引脚必须具有一个良好的旁路电容器，以防止功率干扰。建议使用 0.1µF 电容器，可以并联多个旁路电容器以抑制不同的噪声频率。0.1µF 和 1µF 电容器通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源引脚安装。

7.4 布局

7.4.1 布局指南

由于边沿速率较快，即使是低数据速率数字信号也可能包含高频信号分量。当印刷电路板 (PCB) 布线以 90° 角拐角时，会发生反射。反射的主要原因是布线宽度发生了变化。在拐角的顶点，布线宽度增加到原来宽度的 1.414 倍。这种增加会影响传输线特性，尤其是导致反射的布线的分布式电容和自感特性。并非所有 PCB 布线都是直线，因此某些布线必须拐角。图 7-3 展示了渐入佳境的圆角技术。只有最后一个示例（理想）保持恒定的布线宽度并能够更大限度地减少反射。

图 7-4 中提供了 DPW (X2SON-5) 封装的示例布局。此示例布局包括一个 0402（公制）电容器，并使用本数据表末尾所附示例板布局中的测量值。直径为 0.1mm (3.973mil) 的过孔直接放置在器件中心。该过孔可用于通过另一层电路板引出中心引脚连接，也可以不在布局中使用它。

7.4.2 布局示例

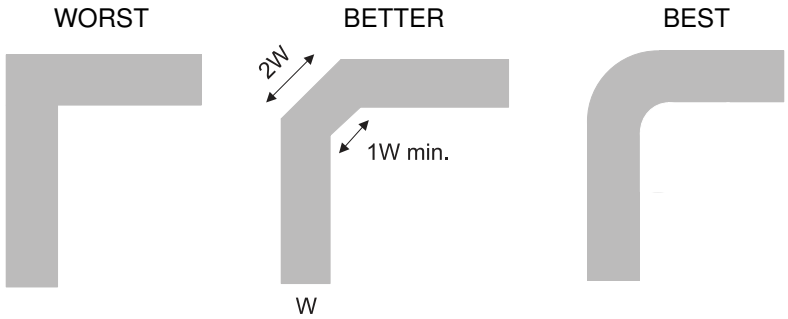

图 7-3. 布线示例

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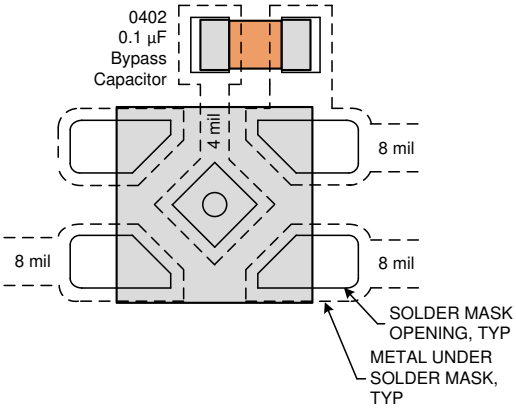

图 7-4. DPW (X2SON-5) 封装的示例布局

8 器件和文档支持

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 商标

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所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision AA (June 2025) to Revision AB (October 2025) — **Page**

- 将 DCK 封装的结至环境热阻值从：276.1°C/W 更改为：371.10C/W 5
- 将 DCK 封装的结至外壳（顶部）热阻值从：178.9°C/W 更改为：297.5°C/W 5
- 将 DCK 封装的结至电路板热阻值从：70.9°C/W 更改为：258.2°C/W 5
- 将 DCK 封装的结至顶部特征值从：47°C/W 更改为：195.6°C/W 5
- 将 DCK 封装的结至电路板特征值从：69.3°C/W 更改为：256.2°C/W 5

Changes from Revision Z (November 2017) to Revision AA (June 2025) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 将*器件信息* 表更改为*封装信息* 1
- 将 DBV 封装的结至环境热阻值从：231.5°C/W 更改为：357.1°C/W 5
- 将 DBV 封装的结至外壳（顶部）热阻值从：139.4°C/W 更改为：263.7°C/W 5
- 将 DBV 封装的结至电路板热阻值从：71.1°C/W 更改为：264.4°C/W 5
- 将 DBV 封装的结至顶部特征值从：45.2°C/W 更改为：195.6°C/W 5
- 将 DBV 封装的结至电路板特征值从：70.7°C/W 更改为：262.2°C/W 5

Changes from Revision Y (February 2017) to Revision Z (November 2017) — **Page**

- 更改了热性能信息表中的值以符合 JEDEC 标准 5

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- 更新了“特性说明”以包含有关特定器件特性的更多详细信息。.....9
- 添加了 DPW 布局示例.....12

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G06DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C065, C06F, C06J, C06R, C06T) (C06H, C06P, C06S)
SN74LVC1G06DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C065, C06F, C06J, C06R, C06T) (C06H, C06P, C06S)
SN74LVC1G06DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C065, C06F, C06J, C06R, C06T) (C06H, C06P, C06S)
SN74LVC1G06DBVRE4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F
SN74LVC1G06DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F
SN74LVC1G06DBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F
SN74LVC1G06DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C065, C06F, C06J, C06R) (C06H, C06P, C06S)
SN74LVC1G06DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C065, C06F, C06J, C06R) (C06H, C06P, C06S)
SN74LVC1G06DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F
SN74LVC1G06DBVTG4.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F
SN74LVC1G06DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTJ, CTK, CTR, CTT) (CTH, CTS)
SN74LVC1G06DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTJ, CTK, CTR, CTT) (CTH, CTS)
SN74LVC1G06DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTJ, CTK, CTR, CTT) (CTH, CTS)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G06DCKRE4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKRE4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT5
SN74LVC1G06DCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT5
SN74LVC1G06DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTJ, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTJ, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKTE4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKTE4.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKTG4.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CO
SN74LVC1G06DPWR.B	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CO
SN74LVC1G06DRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CT7, CTR)
SN74LVC1G06DRLR.B	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CT7, CTR)
SN74LVC1G06DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DRYRG4	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DRYRG4.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CT

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G06DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DSFRG4	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DSFRG4.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CTN
SN74LVC1G06YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CTN
SN74LVC1G06YZVR	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CT N
SN74LVC1G06YZVR.B	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CT N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G06 :

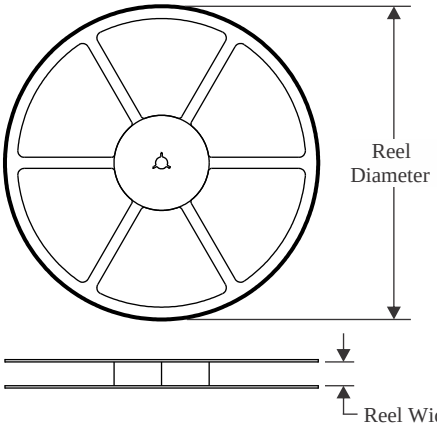
- Automotive : SN74LVC1G06-Q1
- Enhanced Product : SN74LVC1G06-EP

NOTE: Qualified Version Definitions:

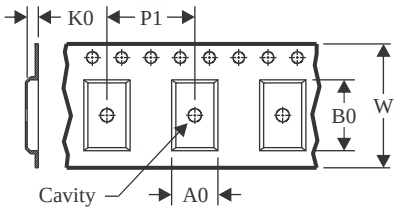
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

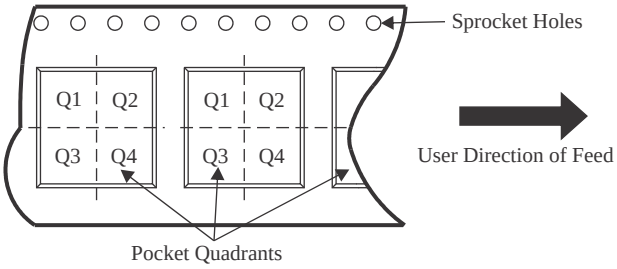


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

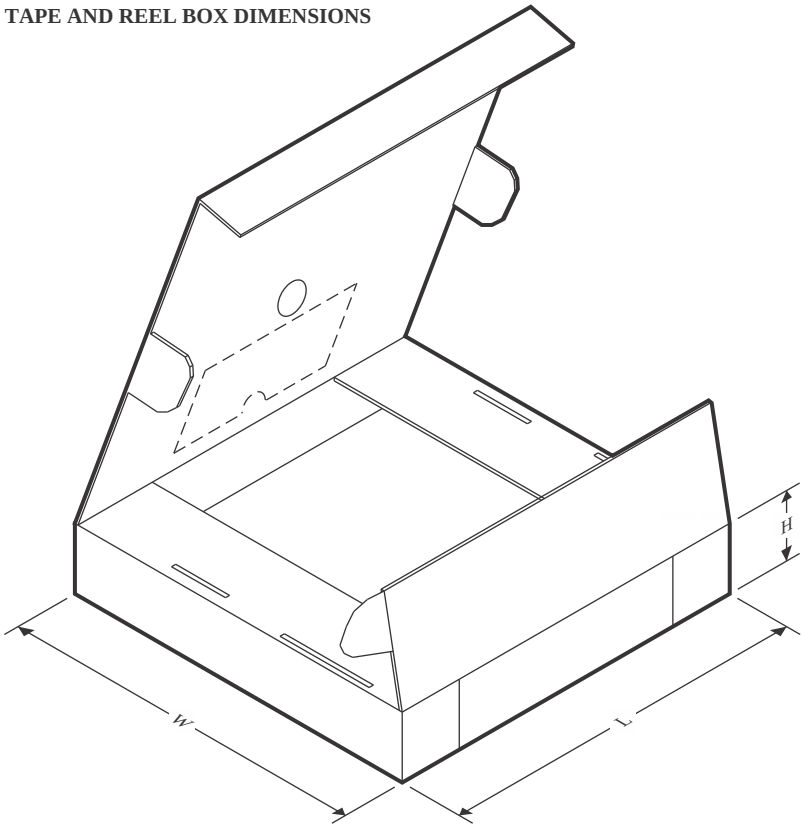


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G06DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G06DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G06DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G06DCKRE4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G06DCKTE4	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G06DCKTE4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKTE4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G06DCKTG4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G06DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G06DCKTG4	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G06DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G06DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G06DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G06DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G06DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G06DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G06YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G06YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

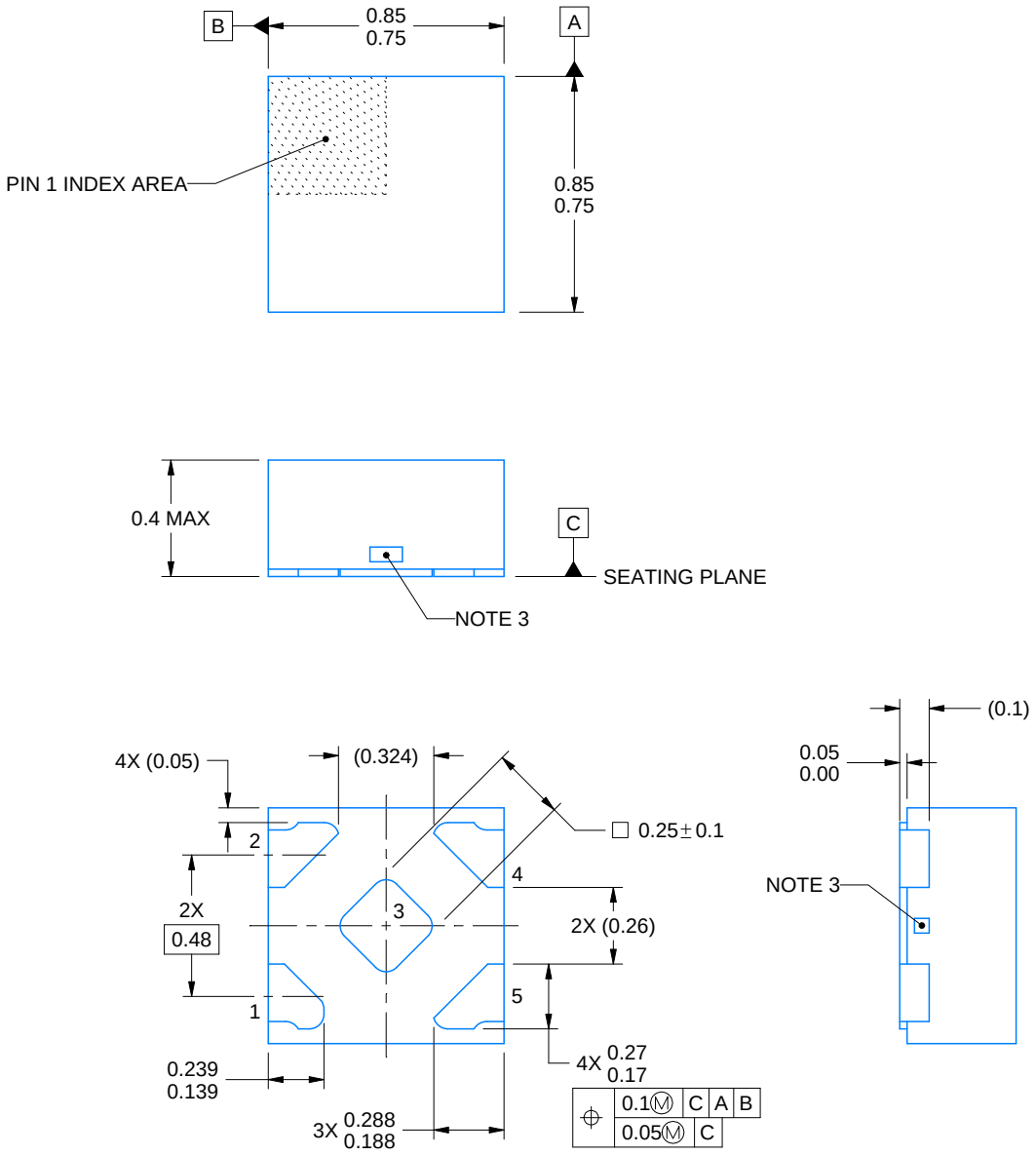
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G06DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G06DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G06DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G06DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G06DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74LVC1G06DCKRE4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G06DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKTE4	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G06DCKTE4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKTE4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKTG4	SC70	DCK	5	250	202.0	201.0	28.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G06DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G06DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G06DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G06DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G06DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G06DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G06YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G06YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

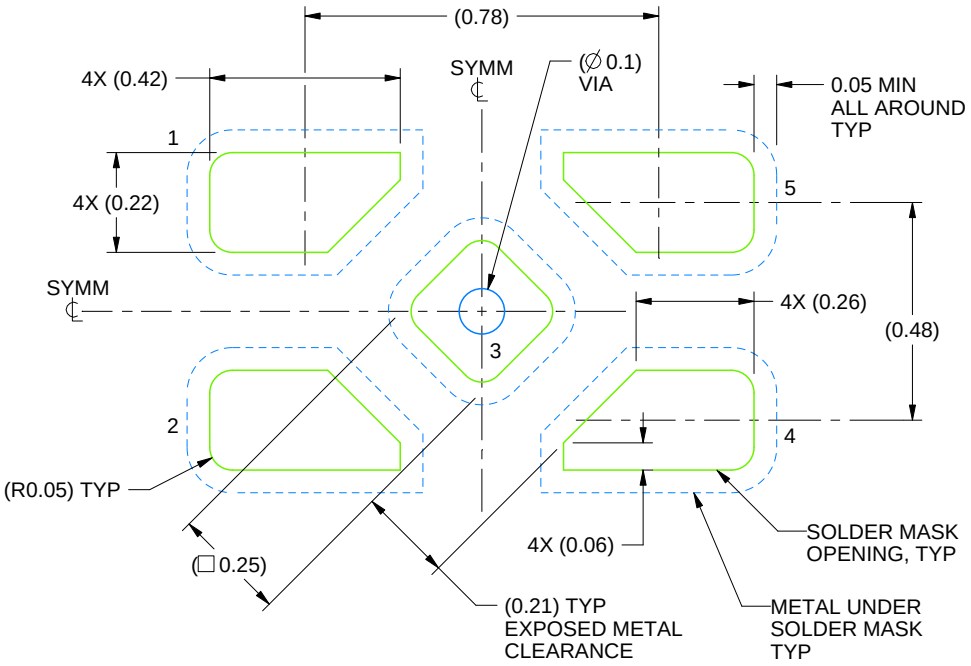
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

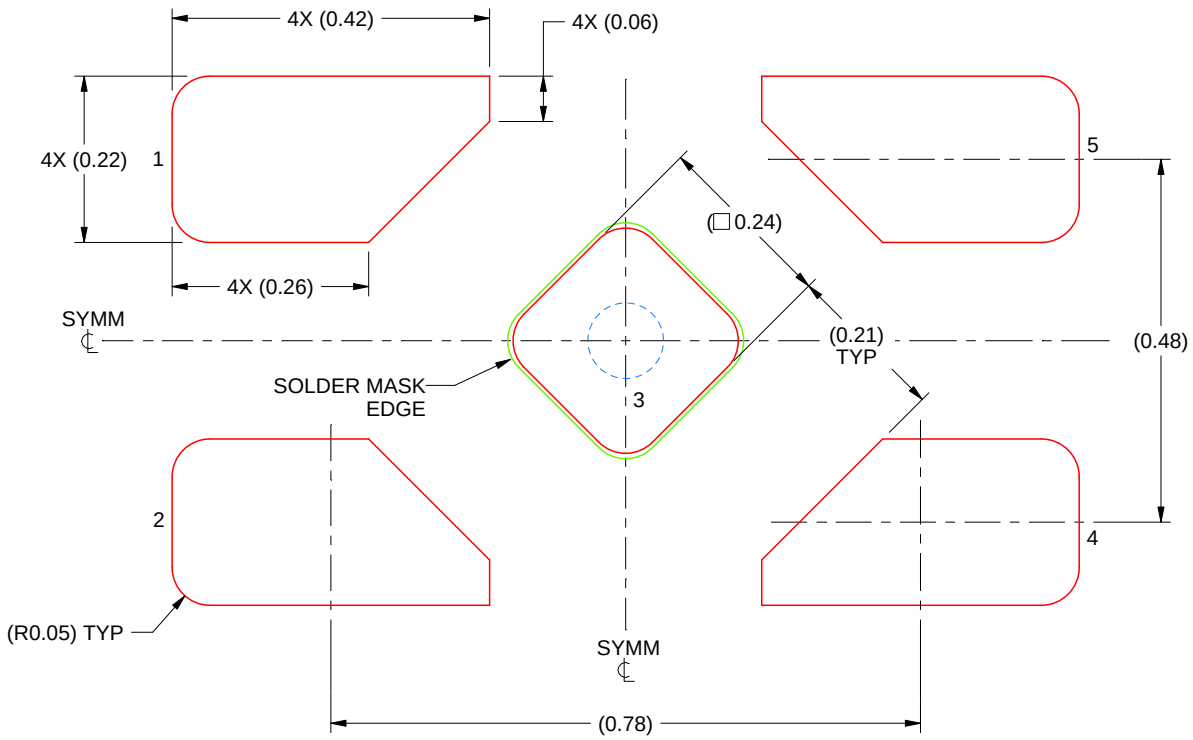


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



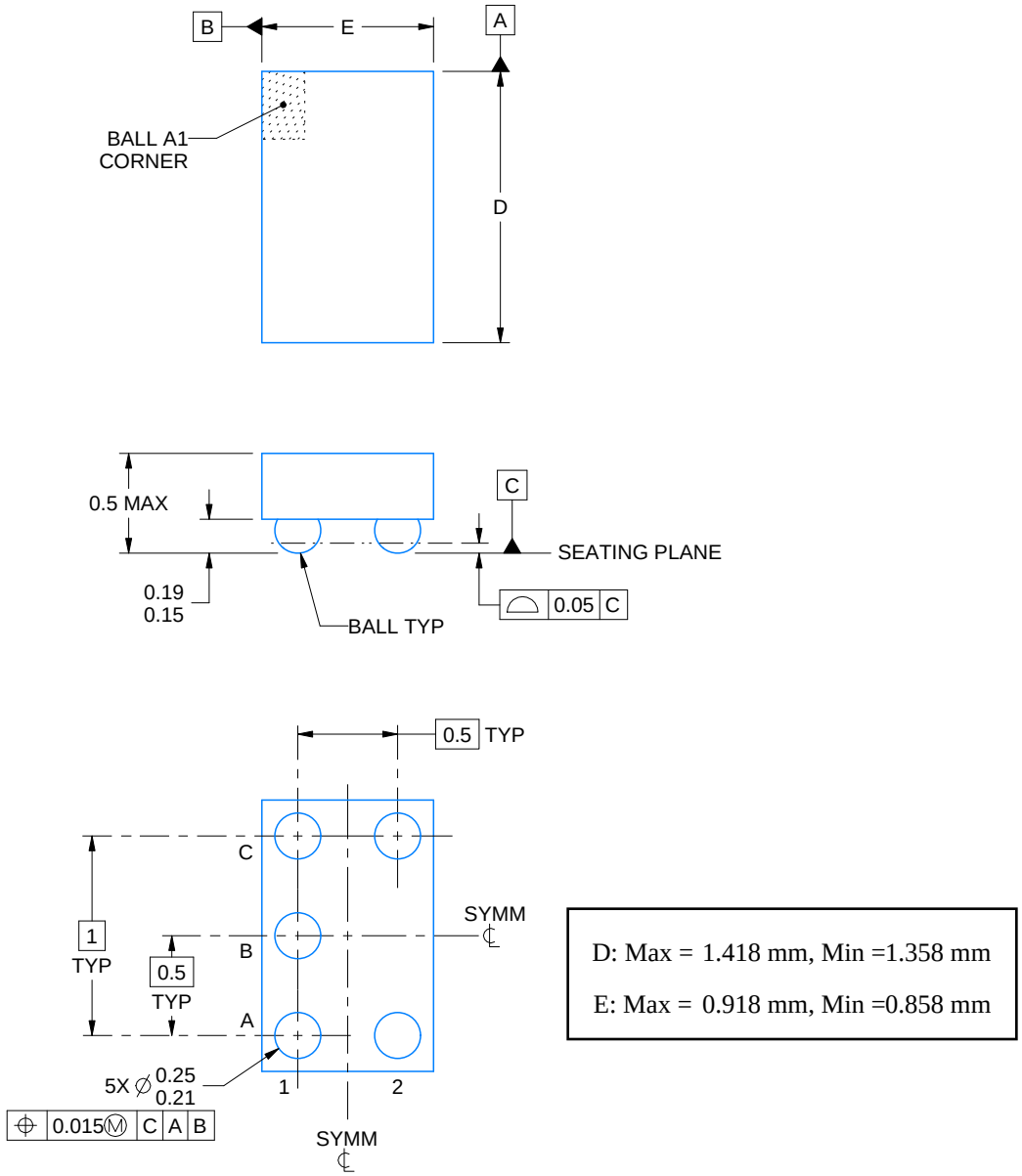
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

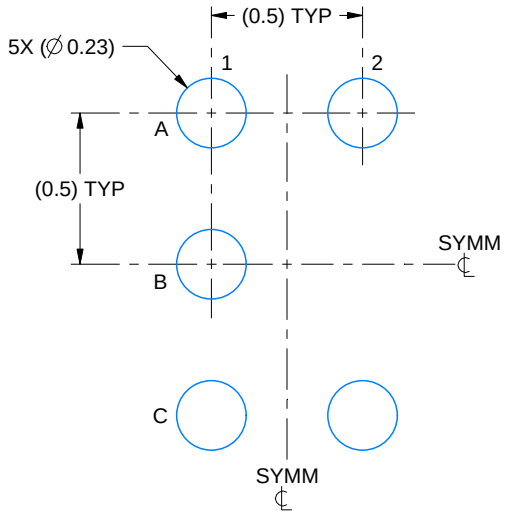
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

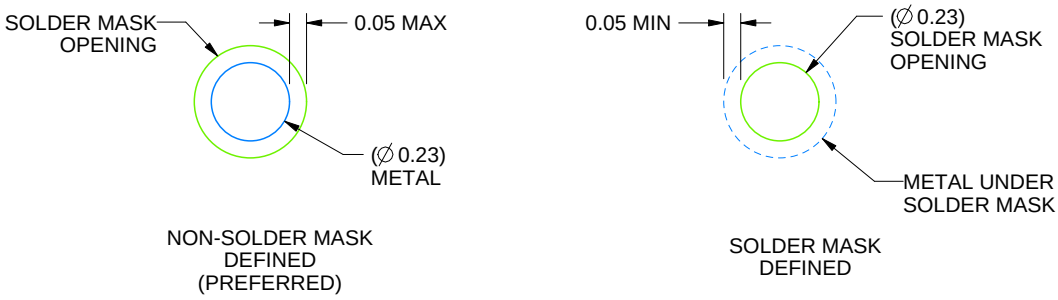


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

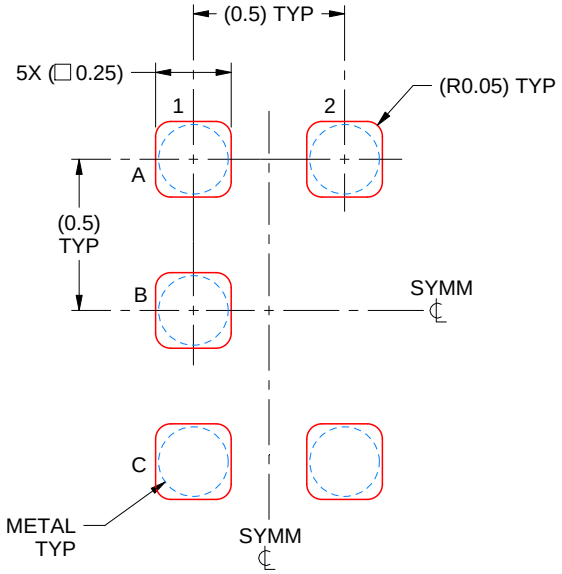


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



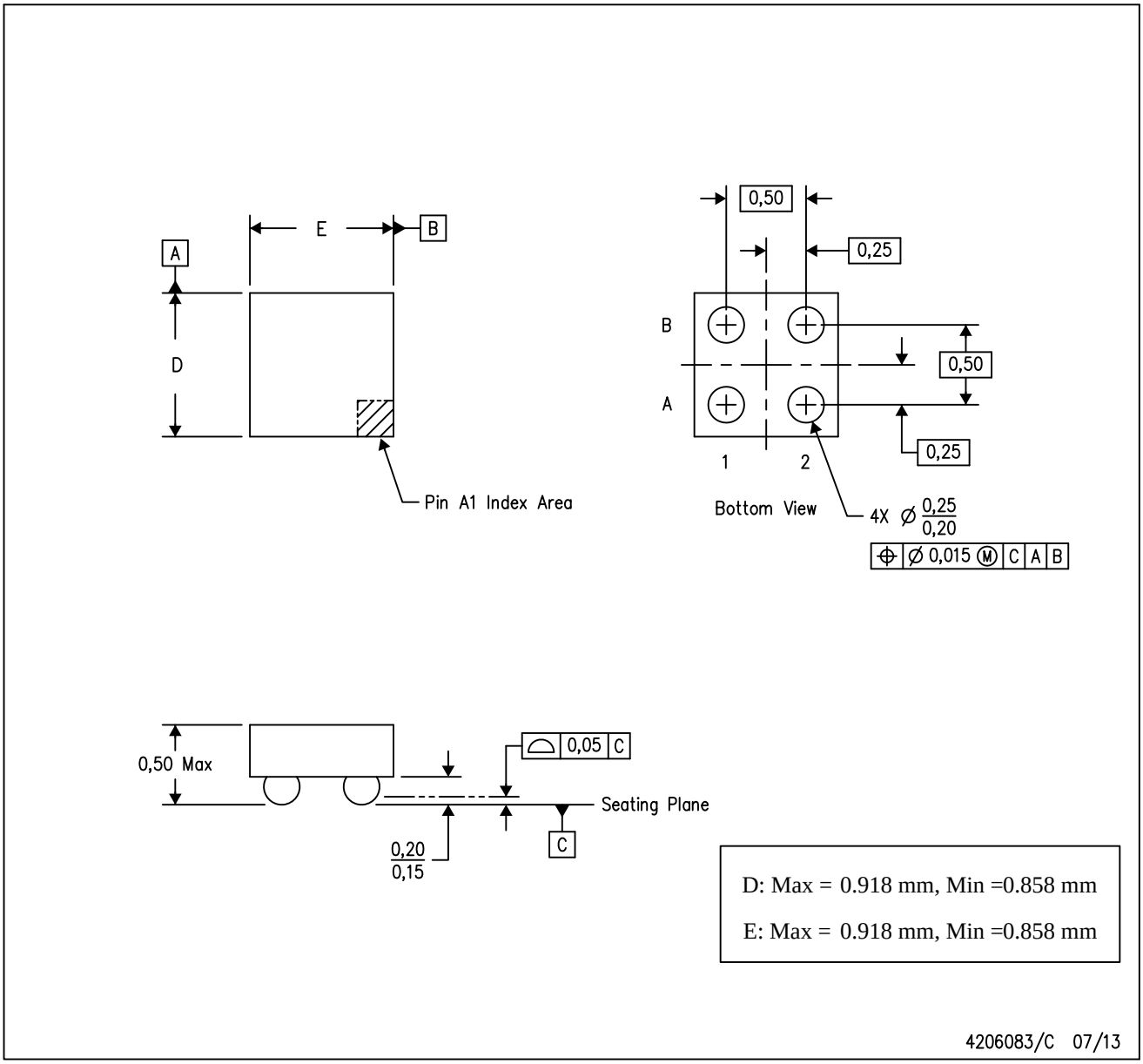
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

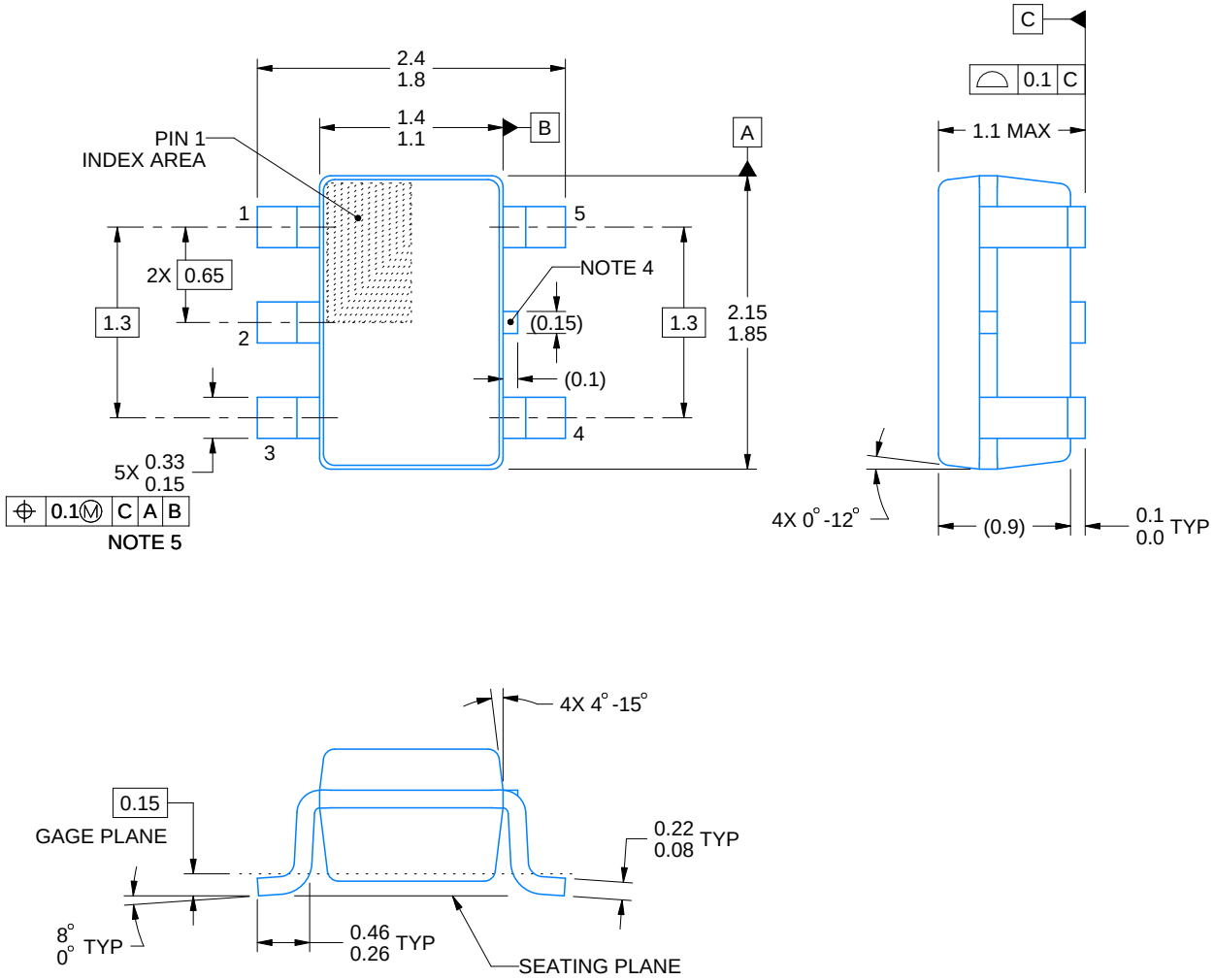
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S-XBGA-N4) DIE-SIZE BALL GRID ARRAY



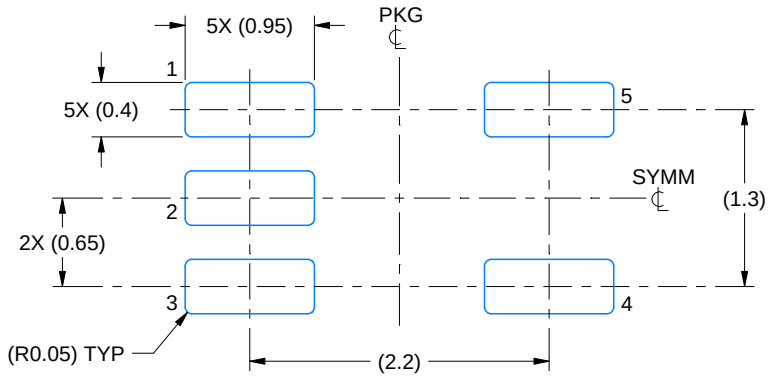
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

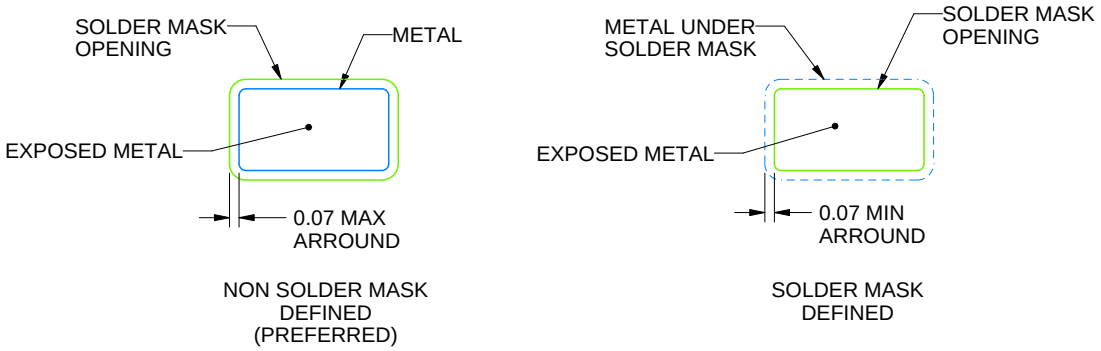


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

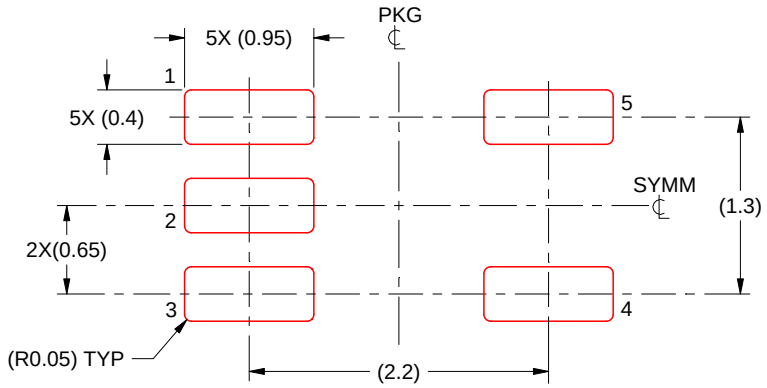


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

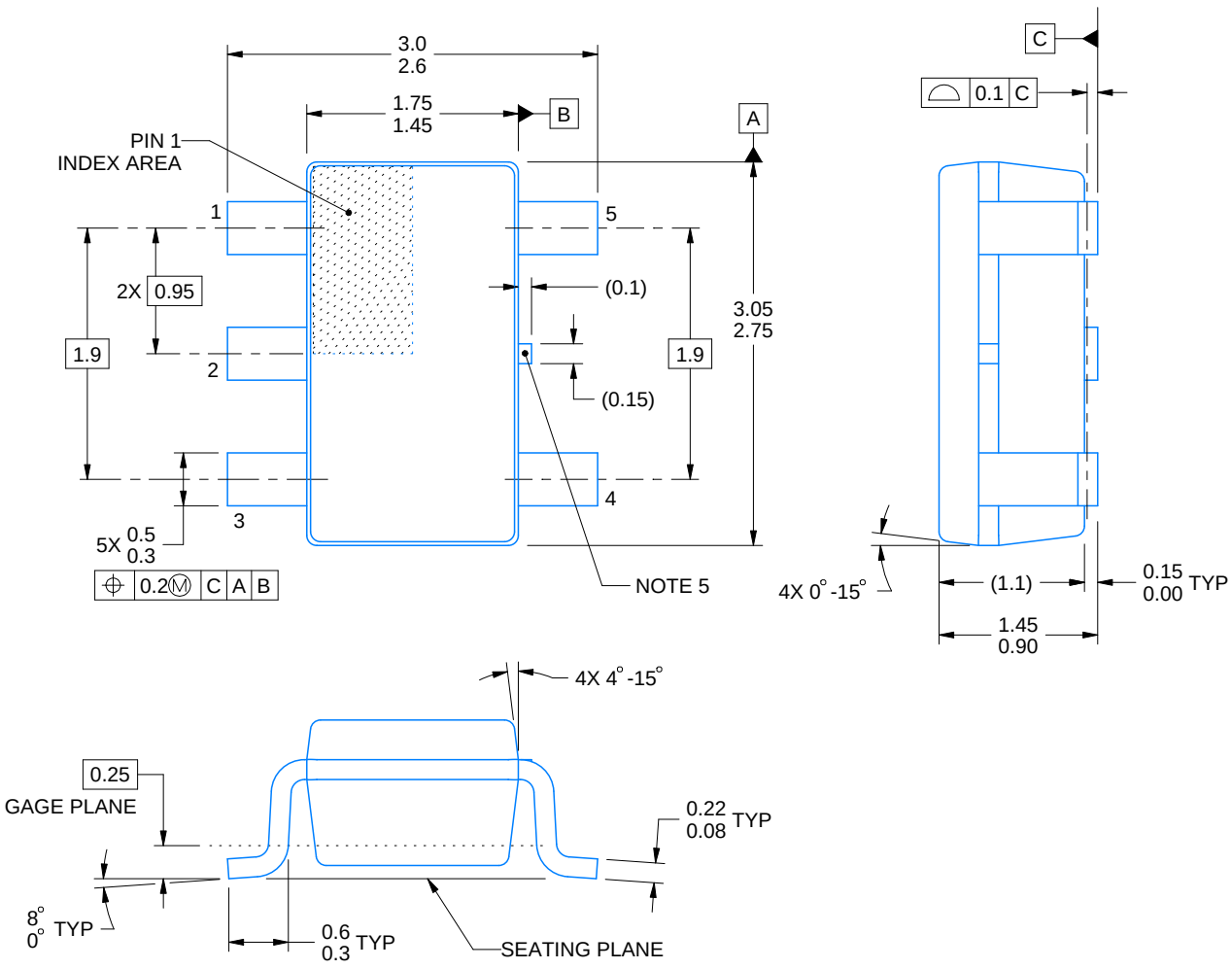


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

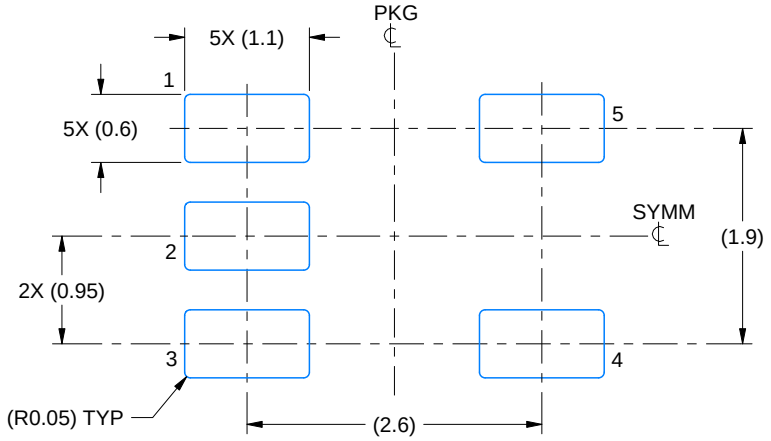
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



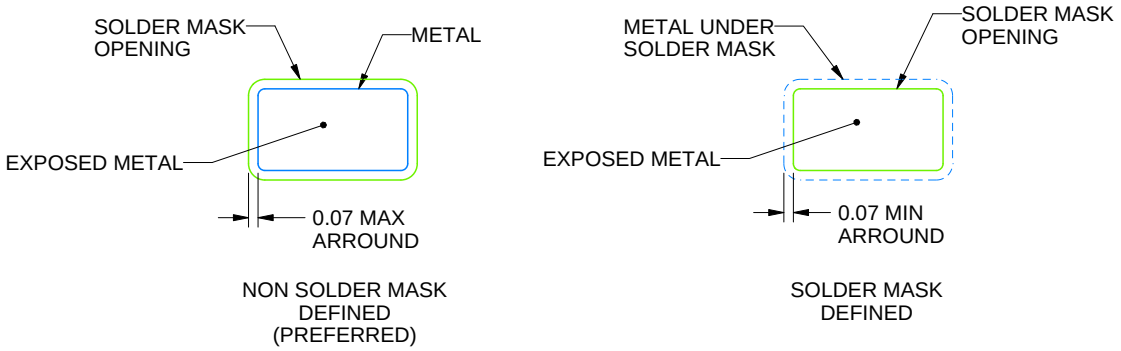
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

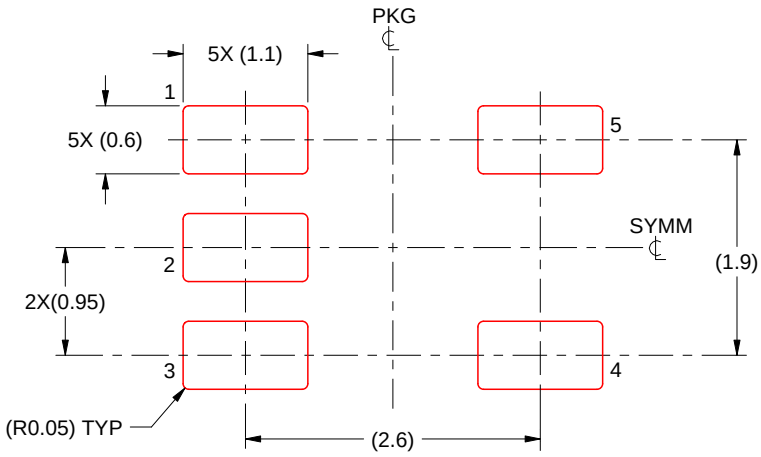


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



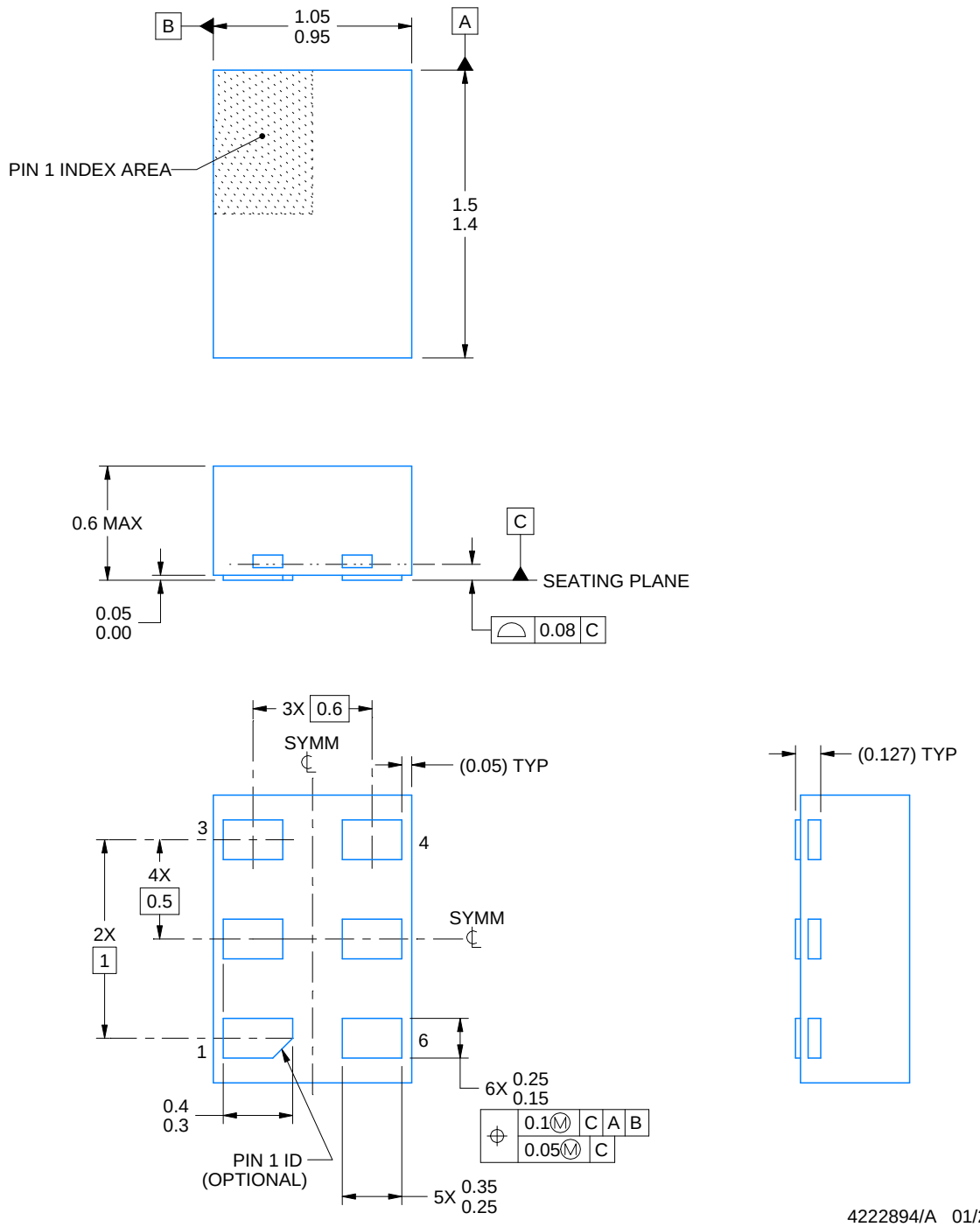
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

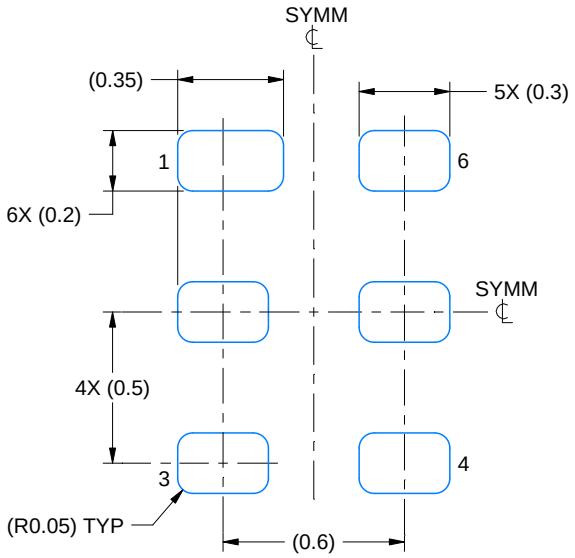
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

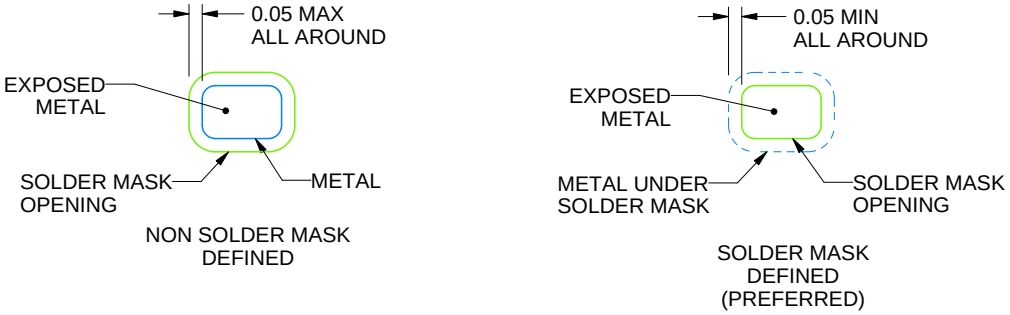


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X

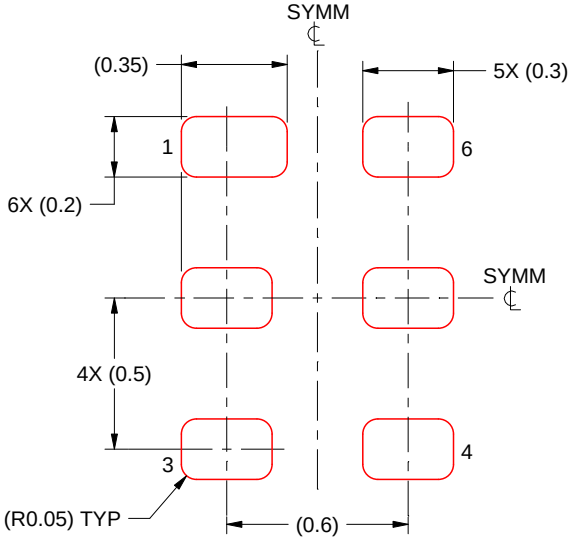


SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

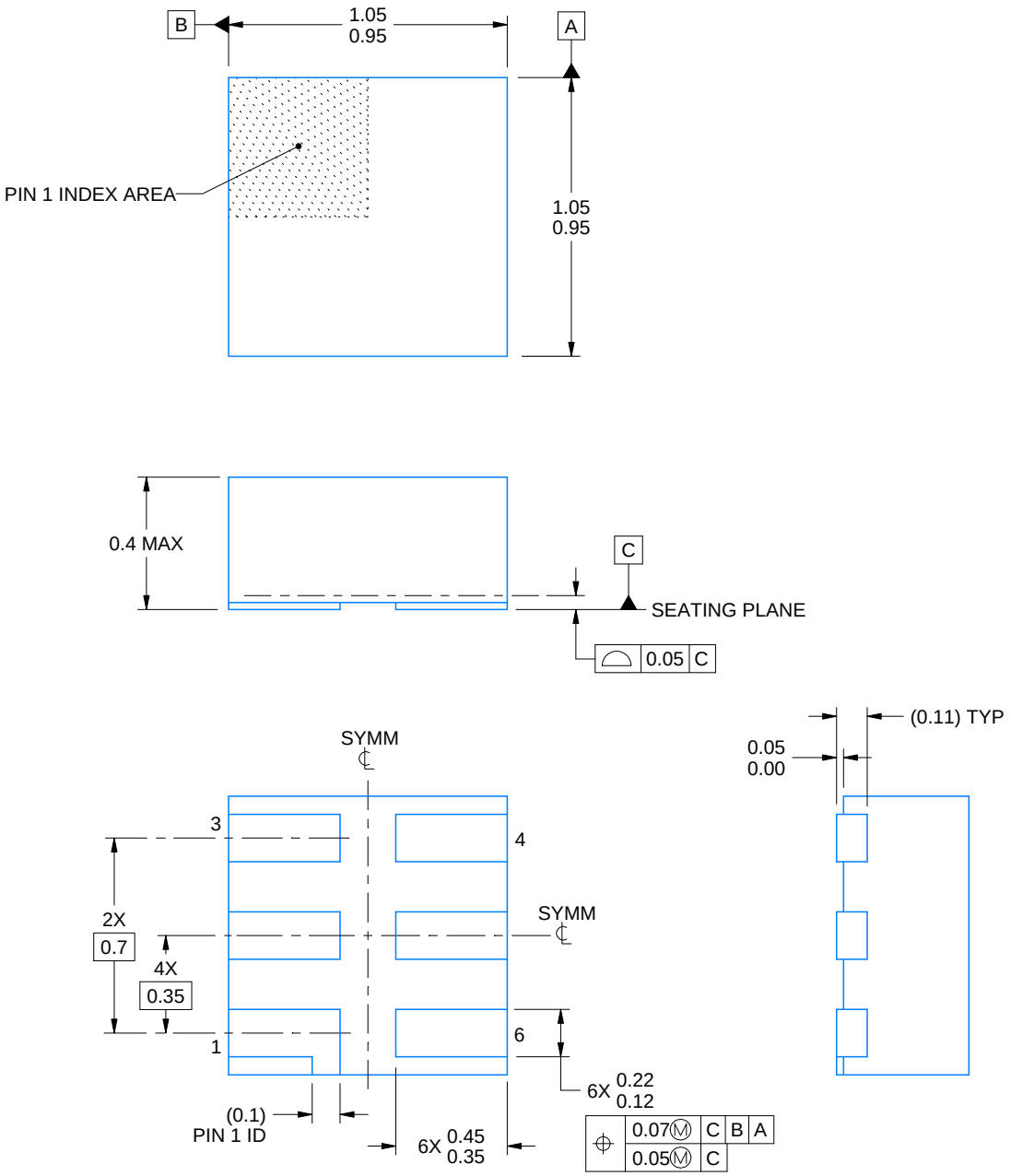


SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

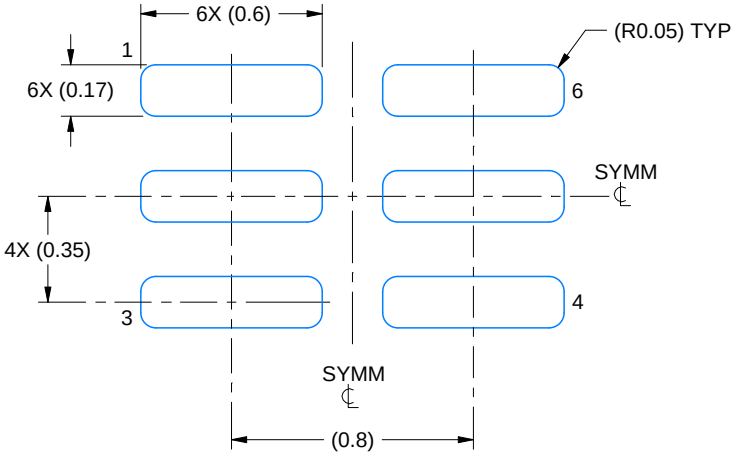
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



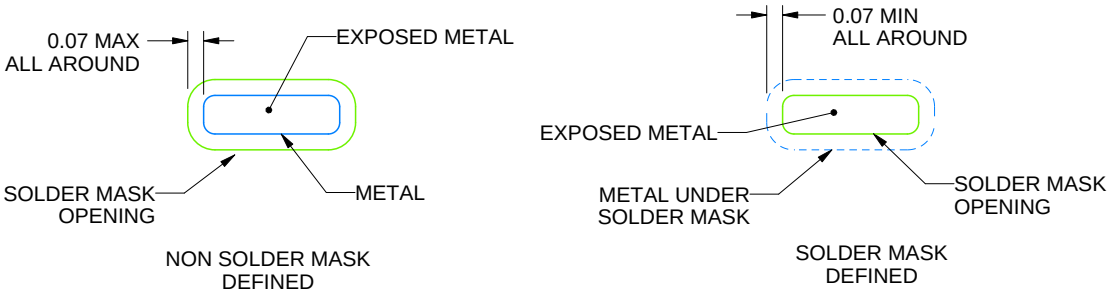
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X

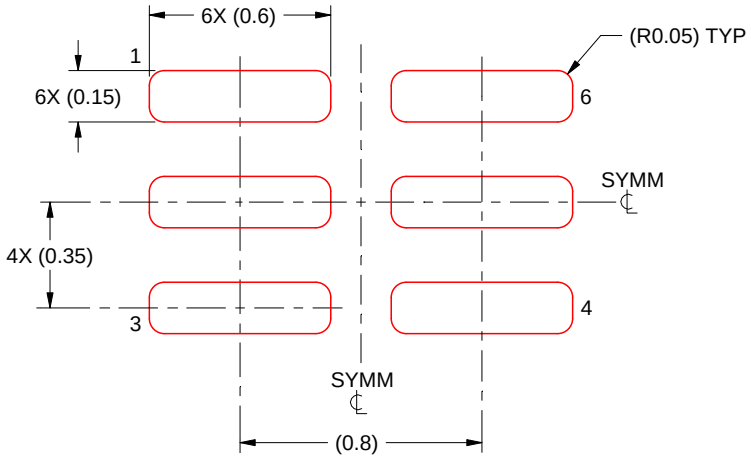


SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

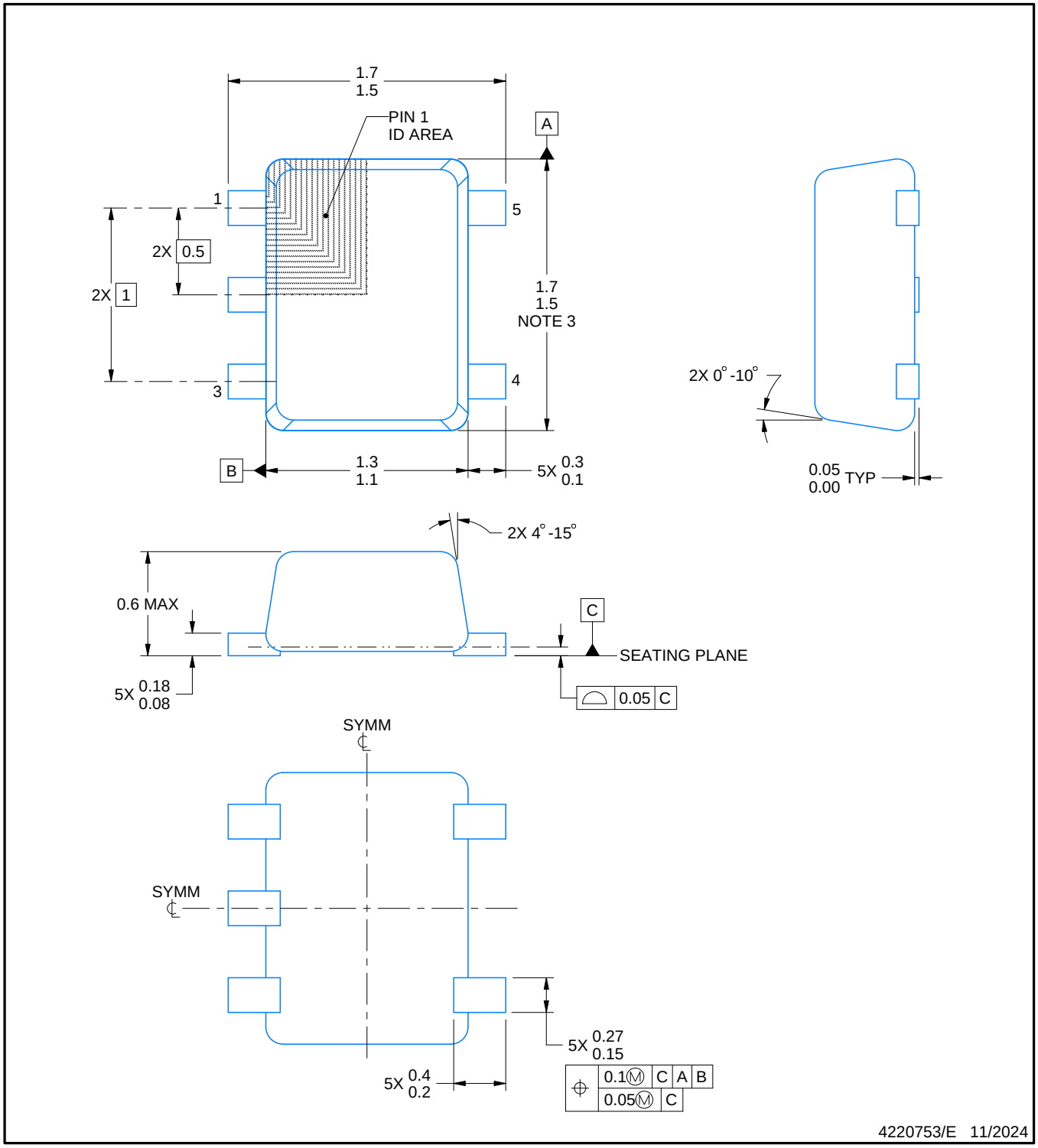


SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

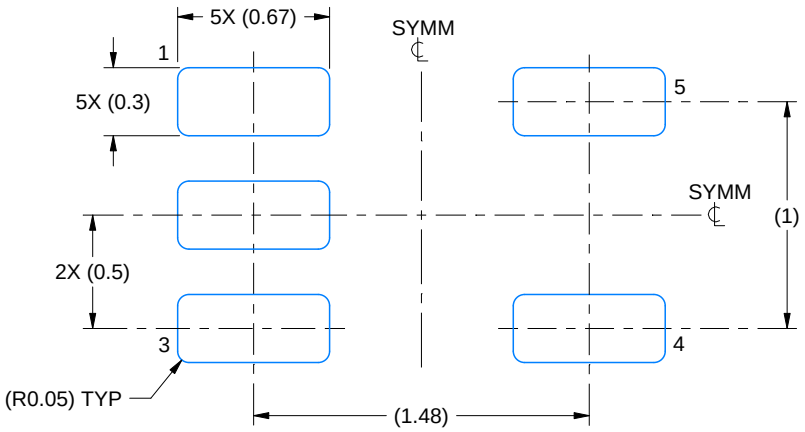
4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

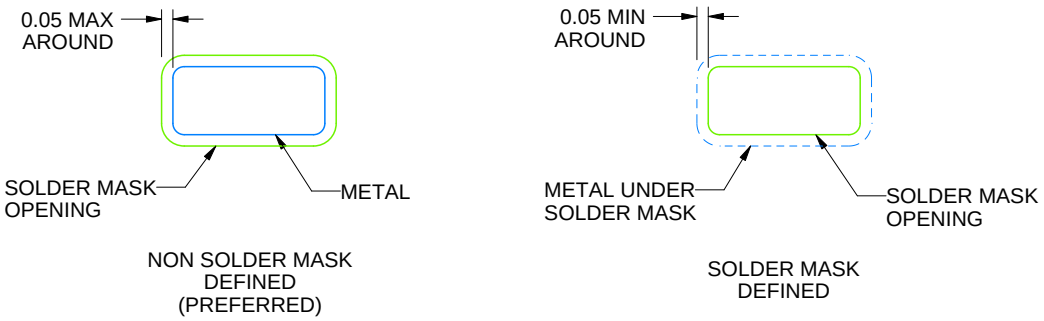


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

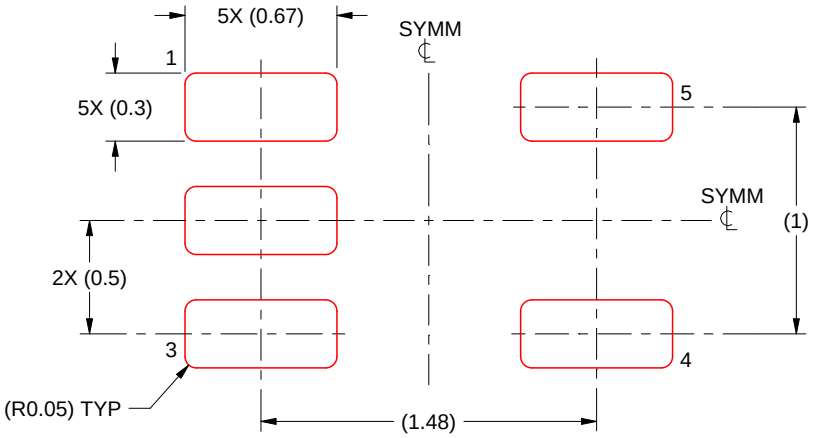


SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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