16 位双电源总线收发器
此收发器具有可配置电压转换和三态输出

查询样品: SN74LVC16T245-EP

特性

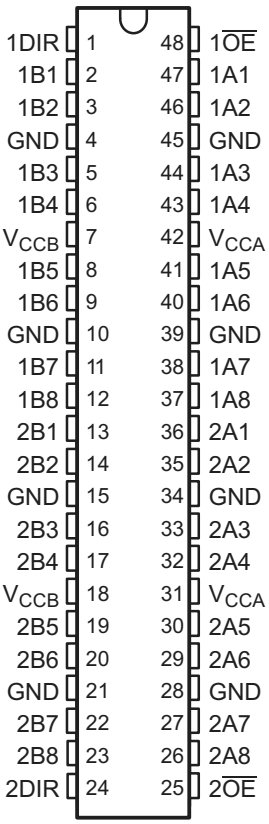
- 控制输入 V_{IH}和 V_{IL}电平以 V_{CCA}电压为基准
- V_{CC}隔离特性-如果任何一个 V_{CC}输入接地 (GND)，那么两个端口都处于高阻抗状态
- 过压耐受输入和输出可实现混合电压模式数据通信
- 完全可配置双电源轨设计可使每个端口在整个 1.65V-5.5V 电源电压范围内运行
- $I_{关闭}$ 支持部分断电模式工作
- 锁断性能超过 100mA（符合 JESD 78，II 类规范的要求）
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求
  - 2000V 人体模型 (A114-A)
  - 200V 机器模型 (A115-A)
  - 1000V 充电器件模型 (C101)

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 军用（-55°C 至 125°C）温度范围内可用 (1)
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

(1) 可定制工作温度范围

DGG 封装
(顶视图)



说明

这个 16 位非反相总线收发器使用两个独立的可配置电源轨。 A 端口被设计用于跟踪 V_{CCA}。 V_{CCA}可接受从 1.65V 到 5.5V 范围内的任意电源电压。B 端口被设计用于跟踪 V_{CCB}。 V_{CCB}可接受从 1.65 至 5.5V 间的任一电源电压值。这可实现 1.8V，2.5V，3.3V和 5V 电压节点间的通用低压双向转换。

说明（继续）

SN74LVC16T245 针对两条数据总线间的异步通信而设计。 方向控制 (DIR) 输入和输出使能 ($\overline{OE}$) 输入的逻辑电平激活 B 端口输出或者 A 端口输出，或者将两个输出端口都置于高阻抗模式。 当 B 端口输出被激活时，此器件将数据从 A 总线发送到 B 总线，而当 A 端口输出被激活时，此器件将数据从 B 总线发送到 A 总线。 A 端口和 B 端口上的输入电路一直处于激活状态并且必须施加一个逻辑高或低电平以防止过多的 I_{CC}和 I_{CCZ}。

SN74LVC16T245 的设计方式决定了控制引脚（1DIR，2DIR，1$\overline{OE}$和2$\overline{OE}$）由 V_{CCA}供电。

该器件完全符合使用 $I_{关闭}$的部分断电应用的规范要求。 $I_{关闭}$电路禁用输出，从而可防止其断电时破坏性电流从该器件回流。

V_{CC}隔离特性可确保 V_{CC}中的任何一个是否接地，然后两个端口都处于高阻抗状态。

为了确保加电或断电期间的高阻抗状态，$\overline{OE}$应通过一个上拉电阻器被连接至 V_{CC}；该电阻器的最小值由驱动器的电流吸收能力来决定。

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	TSSOP-DGG	Reel of 2000	CLVC16T245MDGGREP	LVC16T245M	V62/12667-01XE
		Tube of 40	CLVC16T245MDGGEP		V62/12667-01XE-T

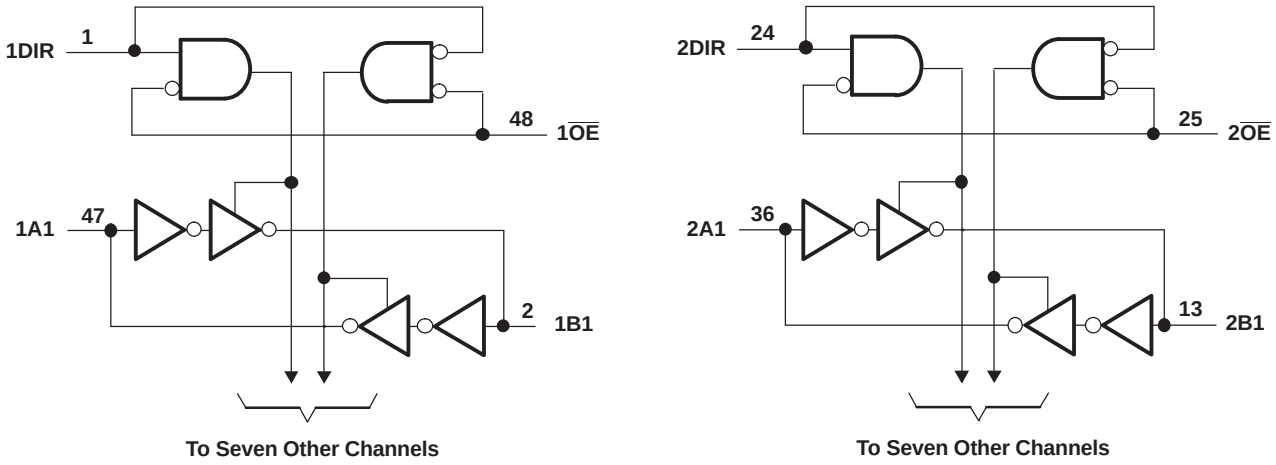
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE(1)
(EACH 8-BIT SECTION)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)	I/O ports (A port)	–0.5	6.5	V
		I/O ports (B port)	–0.5	6.5	
		Control inputs	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	6.5	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA}, V_{CCB}, and GND			±100	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

THERMAL INFORMATION

THERMAL METRIC(1)		SN74LVC16T245 DGG 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	59.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	13.9	
θ_{JB}	Junction-to-board thermal resistance(4)	27.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	26.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

Recommended Operating Conditions (1)(2)(3)(4)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs (5)	1.65 V to 1.95 V		V_{CCI} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCI} × 0.7		
V_{IL}	Low-level input voltage	Data inputs (5)	1.65 V to 1.95 V			V_{CCI} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCI} × 0.3	
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCA}) (6)	1.65 V to 1.95 V		V_{CCA} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCA} × 0.7		
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCA}) (6)	1.65 V to 1.95 V			V_{CCA} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCA} × 0.3	
V_I	Input voltage	Control inputs			0	5.5	V
$V_{I/O}$	Input/output voltage	Active state			0	V_{CCO}	V
		3-State			0	5.5	
I_{OH}	High-level output current			1.65 V to 1.95 V		–4	mA
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–24	
				4.5 V to 5.5 V		–32	
I_{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
T_A	Operating free-air temperature				–55	125	°C

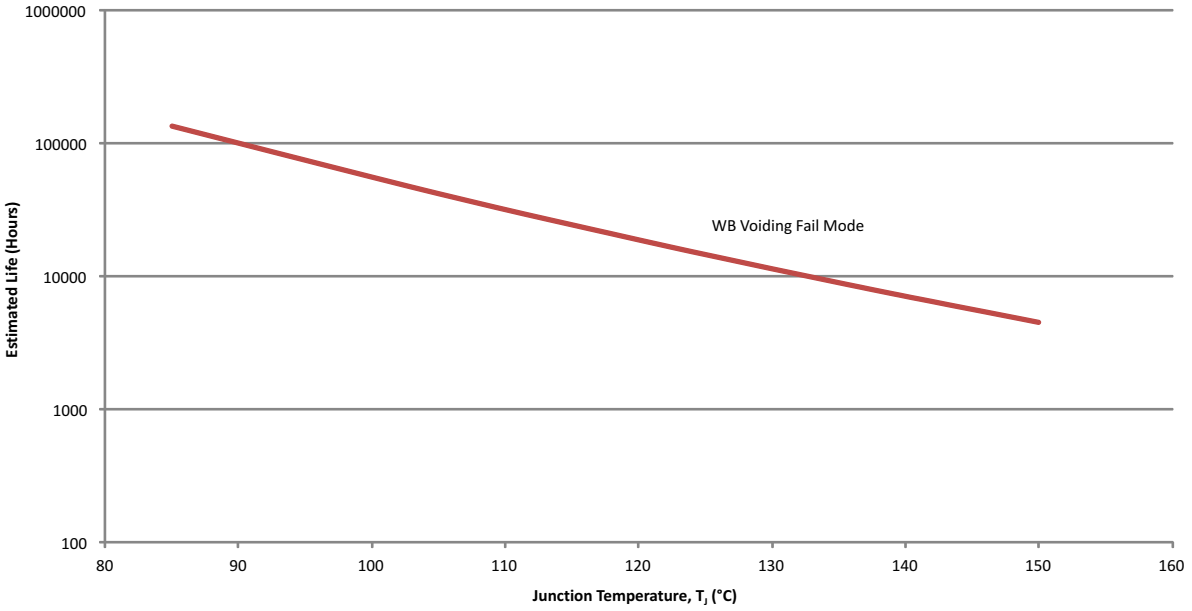
(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) All unused data inputs of the device must be held at V_{CCA} or GND to ensure proper device operation.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(6) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

Electrical Characteristics(1)(2)

T_A = −55°C to 125°C, over recommended input voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100 µA, $V_I = V_{IH}$	1.65 V to 4.5 V	1.65 V to 4.5 V	V_{CCO} – 0.1			V
		I_{OH} = –4 mA, $V_I = V_{IH}$	1.65 V	1.65 V	1.2			
		I_{OH} = –8 mA, $V_I = V_{IH}$	2.3 V	2.3 V	1.9			
		I_{OH} = –24 mA, $V_I = V_{IH}$	3 V	3 V	2.35			
		I_{OH} = –32 mA, $V_I = V_{IH}$	4.5 V	4.5 V	3.75			
V_{OL}		I_{OL} = 100 µA, $V_I = V_{IL}$	1.65 V to 4.5 V	1.65 V to 4.5 V			0.1	V
		I_{OL} = 4 mA, $V_I = V_{IL}$	1.65 V	1.65 V			0.45	
		I_{OL} = 8 mA, $V_I = V_{IL}$	2.3 V	2.3 V			0.3	
		I_{OL} = 24 mA, $V_I = V_{IL}$	3 V	3 V			0.65	
		I_{OL} = 32 mA, $V_I = V_{IL}$	4.5 V	4.5 V			0.65	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	1.65 V to 5.5 V	1.65 V to 5.5 V			±2	µA
I_{off}	A or B port	V_I or V_O = 0 to 5.5 V	0 V	0 to 5.5 V			±10	µA
			0 to 5.5 V	0 V			±10	
I_{OZ}	A or B port	$\overline{V_O} = V_{CCO}$ or GND, $\overline{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V			±10	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V			20	µA
			5 V	0 V			20	
			0 V	5 V			–2.5	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V			20	µA
			5 V	0 V			–2.5	
			0 V	5 V			20	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V			30	µA
ΔI_{CCA}	A port	One A port at V_{CCA} – 0.6 V, DIR at V_{CCA}, B port = open	3 V to 5.5 V	3 V to 5.5 V			50	µA
	DIR	DIR at V_{CCA} – 0.6 V, B port = open, A port at V_{CCA} or GND					50	
ΔI_{CCB}	B port	One B port at V_{CCB} – 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V			50	µA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	3.3 V	3.3 V		4		pF
C_{io}	A or B port	$V_O = V_{CCA/B}$ or GND	3.3 V	3.3 V		8.5		pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

Figure 1. SN74LVC16T245-EP Operating Life Derating Chart

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.7	21.9	1.3	9.2	1	7.4	0.8	7.1	ns
t_{PHL}											
t_{PLH}	B	A	0.9	23.8	0.8	23.6	0.7	23.4	0.7	23.4	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	1.6	29.6	1.5	29.4	1.5	29.3	1.4	29.2	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2.4	32.2	1.9	13.1	1.7	12	1.3	10.3	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	0.4	24	0.4	23.8	0.4	23.7	0.4	23.7	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.8	32	1.6	16	1.2	12.6	0.9	10.8	ns
t_{PZL}											

Switching Characteristics

T_A = −55°C to 125°C, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B		25.9		13.2		11.4		11.1	ns
t_{PHL}											
t_{PLH}	B	A		27.8		27.8		27.4		27.4	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A		33.6		33.4		33.3		33.2	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B		36.2		17.1		16		14.3	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A		28		27.8		27.7		27.7	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B		36		22		16.6		14.8	ns
t_{PZL}											

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.6	21.4	1.2	9	0.8	6.2	0.6	4.8	ns
t_{PHL}											
t_{PLH}	B	A	1.2	9.3	1	9.1	1	8.9	0.9	8.8	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	1.4	9	1.4	9	1.4	9	1.4	9	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2.3	29.6	1.8	11	1.7	9.3	0.9	6.9	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	1	10.9	1	10.9	1	10.9	1	10.9	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.7	28.2	1.6	12.9	1.2	9.4	1	6.9	ns
t_{PZL}											

Switching Characteristics

T_A = −55°C to 125°C, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B		25.4		13		10.2		8.8	ns
t_{PHL}											
t_{PLH}	B	A		13.3		13.1		12.9		12.8	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A		13		13		13		13	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B		33.6		14		14.3		10.9	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A		14.9		14.9		14.9		14.9	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B		32.2		16.9		13.4		10.9	ns
t_{PZL}											

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	21.2	1.1	8.8	0.8	6.1	0.5	4.4	ns
t_{PHL}											
t_{PLH}	B	A	0.9	7.2	0.8	6.2	0.7	6.1	0.6	6	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	1.6	8.2	1.6	8.2	1.6	6.2	1.6	8.2	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2.1	29	1.7	10.3	1.5	8.6	0.8	6.3	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	0.8	7.8	0.8	7.8	0.8	7.8	0.8	7.8	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.6	27.7	1.4	12.4	1.1	8.5	0.9	8.4	ns
t_{PZL}											

Switching Characteristics

T_A = −55°C to 125°C, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B		25.2		12.8		10.2		8.4	ns
t_{PHL}											
t_{PLH}	B	A		11.2		10.2		10.1		10	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A		12.2		12.2		12.2		12.2	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B		33		14.3		12.8		10.3	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A		11.8		12.1		12.1		12.1	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B		31.7		16.4		12.9		10.4	ns
t_{PZL}											

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.6	21.4	1	8.8	0.7	6	0.4	4.2	ns
t_{PHL}											
t_{PLH}	B	A	0.7	6.8	0.4	4.8	0.3	4.5	0.3	4.3	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	0.3	5.4	0.3	5.4	0.3	5.4	0.3	6.4	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2	28.7	1.6	9.7	1.4	8	0.7	5.7	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	0.7	5.5	0.7	5.5	0.7	5.5	0.7	5.5	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.6	27.6	1.3	11.4	1	8.1	0.9	6	ns
t_{PZL}											

Switching Characteristics

T_A = −55°C to 125°C, V_{CCA} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B		25.4		14.3		10		8.2	ns
t_{PHL}											
t_{PLH}	B	A		11		8.8		8.5		8.3	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A		9.4		9.4		9.4		9.4	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B		32.7		13.7		12		9.7	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A		10.4		10.4		10.4		10.4	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B		31.6		19.3		12.6		10	ns
t_{PZL}											

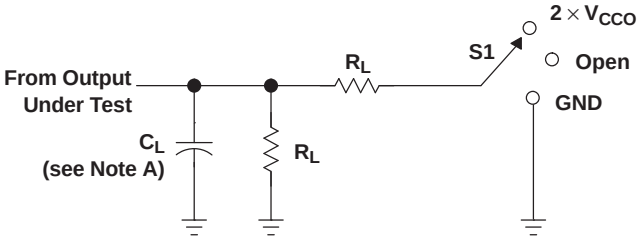
Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	V_{CCA} = V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	2	2	2	3	pF
	B-port input, A-port output		18	19	19	22	
C_{pdB} (1)	A-port input, B-port output		18	19	20	22	
	B-port input, A-port output		2	2	2	2	

(1) Power dissipation capacitance per transceiver

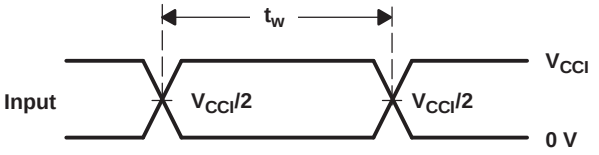
PARAMETER MEASUREMENT INFORMATION



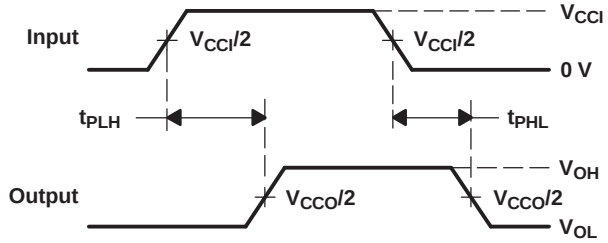
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

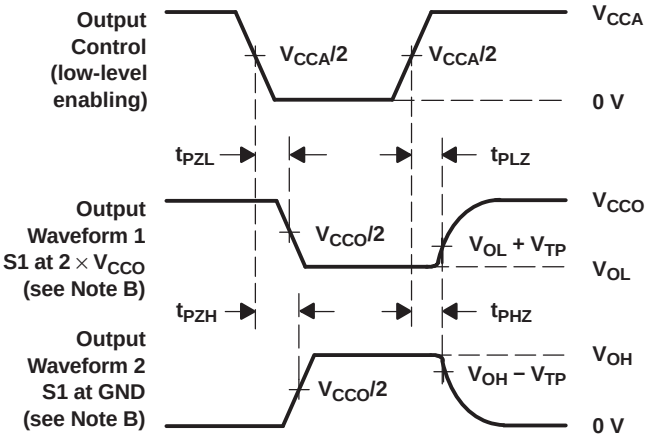
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CLVC16T245MDGGEP	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M
CLVC16T245MDGGREP	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M
V62/12667-01XE	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M
V62/12667-01XE-T	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC16T245-EP :

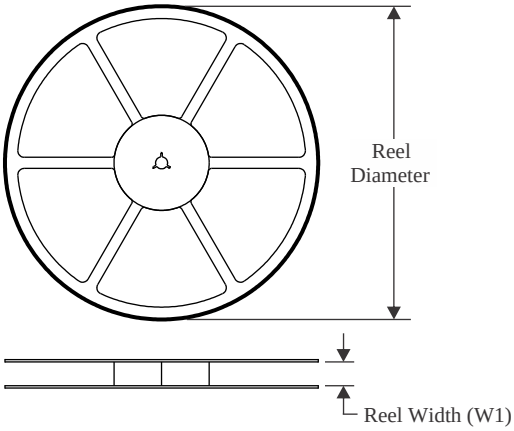
- Catalog : SN74LVC16T245

NOTE: Qualified Version Definitions:

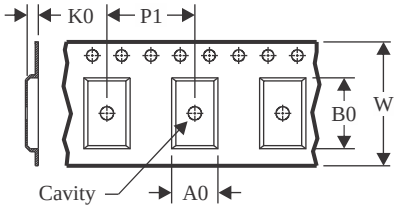
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

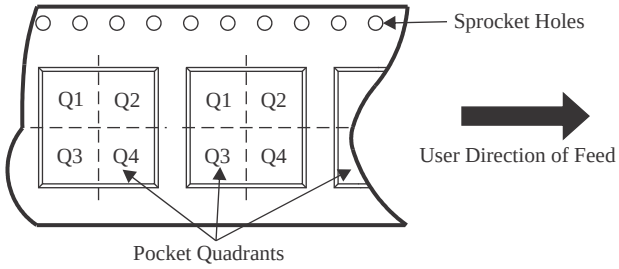


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

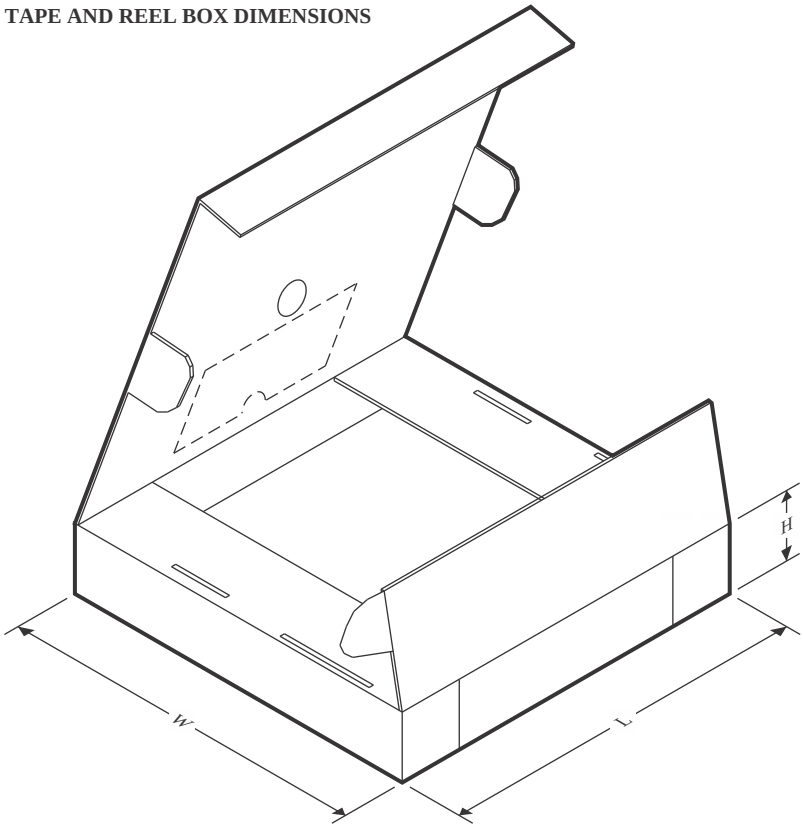
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC16T245MDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

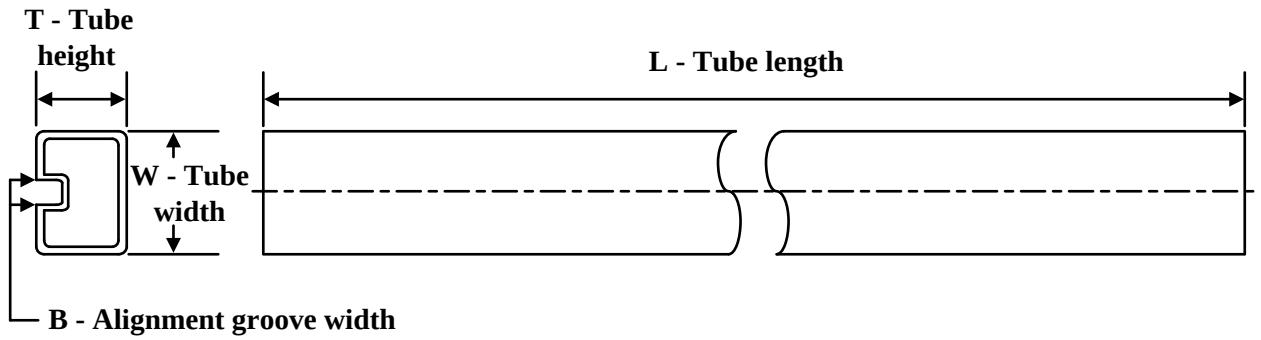
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

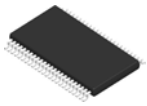
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC16T245MDGGREP	TSSOP	DGG	48	2000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CLVC16T245MDGGEP	DGG	TSSOP	48	40	530	11.89	3600	4.9
V62/12667-01XE-T	DGG	TSSOP	48	40	530	11.89	3600	4.9

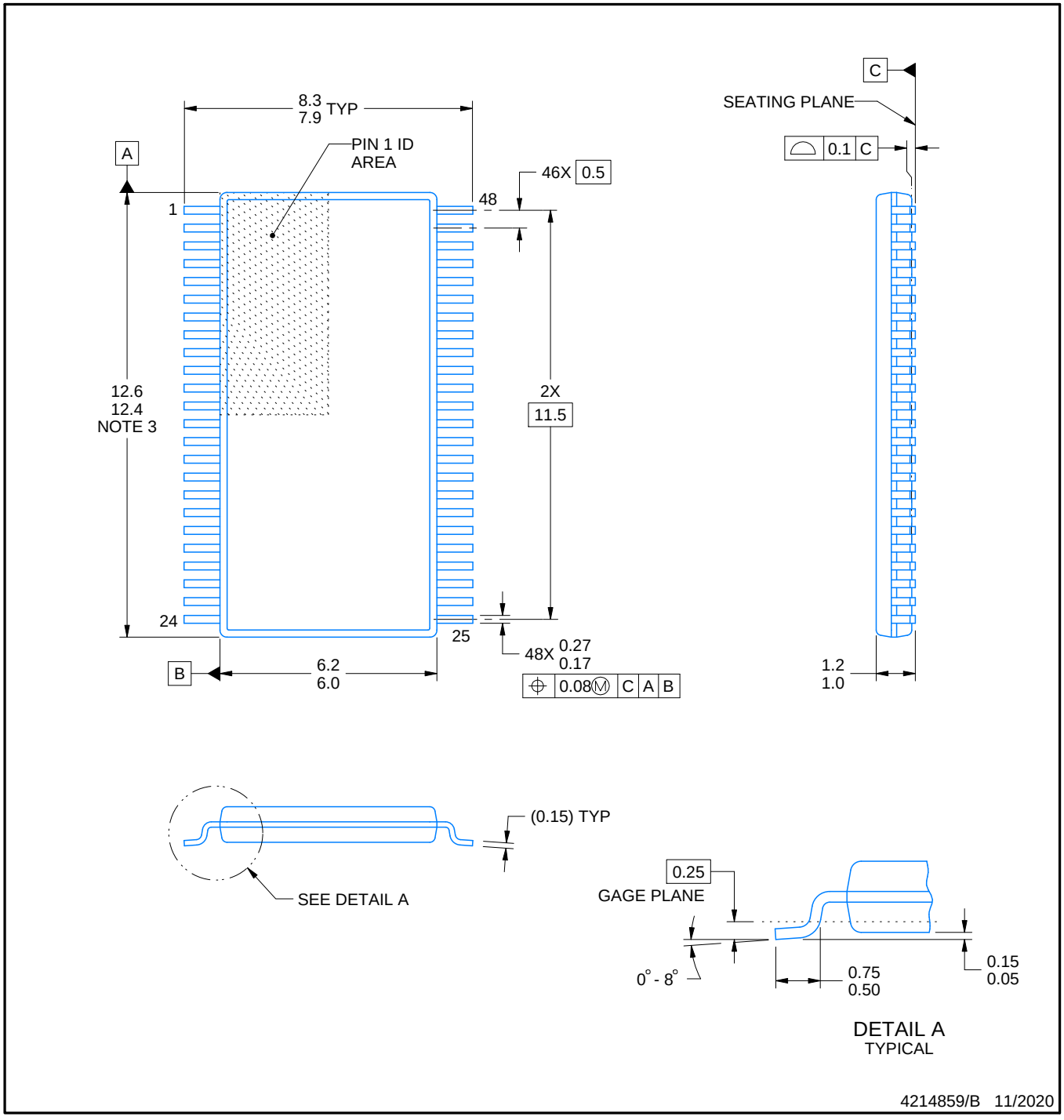


PACKAGE OUTLINE

DGG0048A

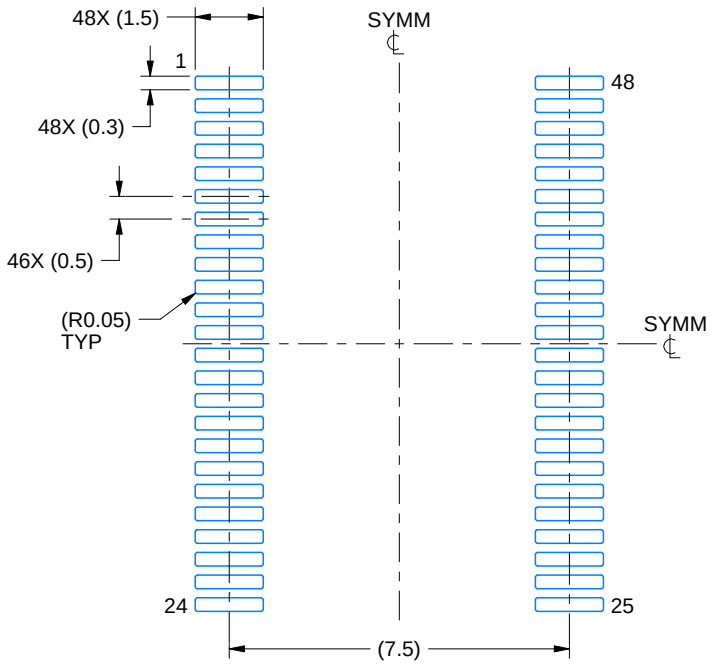
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

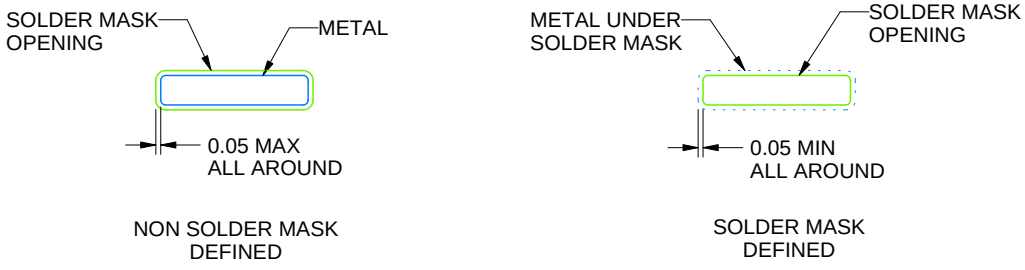


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

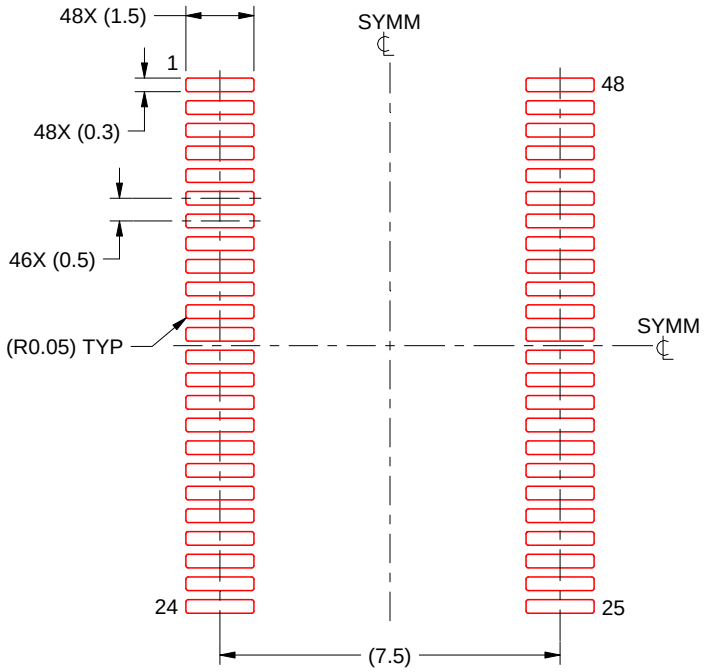


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

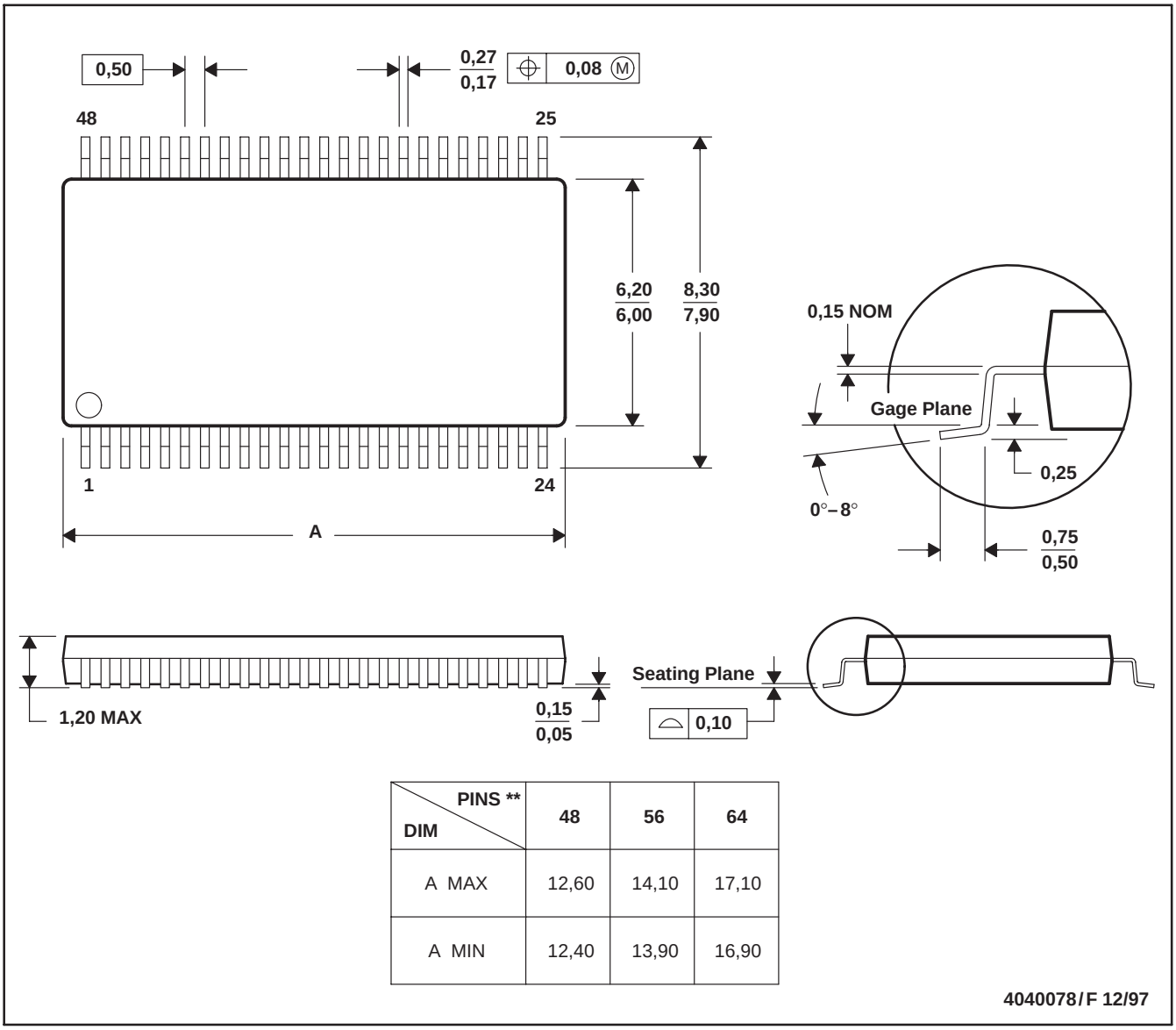
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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