# SN74LV8T245-Q1 具有三态输出和逻辑电平转换器的汽车类 1.65V 至 5V、八路总线收发器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：
    - –40°C 至 +125°C，$T_A$
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 1.8V 至 5.5V 的宽工作电压范围
- 采用具有可湿性侧面的 QFN (WRKS) 封装
- 单电源电压转换器（参阅 LVxT 增强输入电压）：
  - 上行转换：
    - 1.2V 至 1.8V
    - 1.5V 至 2.5V
    - 1.8V 至 3.3V
    - 3.3V 至 5.0V
  - 下行转换：
    - 5.0V、3.3V、2.5V 至 1.8V
    - 5.0V、3.3V 至 2.5V
    - 5.0 V 至 3.3 V
- 5.5V 容限输入引脚
- 支持标准引脚排列
- 速率高达 150 Mbps，具有 5V 或 3.3V $V_{CC}$
- 闩锁性能超过 250mA，符合 JESD 17 规范

## 2 应用

- 启用或禁用数字信号
- 消除缓慢或嘈杂输入信号
- 在控制器复位期间保持信号
- 对开关进行去抖

## 3 说明

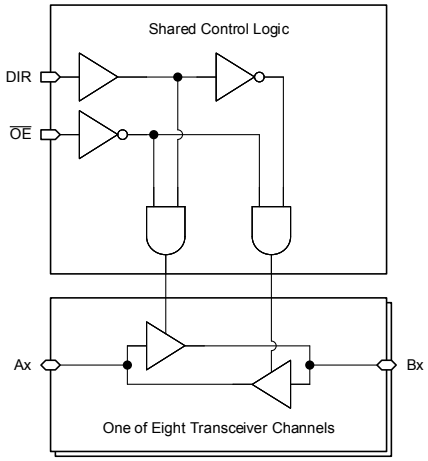
SN74LV8T245-Q1 是一款具有三态输出的八路总线收发器。所有八个通道均由方向 (DIR) 引脚和输出使能 ($\overline{OE}$) 引脚控制。输出电平以电源电压 ($V_{CC}$) 为基准，并且支持 1.8V、2.5V、3.3V 和 5V CMOS 电平。

该输入经设计，具有较低阈值电路，支持较低电压 CMOS 输入的上行转换（例如 1.2V 输入转换为 1.8V 输出或 1.8V 输入转换为 3.3V 输出）。此外，5V 容限输入引脚可实现下行转换（例如 3.3V 至 2.5V 输出）。

**封装信息**(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| SN74LV8T245-Q1 | RKS（VQFN，20） | 4.50mm × 2.50mm |
| | DGS（VSSOP，20） | 5.10mm × 3.00mm |
| | PW（TSSOP，20） | 6.50mm × 4.40mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




简化逻辑图（正逻辑）

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

# Table of Contents

**1 特性** ..... 1
**2 应用** ..... 1
**3 说明** ..... 1
**4 Revision History** ..... 2
**5 Pin Configuration and Functions** ..... 3
**6 Specifications** ..... 4
6.1 Absolute Maximum Ratings ..... 4
6.2 ESD Ratings ..... 4
6.3 Recommended Operating Conditions ..... 5
6.4 Thermal Information ..... 5
6.5 Electrical Characteristics ..... 6
6.6 Switching Characteristics - 1.8-V $V_{CC}$ ..... 6
6.7 Switching Characteristics - 2.5-V $V_{CC}$ ..... 7
6.8 Switching Characteristics - 3.3-V $V_{CC}$ ..... 7
6.9 Switching Characteristics - 5-V $V_{CC}$ ..... 7
6.10 Noise Characteristics ..... 7
6.11 Typical Characteristics ..... 8
**7 Parameter Measurement Information** ..... 10
**8 Detailed Description** ..... 11
8.1 Overview ..... 11
8.2 Functional Block Diagram ..... 11
8.3 Feature Description ..... 11
8.4 Device Functional Modes ..... 14
**9 Application and Implementation** ..... 15
9.1 Application Information ..... 15
9.2 Typical Application ..... 15
9.3 Design Requirements ..... 15
9.4 Application Curves ..... 17
**10 Power Supply Recommendations** ..... 17
**11 Layout** ..... 18
11.1 Layout Guidelines ..... 18
11.2 Layout Example ..... 18
**12 Device and Documentation Support** ..... 19
12.1 Documentation Support ..... 19
12.2 接收文档更新通知 ..... 19
12.3 支持资源 ..... 19
12.4 Trademarks ..... 19
12.5 静电放电警告 ..... 19
12.6 术语表 ..... 19
**13 Mechanical, Packaging, and Orderable Information** ..... 19

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision * (December 2022) to Revision A (April 2023) | Page |
|---|---|
| • 将数据表的状态从*预告信息*更改为*量产数据* | 1 |


Copyright © 2023 Texas Instruments Incorporated

# 5 Pin Configuration and Functions

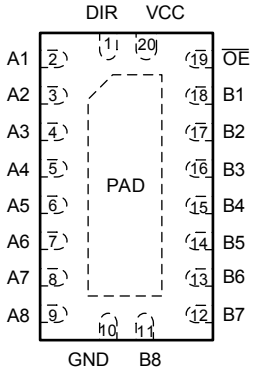



图 5-1. RKS Package, 20-Pin VQFN (Transparent Top View)

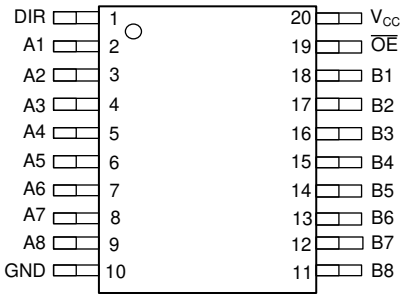



图 5-2. DGS or PW Package, 20-Pin VSSOP or TSSOP (Top View)

表 5-1. Pin Functions

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DIR | 1 | I | Direction control input (L = B → A, H = A → B) |
| A1 | 2 | I/O | Channel 1 output/input A |
| A2 | 3 | I/O | Channel 2 output/input A |
| A3 | 4 | I/O | Channel 3 output/input A |
| A4 | 5 | I/O | Channel 4 output/input A |
| A5 | 6 | I/O | Channel 5 output/input A |
| A6 | 7 | I/O | Channel 6 output/input A |
| A7 | 8 | I/O | Channel 7 output/input A |
| A8 | 9 | I/O | Channel 8 output/input A |
| GND | 10 | G | Ground |
| B8 | 11 | I/O | Channel 8 input/output B |
| B7 | 12 | I/O | Channel 7 input/output B |
| B6 | 13 | I/O | Channel 6 input/output B |
| B5 | 14 | I/O | Channel 5 input/output B |
| B4 | 15 | I/O | Channel 4 input/output B |
| B3 | 16 | I/O | Channel 3 input/output B |
| B2 | 17 | I/O | Channel 2 input/output B |
| B1 | 18 | I/O | Channel 1 input/output B |
| $\overline{OE}$ | 19 | I | Output enable, active low |
| $V_{CC}$ | 20 | P | Positive supply |
| Thermal Pad[2] | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply. |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power
(2) RKS package only

Copyright © 2023 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | -0.5 | 7 | V |
| $V_O$ | Output voltage range(2) | | -0.5 | $V_{CC}$ + 0.5 | V |
| | Voltage range applied to any output in the high-impedance or power-off state(2) | | -0.5 | 4.6 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < -0.5 V | | -20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < -0.5 V or $V_O$ > $V_{CC}$ + 0.5 V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous output current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1) | ±4000 | V |
| | | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B | ±2000 | |

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.


Copyright © 2023 Texas Instruments Incorporated

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| Spec | Description | Condition | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.6 | 5.5 | V |
| $V_I$ | Input Voltage | | 0 | 5.5 | V |
| $V_O$ | Output Voltage | | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 2 V | 1.1 | | V |
| | | $V_{CC}$ = 2.25 V to 2.75 V | 1.28 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 1.45 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 2 | | |
| $V_{IL}$ | Low-Level input voltage | $V_{CC}$ = 1.65 V to 2 V | | 0.51 | V |
| | | $V_{CC}$ = 2.25 V to 2.75 V | | 0.65 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.75 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 0.80 | |
| $I_O$ | Output Current | $V_{CC}$ = 1.65 V to 2.0 V | | ±3 | mA |
| | | $V_{CC}$ = 2.25 V to 2.75 V | | ±7 | |
| | | $V_{CC}$ = 3.3 V to 5.0 V | | ±15 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 1.6 V to 5.5 V | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND for proper device operation. Refer to the TI application report, Implications of Slow or FLoating CMOS Inputs.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74LV8T245-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | RKS (VQFN) | DGS (VSSOP) | PW (TSSOP) | |
| | | 20 PINS | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 67.7 | 118.4 | 122.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 72.4 | 57.7 | 64.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 40.4 | 73.1 | 73.3 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 10.3 | 5.7 | 19.0 | °C/W |
| $Y_{JB}$ | Junction-to-board characterization parameter | 40.4 | 72.7 | 73.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 24.1 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Copyright © 2023 Texas Instruments Incorporated

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = -50 µA | 1.65 V to 5.5 V | $V_{CC}$-0.1 | | | $V_{CC}$-0.1 | | | V |
| | $I_{OH}$ = -2 mA | 1.65 V | 1.28 | 1.6(1) | | 1.21 | | | |
| | $I_{OH}$ = -3 mA | 2.25 V | 2 | 2.3(1) | | 1.93 | | | |
| | $I_{OH}$ = -5.5 mA | 3.0 V | 2.6 | 3.08(1) | | 2.49 | | | |
| | $I_{OH}$ = -8 mA | 4.5 V | 4.1 | 4.65(1) | | 3.95 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 1.65 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 1.65 V | | 0.15(1) | 0.2 | | | 0.25 | |
| | $I_{OL}$ = 3 mA | 2.25 V | | 0.15(1) | 0.17 | | | 0.2 | |
| | $I_{OL}$ = 5.5 mA | 3.0 V | | 0.20(1) | 0.23 | | | 0.25 | |
| | $I_{OH}$ = 8 mA | 4.5 V | | 0.30(1) | 0.3 | | | 0.35 | |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 1.65 V to 5.5 V | | | 1 | | | 10 | µA |
| $\Delta I_{CC}$ | One input at 0.3 V or 3.4 V, other inputs at $V_{CC}$ or GND | 5.5 V | | | 1.35 | | | 1.5 | mA |
| | One input at 0.3 V or 1.1 V, other inputs at $V_{CC}$ or GND | 1.8 V | | | 20 | | | 20 | µA |
| $I_I$ | $V_I$ = 0 V to $V_{CC}$ | $V_I$ = 0 V to $V_{CC}$ | | | ±0.1 | | | ±1 | µA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | | ±2.5 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 2 | 10 | | 2 | 10 | pF |
| $C_O$ | Vo = $V_{CC}$ or GND | 3.3 V | | 5 | | | 5 | | pF |
| $C_{PD}$ (2) (3) | CL = 50 pF, F = 10 MHz | 1.65 V to 5.5 V | | 16 | | | | | pF |

(1) Typical value at nearest nominal voltage (1.8 V; 2.5 V; 3.3 V; 5 V)
(2) $C_{PD}$ is used to determine the dynamic power consumption, per channel
(3) $P_D = V_{CC}{}^2 x F_I x (C_{PD} + C_L)$ where $F_I$= input frequency, $C_L$= output load capacitance, $V_{CC}$= supply voltage

## 6.6 Switching Characteristics - 1.8-V $V_{CC}$

over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{Pd}$ | A or B | B or A | $C_L$ = 15 pF | | 11.8 | 22 | 1 | | 25.1 | nS |
| $t_{en}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 16.4 | 27.2 | 1 | | 32.6 | nS |
| $t_{dis}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 16.4 | 24.8 | 1 | | 30 | nS |
| $t_{Pd}$ | A or B | B or A | $C_L$ = 50 pF | | 15.6 | 27 | 1 | | 31 | nS |
| $t_{en}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 19.5 | 30.9 | 1 | | 38 | nS |
| $t_{dis}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 24.1 | 31.4 | 1 | | 36.6 | nS |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 2.5 | | | 2.5 | nS |


Copyright © 2023 Texas Instruments Incorporated

## 6.7 Switching Characteristics - 2.5-V $V_{CC}$

over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{Pd}$ | A or B | B or A | $C_L$ = 15 pF | | 8.8 | 13.5 | 1 | | 17.5 | nS |
| $t_{en}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 12.3 | 20.4 | 1 | | 24.5 | nS |
| $t_{dis}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 12.3 | 18.6 | 1 | | 22.5 | nS |
| $t_{Pd}$ | A or B | B or A | $C_L$ = 50 pF | | 11.7 | 16.4 | 1 | | 21.5 | nS |
| $t_{en}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 14.6 | 23.2 | 1 | | 28.5 | nS |
| $t_{dis}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 18.1 | 23.6 | 1 | | 27.5 | nS |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 2 | | | 2 | nS |

## 6.8 Switching Characteristics - 3.3-V $V_{CC}$

over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{Pd}$ | A or B | B or A | $C_L$ = 15 pF | | 6.4 | 8.9 | 1 | | 11.5 | nS |
| $t_{en}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 9 | 13.7 | 1 | | 17 | nS |
| $t_{dis}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 10.1 | 17 | 1 | | 21 | nS |
| $t_{Pd}$ | A or B | B or A | $C_L$ = 50 pF | | 8.8 | 12.4 | 1 | | 15 | nS |
| $t_{en}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 11.5 | 17.2 | 1 | | 20.5 | nS |
| $t_{dis}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 14.4 | 20.3 | 1 | | 23.5 | nS |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1.5 | | | 1.5 | nS |

## 6.9 Switching Characteristics - 5-V $V_{CC}$

over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{Pd}$ | A or B | B or A | $C_L$ = 15 pF | | 4.5 | 7.7 | 1 | | 10 | nS |
| $t_{en}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 8.9 | 13.8 | 1 | | 16 | nS |
| $t_{dis}$ | $\overline{OE}$ | A or B | $C_L$ = 15 pF | | 9.2 | 14.4 | 1 | | 16.5 | nS |
| $t_{Pd}$ | A or B | B or A | $C_L$ = 50 pF | | 5.3 | 8.7 | 1 | | 11 | nS |
| $t_{en}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 9.7 | 14.8 | 1 | | 17 | nS |
| $t_{dis}$ | $\overline{OE}$ | A or B | $C_L$ = 50 pF | | 10 | 15.4 | 1 | | 17.5 | nS |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1 | | | 1 | nS |

## 6.10 Noise Characteristics

$V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C(1)

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 1 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | -0.6 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

(1) Characteristics are for surface-mount packages only

Copyright © 2023 Texas Instruments Incorporated

## 6.11 Typical Characteristics

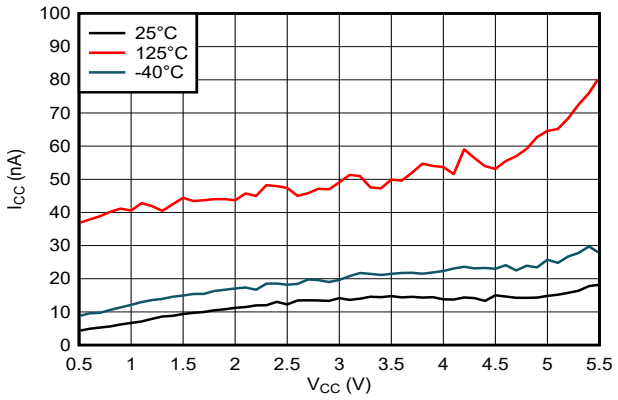



图 6-1. Supply Current Across Operating Voltage

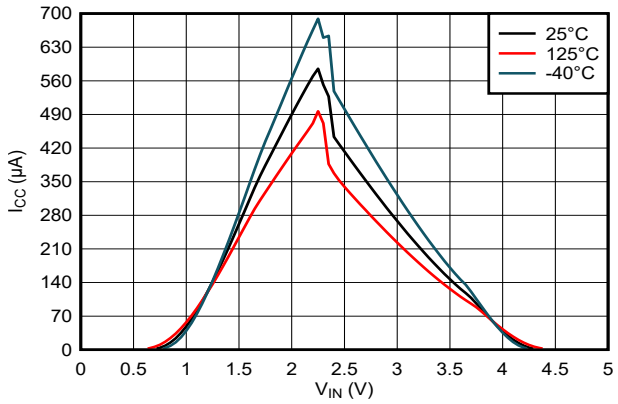



图 6-2. Supply Current Across Input Voltage, 5-V Supply

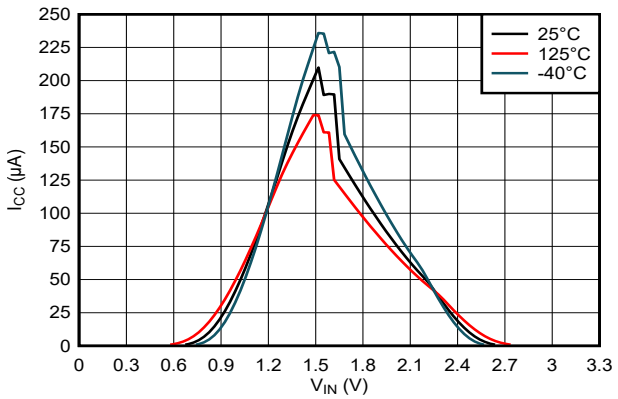



图 6-3. Supply Current Across Input Voltage, 3.3-V Supply

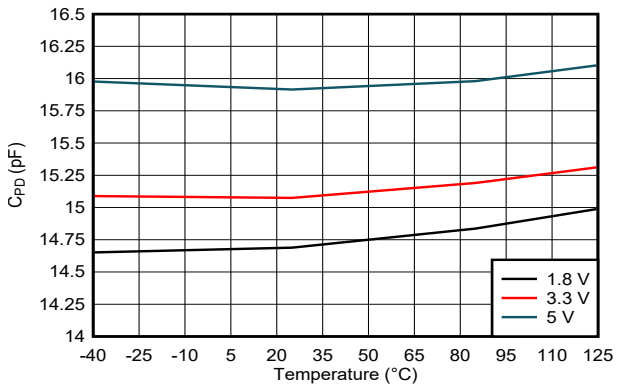



图 6-4. Power Dissipation Capacitance per Gate Across Temperature, 1.8-V, 3.3-V, and 5-V Supply

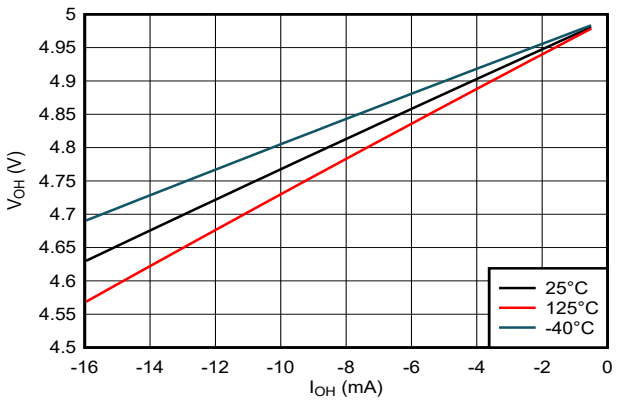



图 6-5. Output Voltage vs Current in HIGH State; 5-V Supply

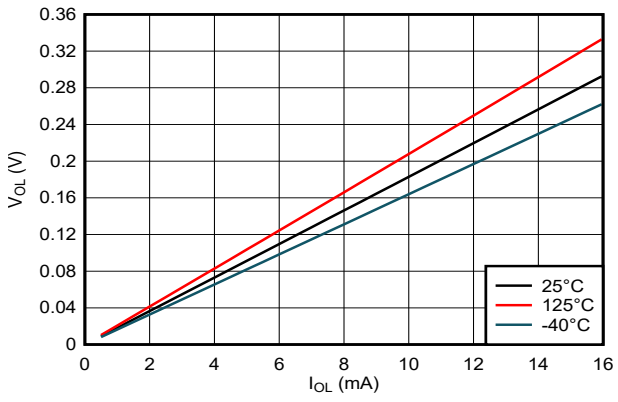



图 6-6. Output Voltage vs Current in LOW State; 5-V Supply


Copyright © 2023 Texas Instruments Incorporated

## 6.11 Typical Characteristics (continued)

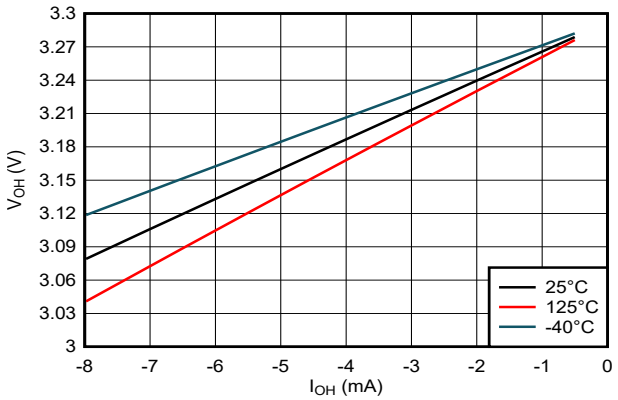



图 6-7. Output Voltage vs Current in HIGH State; 3.3-V Supply

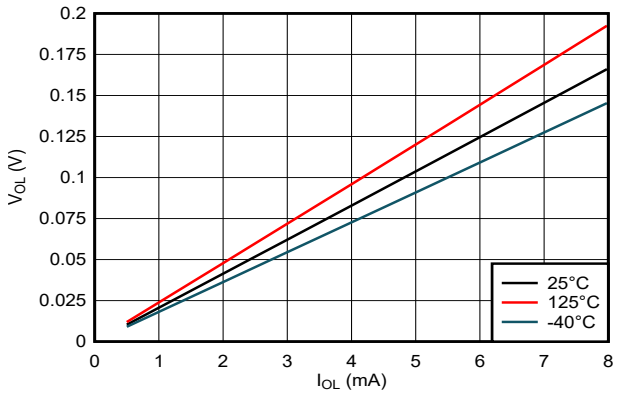



图 6-8. Output Voltage vs Current in LOW State; 3.3-V Supply

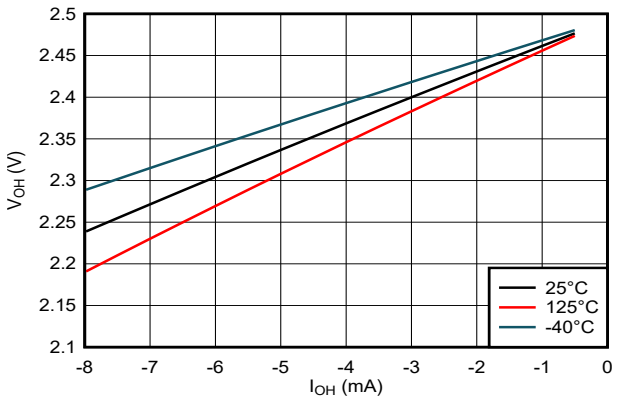



图 6-9. Output Voltage vs Current in HIGH State; 2.5-V Supply

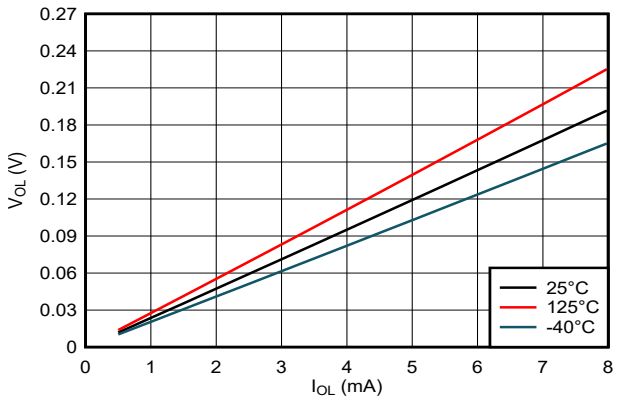



图 6-10. Output Voltage vs Current in LOW State; 2.5-V Supply

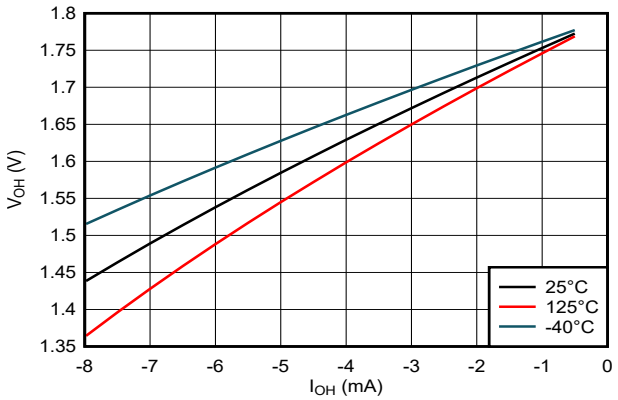



图 6-11. Output Voltage vs Current in HIGH State; 1.8-V Supply

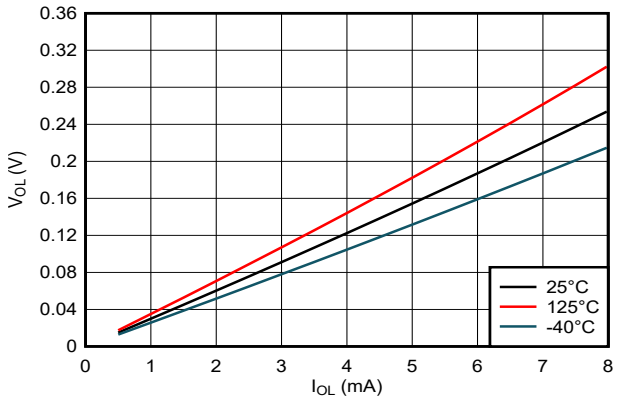



图 6-12. Output Voltage vs Current in LOW State; 1.8-V Supply

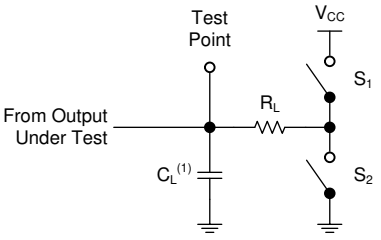
Copyright © 2023 Texas Instruments Incorporated

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω.

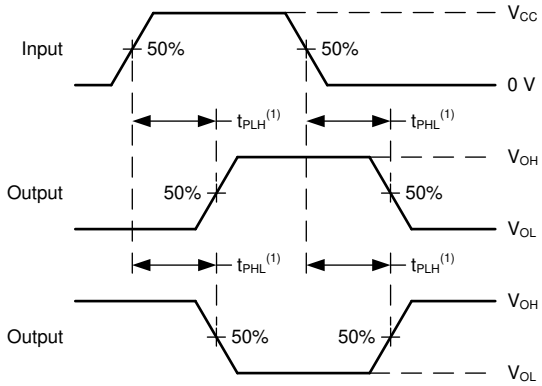
For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



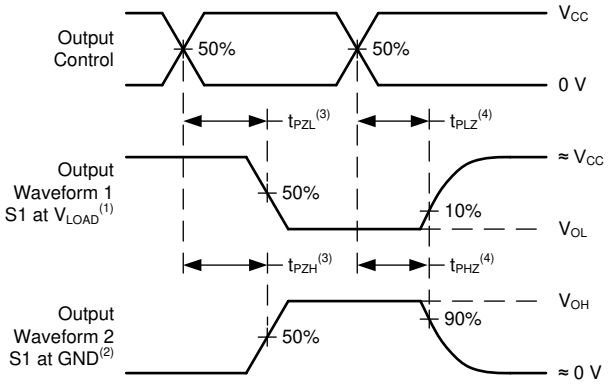

(1) $C_L$ includes probe and test-fixture capacitance.

**图 7-1. Load Circuit for 3-State Outputs**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**图 7-2. Voltage Waveforms Propagation Delays**



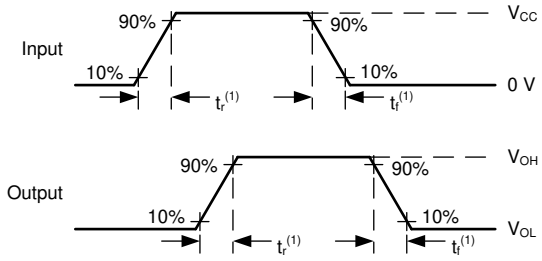

(1) S1 = CLOSED, S2 = OPEN.

(2) S1 = OPEN, S2 = CLOSED.

(3) The greater between $t_{PZL}$ and $t_{PZH}$ is the same as $t_{en}$.

(4) The greater between $t_{PLZ}$ and $t_{PHZ}$ is the same as $t_{dis}$.

**图 7-3. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

**图 7-4. Voltage Waveforms, Input and Output Transition Times**


Copyright © 2023 Texas Instruments Incorporated

# 8 Detailed Description

## 8.1 Overview

The SN74LV8T245-Q1 is an octal bus transceiver with 3-state outputs. All eight channels are controlled by the direction (DIR) pin and output enable ($\overline{OE}$) pin. Each transceiver includes one buffer oriented from Ax to Bx and one from Bx to Ax, with at least one output disabled at all times. The direction (DIR) pin controls which buffer is active. The buffer that is not active has the output placed into the high-impedance state.

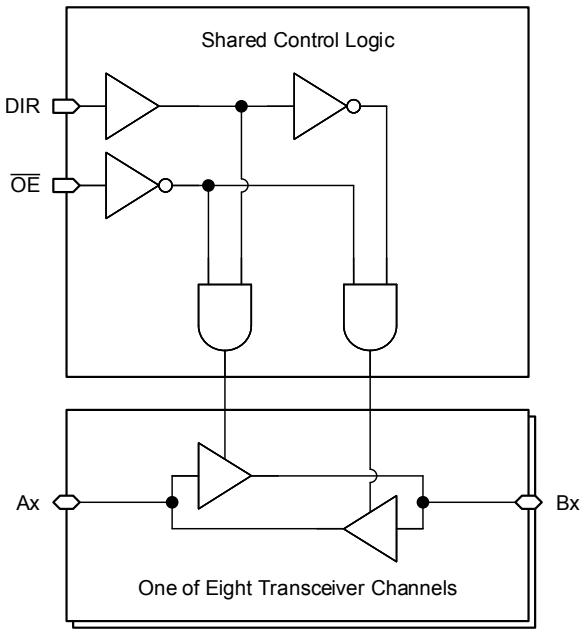
The output enable ($\overline{OE}$) controls all outputs in the device. When the $\overline{OE}$ pin is in the low state, the appropriate outputs as determined by the direction (DIR) pin are enabled. When the $\overline{OE}$ pin is in the high state, all outputs of the device are disabled. All disabled outputs are placed into the high-impedance state.

To ensure the high-impedance state during power up or power down, the $\overline{OE}$ pin should be tied to $V_{CC}$ through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table. Typically a 10-kΩ resistor will be sufficient.

The output level is referenced to the supply voltage ($V_{CC}$) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

The input is designed with a lower threshold circuit to support up translation for lower voltage CMOS inputs (for example 1.2 V input to 1.8 V output or 1.8 V input to 3.3 V output). Additionally, the 5-V tolerant input pins enable down translation (for example 3.3 V to 2.5 V output).

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Copyright © 2023 Texas Instruments Incorporated

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

### 8.3.2 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as depicted in 图 8-1.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

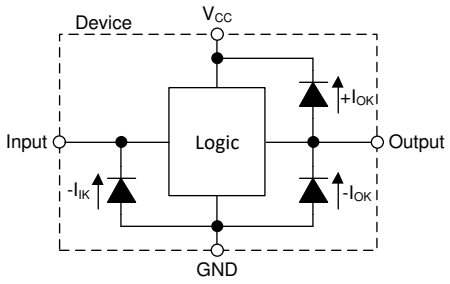



**图 8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.3.3 LVxT Enhanced Input Voltage

The SN74LV8T245-Q1 belongs to TIs LVxT family of Logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage ($V_{CC}$), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. 图 8-2 shows the typical $V_{IH}$ and $V_{IL}$ levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at $V_{CC}$ or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10-kΩ resistor, however, is recommended and will typically meet all requirements.


Copyright © 2023 Texas Instruments Incorporated

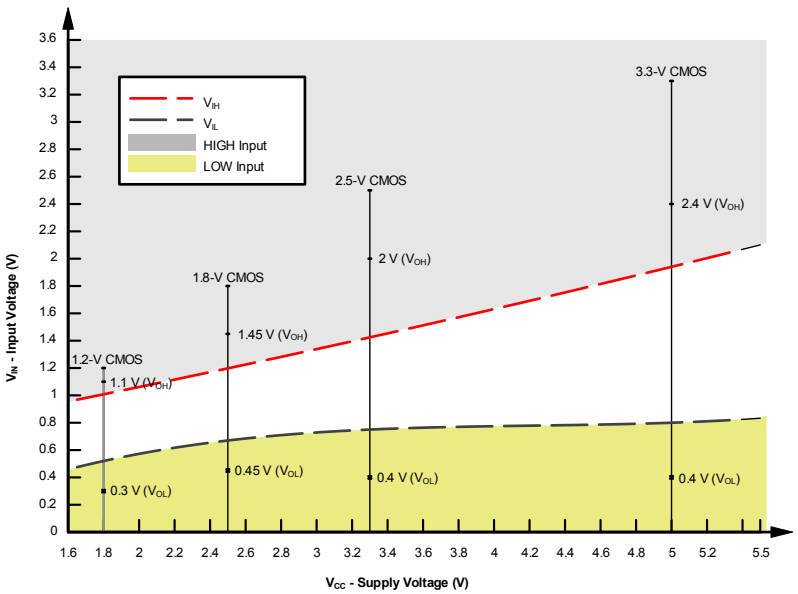



**图 8-2. LVxT Input Voltage Levels**

### *8.3.3.1 Down Translation*

Signals can be translated down using the SN74LV8T245-Q1. The voltage applied at the $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0 V in the LOW state. Ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in 图 8-2.

For example, standard CMOS inputs for devices operating at 5.0 V, 3.3 V, or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V $V_{CC}$. See 图 8-3.

*Down Translation Combinations*:

- 1.8-V $V_{CC}$ – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V $V_{CC}$ – Inputs from 3.3 V and 5.0 V
- 3.3-V $V_{CC}$ – Inputs from 5.0 V

### *8.3.3.2 Up Translation*

Input signals can be up translated using the SN74LV8T245-Q1. The voltage applied at $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input high-state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN74LV8T245-Q1, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from typical 2.5-V to 5-V signals.

Ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in 图 8-3.

*Up Translation Combinations*:

- 1.8-V $V_{CC}$ – Inputs from 1.2 V
- 2.5-V $V_{CC}$ – Inputs from 1.8 V
- 3.3-V $V_{CC}$ – Inputs from 1.8 V and 2.5 V

Copyright © 2023 Texas Instruments Incorporated

- 5.0-V $V_{CC}$ – Inputs from 2.5 V and 3.3 V

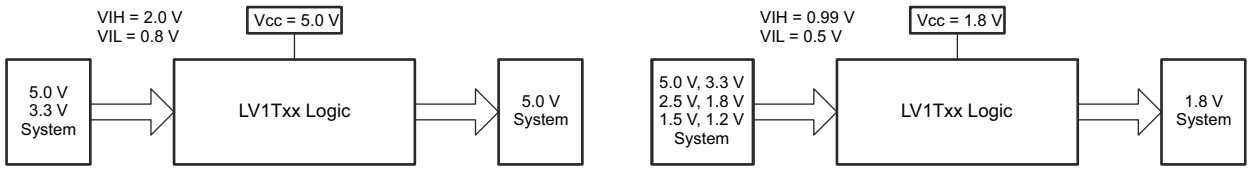



**图 8-3. LVxT Up and Down Translation Example**

### 8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

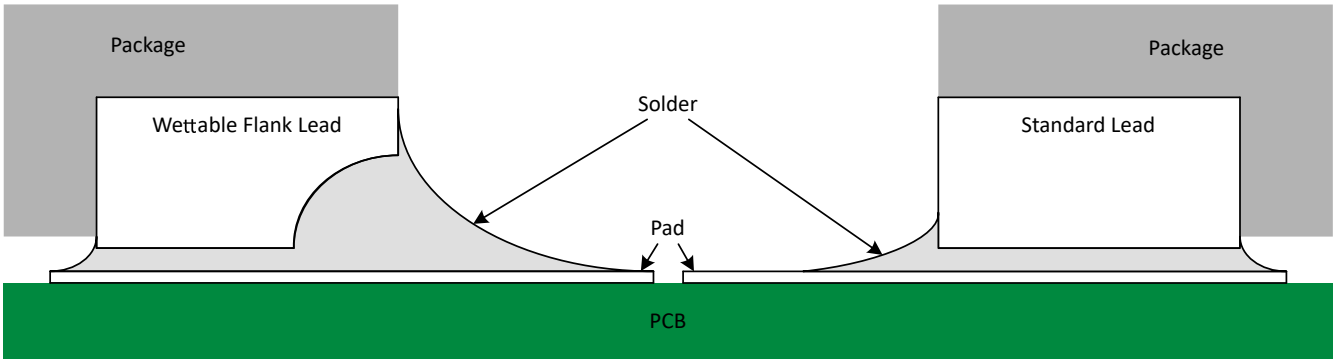



**图 8-4. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering**

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in 图 8-4, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

## 8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74LV8T245-Q1.

**表 8-1. Function Table**

| INPUTS(1) | | OUTPUTS(2) | |
|---|---|---|---|
| $\overline{OE}$ | DIR | A | B |
| L | L | B | Z |
| L | H | Z | A |
| H | X | Z | Z |

(1) H = High voltage level, L = Low voltage level, X = Do not care
(2) A = Logic value at 'A' input, B = Logic value at 'B' input, Z = High impedance


Copyright © 2023 Texas Instruments Incorporated

# 9 Application and Implementation

**备注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LV8T245-Q1 can be used to drive signals over relatively long traces or transmission lines. To reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver, a series damping resistor placed in series with the transmitter’s output can be used. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

## 9.2 Typical Application

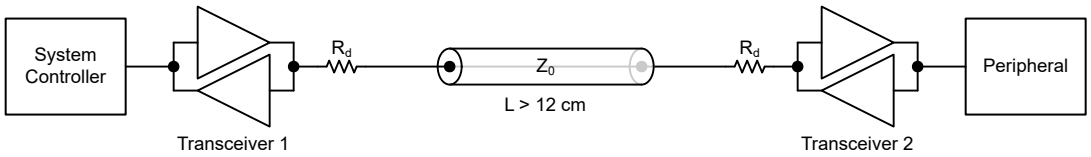



**图 9-1. Application Block Diagram**

## 9.3 Design Requirements

### 9.3.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV8T245-Q1 plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

Copyright © 2023 Texas Instruments Incorporated

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV8T245-Q1 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV8T245-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV8T245-Q1 can drive a load with total resistance described by $R_L \geqslant V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.3.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74LV8T245-Q1, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74LV8T245-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 9.3.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.


Copyright © 2023 Texas Instruments Incorporated

### 9.3.4 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ⩽ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV8T245-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

## 9.4 Application Curves

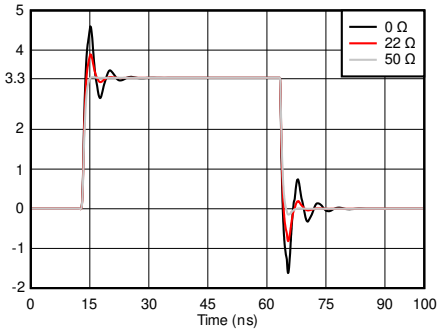



**图 9-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor ($R_d$) Values**

# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

Copyright © 2023 Texas Instruments Incorporated

# 11 Layout

## 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

## 11.2 Layout Example

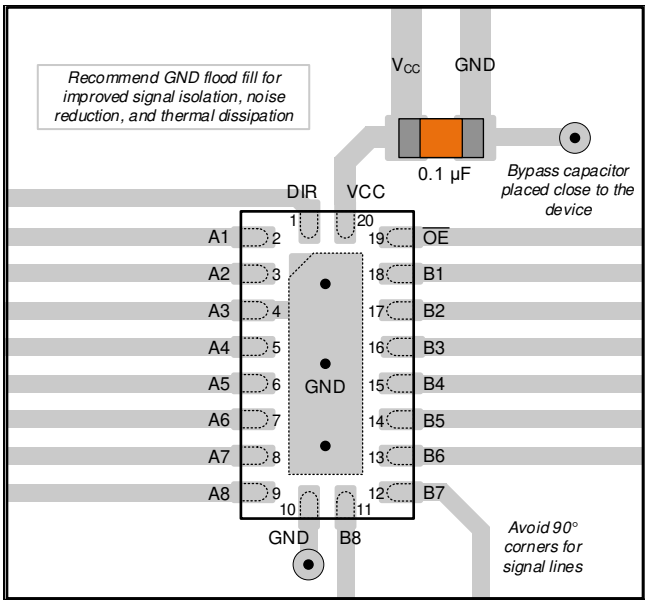



**图 11-1. Example Layout for the SN74LV8T245-Q1 in RKS**


Copyright © 2023 Texas Instruments Incorporated

# 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application report
- Texas Instruments, *Designing With Logic* application report

## 12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 12.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 74LV8T245QWRKSRQ1 | Active | Production | VQFN (RKS) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV8245Q |
| 74LV8T245QWRKSRQ1.A | Active | Production | VQFN (RKS) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV8245Q |
| SN74LV8T245QDGSRQ1 | Active | Production | VSSOP (DGS) \| 20 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 8245Q |
| SN74LV8T245QDGSRQ1.A | Active | Production | VSSOP (DGS) \| 20 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 8245Q |
| SN74LV8T245QDGSRQ1.B | Active | Production | VSSOP (DGS) \| 20 | 5000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| SN74LV8T245QPWRQ1 | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV8T245Q |
| SN74LV8T245QPWRQ1.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV8T245Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV8T245-Q1 :**

- Catalog : SN74LV8T245

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

# 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月