

SN74LV4040A 12 位异步二进制计数器

1 特性

- 2V 至 5.5V V_{CC} 运行
- V_{OLP} (输出接地反弹) 典型值小于 0.8V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ 时)
- V_{OHV} (输出 V_{OH} 下冲) 典型值为 2.3V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ 时)
- 所有端口上均支持混合模式电压运行
- 高开关输出电压比
- 低开关间串扰
- 单独的开关控制
- 极低输入电流
- I_{off} 支持局部省电模式运行
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范的要求

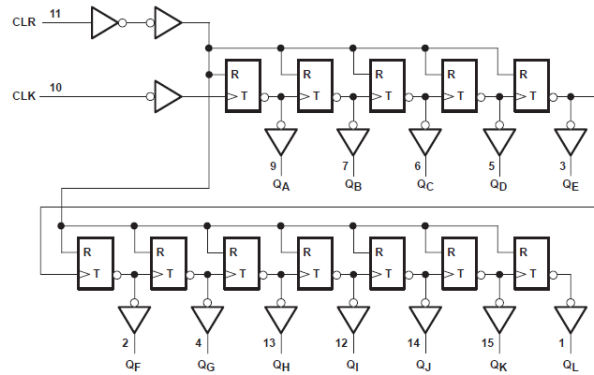
2 说明

’ LV4040A 器件是 12 位异步二进制计数器, 可从外部获得所有级的输出。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SN74LV4040A	N (PDIP, 16)	19.3mm x 9.4mm	19.3mm x 6.35mm
	D (SOIC, 16)	9.9mm x 6mm	9.9mm x 3.9mm
	NS (SOP, 16)	10.2mm x 7.8mm	10.2mm x 5.3mm
	DB (SSOP, 16)	6.2mm x 7.8mm	6.2mm x 5.3mm
	PW (TSSOP, 16)	5mm x 6.4mm	5mm x 4.4mm
	DGV (TVSOP, 16)	3.6mm x 6.4mm	3.6mm x 4.4mm
	RGY (VQFN, 16)	4mm x 3.5mm	4mm x 3.5mm

- (1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。
- (2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。
- (3) 本体尺寸 (长 × 宽) 为标称值, 不包括引脚。



逻辑图 (正逻辑)



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3 Pin Configuration and Functions



图 3-1. SN74LV4040A D, DB, DGV, N, NS, or PW Package (Top View)

图 3-2. SN74LV4040A RGY Package (Top View)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
Q _L	1	O	Q _L output
Q _F	2	O	Q _F output
Q _E	3	O	Q _E output
Q _G	4	O	Q _G output
Q _D	5	O	Q _D output
Q _C	6	O	Q _C output
Q _B	7	O	Q _B output
GND	8	-	Ground
Q _A	9	O	Q _A output
CLK	10	I	Clock, falling edge triggered
CLR	11	I	Clear, active high
Q _I	12	O	Q _I output
Q _H	13	O	Q _H output
Q _J	14	O	Q _J output
Q _K	15	O	Q _K output
V _{CC}	16	-	Positive supply

(1) I = input, O = output

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range	-0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state	-0.5	7	V
V _O	Output voltage range	-0.5 V to V _{CC}	0.5	V
I _{IK}	Input clamp current ⁽²⁾	(V _I < 0)	-20	mA
I _{OK}	Output clamp current ⁽²⁾	(V _O < 0)	±50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ¹	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ²	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V V _{CC} = 2.3 V to 2.7 V V _{CC} = 3 V to 3.6 V V _{CC} = 4.5 V to 5.5 V	1.5 V _{CC} × 0.7 V _{CC} × 0.7 V _{CC} × 0.7	V
V _{IL}	Low-level input voltage	V _{CC} = 2 V V _{CC} = 2.3 V to 2.7 V V _{CC} = 3 V to 3.6 V V _{CC} = 4.5 V to 5.5 V	0.5 V _{CC} × 0.3 V _{CC} × 0.3 V _{CC} × 0.3	V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V V _{CC} = 2.3 V to 2.7 V V _{CC} = 3 V to 3.6 V V _{CC} = 4.5 V to 5.5 V	- 50 - 2 - 6 - 12	μA mA
I _{OL}	Low-level output current	V _{CC} = 2 V V _{CC} = 2.3 V to 2.7 V V _{CC} = 3 V to 3.6 V V _{CC} = 4.5 V to 5.5 V	50 2 6 12	

4.3 Recommended Operating Conditions (续)

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
$\Delta t / \Delta v$	Input transition rise/fall time	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		200	ns
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		100	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		20	
T_A	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

4.4 Thermal Information

THERMAL METRIC ⁽¹⁾	D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	UNIT
$R_{\theta JA}$	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	°C/W
Junction-to-ambient thermal resistance	99.5	82	120	67	64	122.3	39	

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LV4040A			UNIT
			MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} - 0.1			V
	I _{OH} = -2 mA	2.3 V	2			
	I _{OH} = -6 mA	3 V	2.48			
	I _{OH} = -12 mA	4.5 V	3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			
	I _{OL} = 6 mA	3 V	0.44			
	I _{OL} = 12 mA	4.5 V	0.55			
I _I	V _I = 5.5 V or GND	0 to 5.5 V	±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			μ A
I _{off}	V _I or V _O = 0 to 5.5 V	0	5			μ A
C _i	V _I = V _{CC} or GND	3.3 V	1.9			pF

4.6 Timing Requirements, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

			$T_A = 25^\circ\text{C}$		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	7		7		ns
		CLR high	6.5		6.5		
t_{su}	Setup time	CLR inactive before CLK ↓	6.5		6.5		

4.7 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

			$T_A = 25^\circ\text{C}$		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t_{su}	Setup time	CLR inactive before CLK ↓	5		5		

4.8 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

			$T_A = 25^\circ\text{C}$		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t_{su}	Setup time	CLR inactive before CLK ↓	5		5		

4.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) ([Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	50 ⁽¹⁾	115 ⁽¹⁾		40 ⁽¹⁾		MHz
			$C_L = 50\text{ pF}$	40	95		35		
t_{PLH}	CLK	Q_A	$C_L = 15\text{ pF}$		8.7 ⁽¹⁾	19.4 ⁽¹⁾	1 ⁽¹⁾	23 ⁽¹⁾	ns
t_{PHL}					8.7 ⁽¹⁾	19.4 ⁽¹⁾	1 ⁽¹⁾	23 ⁽¹⁾	
t_{PHL}	CLR	Any Q	$C_L = 15\text{ pF}$		9.3 ⁽¹⁾	19.9 ⁽¹⁾	1 ⁽¹⁾	24 ⁽¹⁾	
t_{PLH}	$\overline{\text{CLK}}$	Q_A	$C_L = 50\text{ pF}$		10.5	24.1	1	28	
t_{PHL}					10.5	24.1	1	28	ns
t_{PHL}	CLR	Any Q	$C_L = 50\text{ pF}$		11.7	24.5	1	28	
Δt_{pd}	Q_n	Q_{n+1}	$C_L = 50\text{ pF}$		1.7	5.9		7	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3$ (unless otherwise noted) ([Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	75 ⁽¹⁾	160 ⁽¹⁾		75		MHz
			$C_L = 50\text{ pF}$	55	130		50		
t_{PLH}	CLK	Q_A	$C_L = 15\text{ pF}$		6.1 ⁽¹⁾	11.9 ⁽¹⁾	1	14	ns
t_{PHL}					6.1 ⁽¹⁾	11.9 ⁽¹⁾	1	14	ns
t_{PHL}	CLR	Any Q	$C_L = 15\text{ pF}$		7.1 ⁽¹⁾	12.8 ⁽¹⁾	1	15	ns
t_{PLH}	$\overline{\text{CLK}}$	Q_A	$C_L = 50\text{ pF}$		7.5	15.4	1	17.5	ns
t_{PHL}					7.5	15.4	1	17.5	ns
t_{PHL}	CLR	Any Q	$C_L = 50\text{ pF}$		9	16.3	1	18.5	ns

4.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (续)

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3$ (unless otherwise noted) ([Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
Δt_{pd}	Q_n	Q_{n+1}	$C_L = 50\text{ pF}$		1.2	4.4		5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) ([Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{\max}$			$C_L = 15\text{ pF}$	150 ¹	235 ¹		125		MHz
			$C_L = 50\text{ pF}$	95	185		80		
t_{PLH}	CLK	Q_A	$C_L = 15\text{ pF}$		4.2 ¹	7.3 ¹	1	8.5	ns
t_{PHL}					4.2 ¹	7.3 ¹	1	8.5	ns
t_{PHL}	CLR	Any Q	$C_L = 15\text{ pF}$		5.3 ¹	8.6 ¹	1	10	ns
t_{PLH}	$\overline{\text{CLK}}$	Q_A	$C_L = 50\text{ pF}$		5.3	9.3	1	10.5	ns
t_{PHL}					5.3	9.3	1	10.5	ns
t_{PHL}	CLR	Any Q	$C_L = 50\text{ pF}$		6.8	10.6	1	12	ns
Δt_{pd}	Q_n	Q_{n+1}	$C_L = 50\text{ pF}$		0.8	3.1		3.5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.12 Noise Characteristics

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER ⁽¹⁾		SN74LV4040A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		– 0.5	– 0.8	V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

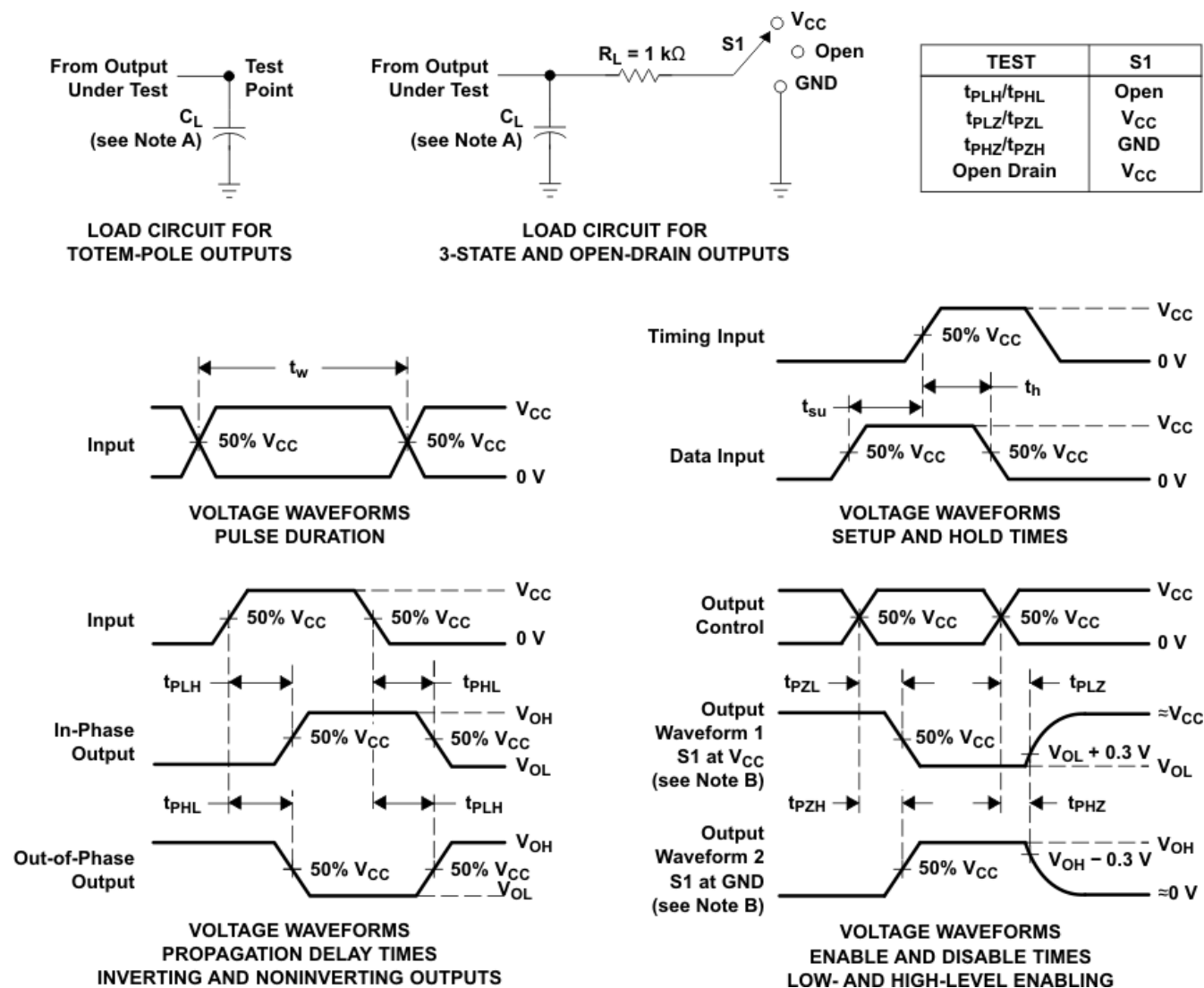
(1) Characteristics for surface-mount packages only.

4.13 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$,	$f = 10\text{ MHz}$	3.3 V	11.9	pF
				5 V	13.1	

5 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, and $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

图 5-1. Load Circuit and Voltage Waveforms

6 Detailed Description

6.1 Overview

The 'LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

6.2 Functional Block Diagram

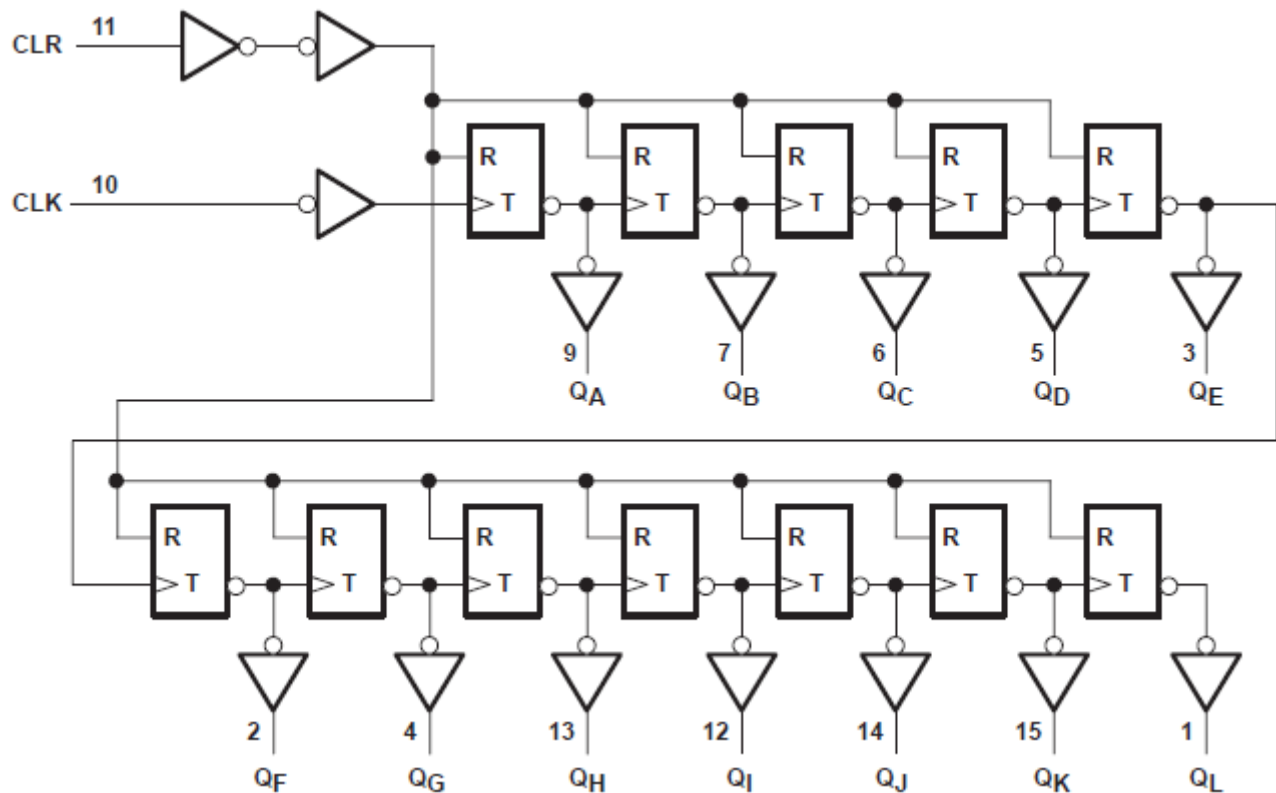


图 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

表 6-1. Function Table
(Each Buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV4040A	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision J (July 2023) to Revision K (September 2024)	Page
• 向 封装信息 表中添加了本体尺寸.....	1
• Updated <i>Pin Functions</i> table.....	3
• Added <i>Application and Implementation</i> section.....	10

Changes from Revision I (May 2005) to Revision J (July 2023)	Page
• 添加了封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• Updated thermal values for R _{θJA} : D = 73 to 99.5, PW = 108 to 122.3, all values in °C/W	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4040AD	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	LV4040A
SN74LV4040ADBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ADBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ADGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ADGVR.A	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4040A
SN74LV4040ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4040A
SN74LV4040AN	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4040AN
SN74LV4040AN.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4040AN
SN74LV4040ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4040A
SN74LV4040ANSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4040A
SN74LV4040APW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	LW040A
SN74LV4040APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040APWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040APWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040APWRG4.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040APWT	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	LW040A
SN74LV4040ARGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ARGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ARGYRG4	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A
SN74LV4040ARGYRG4.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW040A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4040A :

- Enhanced Product : [SN74LV4040A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

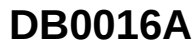
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



SSOP - 2 mm max height

[illegible]

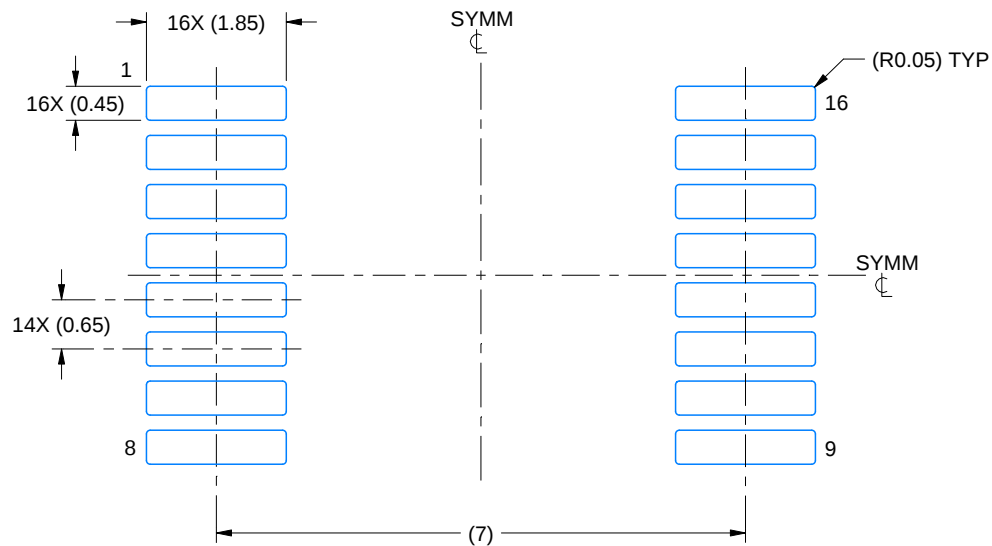
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

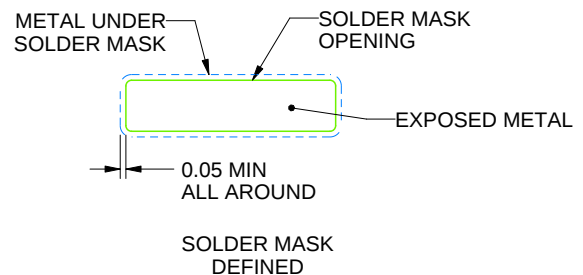
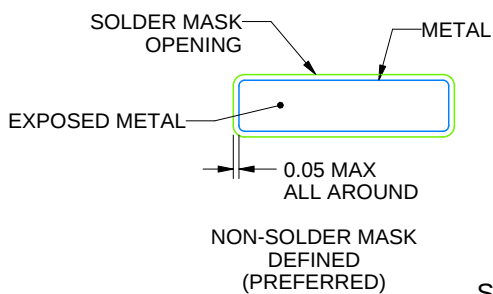
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

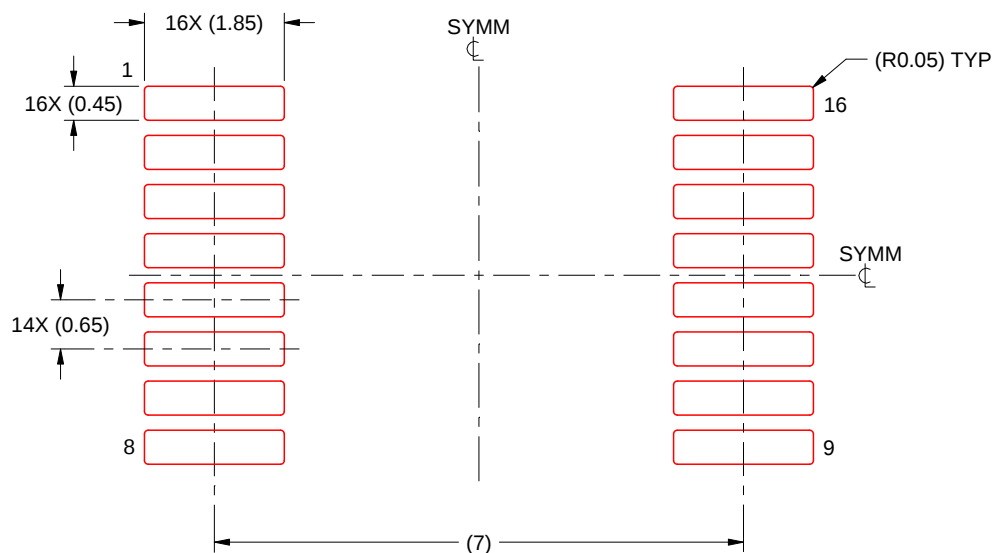
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

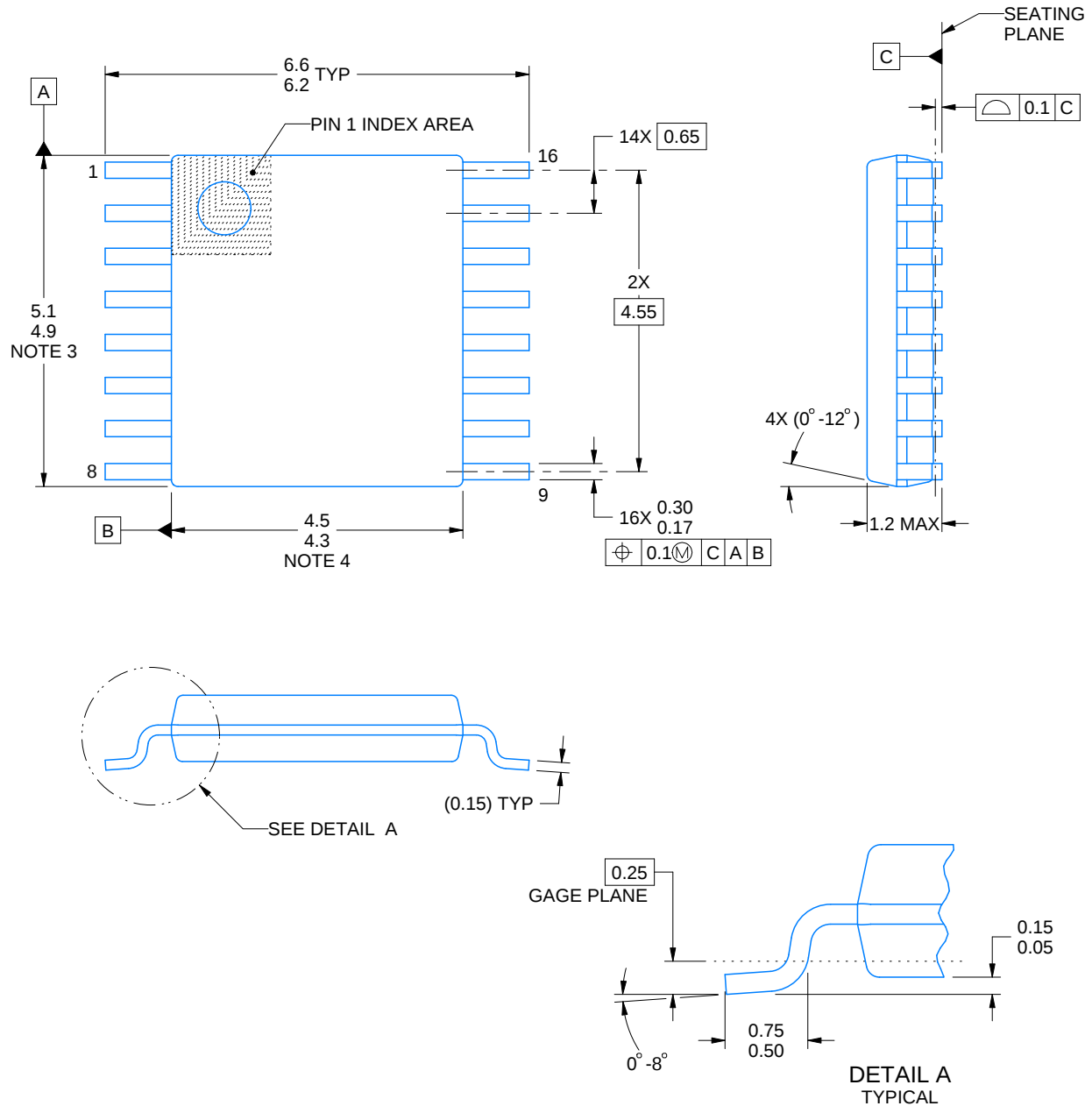
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4220204/B 12/2023

NOTES:

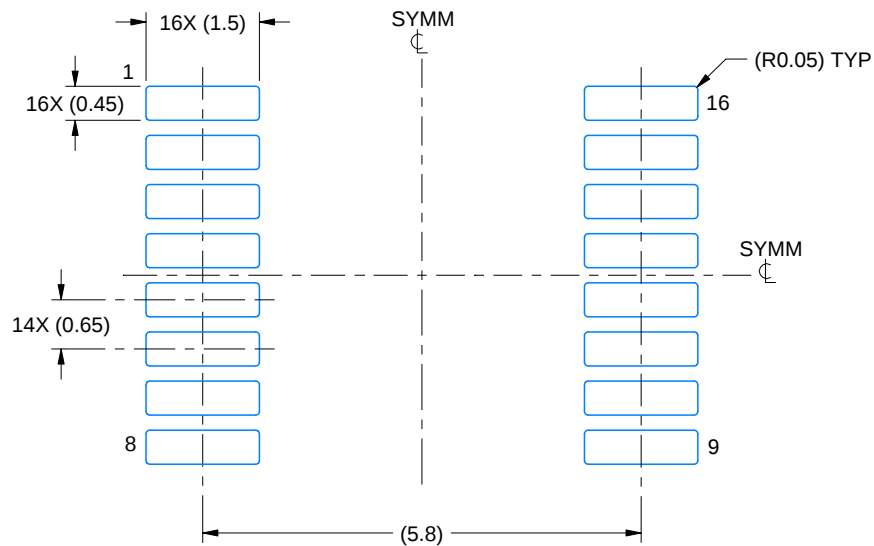
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

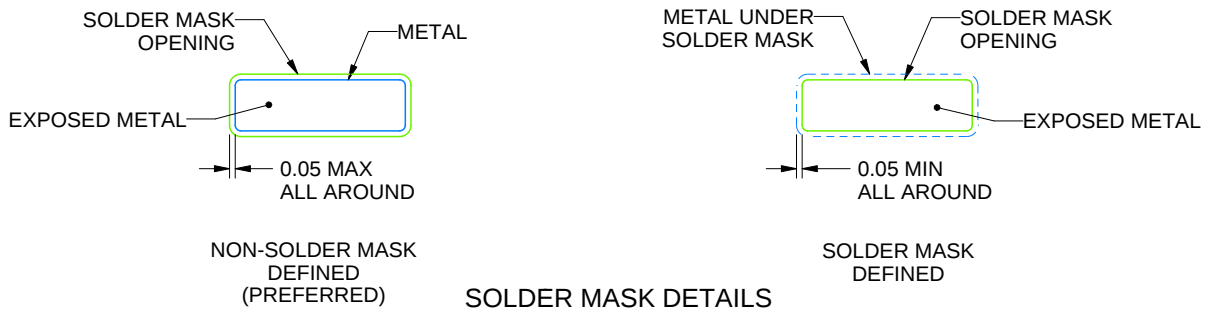
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



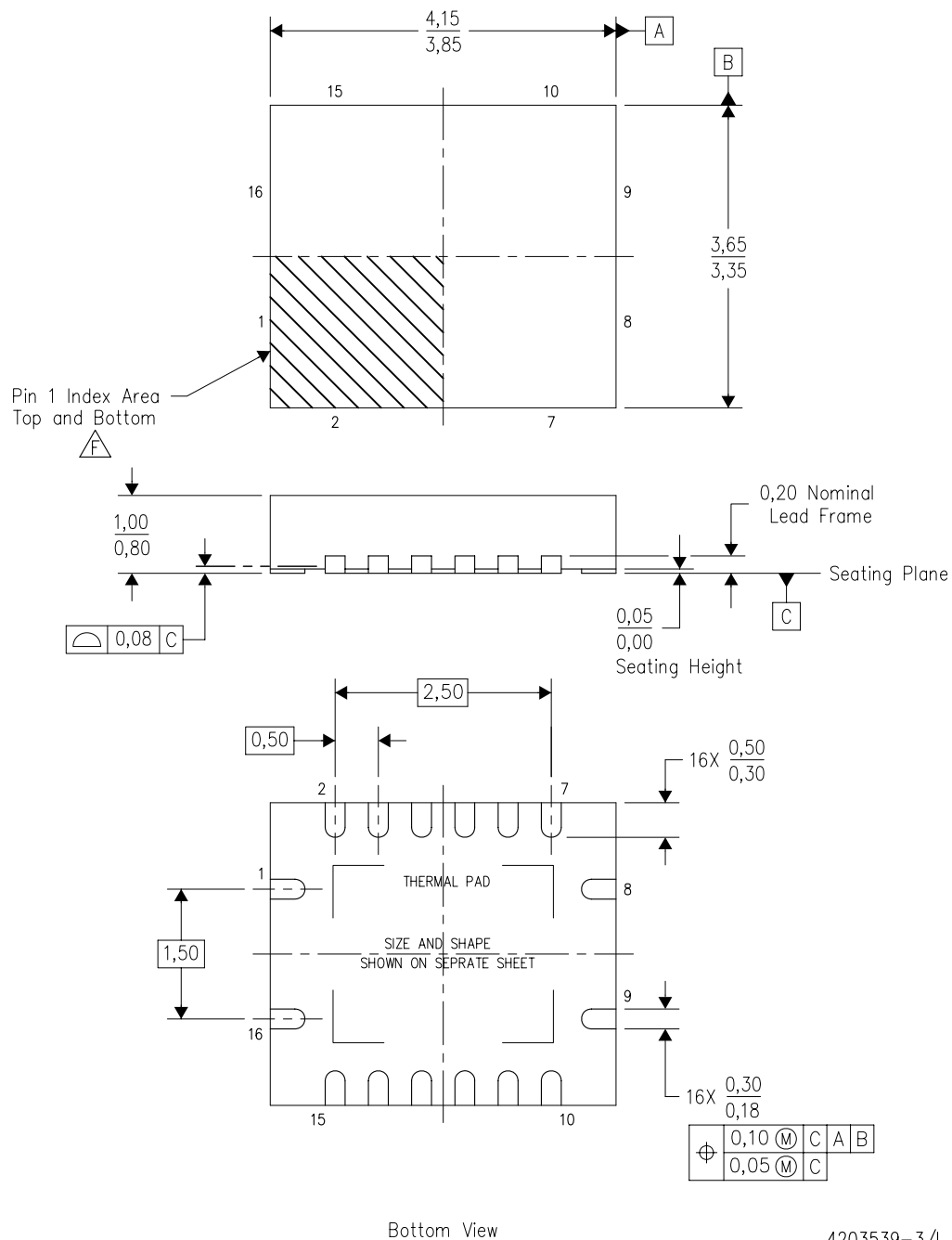
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

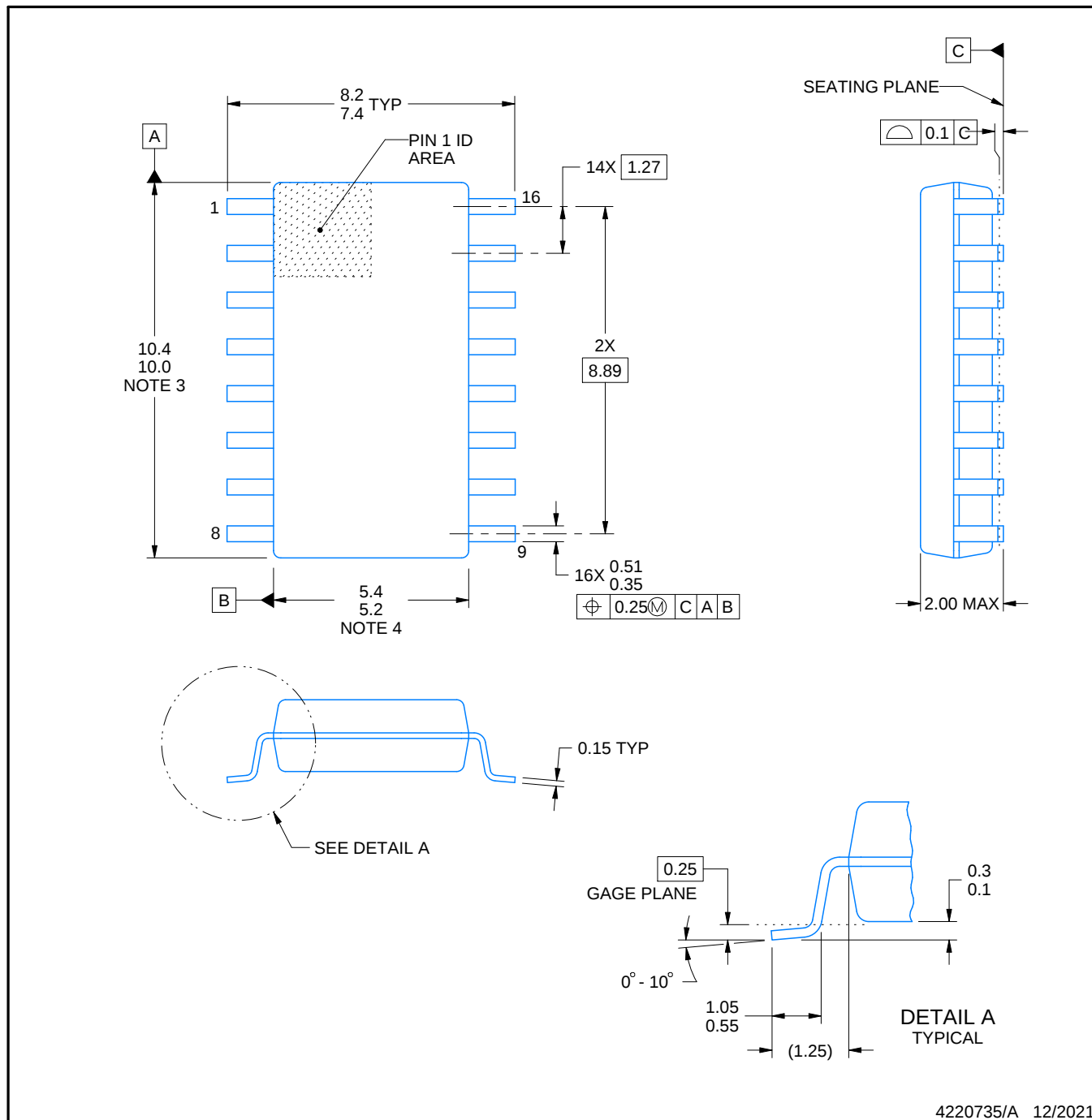


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月