

SN74LV393A 双路 4 位二进制计数器

1 特性

- V_{CC} 工作范围为 2V 至 5.5V
- 电压为 5V 时, t_{pd} 最大值为 10ns
- $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ 时, V_{OLP} (输出接地反弹) 典型值小于 0.8V
- $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ 时, V_{OHV} (输出 V_{OH} 下冲) 典型值大于 2.3V
- I_{off} 支持局部断电模式运行
- 具有独立时钟的双路 4 位二进制计数器
- 针对每个 4 位计数器的直接清零
- 可将计数器封装数量减少 50%, 从而显著提高系统密度
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范

2 应用

- [同步反相时钟输入](#)
- [对开关进行去抖](#)
- [对数字信号进行反相](#)

3 说明

'LV393A 器件包含八个触发器和额外的门控, 可在单个封装中实现两个独立的 4 位计数器。这些器件旨在 2V 至 5.5V V_{CC} 下运行。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
SN74LV393A	D (SOIC, 14)	8.65mm x 3.9mm
	NS (SOP, 14)	10.3mm x 5.3mm
	DB (SSOP, 14)	6.2mm x 5.3mm
	PW (TSSOP, 14)	5mm x 4.4mm
	DGV (TVSOP, 14)	3.6mm x 4.4mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

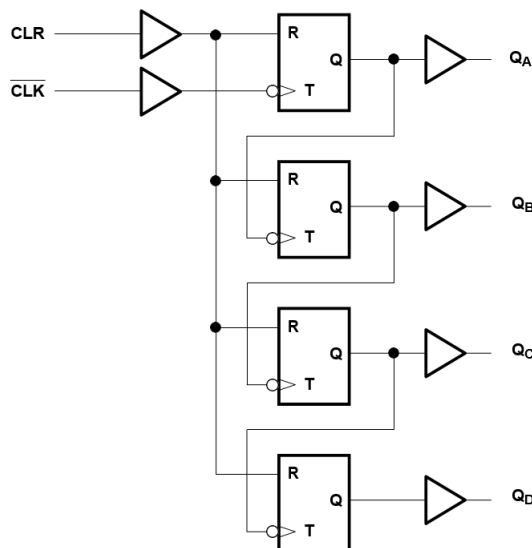


图 3-1. 逻辑图, 每个计数器 (正逻辑)



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (February 2001) to Revision E (March 2023)	Page
• 添加了应用、封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1

5 Pin Configuration and Functions

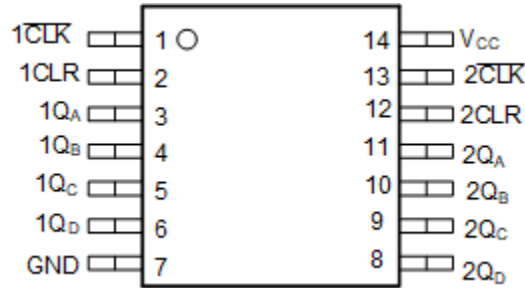


图 5-1. D, DB, DGV, NS, or PW Package (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1CLK	1	I	Counter 1 Clock Input
1CLR	2	I	Counter 1 Clear Input
1Q _A	3	O	Counter 1 A Output
1Q _B	4	O	Counter 1 B Output
1Q _C	5	O	Counter 1 B Output
1Q _D	6	O	Counter 1 B Output
GND	7	G	Ground
2Q _D	8	O	Counter 2 D Output
2Q _C	9	O	Counter 2 C Output
2Q _B	10	O	Counter 2 B Output
2Q _A	11	O	Counter 2 A Output
2CLR	12	I	Counter 2 Clear Input
2CLK	13	I	Counter 2 Clock Input
V _{CC}	14	P	V _{CC}

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	- 0.5	7	V
V _I	Input voltage ⁽¹⁾	- 0.5	7	V
V _O	Output voltage range applied in high or low state ^{(1) (2)}	- 0.5	V _{CC} + 0.5	V
V _O	Output voltage range applied in power-off state ⁽¹⁾	- 0.5	7	V
I _{IK}	Input clamp current	V _I < 0	- 20	mA
I _{OK}	Output clamp current	V _O < 0	- 50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25	mA
Continuous current through V _{CC} or GND			±50	mA
T _{stg}	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 - This value is limited to 7 V maximum.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-Body Model (A114-A) ⁽¹⁾	±2000
		Charged-Device Model (C101) ⁽²⁾	±1000
		Machine Model (A115-A)	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50		μA
		V _{CC} = 2.3 V to 2.7 V	-2		
		V _{CC} = 3 V to 3.6 V	-6		mA
		V _{CC} = 4.5 V to 5.5 V	-12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		μA
		V _{CC} = 2.3 V to 2.7 V	2		
		V _{CC} = 3 V to 3.6 V	6		mA
		V _{CC} = 4.5 V to 5.5 V	12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	200		ns/V
		V _{CC} = 3 V to 3.6 V	100		
		V _{CC} = 4.5 V to 5.5 V	20		
T _A	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV393A					UNIT
		D (SOIC)	NS (SOP)	DB (SSOP)	PW (TSSOP)	DGV (TVSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	86	96	127	76	113	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} - 0.1			V
	I _{OH} = -2 mA	2.3 V	2			
	I _{OH} = -6 mA	3 V	2.48			
	I _{OH} = -12 mA	4.5 V	3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V			0.1	V
	I _{OL} = 2 mA	2.3 V			0.4	
	I _{OL} = 6 mA	3 V			0.44	
	I _{OL} = 12 mA	4.5 V			0.55	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20	μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V			5	μA
C _i	V _I = V _{CC} or GND	3.3 V		1.8		pF

6.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

			T _A = 25°C		SN74LV393A		UNIT
			MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t _{su}	Setup time	CLR inactive before CLK ↓	6		6		ns

6.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

			T _A = 25°C		SN74LV393A		UNIT
			MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t _{su}	Setup time	CLR inactive before CLK ↓	5		5		ns

6.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			T _A = 25°C		SN74LV393A		UNIT
			MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t _{su}	Setup time	CLR inactive before CLK ↓	4		4		ns

6.9 Switching Characteristics, $V_{CC} = 2.5 V \pm 0.2 V$

over operating free-air temperature range, $V_{CC} = 2.5 V \pm 0.2 V$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	50 ¹	90 ¹		40		MHz
			C _L = 50 pF	30	70		25		
t _{pd}	CLK	Q _A	C _L = 15 pF		7.1 ¹	17.7 ¹	1	20.5	ns
		Q _B			8.5 ¹	20.3 ¹	1	23.5	
		Q _C			10 ¹	122.5 ¹	1	26	
		Q _D			11.1 ¹	24.2 ¹	1	28	
t _{PHL}	CLR	Q _n		6.7 ¹	14.8 ¹		1	17	
t _{pd}	CLK	Q _A	C _L = 50 pF		9.3	21.3	1	24.5	ns
		Q _B			10.9	23.9	1	27.5	
		Q _C			12.3	26.1	1	30	
		Q _D			13.4	27.8	1	32	
t _{PHL}	CLR	Q _n		9.1	17.4		1	20	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Switching Characteristics, $V_{CC} = 3.3 V \pm 0.3 V$

over operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	75 ¹	130 ¹		65		MHz
			C _L = 50 pF	45	105		35		
t _{pd}	CLK	Q _A	C _L = 15 pF		5.1 ¹	13.2 ¹	1	15.5	ns
		Q _B			6 ¹	15.8 ¹	1	18.5	
		Q _C			7 ¹	18 ¹	1	21	
		Q _D			7.7 ¹	19.7 ¹	1	23	
t _{PHL}	CLR	Q _n		5.1 ¹	12.3 ¹		1	14.5	
t _{pd}	CLK	Q _A	C _L = 50 pF		6.7	16.7	1	19	ns
		Q _B			7.8	19.3	1	22	
		Q _C			8.7	21.5	1	24.5	
		Q _D			9.5	23.2	1	26.5	
t _{PHL}	CLR	Q _n		6.8	15.8		1	18	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.11 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	125 ¹	185 ¹		105		MHz
			C _L = 50 pF	85	150		75		

6.11 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$ (continued)

over operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TA = 25°C			SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	CLK	Q _A	C _L = 15 pF		3.7 ¹	8.5 ¹	1	10	ns
		Q _B		4.3 ¹	9.8 ¹	1	11.5		
		Q _C		4.9 ¹	11.2 ¹	1	13		
		Q _D		5.3 ¹	12.5 ¹	1	14.5		
t _{PHL}	CLR	Q _n		3.9 ¹	8.1 ¹	1	9.5		
t _{pd}	CLK	Q _A	C _L = 50 pF		4.9	10.5	1	12	ns
		Q _B		5.6	11.8	1	13.5		
		Q _C		6.2	13.2	1	15		
		Q _D		6.6	14.5	1	16.5		
t _{PHL}	CLR	Q _n		5.2	10.1	1	11.5		

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.12 Timing Diagrams

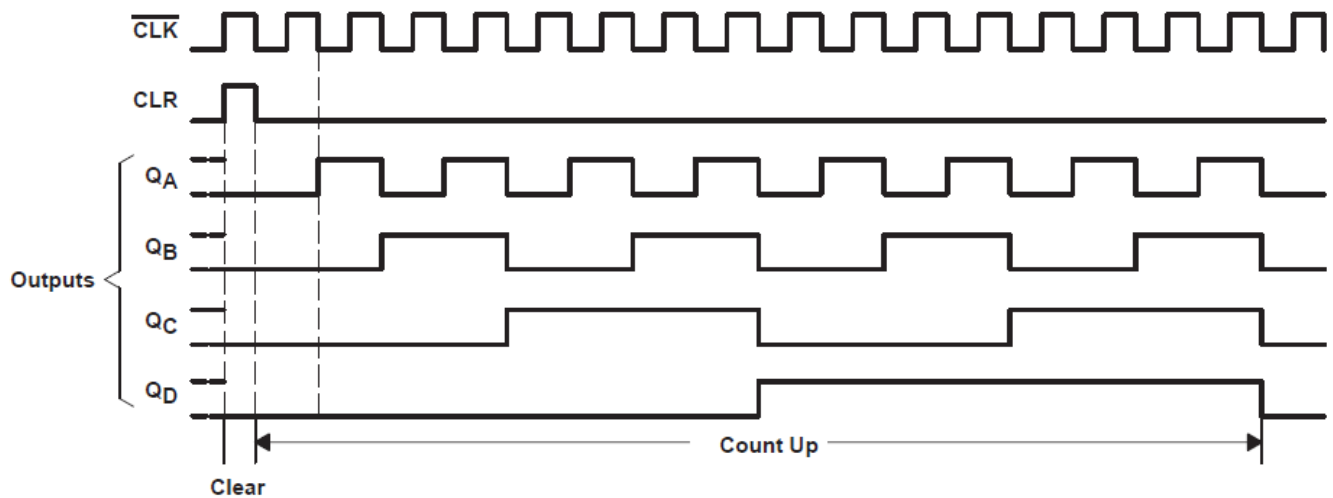


图 6-1. Timing Diagram

6.13 Noise Characteristics

$V_{CC} = 3.3 V$, $C_L = 50 pF$, $T_A = 25^\circ C$

PARAMETER ⁽¹⁾		SN74LV393A			UNIT
		MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.3	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.2	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		2.8		V
V _{IH(D)}	High-level dynamic input voltage	2.31			V
V _{IL(D)}	Low-level dynamic input voltage			0.99	V

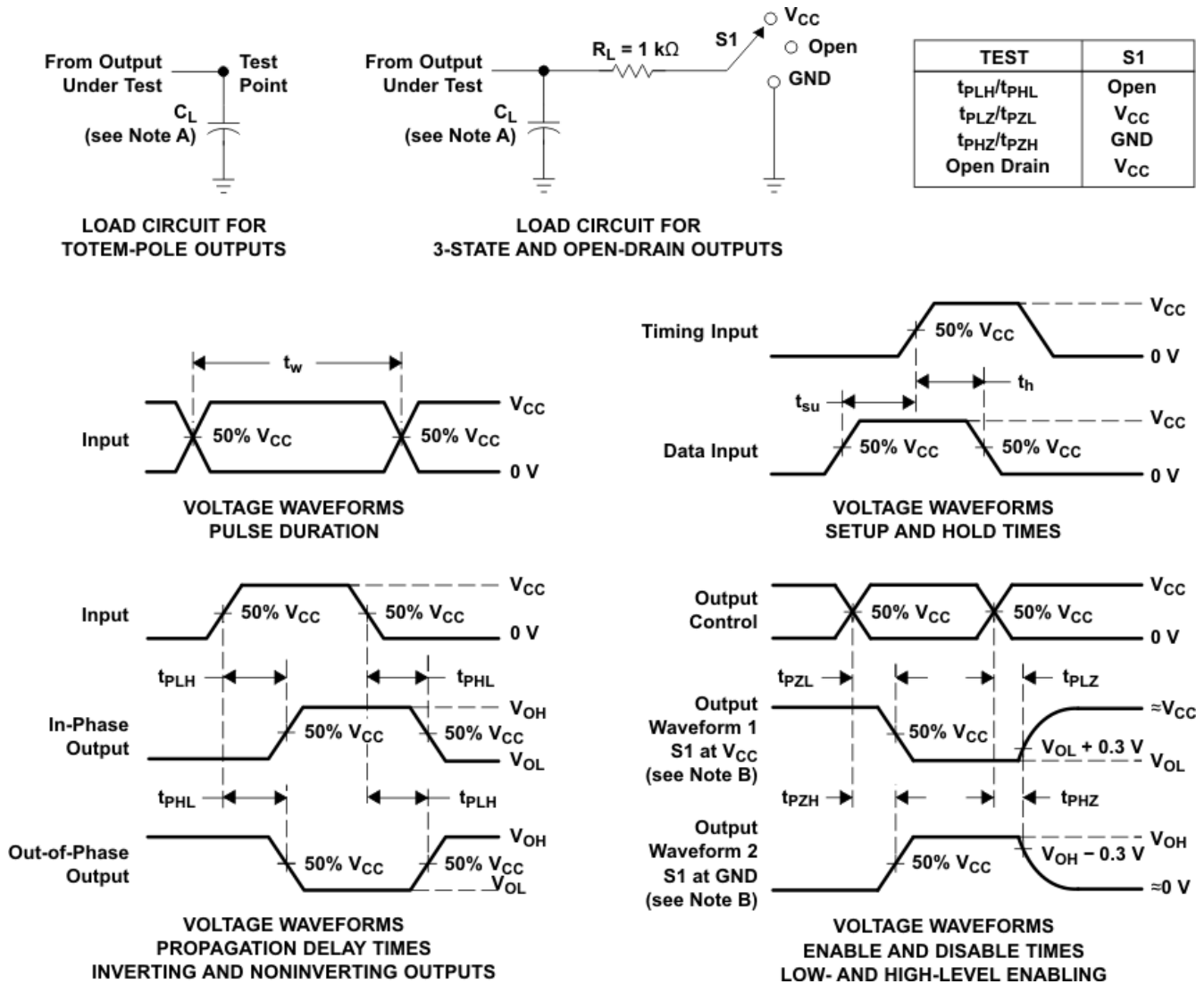
(1) Characteristics for surface-mount packages only.

6.14 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance (outputs enabled)	C _L = 50 pF, f = 10 MHz	3.3 V	15.2	pF
			5 V	17.3	

7 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, and $t_f \leq 3$ ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

These devices comprise two independent 4-bit binary counters, each having a clear (CLR) and a clock ($\overline{\text{CLK}}$) input. These devices change state on the negative-going transition of the $\overline{\text{CLK}}$ pulse. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The 'LV393A devices have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram

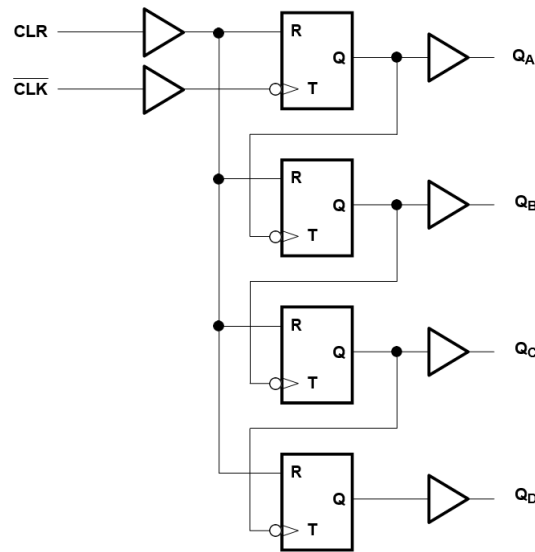


图 8-1. Logic Diagram, Each Counter (Positive Logic)

8.3 Device Functional Modes

表 8-1. Function Table

INPUTS		FUNCTION
$\overline{\text{CLK}}$	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μ F capacitor; if there are multiple V_{CC} terminals, then TI recommends a 0.01- μ F or 0.022- μ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

9.2 Layout

9.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

9.2.1.1 Layout Example

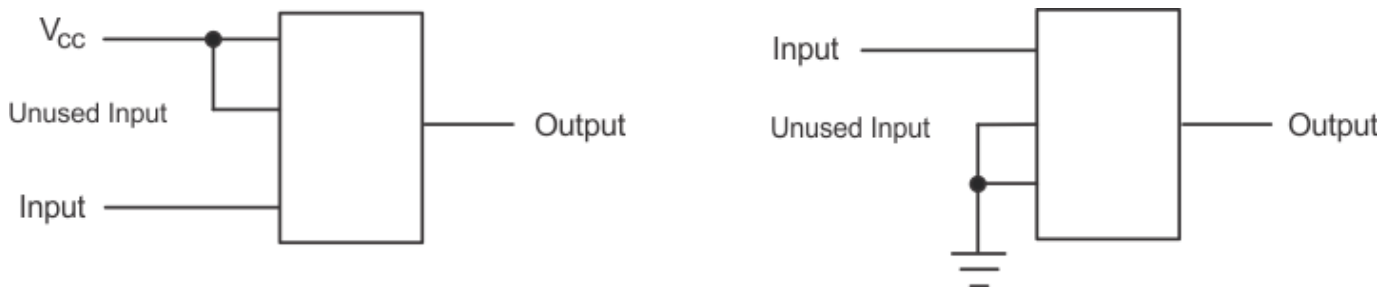


图 9-1. Layout Diagram

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV393A	Click here	Click here	Click here	Click here	Click here

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV393AD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	LV393A
SN74LV393ADBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393ADBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393ADGVR	NRND	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393ADGVR.A	NRND	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393ADR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393ANSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV393A
SN74LV393ANSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV393A
SN74LV393APW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	LV393A
SN74LV393APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393APWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393APWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393APWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393APWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A
SN74LV393APWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	No	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LV393A :

- Automotive : [SN74LV393A-Q1](#)
- Enhanced Product : [SN74LV393A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

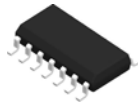

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV393ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV393ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV393ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV393ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV393APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV393APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV393ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LV393ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LV393ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV393ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LV393APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV393APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220762/A 05/2024

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

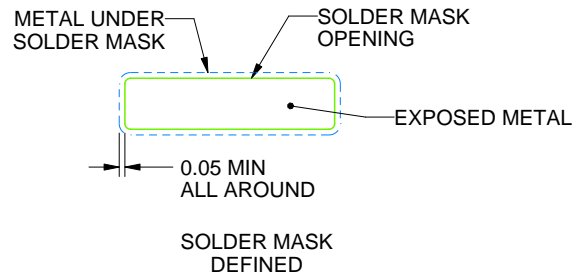
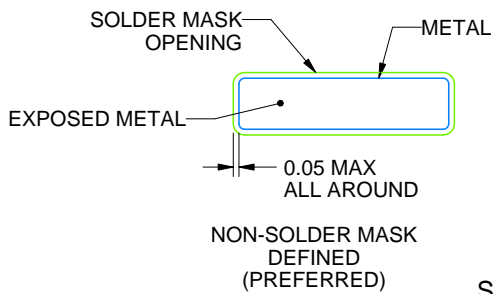
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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