SN74LV164A-Q1 汽车类 8 位并行输出串行移位寄存器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：–40°C 至 +125°C，T_A
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 2V 至 5.5V V_{CC} 运行
- 5V 时 t_{pd} 最大值为 10.5 ns
- V_{OLP}（输出接地反弹）典型值小于 0.8V（V_{CC} = 3.3V、T_A = 25°C 时）
- V_{OHV}（输出 V_{OH} 下冲）典型值大于 2.3V（V_{CC} = 3.3V、T_A = 25°C 时）
- Ioff 支持带电插入、局部关断模式以及后驱动保护
- 所有端口上均支持以混合模式电压运行
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 输出扩展
- LED 矩阵控制
- 7 段显示控制

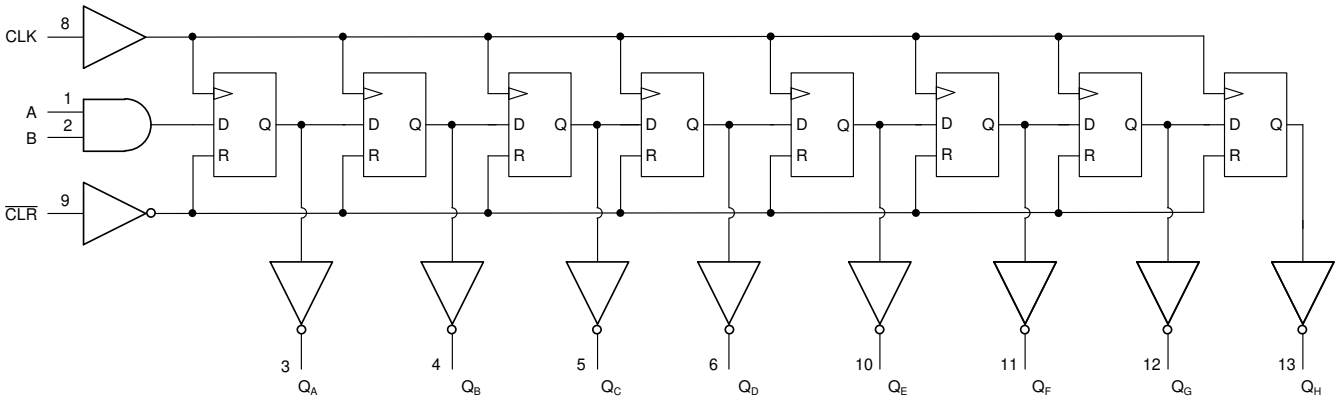
3 说明

SN74LV164A-Q1 器件是 8 位并行输出串行移位寄存器，可在 2V 至 5.5V V_{CC} 下运行。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74LV164A-Q1	BQA（WQFN，14）	3.00mm x 2.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图（正逻辑）

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

DATE	REVISION	NOTES
December 2022	*	Initial Release

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5 Pin Configuration and Functions

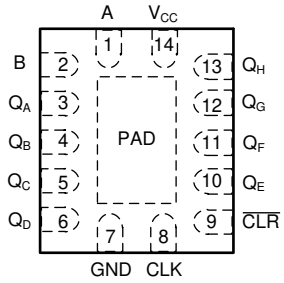


图 5-1. BQA Package, 14-PIN WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A	1	I	Serial input A
B	2	I	Serial input B
Q_A	3	O	Output A
Q_B	4	O	Output B
Q_C	5	O	Output C
Q_D	6	O	Output D
GND	7	G	Ground pin
CLK	8	I	Storage clock
$\overline{CLR}$	9	I	Storage clear
Q_E	10	O	Output E
Q_F	11	O	Output F
Q_G	12	O	Output G
Q_H	13	O	Output H
$Q_{H'}$	11	O	Q_H inverted
V_{CC}	14	P	Power pin
Thermal pad		—	Thermal pad[2]

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) WBQA package only

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6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±2000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	μA
		V_{CC} = 2.3 V to 2.7 V		– 2	mA
		V_{CC} = 3 V to 3.6 V		– 6	
		V_{CC} = 4.5 V to 5.5 V		– 12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		– 40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV164A-Q1 BQA (WQFN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	56.8	
ψ_{JT}	Junction-to-top characterization parameter	9.9	
ψ_{JB}	Junction-to-board characterization parameter	56.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	33.4	

(1) For more information about traditional and new thermal metrics, see *IC Package Thermal Metrics*

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	–40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V
	I_{OH} = –2 mA	2.3 V	2			
	I_{OH} = –6 mA	3 V	2.48			
	I_{OH} = –12 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4	
	I_{OL} = 6 mA	3 V			0.44	
	I_{OL} = 12 mA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		2.2		pF

6.6 Timing Requirements: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

			T_A = 25°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	6		6.5		ns
		CLK high or low	6.5		7.5		
t_{su}	Setup time	Data before CLK ↑	6.5		8.5		ns
		$\overline{CLR}$ inactive	3		3		
t_h	Hold time	Data after CLK ↑	–0.5		0		ns

6.7 Timing Requirements: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

			T_A = 25°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		5		ns
		CLK high or low	5		5		
t_{su}	Setup time	Data before CLK ↑	5		6		ns
		$\overline{CLR}$ inactive	2.5		2.5		
t_h	Hold time	Data after CLK ↑	0		0		ns

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6.8 Timing Requirements: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

			T_A = 25°C		– 40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		5		ns
		CLK high or low	5		5		
t_{su}	Setup time	Data before CLK ↑	4.5		4.5		ns
		$\overline{CLR}$ inactive	2.5		2.5		
t_h	Hold time	Data after CLK ↑	1		1		ns

6.9 Switching Characteristics: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			– 40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	55	105		50		MHz
			C_L = 50 pF	45	85		40		
t_{pd}	CLK	Q	C_L = 15 pF		9.2	17.6	1	21	ns
t_{PHL}	$\overline{CLR}$	Q			8.6	16	1	18.5	
t_{pd}	CLK	Q	C_L = 50 pF		11.5	21.1	1	25	ns
t_{PHL}	$\overline{CLR}$	Q			10.8	19.5	1	22.5	

6.10 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			– 40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80	155		65		MHz
			C_L = 50 pF	50	120		45		
t_{pd}	CLK	Q	C_L = 15 pF		6.4	12.8	1	16	ns
t_{PHL}	$\overline{CLR}$	Q			6	12.8	1	16	
t_{pd}	CLK	Q	C_L = 50 pF		8.3	16.3	1	19.5	ns
t_{PHL}	$\overline{CLR}$	Q			7.9	16.3	1	19.5	

6.11 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			– 40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	125	220		95		MHz
			C_L = 50 pF	85	165		65		
t_{pd}	CLK	Q	C_L = 15 pF		4.5	9	1	11.5	ns
t_{PHL}	$\overline{CLR}$	Q			4.2	8.6	1	11	
t_{pd}	CLK	Q	C_L = 50 pF		6	11	1	13	ns
t_{PHL}	$\overline{CLR}$	Q			5.8	10.6	1	13	

6.12 Noise Characteristics(1)

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER		SN74LV164A-Q1			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.28	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		– 0.22	– 0.8	V

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V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER		SN74LV164A-Q1			UNIT
		MIN	TYP	MAX	
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.09		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.13 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	48.1	pF
				5 V	47.5	

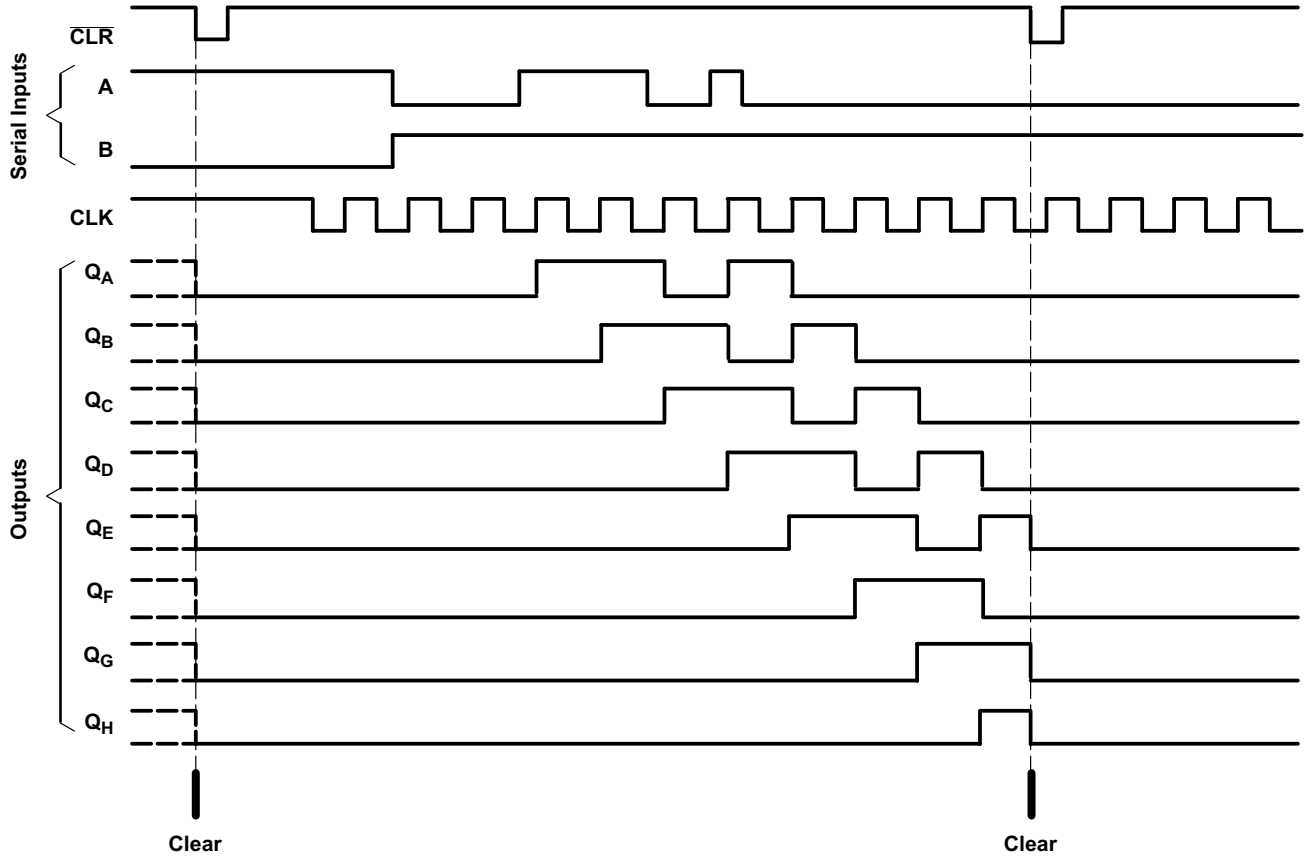


图 6-1. Typical Clear, Shift, and Clear Sequences

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6.14 Typical Characteristics

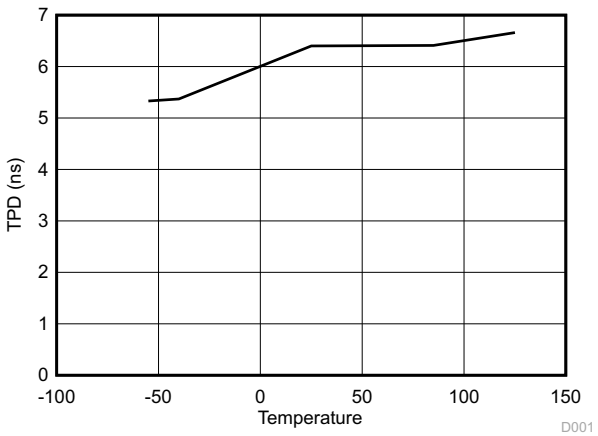


图 6-2. TPD vs. Temperature at 3.3 V

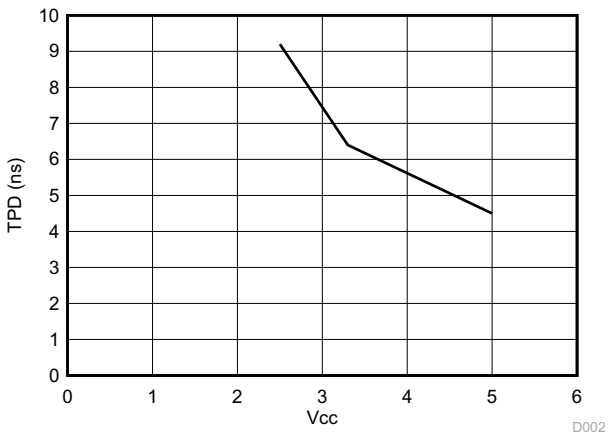
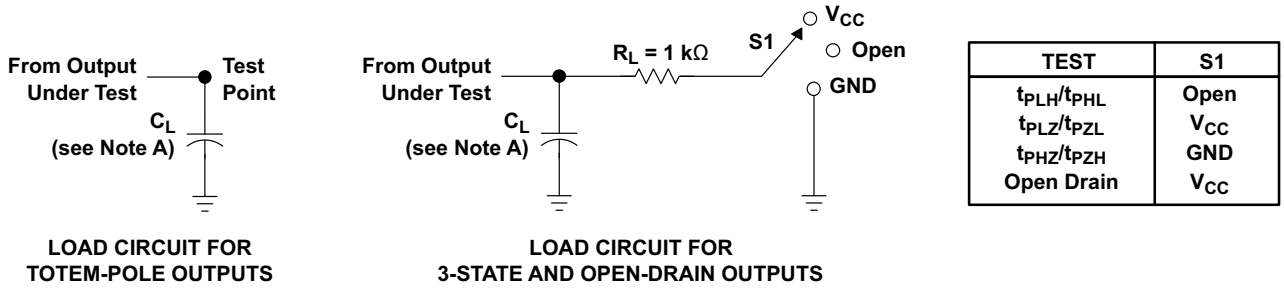


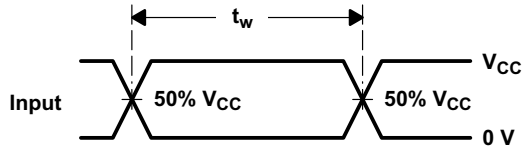
图 6-3. TPD vs. V_{CC} at 25°C

7 Parameter Measurement Information

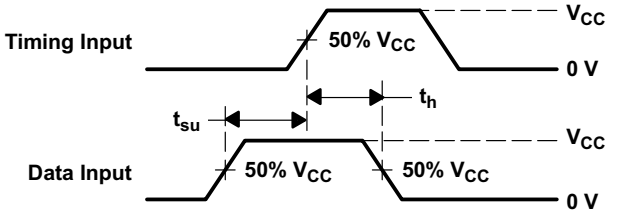


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

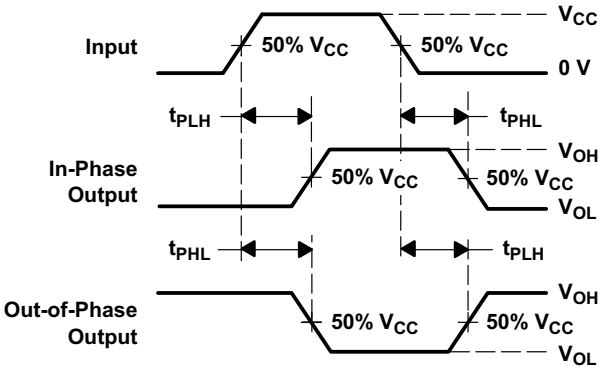
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



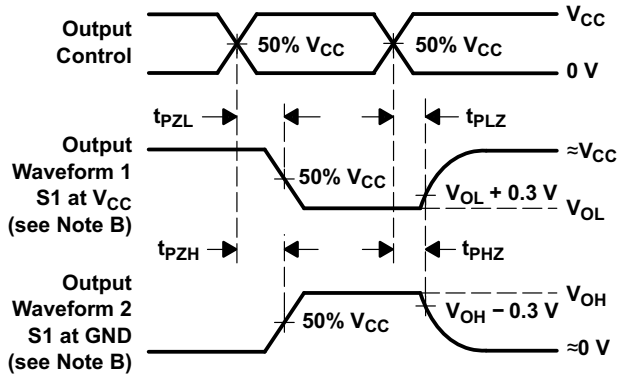
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

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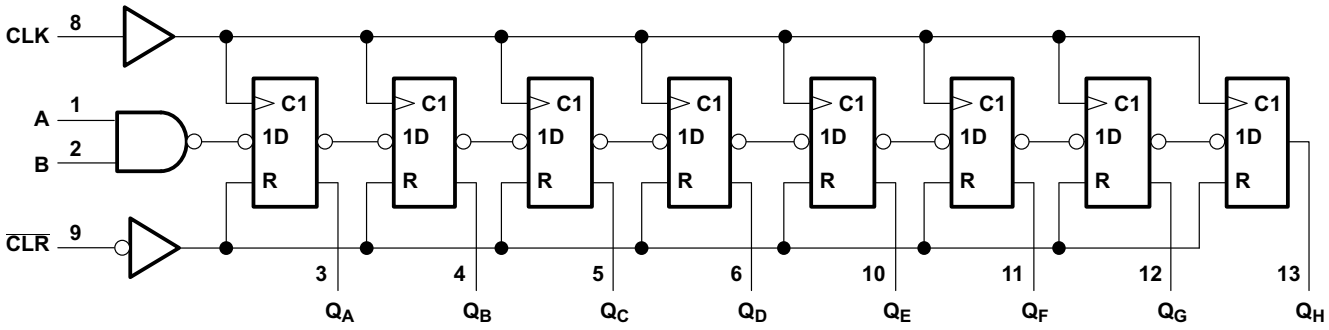
8 Detailed Description

8.1 Overview

The SN74LV164A-Q1 devices are 8-bit parallel-out serial shift registers designed for 2-V to 5.5-V V_{CC} operation.

These devices feature NAND-gated serial (A and B) inputs and an asynchronous clear ($\overline{CLR}$) input. The gated serial inputs permit complete control over incoming data, as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

8.3 Feature Description

The wide operating range allows the device to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

8.4 Device Functional Modes

表 8-1. Function Table(1)(2)

INPUTS				OUTPUTS			
$\overline{CLR}$	CLK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

(1) Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

(2) Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock: indicates a 1-bit shift.

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9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV164A-Q1 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low-drive and slow-edge rates will minimize overshoot and undershoot on the outputs.

9.2 Typical Application

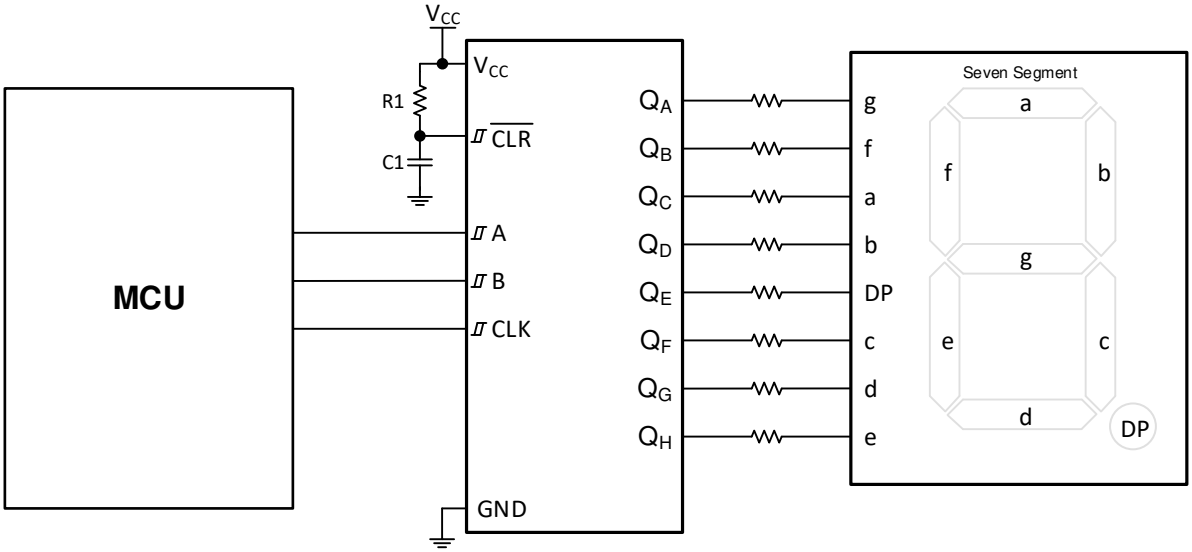


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Rise time and fall time specs. See ($\Delta t/\Delta V$) in *Recommended Operating Conditions*.
  - Specified high and low level. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

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9.2.3 Application Curves

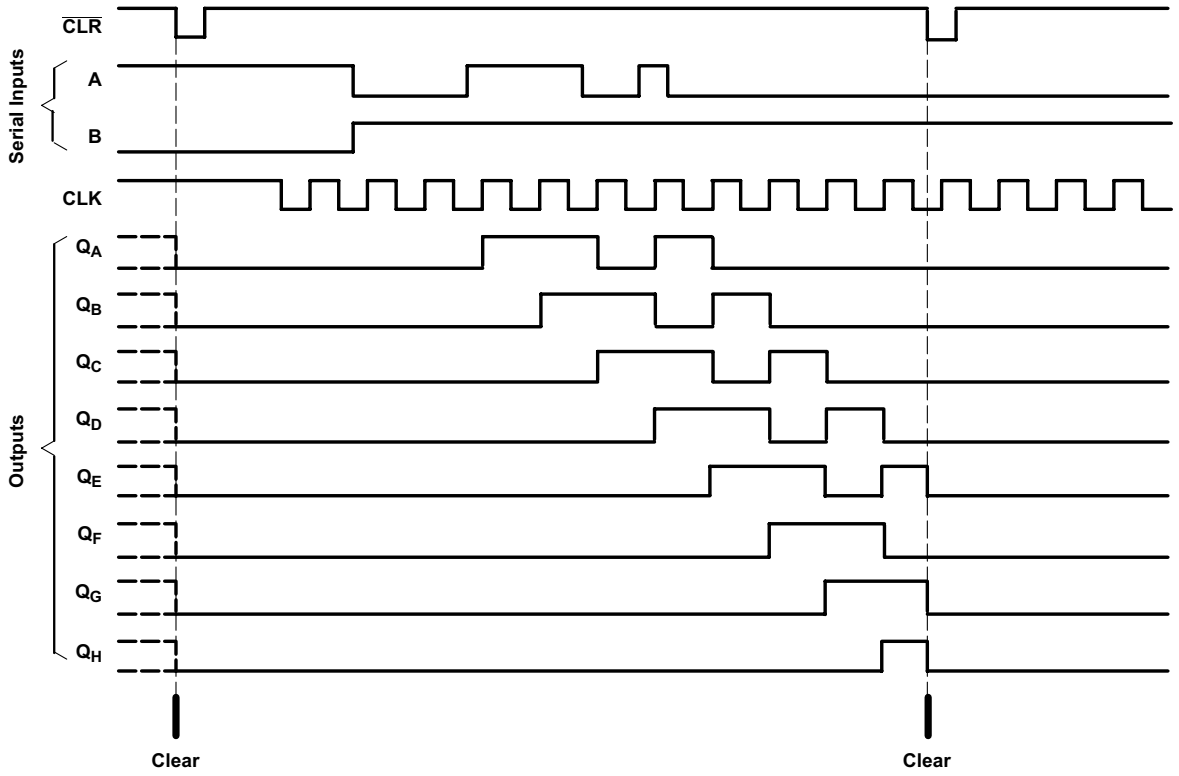


图 9-2. Application Timing Diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01-μF or 0.022-μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

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11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O’s so they also cannot float when disabled.

11.2 Layout Example

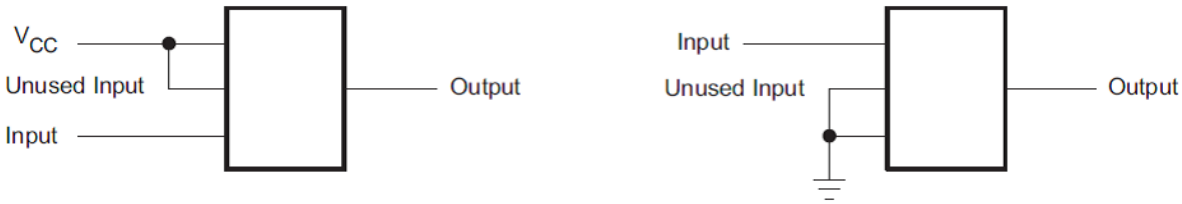


图 11-1. Layout Example

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12 Device and Documentation Support

12.1 接收文档更新通知

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12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV164AQWBQARQ1	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVA164
SN74LV164AQWBQARQ1.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVA164

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV164A-Q1 :

- Catalog : SN74LV164A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

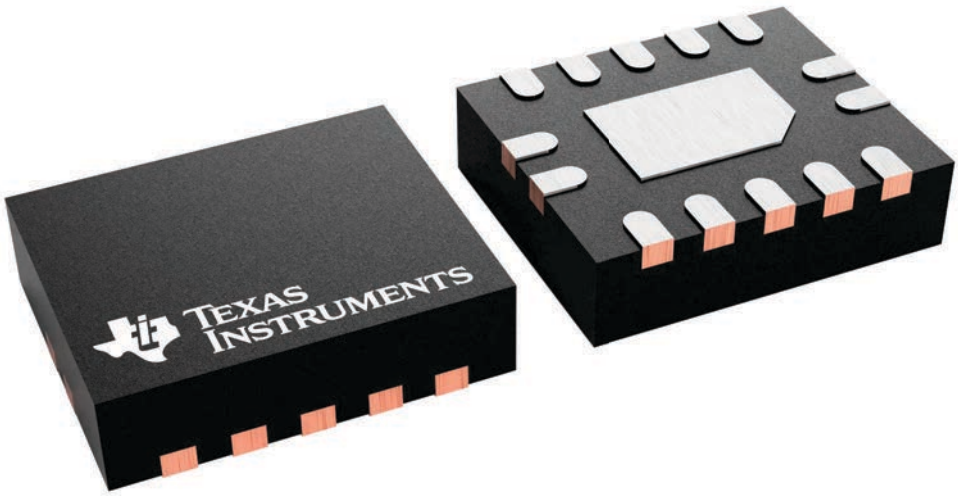
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

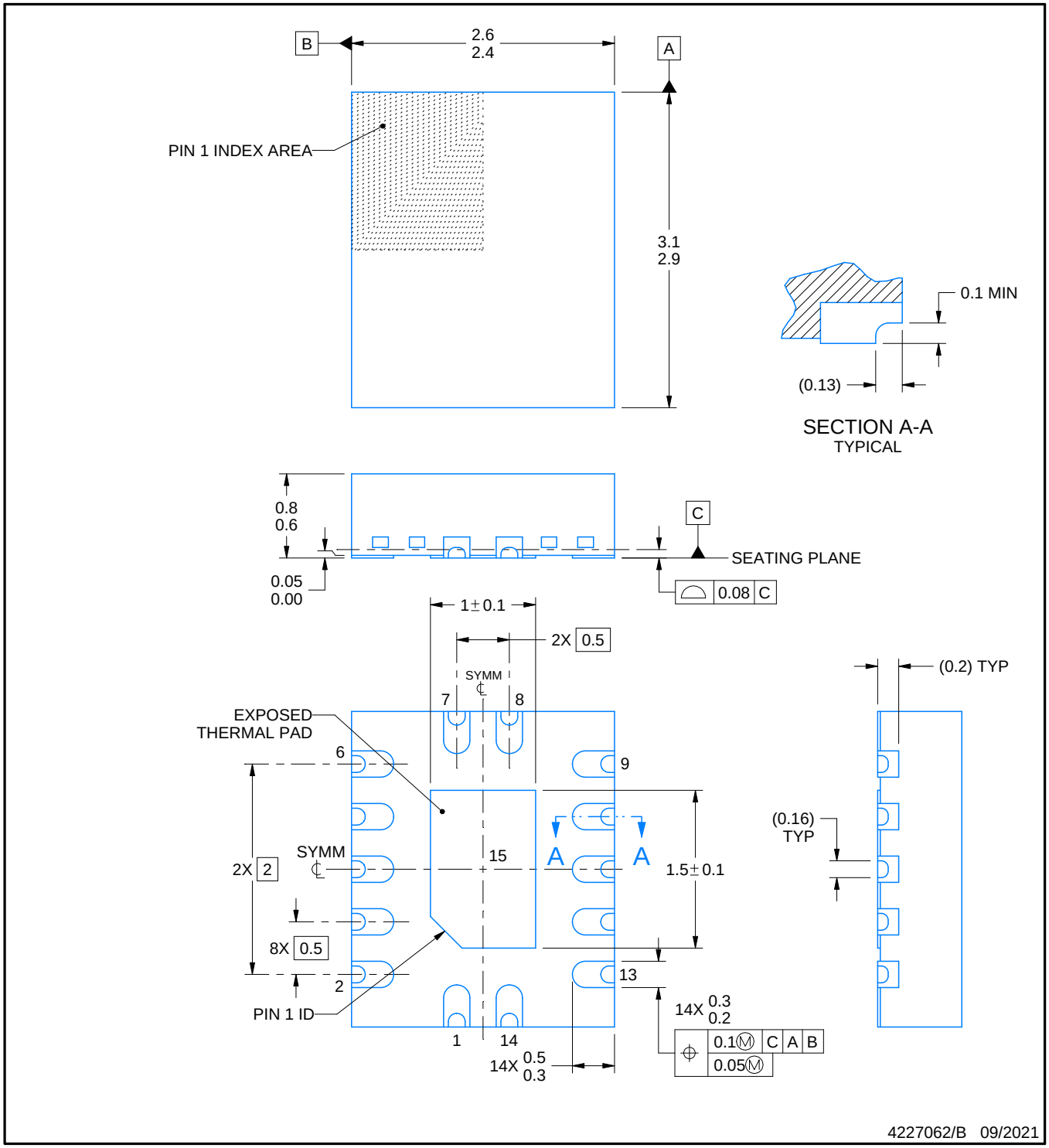


BQA0014B

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

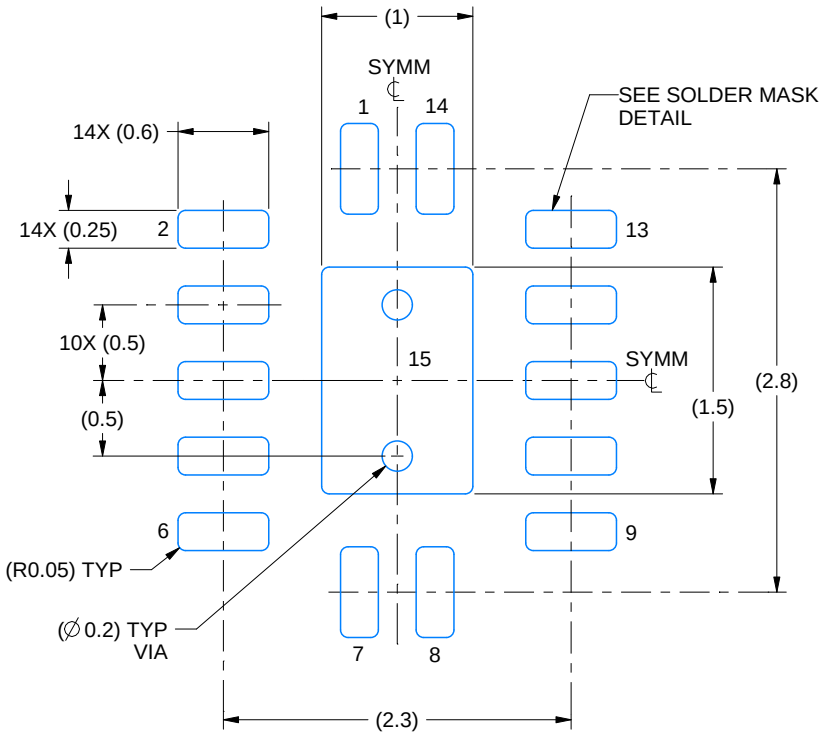
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

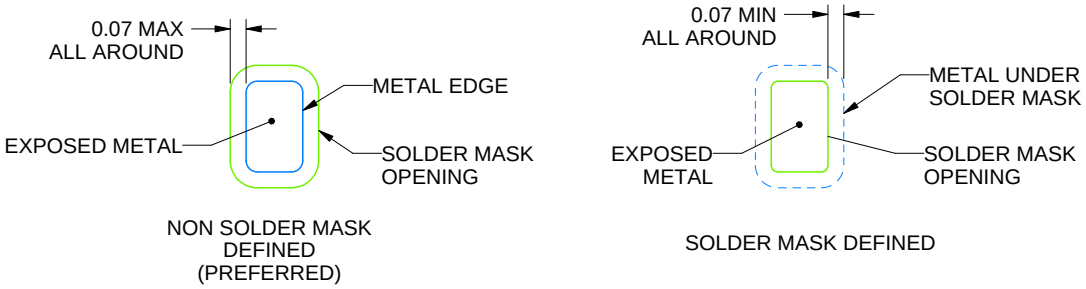
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

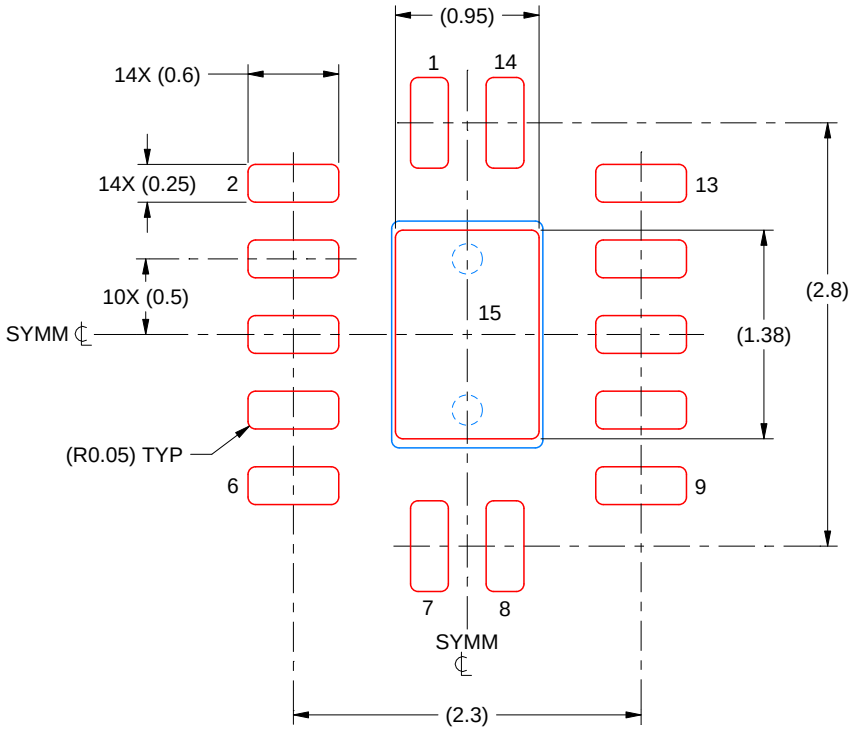


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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