SN74HCS595-Q1 具有施密特触发输入和三态输出寄存器的汽车类 8 位移位寄存器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：
    - –40°C 至 +125°C，T_A
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 采用可湿侧面 QFN (WBQB) 封装
- 宽工作电压范围：2V 至 6V
- 施密特触发输入可实现慢速或高噪声输入信号
- 低功耗
  - I_{CC} 典型值为 100nA
  - 输入泄漏电流典型值为 ±100nA
- 电压为 6V 时，输出驱动为 ±7.8mA

2 应用

- 输出扩展
- LED 矩阵控制
- 7 段显示控制
- 8 位数据存储

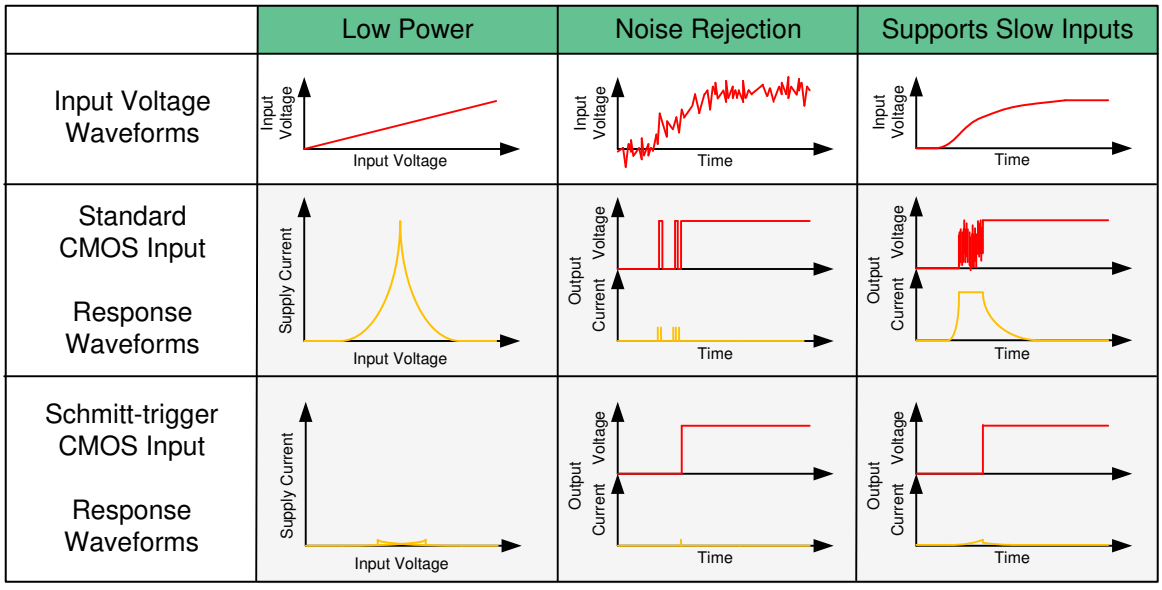
3 说明

SN74HCS595-Q1 器件包含对 8 位 D 类存储寄存器进行馈送的 8 位串行输入、并行输出移位寄存器。所有输入均包括施密特触发架构，因此消除了由边沿变化缓慢或高噪声输入信号导致的任何错误数据输出。存储寄存器具有并行三态输出。移位寄存器和存储寄存器分别有单独的时钟。移位寄存器具有一个直接覆盖清零 ($\overline{SRCLR}$) 的串行 (SER) 输入和一个串行输出 ($Q_{H'}$)，以用于级联。当输出使能端 ($\overline{OE}$) 输入为高电平时，存储寄存器输出处于高阻抗状态。内部寄存器数据和串行输出 ($Q_{H'}$) 不受 $\overline{OE}$ 端输入的影响。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74HCS595PW-Q1	TSSOP (16)	5.00mm × 4.40mm
SN74HCS595D-Q1	SOIC (16)	9.90mm × 3.90mm
SN74HCS595BQB-Q1	WQFN (16)	3.60mm × 2.60mm
SN74HCS595DYY-Q1	SOT-23-THN (16)	4.20mm × 2.00mm
SN74HCS595WBQB-Q1	WQFN (16)	3.60mm × 2.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



施密特触发输入的优势

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (September 2021) to Revision F (December 2021) — **Page**

- 将 WBQB 封装状态从*产品预发布*更改为*量产* 1

Changes from Revision D (June 2021) to Revision E (September 2021) — **Page**

- 添加了 WBQB 封装的功能 1
- 在器件信息表中添加了 WBQB 器件型号 1
- Added WBQB package to WQFN pinout diagram and to pin functions table 3
- Added WBQB package to *Thermal Information table* 5

Changes from Revision C (March 2021) to Revision D (June 2021) — **Page**

- 将 DYY 封装从*产品预发布*更改为*量产数据* 1

Changes from Revision B (August 2020) to Revision C (March 2021) — **Page**

- 在*器件信息*表中添加了 DYY 封装 1
- Added DYY Package pinout diagram and information to *Pin Configuration and Functions* 3
- Added DYY Package to *Thermal Information* table 5

Changes from Revision A (February 2020) to Revision B (August 2020) — **Page**

- 更新了整个文档中的表、图和交叉参考的编号格式 1
- 在可订购产品表中增加了 BQB 封装 1
- Added BQB Package to *Thermal Information* table 5

Changes from Revision * (December 2019) to Revision A (February 2020) — **Page**

- 将“应用信息”更改为“量产数据” 1
- 在可订购产品表中增加了 D 封装 1
- Added D Package to *Thermal Information* table 5

5 Pin Configuration and Functions

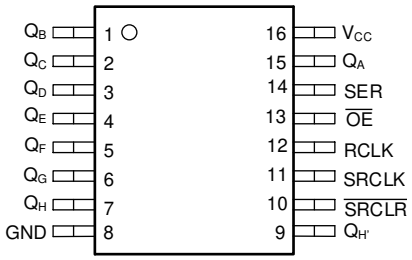


图 5-1. D, PW, or DYY Package 16-Pin SOIC, TSSOP, or SOT Top View

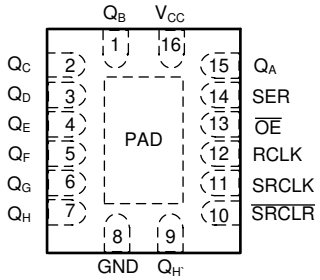


图 5-2. WBQB (Preview) or BQB Package 16-Pin WQFN Transparent Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Q_B	1	Output	Q_B output
Q_C	2	Output	Q_C output
Q_D	3	Output	Q_D output
Q_E	4	Output	Q_E output
Q_F	5	Output	Q_F output
Q_G	6	Output	Q_G output
Q_H	7	Output	Q_H output
GND	8	—	Ground
$Q_{H'}$	9	Output	Serial output, can be used for cascading
$\overline{SRCLR}$	10	Input	Shift register clear, active low
SRCLK	11	Input	Shift register clock, rising edge triggered
RCLK	12	Input	Output register clock, rising edge triggered
$\overline{OE}$	13	Input	Output Enable, active low
SER	14	Input	Serial input
Q_A	15	Output	Q_A output
V_{CC}	16	—	Positive supply
Thermal Pad(1)		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1) BQB and WBQB package only.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current(2)	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Assured by design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74HCS595-Q1					UNIT
		PW (TSSOP)	D (SOIC)	BQB (WQFN)	DYY (SOT)	WBQB (WQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.2	122.2	108.4	186.2	97.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	80.9	77.3	109.1	93.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.8	80.6	74.4	111.0	66.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.7	40.4	12.6	18.0	14.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	85.5	80.3	74.5	110.9	66.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	54.3	N/A	44.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis (V_{T+} - V_{T-})[1]			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 μA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4.0	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.30	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V		±0.1	±1	μA
I_{OZ}	Off-state (high-impedance state) output current	V_O = V_{CC} or 0		6 V		±0.5	±5	μA
I_{CC}	Supply current	V_I = V_{CC} or 0, I_O = 0		6 V		0.1	2	μA
C_i	Input capacitance			2 V to 6 V			5	pF

(1) Assured by design.

6.6 Timing Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information.*

PARAMETER			V_{CC}	Operating free-air temperature (T_A)				UNIT
				25°C		−40°C to 125°C		
				MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK or RCLK high or low	2 V	7		9		ns
			4.5 V	7		7		
			6 V	7		7		
		$\overline{SRCLR}$ low	2 V	8		10		
			4.5 V	7		7		
			6 V	7		7		
t_{su}	Setup time	SER before SRCLK ↑	2 V	8		13		ns
			4.5 V	4		5		
			6 V	3		4		
		SRCLK ↑ before RCLK ↑	2 V	11		18		
			4.5 V	5		7		
			6 V	4		6		
		$\overline{SRCLR}$ low before RCLK ↑	2 V	8		13		
			4.5 V	4		6		
			6 V	4		5		
		$\overline{SRCLR}$ high (inactive) before SRCLK ↑	2 V	8		13		
			4.5 V	4		6		
			6 V	4		5		
t_h	Hold time	SER after SRCLK ↑	2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		

6.7 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information.*

PARAMETER		FROM	TO	V_{CC}	Operating free-air temperature (T_A)						UNIT
					25°C			−40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Max switching frequency			2 V	35			19			MHz
				4.5 V	110			60			
				6 V	130			75			
t_{pd}	Propagation delay	SRCLK	$Q_{H'}$	2 V		14	19			28	ns
				4.5 V		6	8			10	
				6 V		5	7			9	
		RCLK	Q_A - Q_H	2 V		16	21			37	
				4.5 V		6	9			12	
				6 V		6	8			10	
t_{PHL}	Propagation delay	$\overline{SRCLR}$	$Q_{H'}$	2 V		13	19			27	ns
				4.5 V		6	8			11	
				6 V		6	8			10	
t_{en}	Enable time	$\overline{OE}$	Q_A - Q_H	2 V		12	18			27	ns
				4.5 V		6	9			13	
				6 V		5	8			11	

6.7 Switching Characteristics (continued)

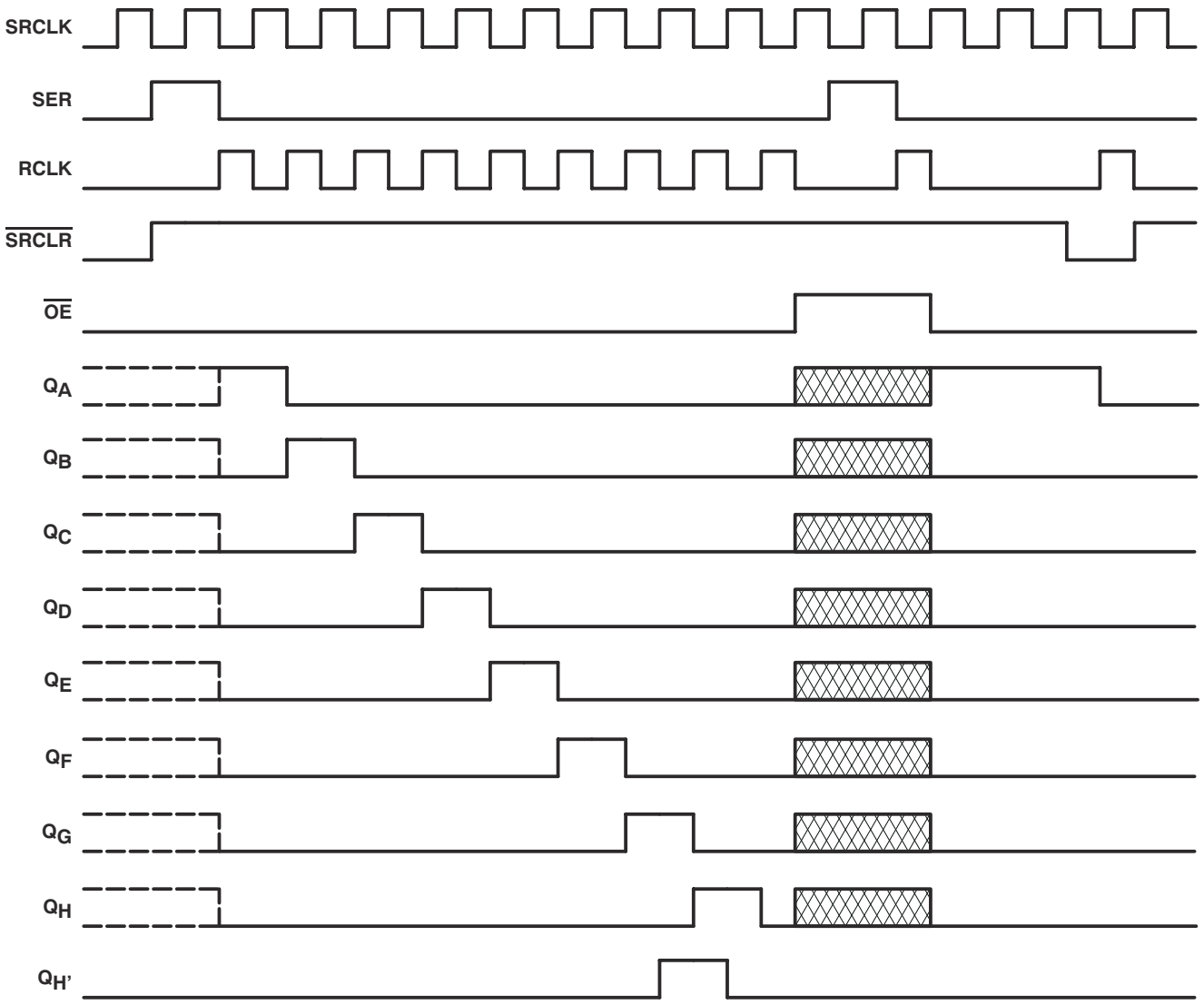
C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information.*

PARAMETER		FROM	TO	V_{CC}	Operating free-air temperature (T_A)						UNIT
					25°C			– 40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{dis}	Disable time	$\overline{OE}$	Q_A - Q_H	2 V		13	16			20	ns
				4.5 V		9	11			13	
				6 V		8	10			12	
t_t	Transition-time		Any output	2 V			9			16	ns
				4.5 V			5			9	
				6 V			4			8	

6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V		40		pF



NOTE: ▨ implies that the output is in 3-State mode.

图 6-1. Timing Diagram

6.9 Typical Characteristics

T_A = 25°C

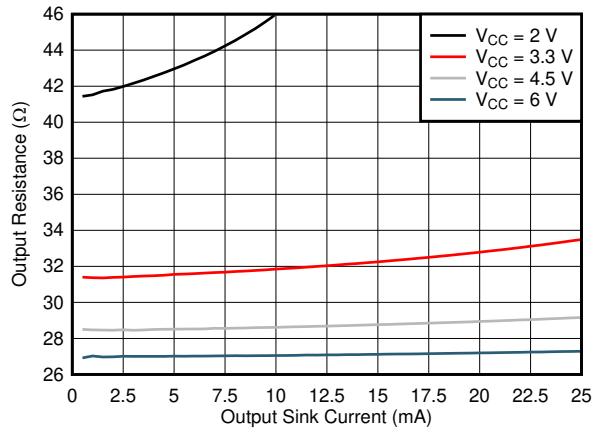


图 6-2. Output Driver Resistance in LOW State

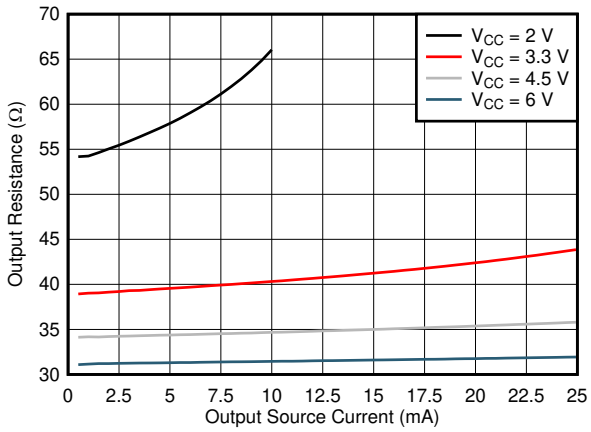


图 6-3. Output Driver Resistance in HIGH State

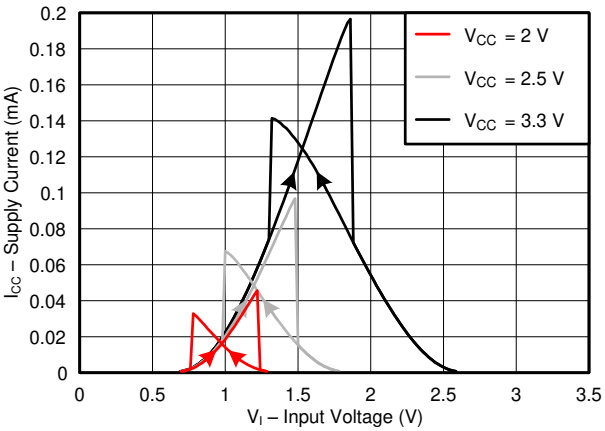


图 6-4. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3-V Supply

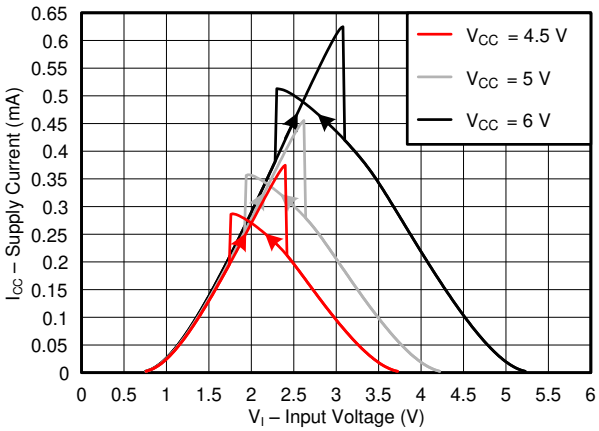


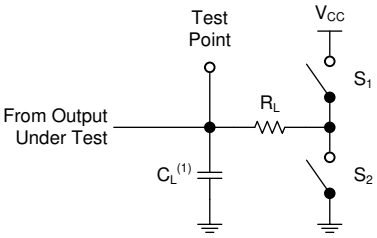
图 6-5. Supply Current Across Input Voltage, 4.5-, 5-, and 6-V Supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

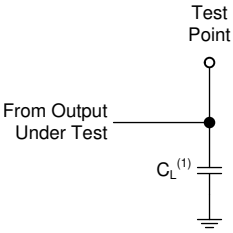
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

图 7-1. Load Circuit for 3-State Outputs



(1) C_L includes probe and test-fixture capacitance.

图 7-2. Load Circuit for Push-Pull Outputs

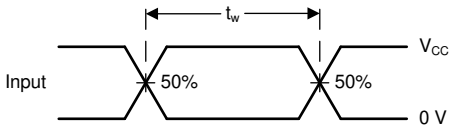


图 7-3. Voltage Waveforms, Pulse Duration

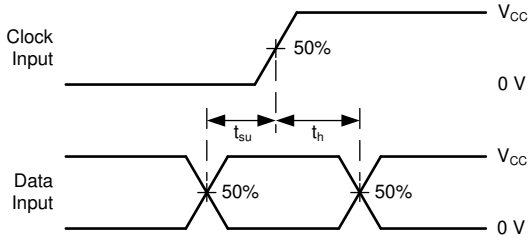
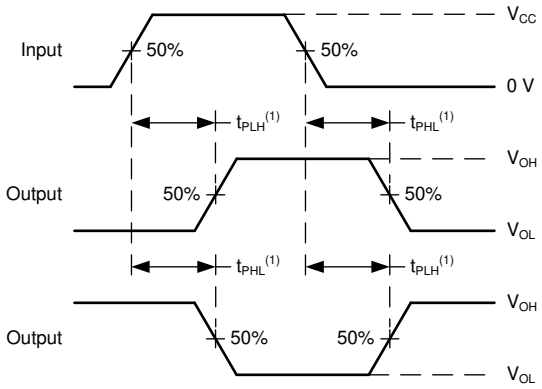


图 7-4. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

图 7-5. Voltage Waveforms Propagation Delays

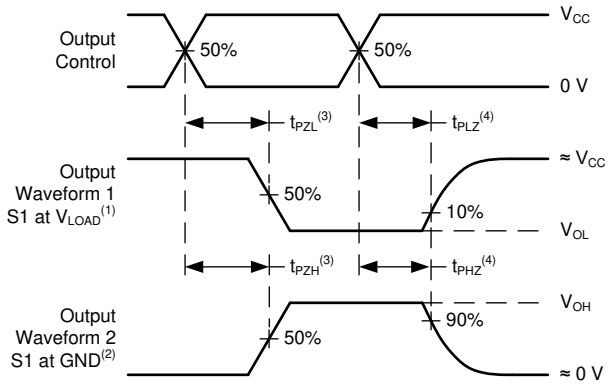
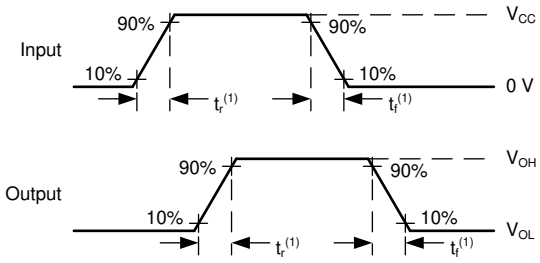


图 7-6. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

图 7-7. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Functional Block Diagram

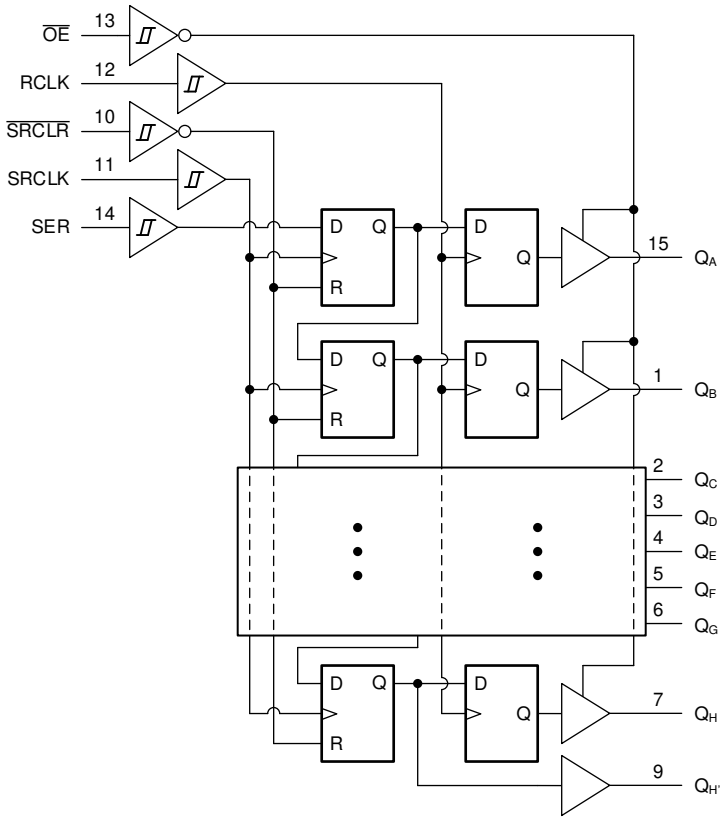


图 8-1. Logic Diagram (Positive Logic) for the SN74HCS595-Q1

8.2 Feature Description

8.2.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-State outputs. The three states that these outputs can be in are driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10 kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.2.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.2.3 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

8.2.4 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 图 8-2.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

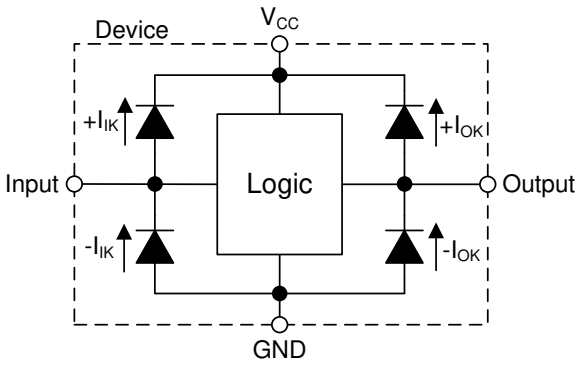


图 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.2.5 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

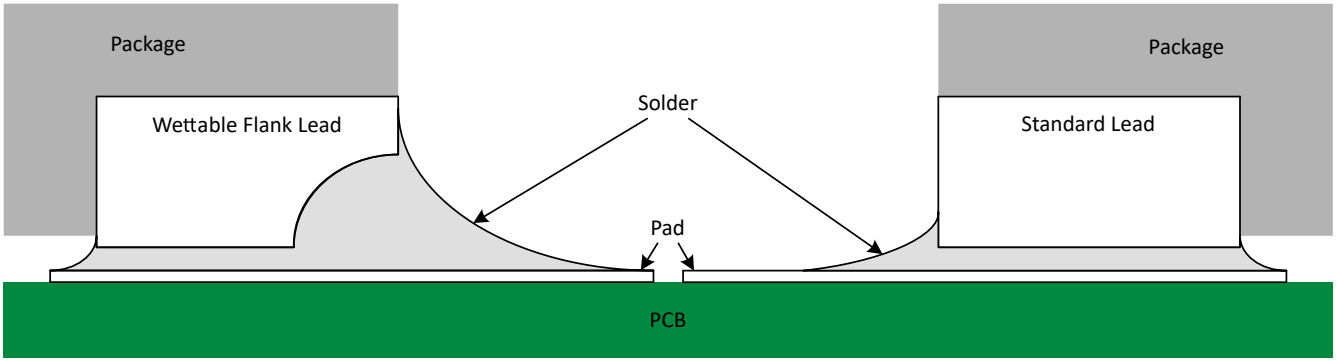


图 8-3. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering which makes QFN packages easier to inspect with automatic optical inspection (AOI). A wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet as shown in 图 8-3. Please see the mechanical drawing for additional details.

8.3 Device Functional Modes

Function Table lists the functional modes of the SN74HCS595-Q1.

表 8-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	H	↑	X	Shift-register data is stored in the storage register.
X	↑	H	↑	X	Data in shift register is stored in the storage register, the data is then shifted through.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

In this application, the SN74HCS595-Q1 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74HCS595-Q1 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

The OE pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the SN74HCS595-Q1 can be controlled accordingly to turn off all the outputs reducing the I/O needed to three. There is no practical limitation to how many SN74HCS595-Q1 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, the shift register needs to be cleared and then clocked into the output register. An RC can be connected to the $\overline{\text{SRCLR}}$ pin as shown in the Typical Application Block Diagram to initialize the shift register to all zeros. With the $\overline{\text{OE}}$ pin pulled up with a resistor, this process can be performed while the outputs are in a high impedance state eliminating any erroneous data causing issues with the displays.

9.2 Typical Application

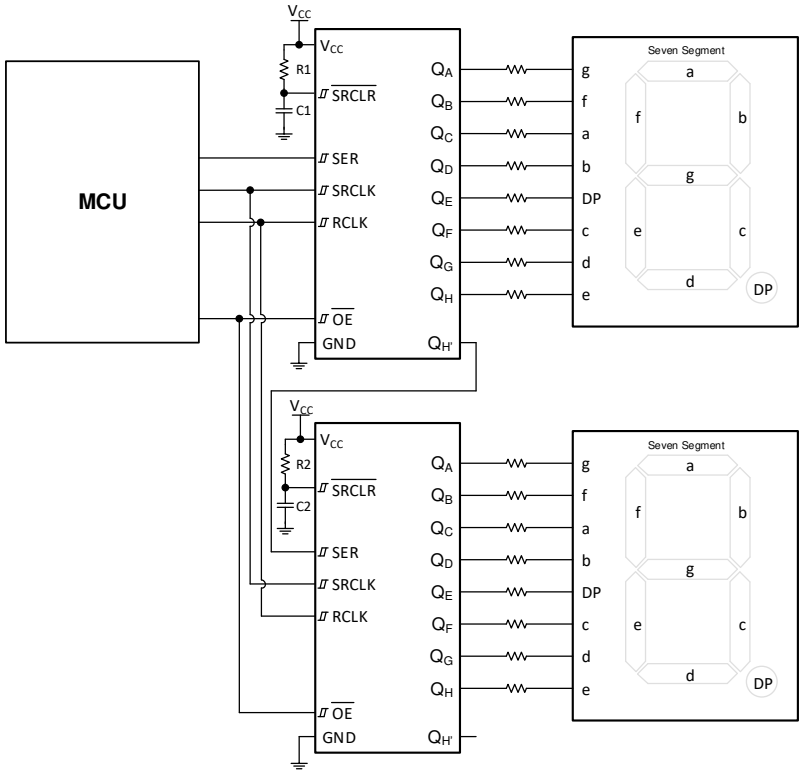


图 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

- All signals in the system operate at 5 V
- Avoid unstable state by not having LOW signals on both inputs
- Q output is HIGH when $\overline{S}$ is LOW
  - Q output remains HIGH until $\overline{R}$ is LOW

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS595-Q1 plus the maximum static supply current, I_{CC}, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS595-Q1 plus the maximum supply current, I_{CC}, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS595-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74HCS595-Q1 can drive a load with total resistance described by $R_L \geqslant V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS595-Q1, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS595-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is $\leq$ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS595-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.

9.2.3 Application Curve

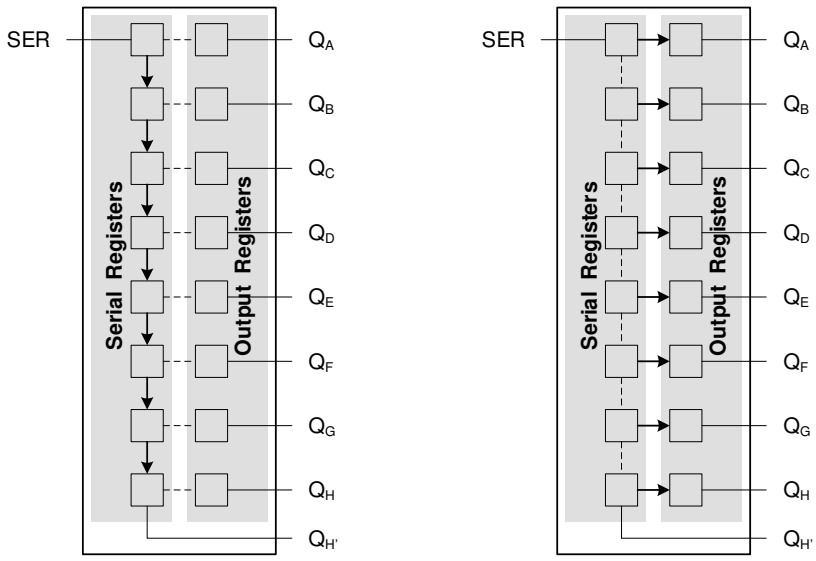


图 9-2. Simplified Functional Diagram Showing Clock Operation

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

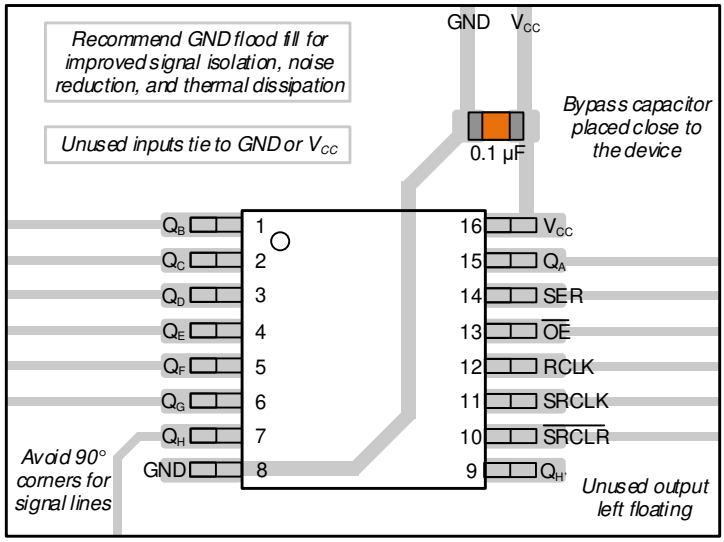


图 11-1. Example Layout for the SN74HCS595-Q1.

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *HCMOS Design Considerations* application report
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS595QBQBRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS595Q	Samples
SN74HCS595QDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595Q	Samples
SN74HCS595QDYYRQ1	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595Q	Samples
SN74HCS595QPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS595Q	Samples
SN74HCS595QWBQBRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS595Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74HCS595-Q1 :

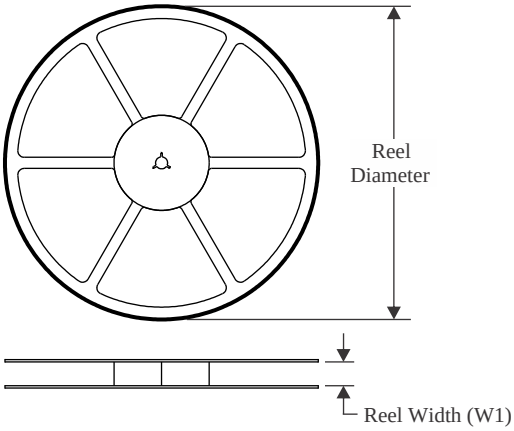
- Catalog : SN74HCS595

NOTE: Qualified Version Definitions:

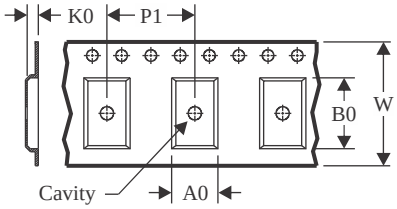
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

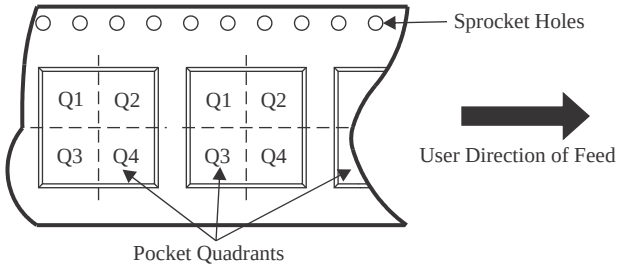


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

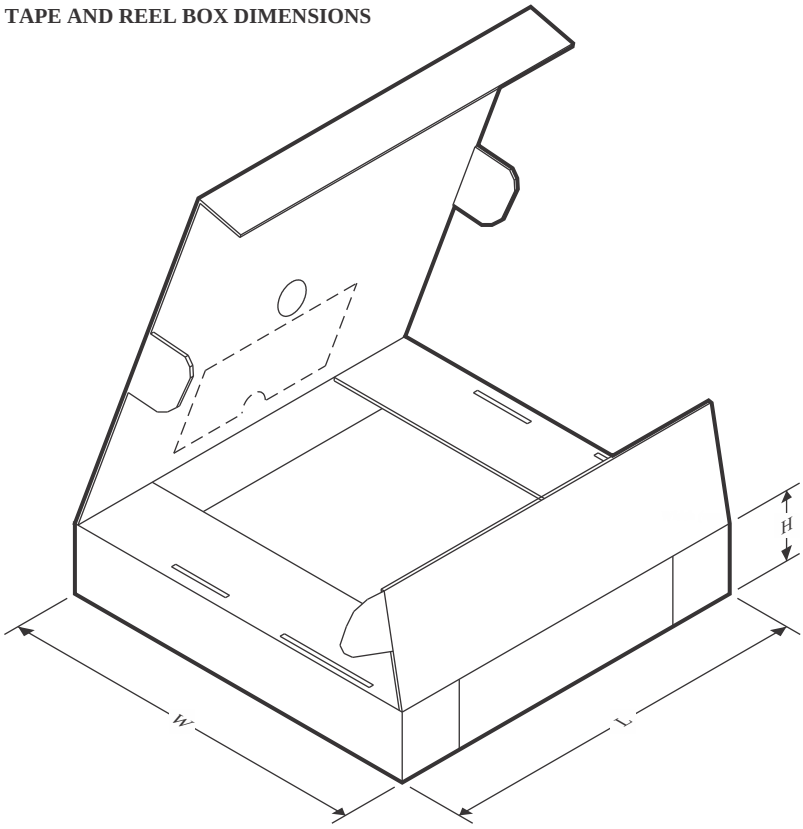
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS595QBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74HCS595QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCS595QDYYRQ1	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74HCS595QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS595QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

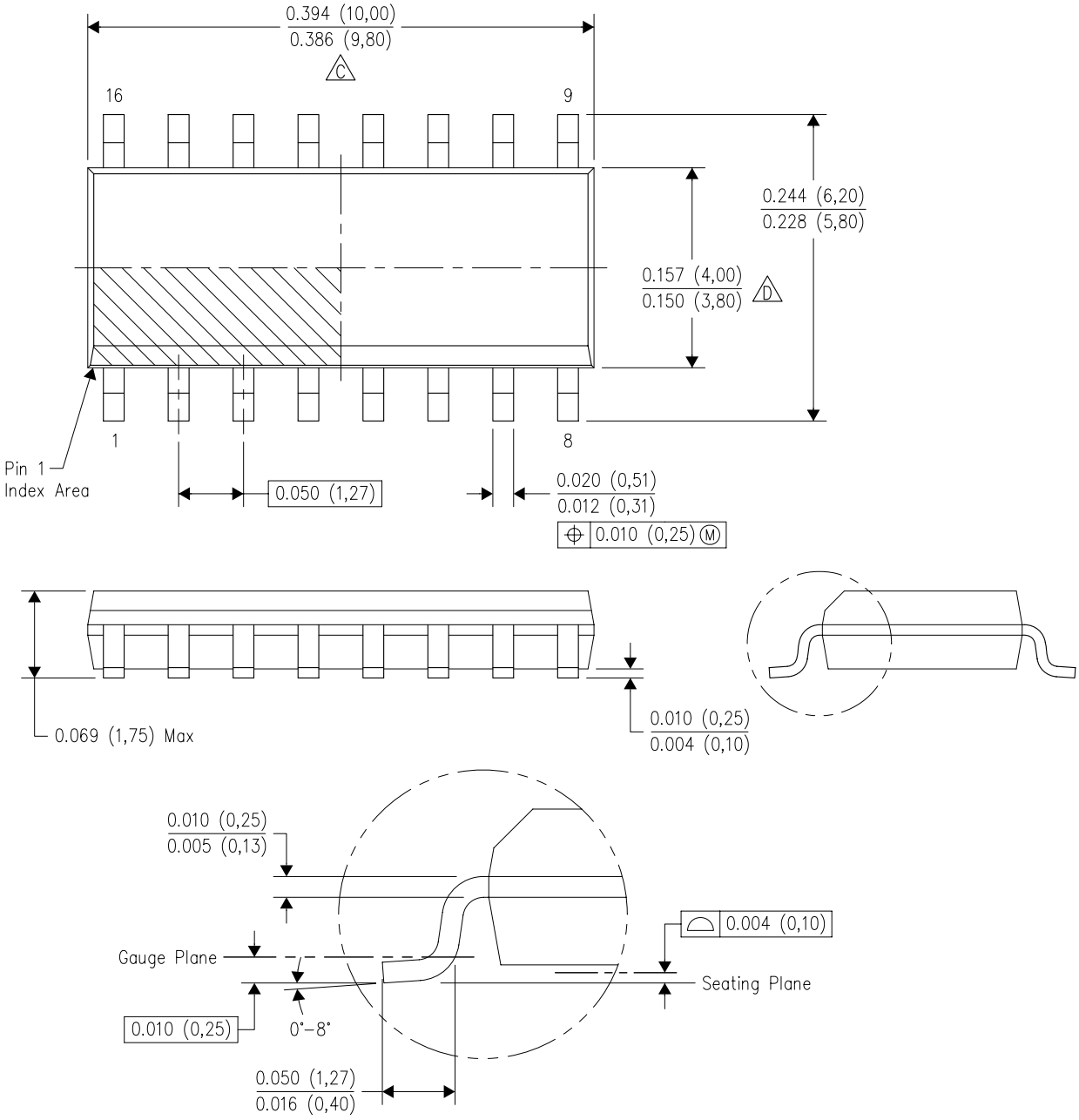
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS595QBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74HCS595QDRQ1	SOIC	D	16	2500	356.0	356.0	35.0
SN74HCS595QDYYRQ1	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
SN74HCS595QPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HCS595QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



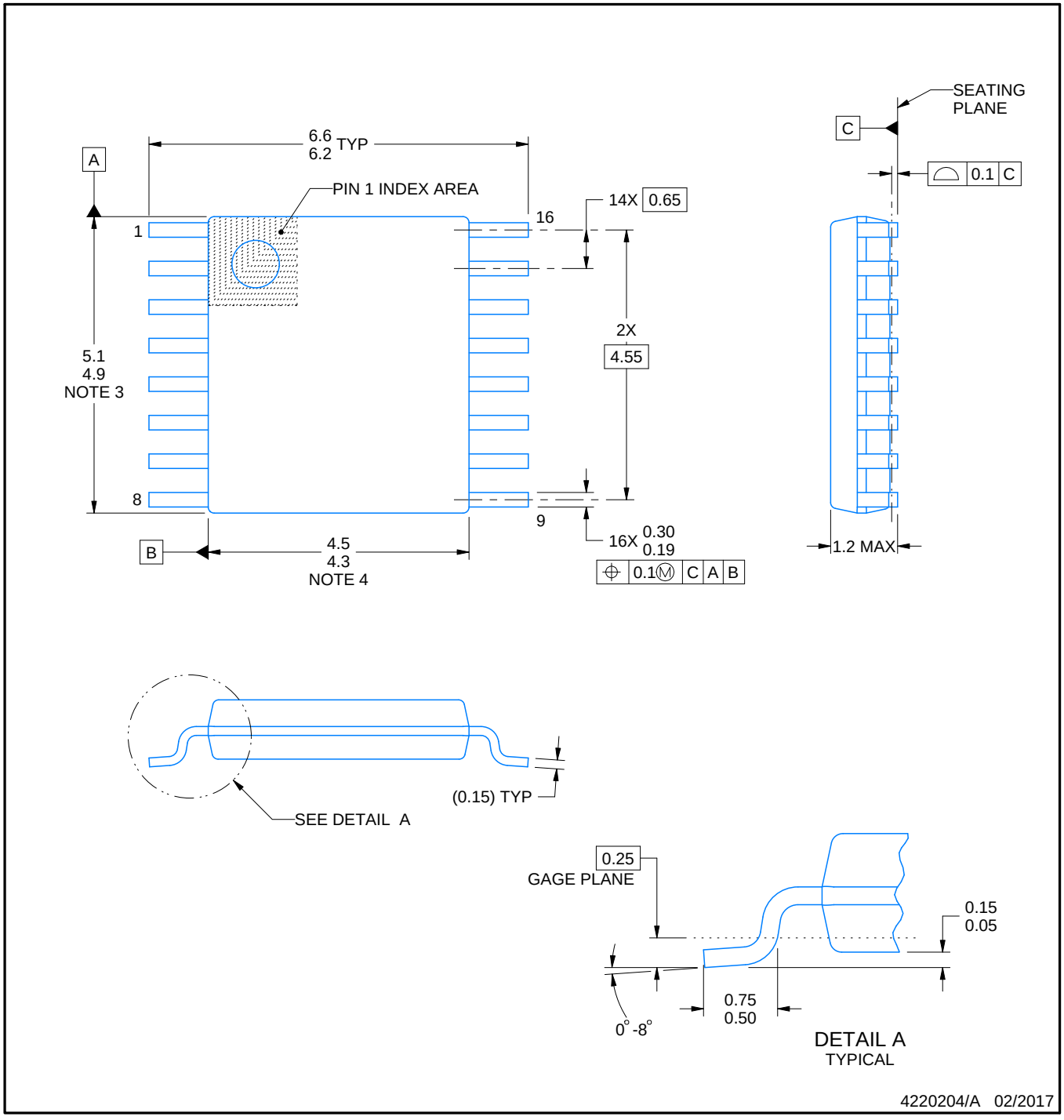
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

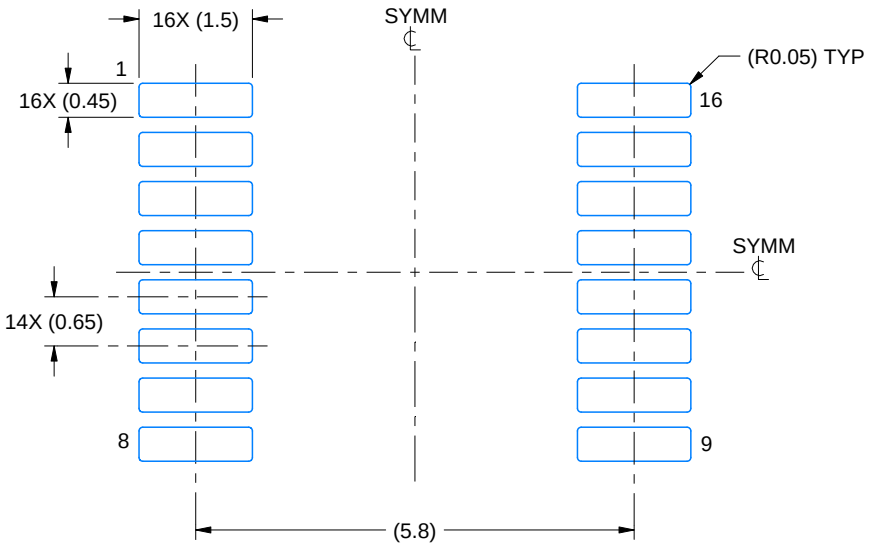
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

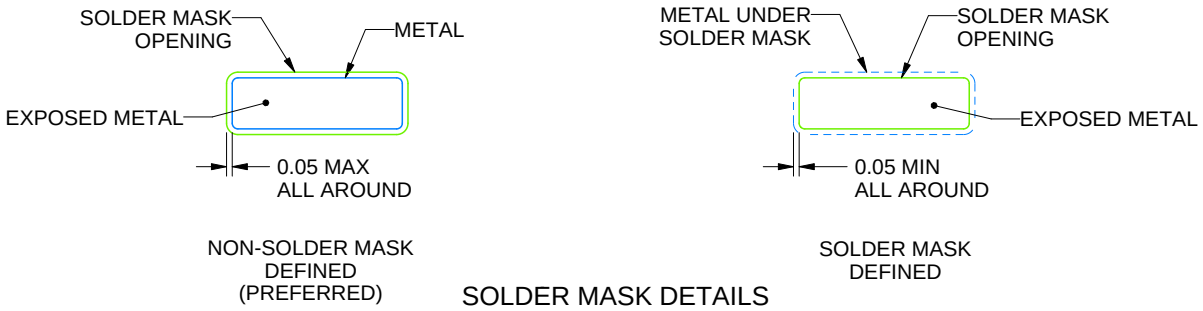


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

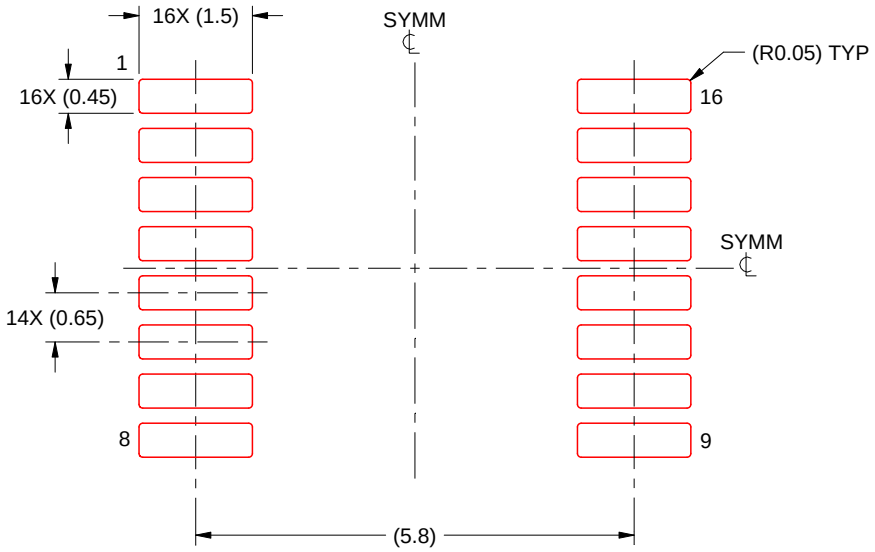


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

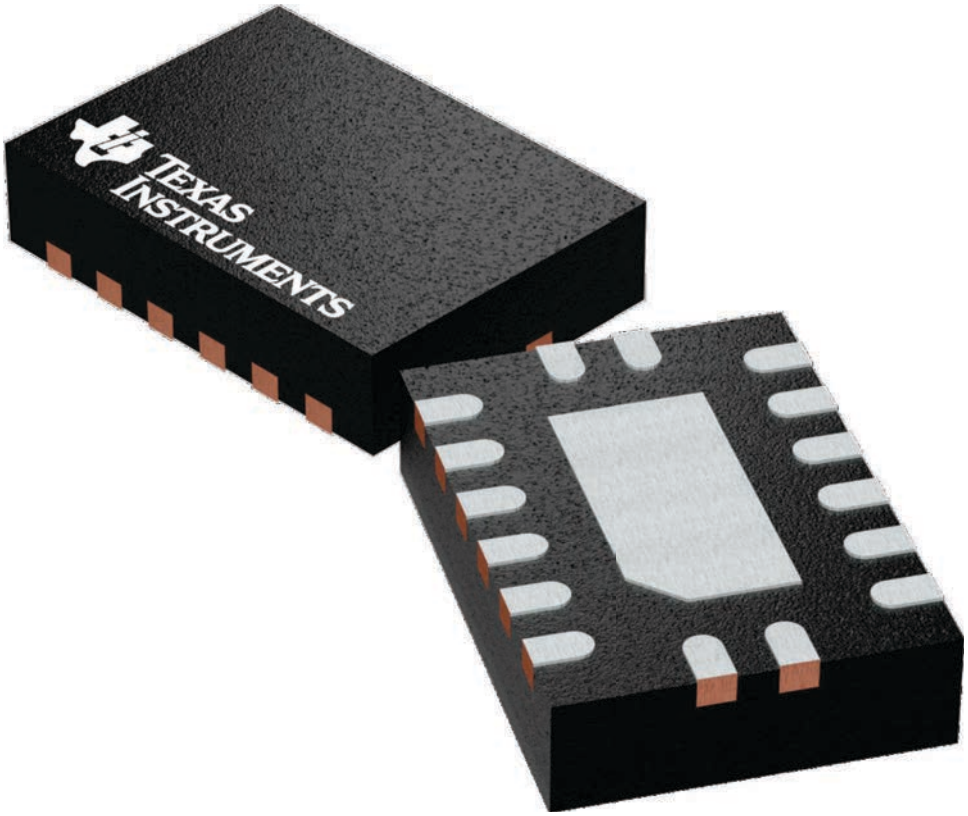
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



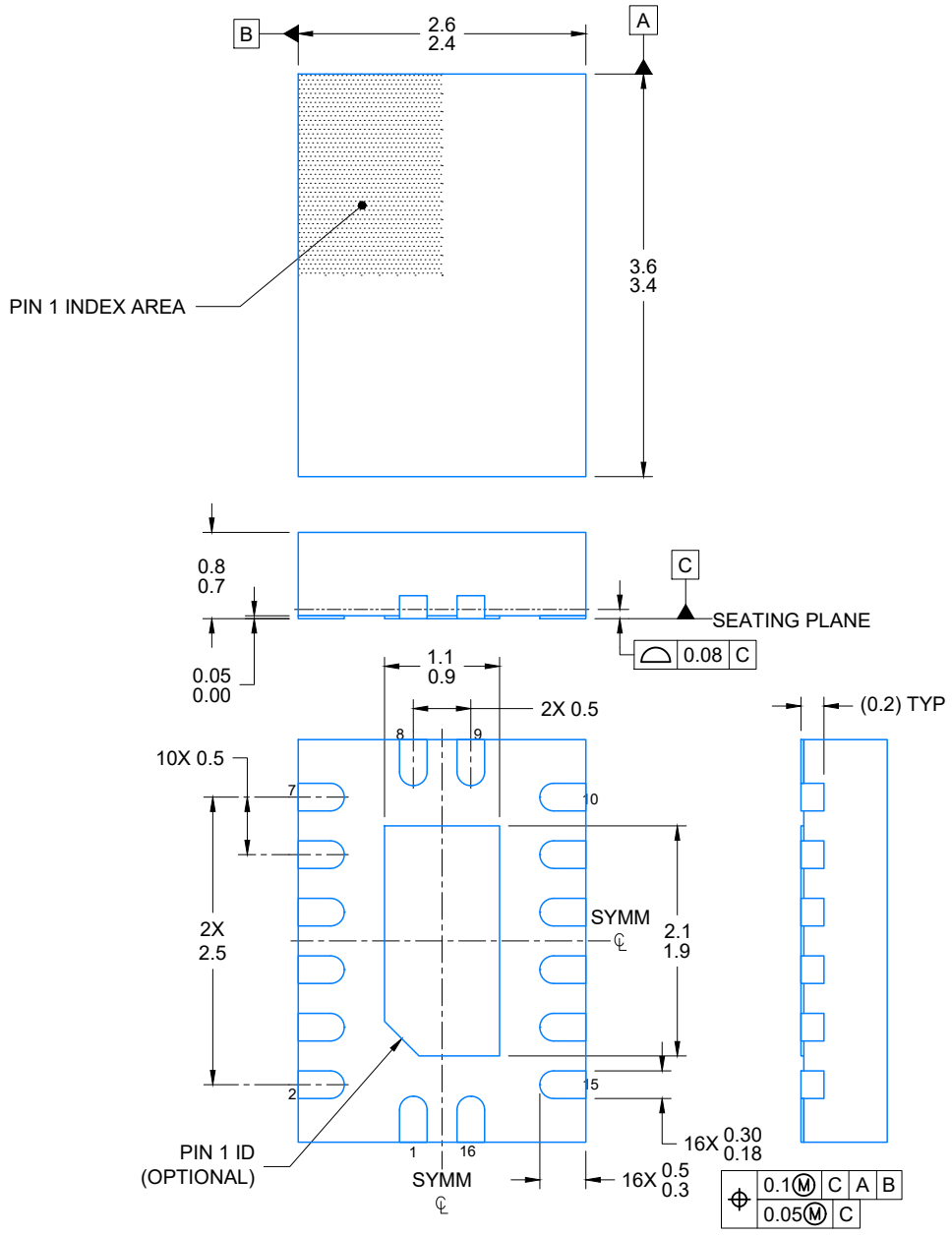
4226161/A

PACKAGE OUTLINE

BQB0016A

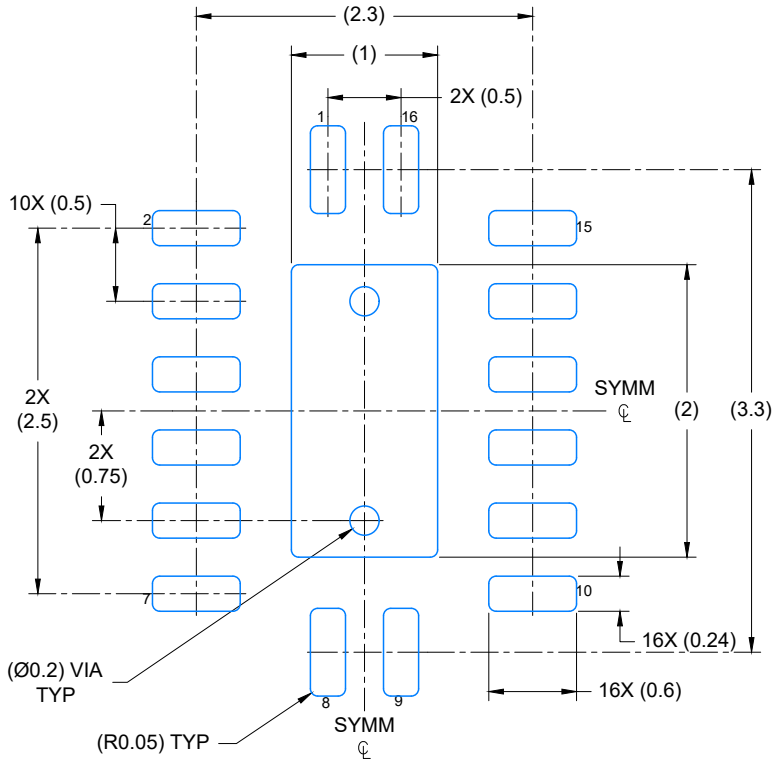
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

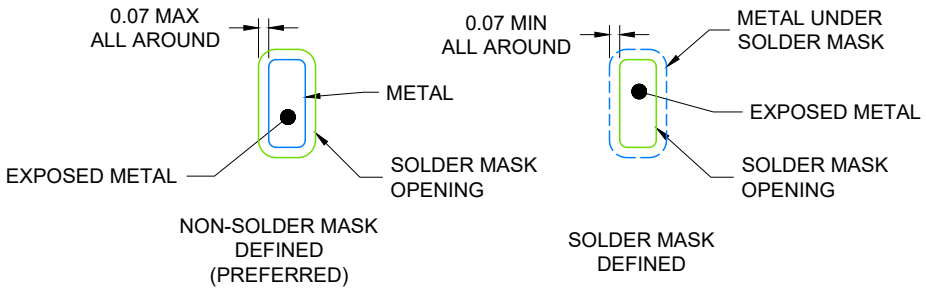


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



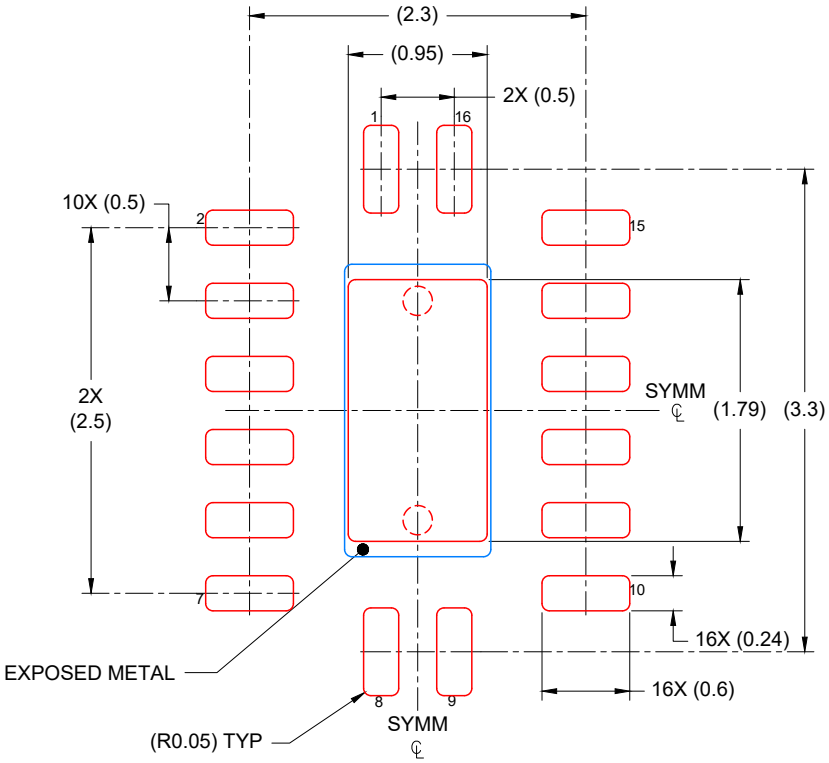
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

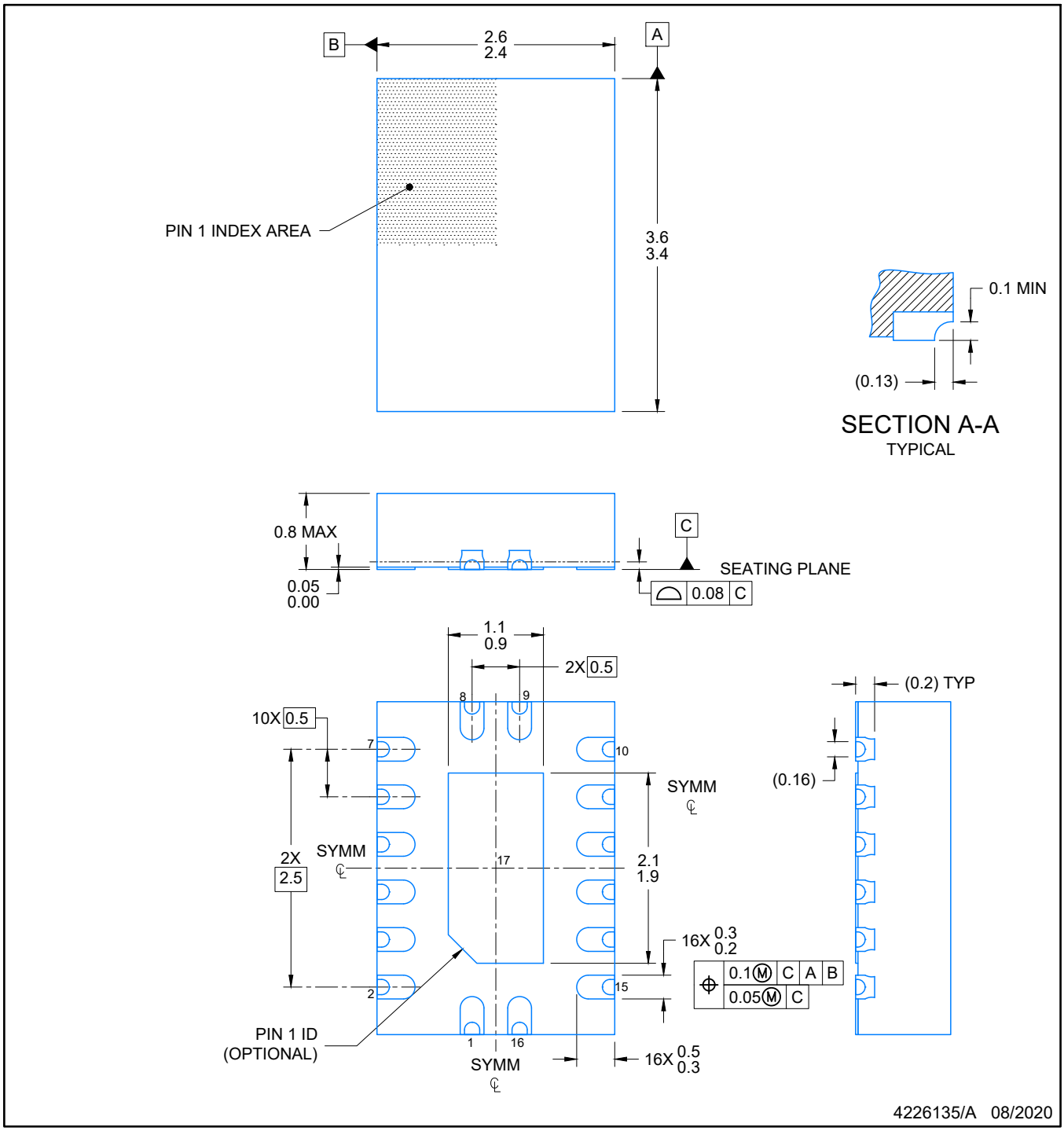
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

BQB0016B

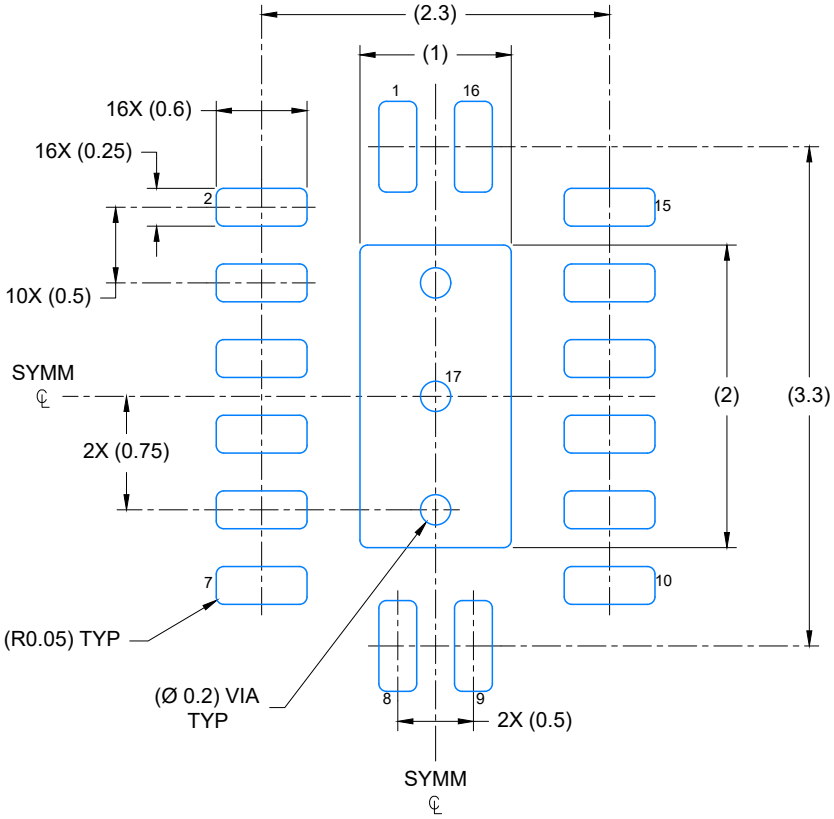
WQFN - 0.8 mm max height

INDSTNAME



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

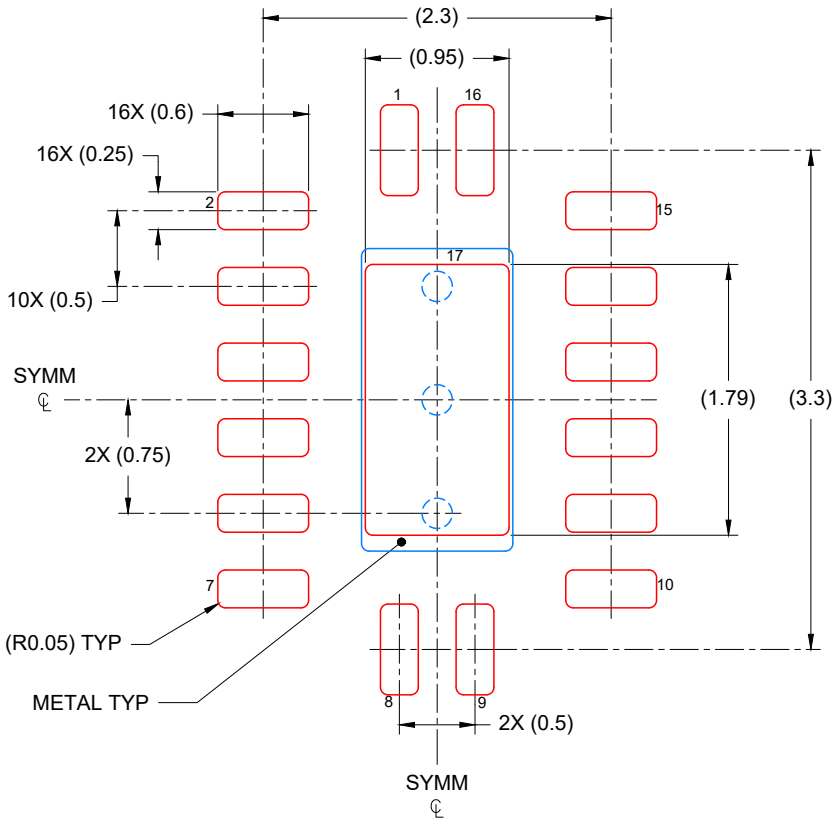


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

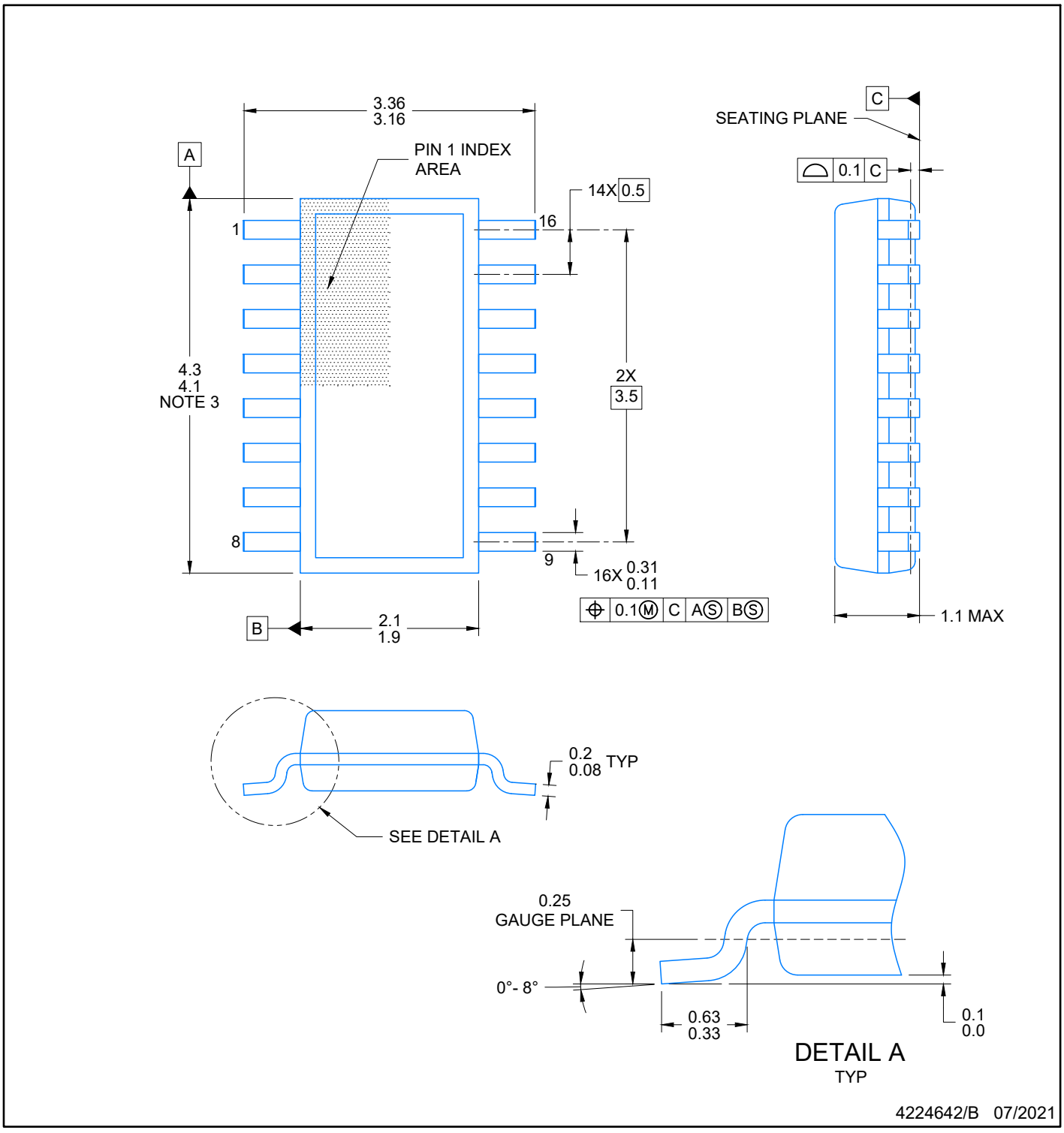
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0016A

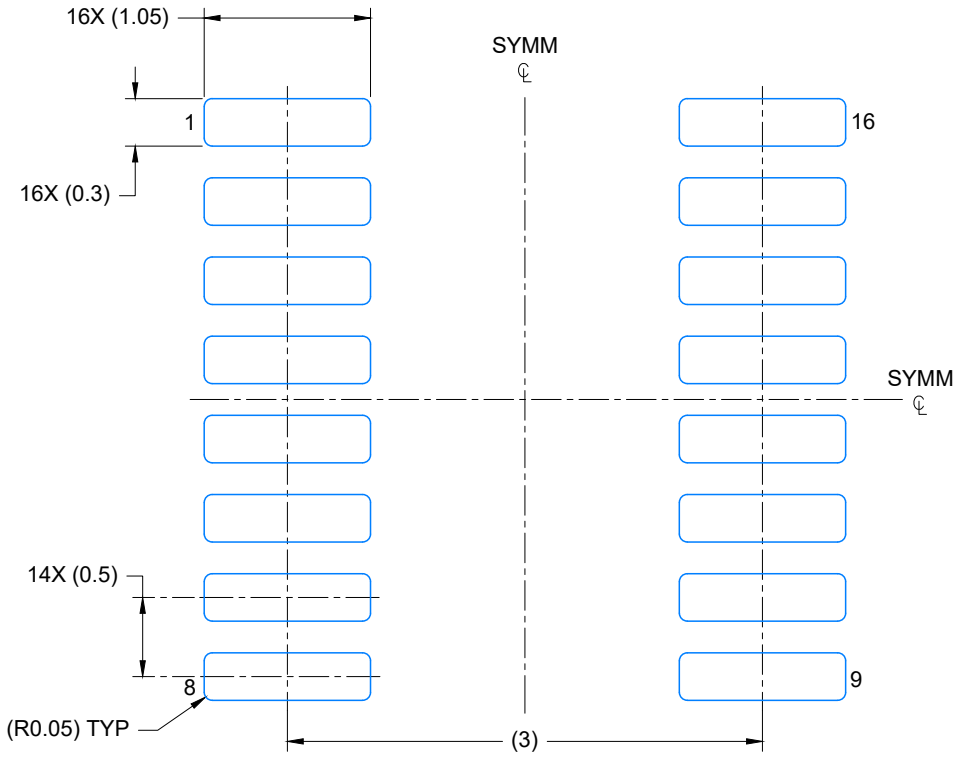
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

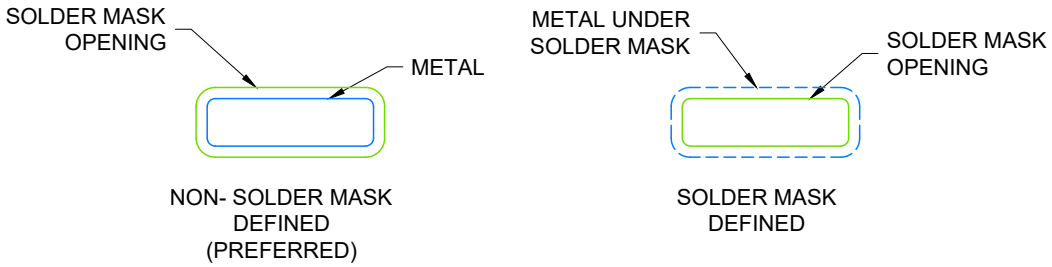


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

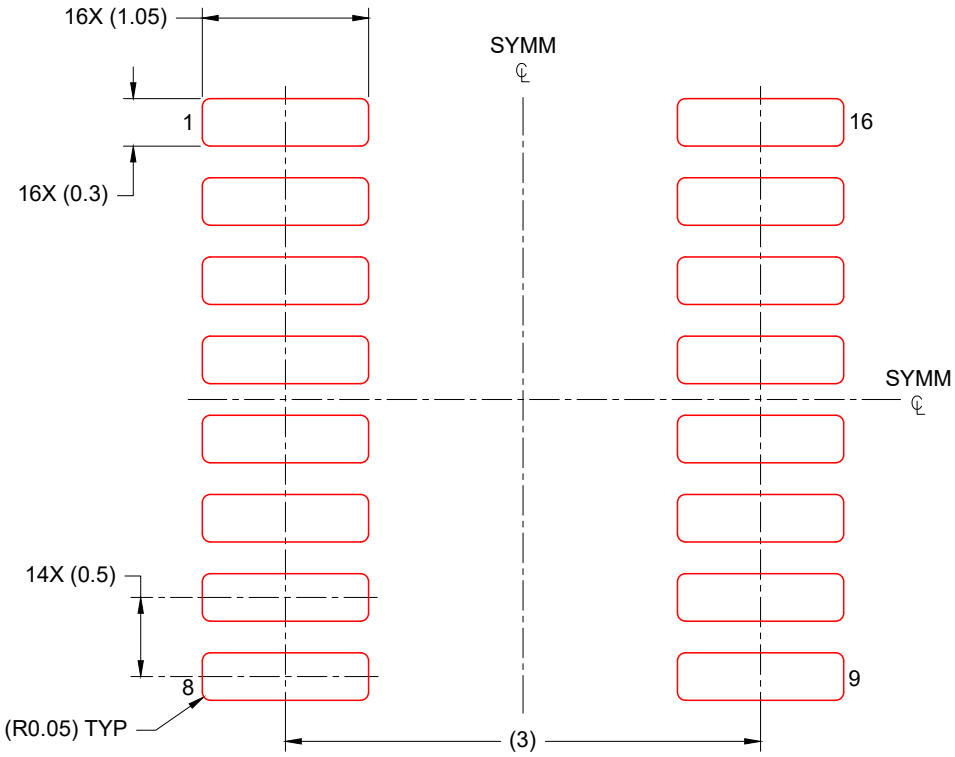


SOLDER MASK DETAILS

4224642/B 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/B 07/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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