SN74HC08-Q1 汽车类四路双输入与门

1 特性

- 符合AEC-Q100 标准，面向汽车 应用 ：
  - 器件温度等级 1：
    –40°C 至 +125°C，T_A
- 缓冲输入
- 正负输入钳位二极管
- 宽工作电压范围：2V 至 6V
- 支持高达 10 个 LSTTL 负载的扇出
- 与 LSTTL 逻辑 IC 相比，可显著降低功耗

2 应用

- 将电源正常信号进行结合
- 启动数字信号

3 说明

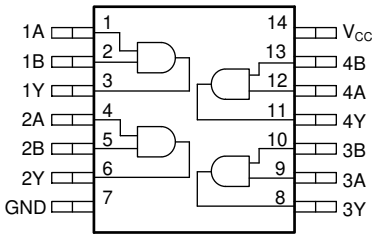
此器件包含四个独立双输入与门。每个逻辑门以正逻辑执行布尔函数 Y = A ● B。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74HC08QDRQ1	SOIC (14)	8.70mm × 3.90mm
SN74HC08QPWRQ1	TSSOP (14)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

SN74HC08-Q1 的功能引脚



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

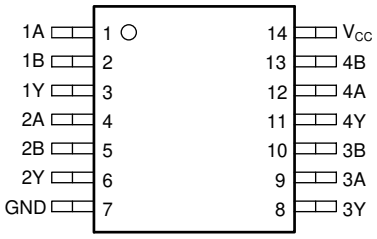
Changes from Revision C (February 2008) to Revision D **Page**

- 更新至全新数据表标准 ... 1
- 从数据表中删除了涉及 D 封装的内容，因为该封装不可用 ... 1
- Deleted Q version of device from Electrical Specifications as it is no longer available ... 4
- Changed $R_{\theta JA}$ for PW package from 113 °C/W to 151.7 °C/W ... 4
- Changed $R_{\theta JA}$ for D package from 86 °C/W to 133.6 °C/W ... 4

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5 Pin Configuration and Functions

D or PW Package
14-Pin SOIC or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
V_{CC}	14	—	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1) HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall rate	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	SN74HC08I-Q1	–40		85	°C

6.4 Thermal Information

THERMAL METRIC		SN74HC08-Q1		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	89.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	89.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	45.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	89.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

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6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	Operating free-air temperature (T_A)						UNIT
					25°C			-40°C to 85°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 µA	2 V	1.9	1.998		1.9			V
				4.5 V	4.4	4.499		4.4			
				6 V	5.9	5.999		5.9			
			I_{OH} = -4 mA	4.5 V	3.98	4.3		3.84			
			I_{OH} = -5.2 mA	6 V	5.48	5.8		5.34			
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1			0.1	V
				4.5 V		0.001	0.1			0.1	
				6 V		0.001	0.1			0.1	
			I_{OL} = 4 mA	4.5 V		0.17	0.26			0.33	
			I_{OL} = 5.2 mA	6 V		0.15	0.26			0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V		±0.1	±100			±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0	I_O = 0	6 V			2			20	µA
C_i	Input capacitance			2 V to 6 V		3	10			10	pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM	TO	V_{CC}	Operating free-air temperature (T_A)						UNIT
					25°C			–40°C to 85°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A or B	Y	2 V		50	100			125	ns
				4.5 V		10	20			25	
				6 V		8	17			21	
t_t	Transition-time		Y	2 V		38	75			95	ns
				4.5 V		8	15			19	
				6 V		6	13			16	

6.7 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load		20		pF

6.8 Typical Characteristics

T_A = 25°C

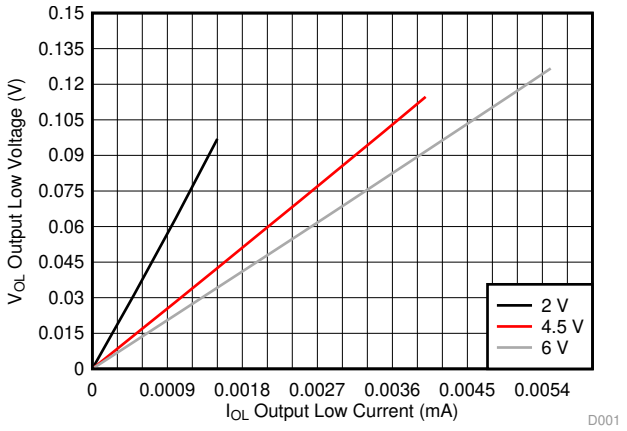


图 1. Output voltage versus output current in low state

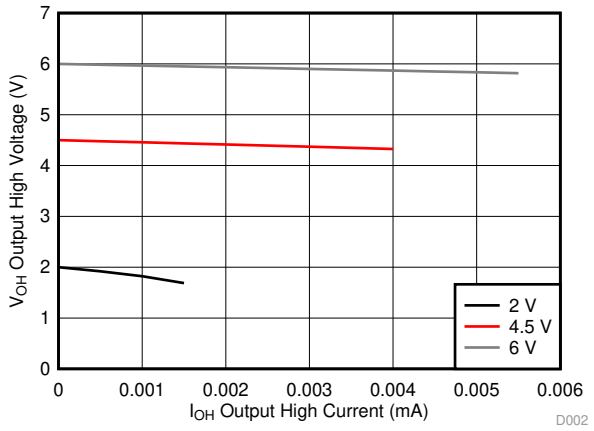
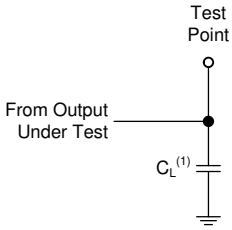


图 2. Output voltage versus output current in high state

7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.
- The outputs are measured one at a time, with one input transition per measurement.



C_L= 50 pF and includes probe and jig capacitance.

图 3. Load Circuit

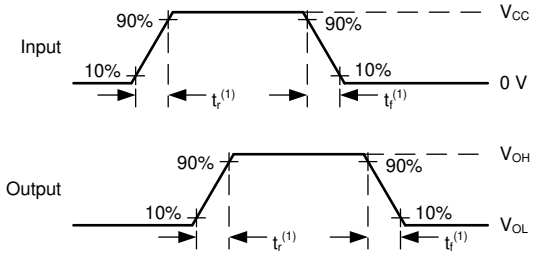
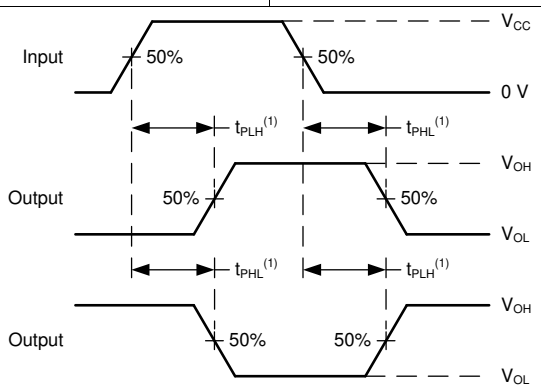


图 4. Voltage Waveforms Transition Times



The maximum between t_{PLH} and T_{PHL} is used for t_{pd}.

图 5. Voltage Waveforms Propagation Delays

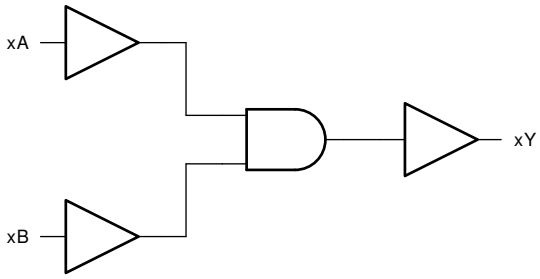
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8 Detailed Description

8.1 Overview

This device contains four independent 2-input AND gates. Each gate performs the Boolean function Y = A ● B in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The SN74HC08-Q1 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the *Absolute Maximum Ratings*.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

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Feature Description (接下页)

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 图 6.

CAUTION

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

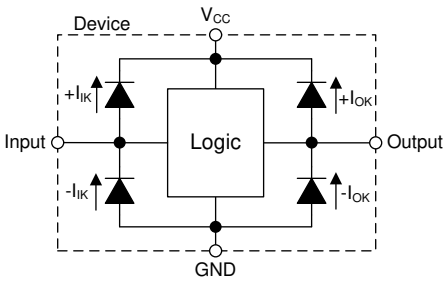


图 6. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 1. Function Table

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in 图 7. The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SN74HC08-Q1 is used to directly control the RESET pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

9.2 Typical Application

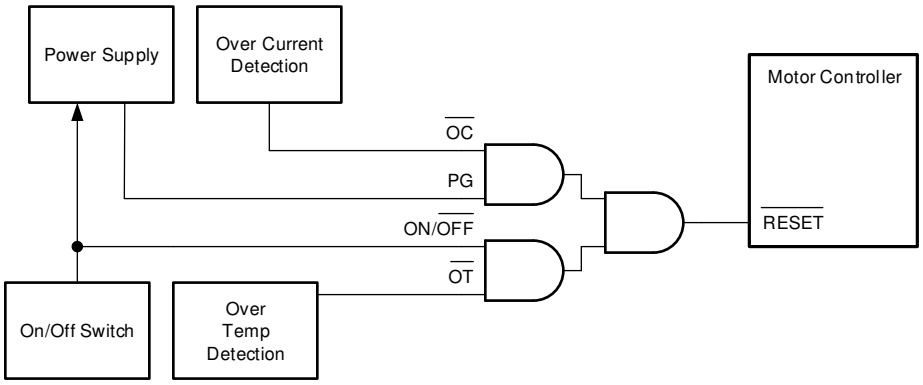


图 7. Typical application block diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HC08-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *Absolute Maximum Ratings*.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and C_{pd} Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

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Typical Application (接下页)

CAUTION

The maximum junction temperature, T_J(max) listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC08-Q1, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HC08-Q1 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions*.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout*.
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC08-Q1 to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / I_O(max)) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

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Typical Application (接下页)

9.2.3 Application Curves

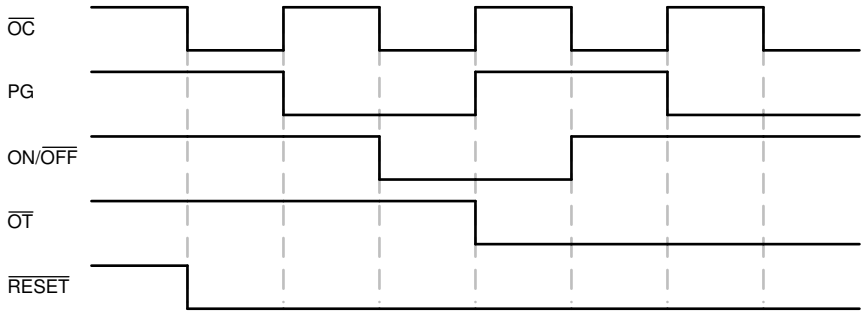


图 8. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in 图 9.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

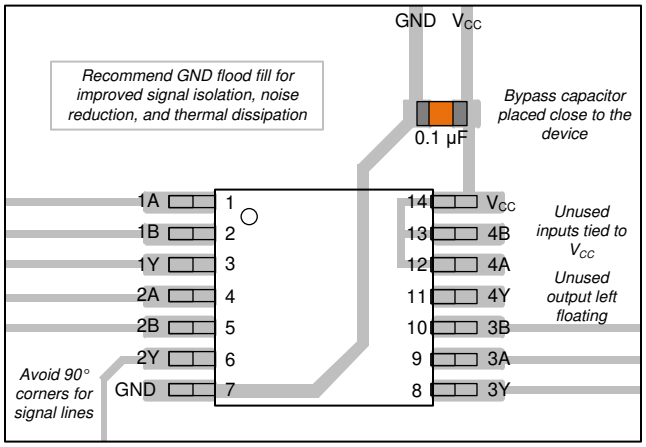


图 9. Example layout for the SN74HC08-Q1

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12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 《HCMOS 设计注意事项》
- 《CMOS 功耗与 CPD 计算》
- 《使用逻辑器件进行设计》

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

12.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC08IPWRG4Q1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08I
SN74HC08IPWRG4Q1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08I
SN74HC08IPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC08I
SN74HC08IPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08I
SN74HC08QDRG4Q1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC08Q1
SN74HC08QDRG4Q1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC08Q1
SN74HC08QDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC08Q1
SN74HC08QDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC08Q1
SN74HC08QPWRG4Q1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC08Q1
SN74HC08QPWRG4Q1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC08Q1
SN74HC08QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HC08Q1
SN74HC08QPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC08Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74HC08-Q1 :

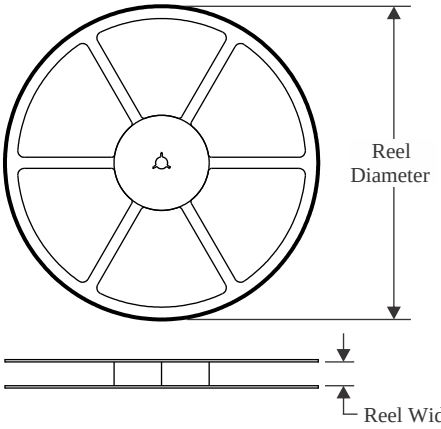
- Catalog : SN74HC08
- Military : SN54HC08

NOTE: Qualified Version Definitions:

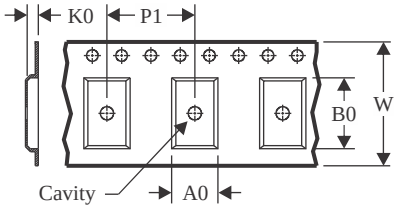
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

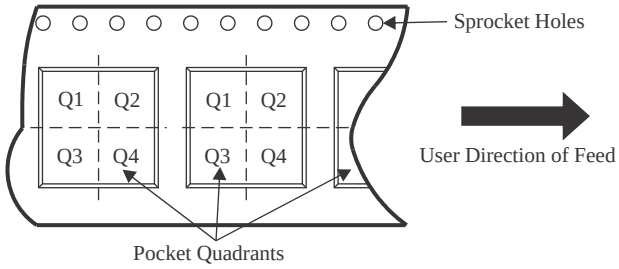


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

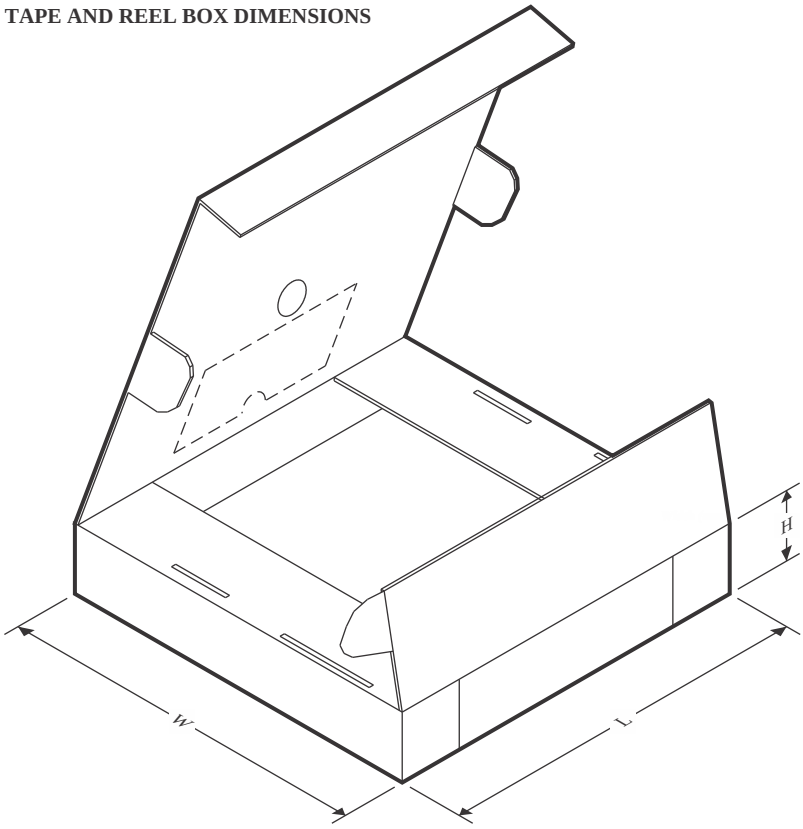
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC08IPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC08IPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC08IPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC08QDRG4Q1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC08QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC08QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC08QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

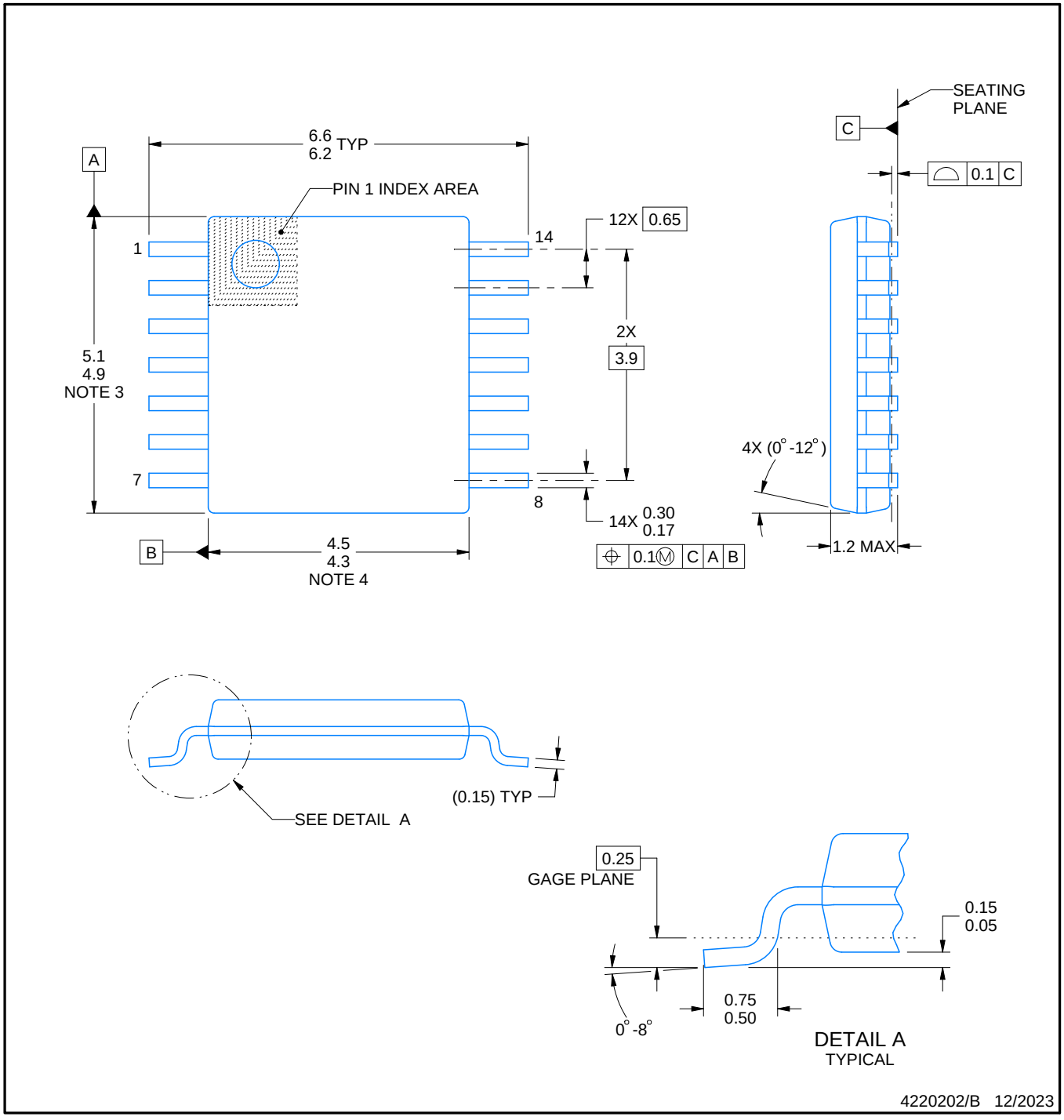
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC08IPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74HC08IPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74HC08IPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HC08QDRG4Q1	SOIC	D	14	2500	353.0	353.0	32.0
SN74HC08QDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
SN74HC08QPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74HC08QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0014A

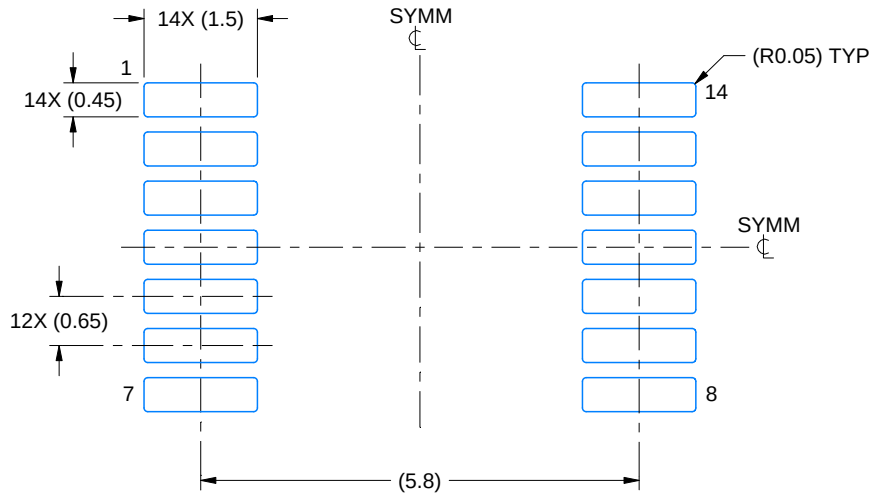
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

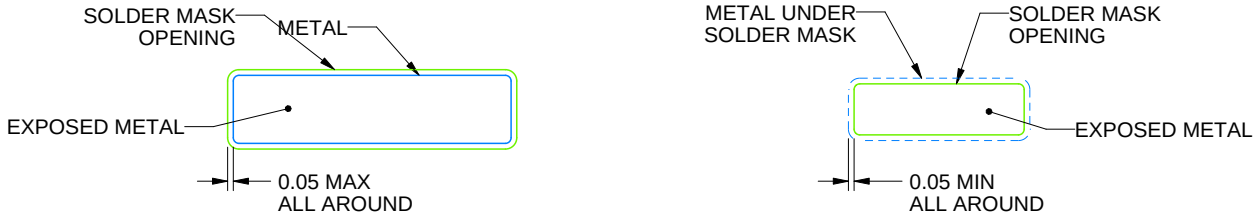


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

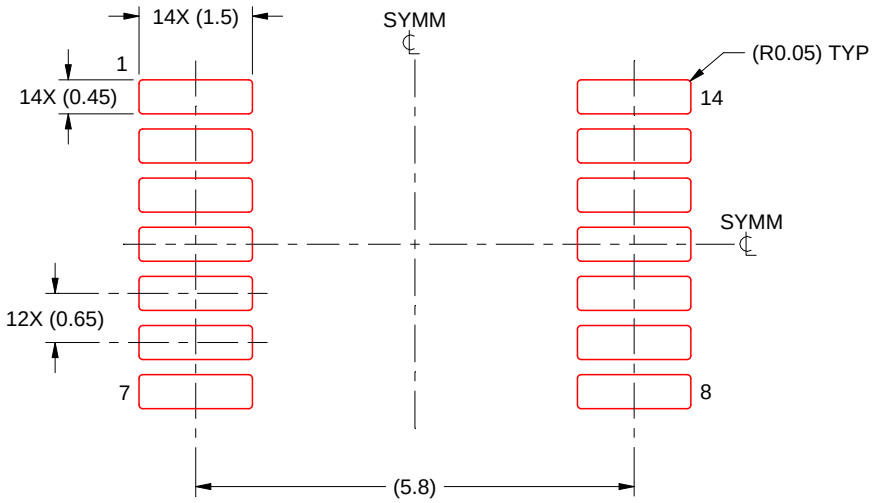


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

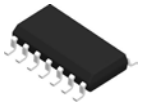


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

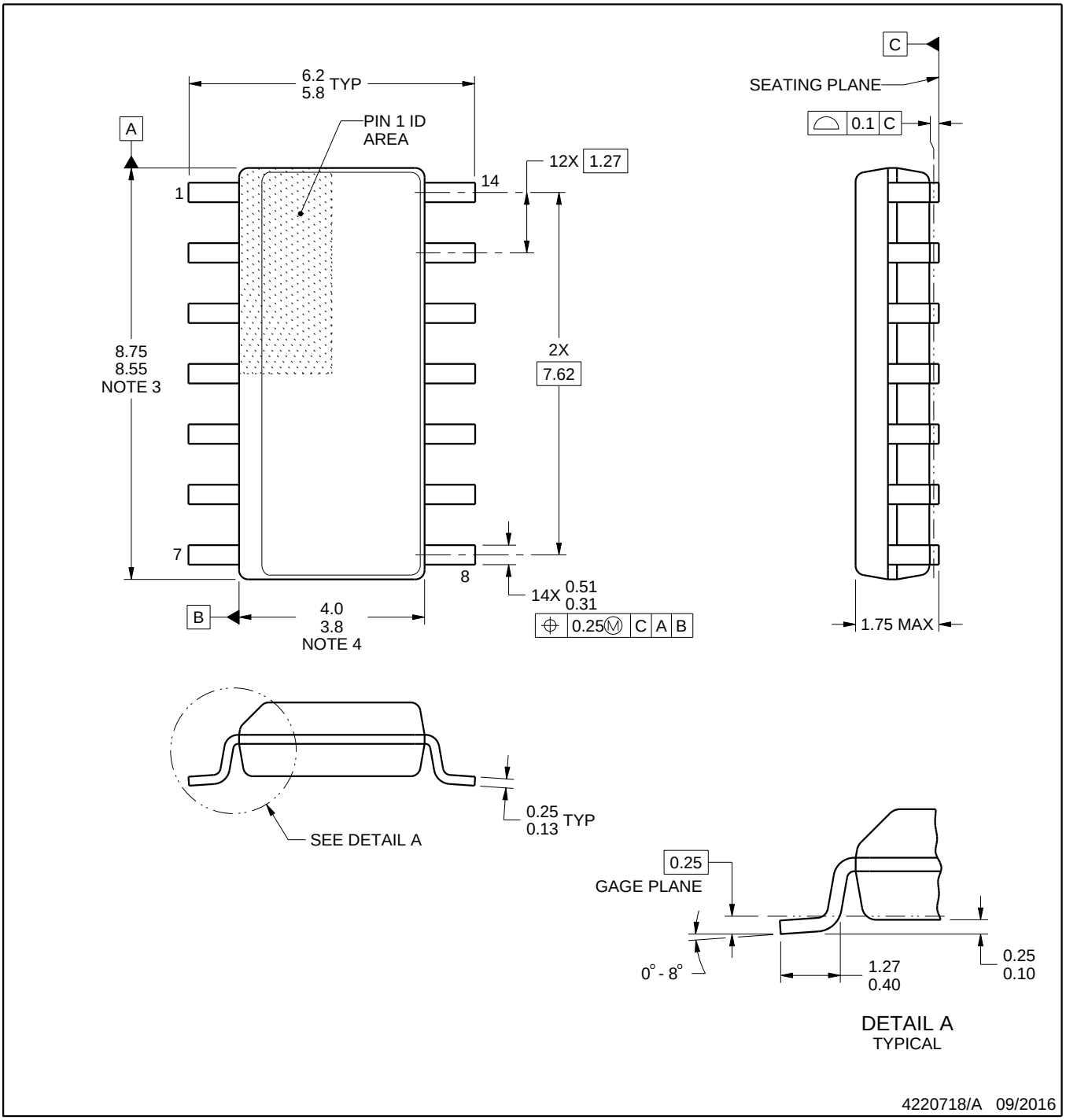


PACKAGE OUTLINE

D0014A

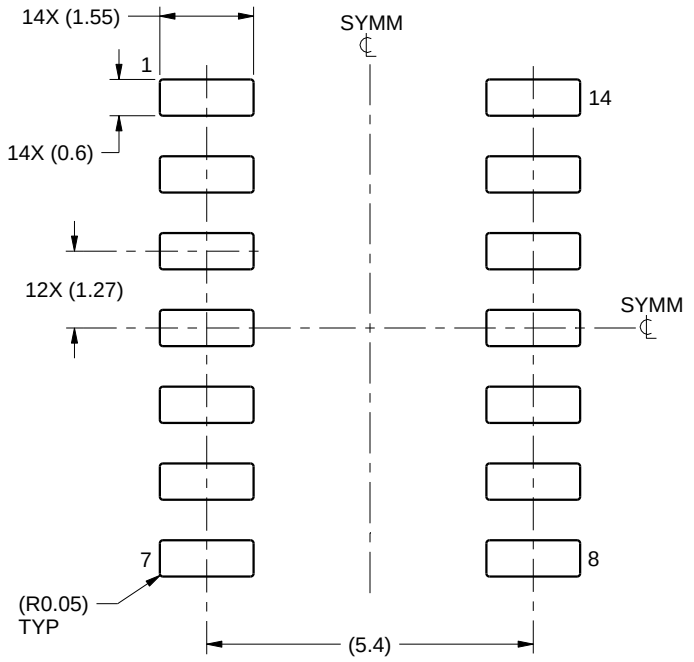
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

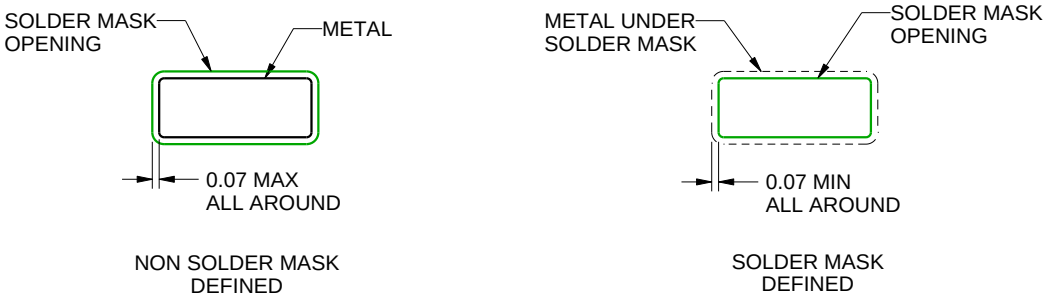


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

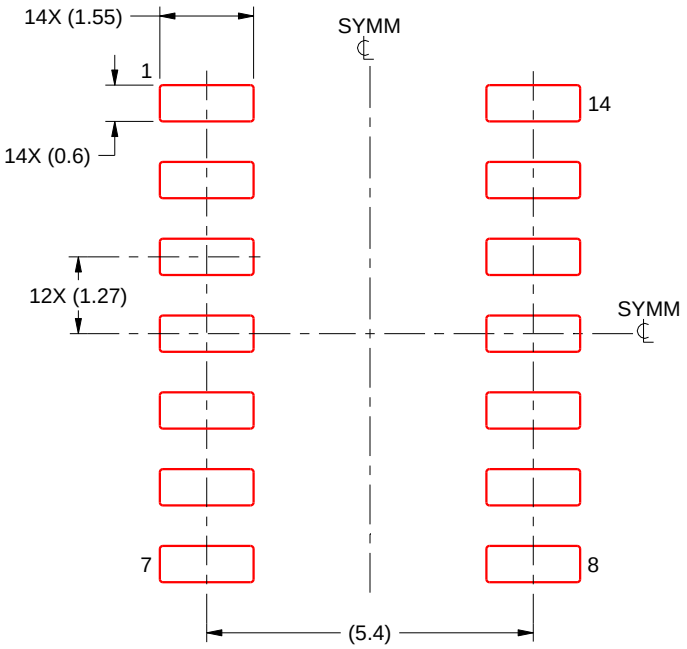
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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