SN74CBTLV3383 低电压 10 位 FET 总线交换开关

1 特性

- 两个端口间使用 5Ω 开关连接
- 支持在数据 I/O 端口进行轨至轨开关
- I_{off} 支持局部断电模式运行
- 锁存性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超出 JESD 22 标准
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器模型 (A115-A)

2 应用

- 游戏
- 机架式服务器
- 通信板

3 说明

SN74CBTLV3383 可提供十位高速总线开关或交换。此开关具有低通态电阻，可以在最短传播延迟情况下建立连接。

该器件作为 10 位总线开关或 5 位总线交换器运行，可将 A 对信号和 B 对信号进行交换。总线交换功能会在 BX 高、$\overline{BE}$ 低时选中。

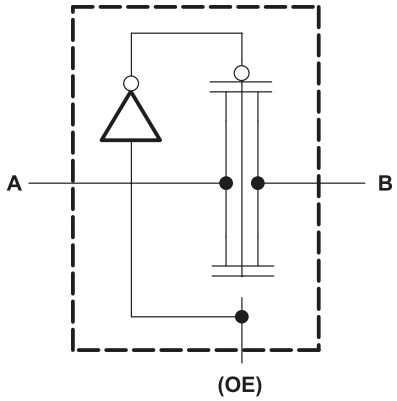
该器件完全 适用于 使用 I_{off} 的局部断电应用。I_{off} 特性确保在关断时防止损坏电流通过器件回流。该器件可在关断时提供隔离。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74CBTLV3383	QSOP – DBQ	8.65mm x 3.90mm
	SOIC – DW	15.4mm x 7.50mm
	TSSOP – PW	7.80mm x 4.40mm
	TVSOP – DGV	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

每个 **FET** 开关的简化原理图



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4 修订历史记录

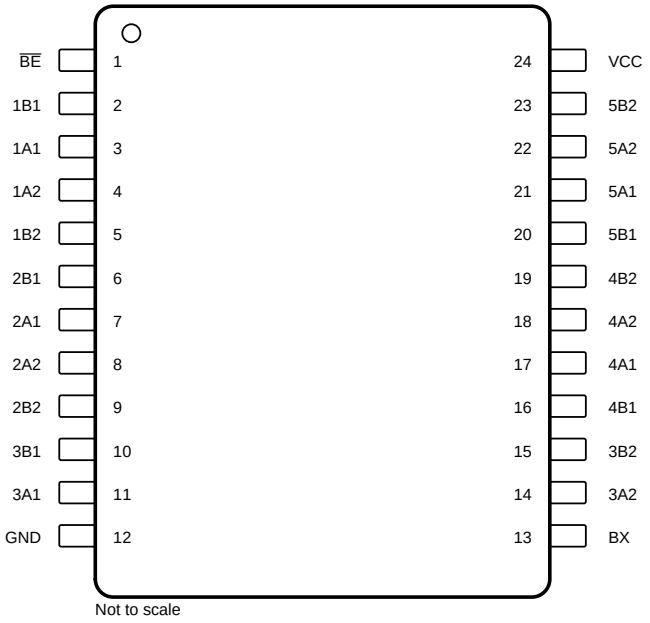
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (October 2003) to Revision H **Page**

- 添加了*器件信息* 表、*ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1

5 Pin Configuration and Functions

DBQ, DGV, DW, OR PW Package
24-Pin
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{BE}$	1	I	Active low enable: When this pin is high, all switches are turned off. When this pin is low, BX pin controls the signal path selection.
1B1	2	I/O	Signal path. Can be an input or output
1A1	3	I/O	Signal path. Can be an input or output
1A2	4	I/O	Signal path. Can be an input or output
1B2	5	I/O	Signal path. Can be an input or output
2B1	6	I/O	Signal path. Can be an input or output
2A1	7	I/O	Signal path. Can be an input or output
2A2	8	I/O	Signal path. Can be an input or output
2B2	9	I/O	Signal path. Can be an input or output
3B1	10	I/O	Signal path. Can be an input or output
3A1	11	I/O	Signal path. Can be an input or output
GND	12	P	Ground (0V) reference
BX	13	I	Controls state of switches
3A2	14	I/O	Signal path. Can be an input or output
3B2	15	I/O	Signal path. Can be an input or output
4B1	16	I/O	Signal path. Can be an input or output
4A1	17	I/O	Signal path. Can be an input or output
4A2	18	I/O	Signal path. Can be an input or output
4B2	19	I/O	Signal path. Can be an input or output
5B1	20	I/O	Signal path. Can be an input or output
5A1	21	I/O	Signal path. Can be an input or output
5A2	22	I/O	Signal path. Can be an input or output
5B2	23	I/O	Signal path. Can be an input or output
V_{CC}	24	P	Positive power supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	4.6	V
V_I	Input voltage range	–0.5	4.6	V
	Continuous channel current .		128	mA
I_{IK}	Input clamp current, $V_{I/O} < 0$		–50	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.3		3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7			V
		V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V			0.7	V
		V_{CC} = 2.7 V to 3.6 V			0.8	V
T_A	Operating free-air temperature		–40		85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

THERMAL METRIC(1)		SN74CBTLV3383				UNIT
		DBQ (QSOP)	DVG (TVSOP)	DW (SPIC)	PW (TSSOP)	
		24 PINS	24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.6	105.6	66.6	90.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.5	36.9	36.7	34.12	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.8	51.1	36.6	45.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.8	2.6	13.1	2.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.4	50.6	36.4	44.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}	Clamp current	V_{CC} = 3 V	I_I = –18 mA				–1.2	V
I_I	Input current	V_{CC} = 3.6 V	V_I = V_{CC} or GND		–1		1	µA
I_{off}	Partial power down mode operation	V_{CC} = 0 V	V_I or V_{IO} = 0 to 3.6 V				10	µA
I_{CC}	Supply current	V_{CC} = 3.6	I_O = 0, V_I = V_{CC} or GND				10	µA
ΔI_{CC}(2)	Supply current - Control inputs	V_{CC} = 3.6 V	One input at 3V	Other inputs at VCC or GND			300	µA
C_I	Input Capacitance - Control inputs	V_I = 3 V or 0				3.5		pF
$C_{IO(OFF)}$	Input to output capacitance	V_O = 3 V or 0	$\overline{BE}$ = V_{CC}			13.5		pF
$r_{(on)}$(3)	On-state resistance	V_{CC} = 2.3 V TYP at VCC = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	Ω
			V_I = 1.7 V	I_I = 15 mA		27	40	Ω
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 24 mA		5	7	Ω
			V_I = 2.4 V	I_I = 15 mA		10	15	Ω

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C
(2) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

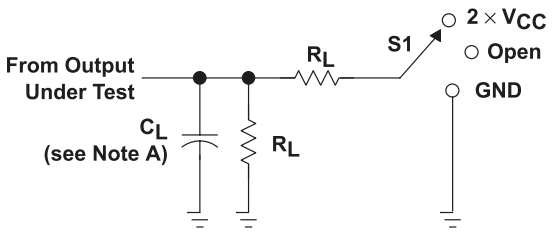
6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	MIN	MAX	
t_{pd} (1)	Propagation delay time	A or B	Bo or A		0.15		0.25	ns
t_{pd}	Propagation delay time	BX	A or B	1.5	5.8	1.5	4.7	ns
t_{en}	Enable time	$\overline{BE}$	A or B	1.5	5.3	1.5	4.7	ns
t_{dis}	Disable time	$\overline{BE}$	A or B	1	6	1	6	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V

图 1. Load Current

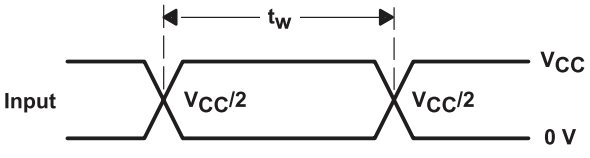


图 2. Voltage Waveforms Pulse Duration

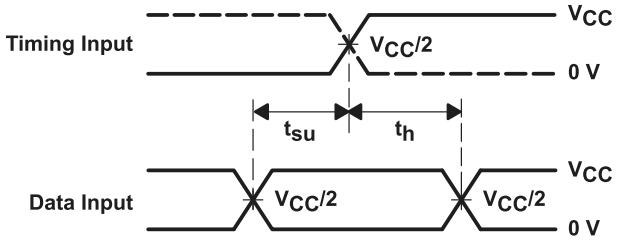


图 3. Voltage Waveforms Setup and Hold Times

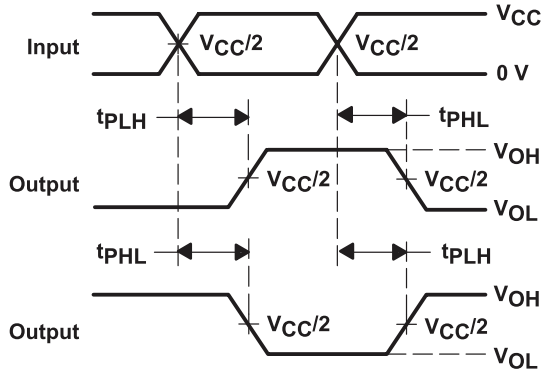


图 4. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

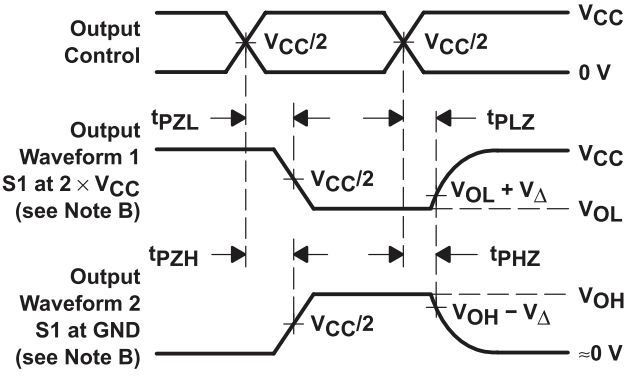


图 5. Voltage Waveforms Enable And Disable Times Low- and High-Level Enabling

Notes:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

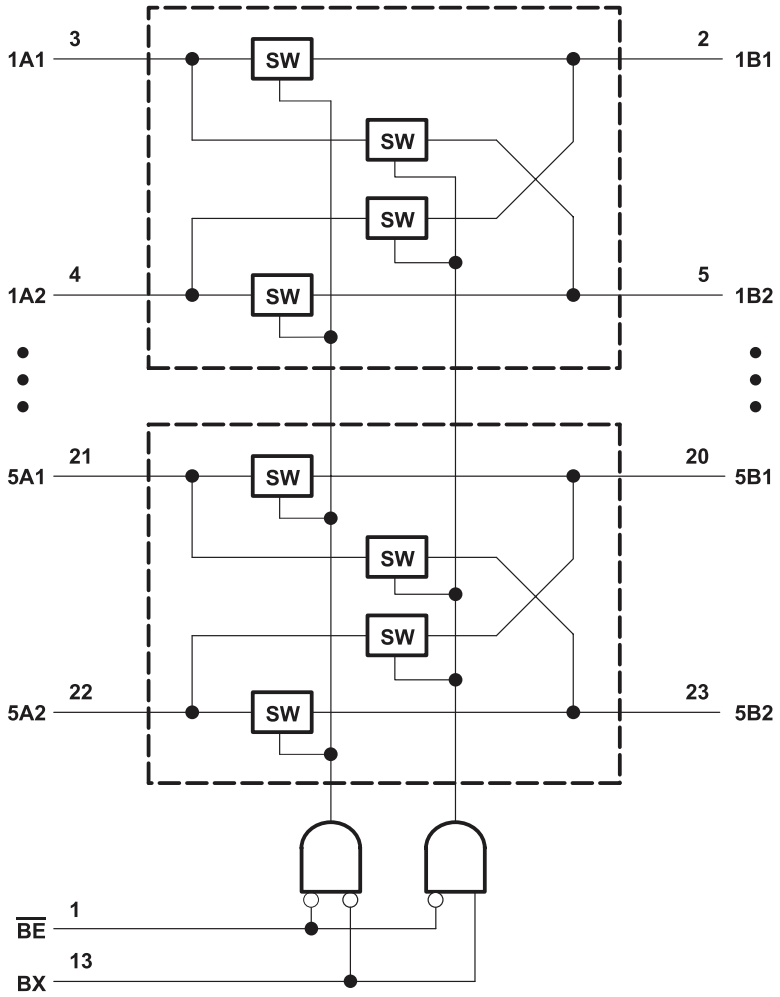
H. H. All parameters and waveforms are not applicable to all devices.

8 Detailed Description

8.1 Overview

The SN74CBTLV3383 device is a 10-bit high-speed bus exchange FET switch. The low ONstate resistance of the switch allows connections to be made with minimal propagation delay. The select (BX) input controls the data flow. The FET multiplexers and demultiplexers are disabled when the output-enable (BE) input is high. This device is fully specified for partial-power-down applications using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



8.3 Feature Description

Bidirectional Operation

The SN74CBTLV3383 conducts equally well from source (xA1, xA2) to drain (xB1,xB2). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

Rail-to-rail switching

The SN74CBTLV3383 will support signals on the I/O path across the full supply range 0 to V_{CC}

8.4 Device Functional Modes

Shows the functional modes of the SN74CBTLV3383.

表 1. Function Table

INPUTS		INPUTS–OUTPUTS	
$\overline{BE}$	BX	1A1–5A1	1A2-5A2
L	L	1B1–5B1	1B2–5B2
L	H	1B2–5B2	1B1–5B1
H	X	Z	Z

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CBTLV3383 device operates as a 10-bit bus switch or as a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high, and BE is low. The application shown here is a 5-bit bus being multiplexed between two devices. The BE and BX pins are used to control the chip from the bus controller. This is a generic example, and could apply to many situations.

9.2 Typical Application

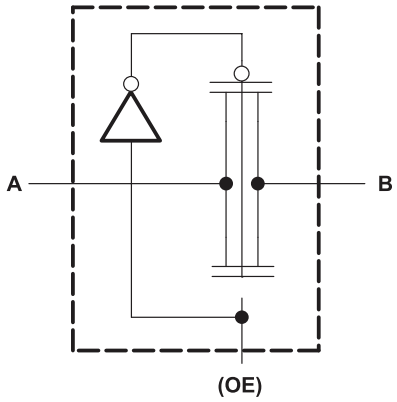


图 6. Simple Schematic

9.2.1 Design Requirements

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in Recommended Operating Conditions.
   - Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6 V at any valid VCC.
2. Recommended Output Conditions:
   - Load currents should not exceed ±128 mA per channel.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 200 MHz.

9.2.2 Detailed Design Procedure

The SN74CBTLV3383 can be operated without any external components. All inputs signals passing through the switch must fall within the recommend operating conditions of the SN74CBTLV3383 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. The max continuous current can be 128 mA.

10 Power Supply Recommendations

The SN74CBTLV3383 operates across a wide supply range of 2.3 V to 3.6 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Power-supply bypassing improves noise margin and prevents switching noise propagation from the VDD supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from VDD to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

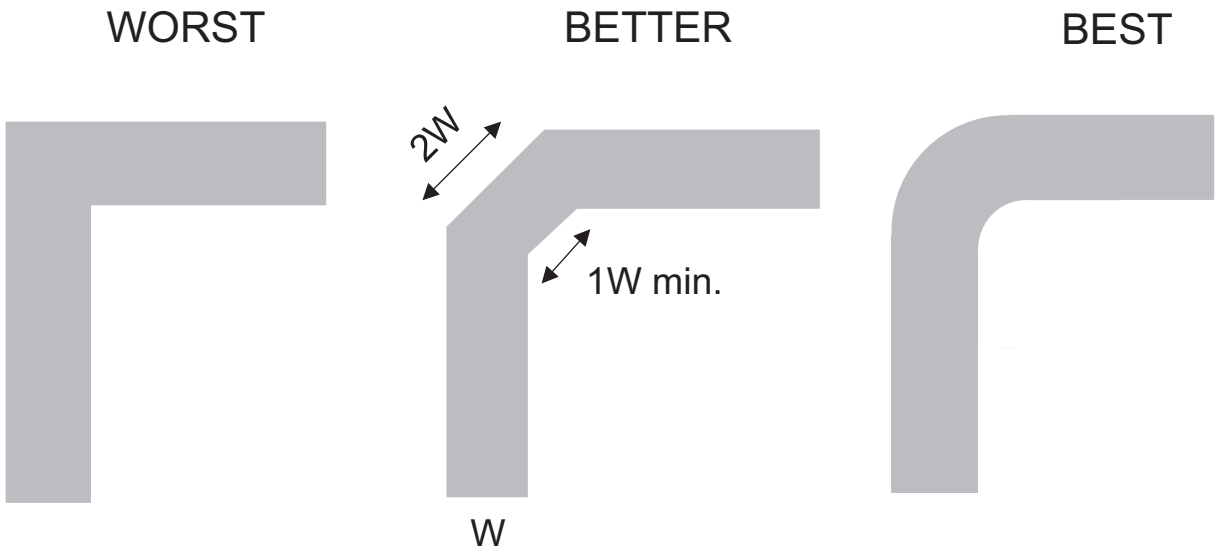


图 7. Example Layout

12 器件和文档支持

12.1 文档支持

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBTLV3383DBQR	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTLV3383
SN74CBTLV3383DBQR.B	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTLV3383
SN74CBTLV3383DGVR	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL383
SN74CBTLV3383DGVR.B	Active	Production	TVSOP (DGV) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL383
SN74CBTLV3383DW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3383
SN74CBTLV3383DW.B	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3383
SN74CBTLV3383DWE4	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3383
SN74CBTLV3383DWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3383
SN74CBTLV3383DWR.B	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3383
SN74CBTLV3383PW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL383
SN74CBTLV3383PW.B	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL383
SN74CBTLV3383PWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL383
SN74CBTLV3383PWR.B	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL383

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

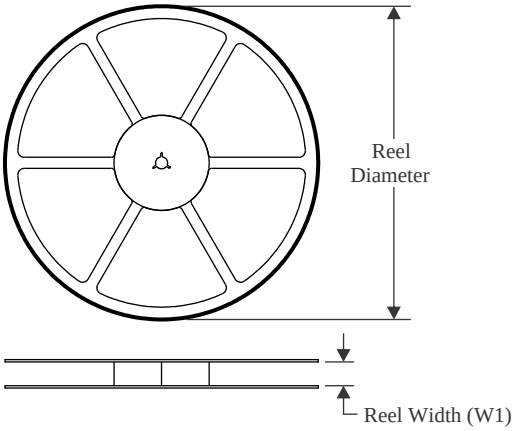
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

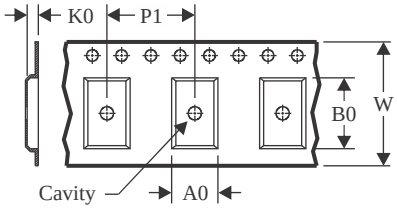
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

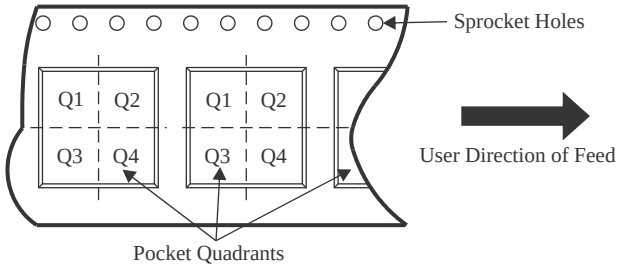


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

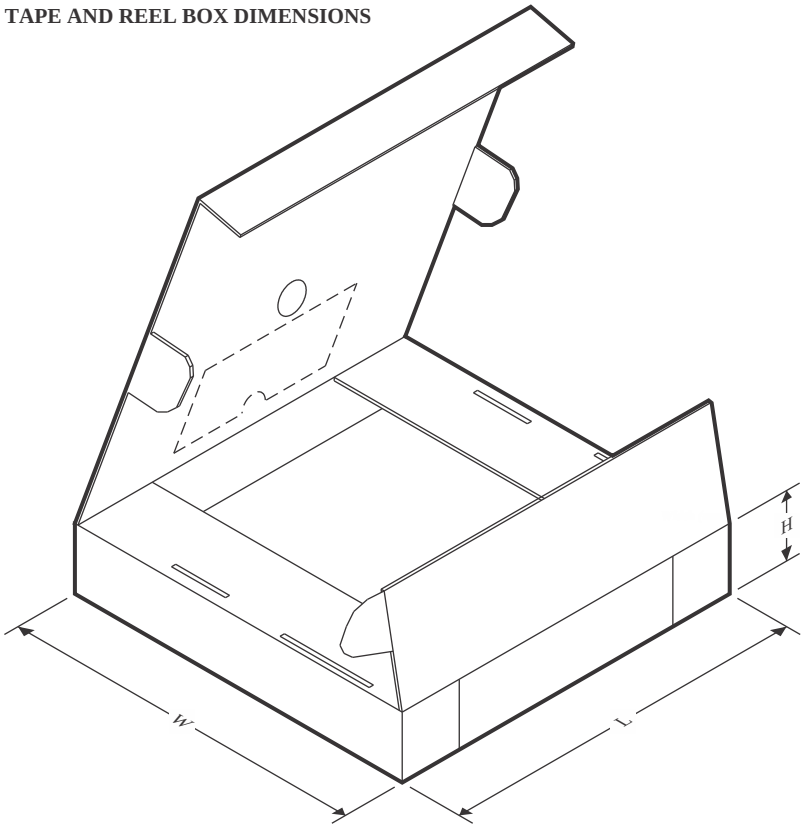
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV3383DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTLV3383DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3383DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBTLV3383PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

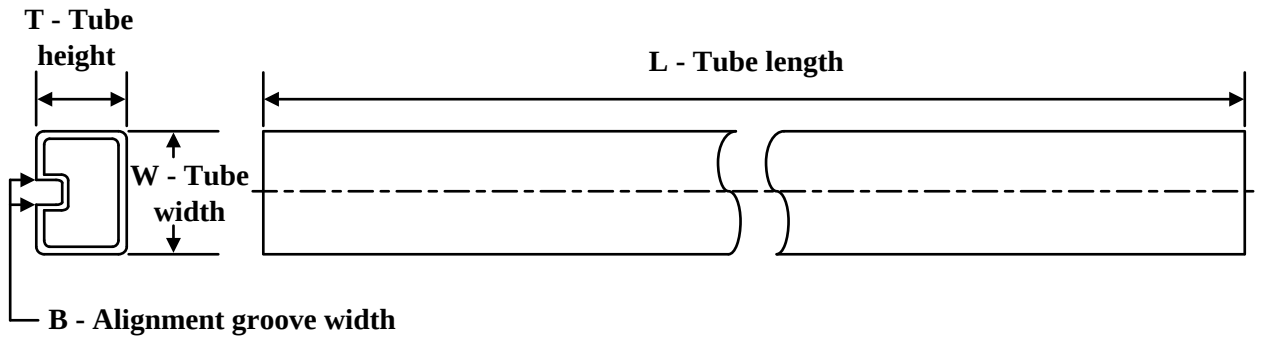
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV3383DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
SN74CBTLV3383DGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0
SN74CBTLV3383DWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74CBTLV3383PWR	TSSOP	PW	24	2000	353.0	353.0	32.0

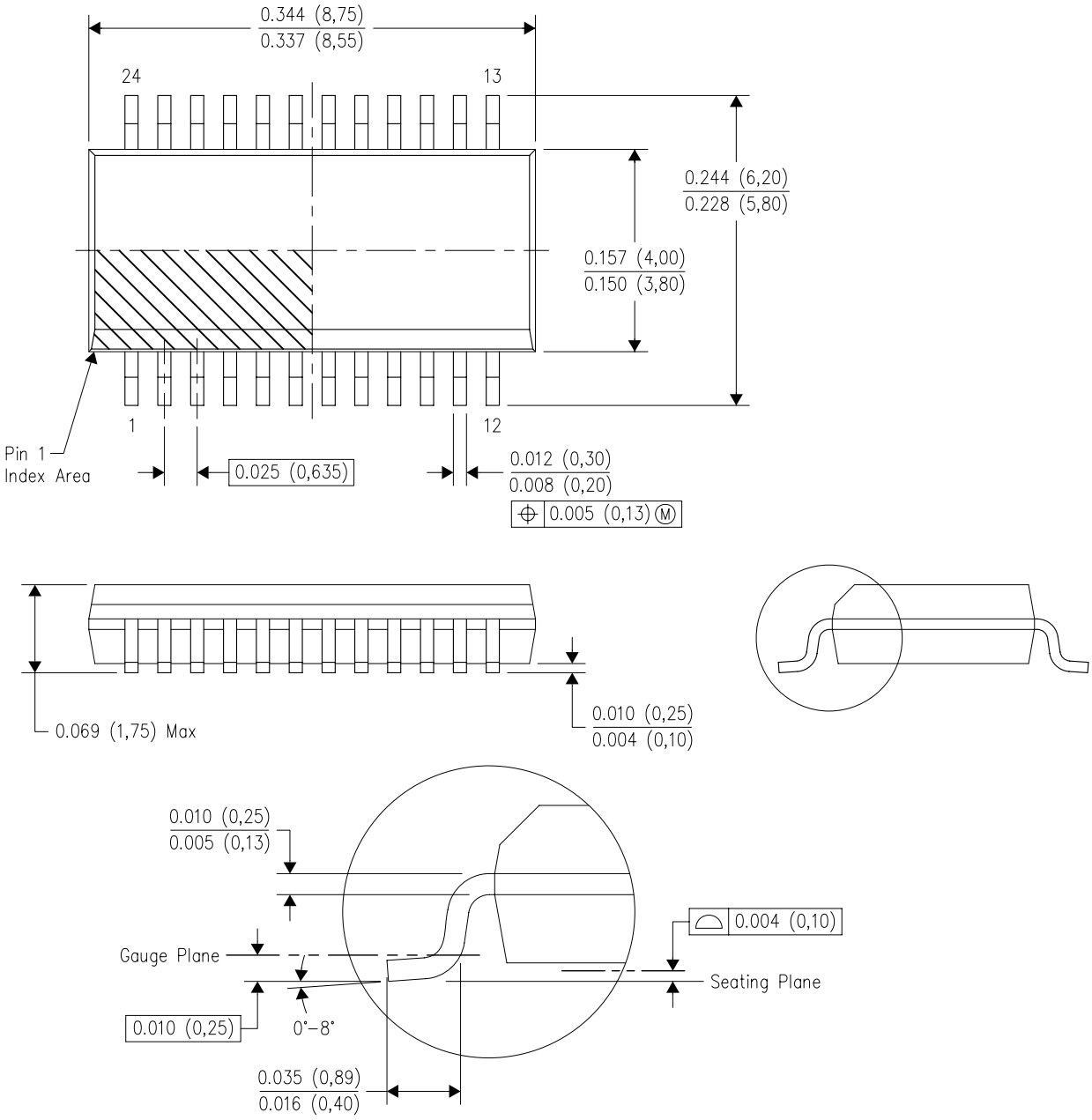
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBTLV3383DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74CBTLV3383DW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74CBTLV3383DWE4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74CBTLV3383PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74CBTLV3383PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



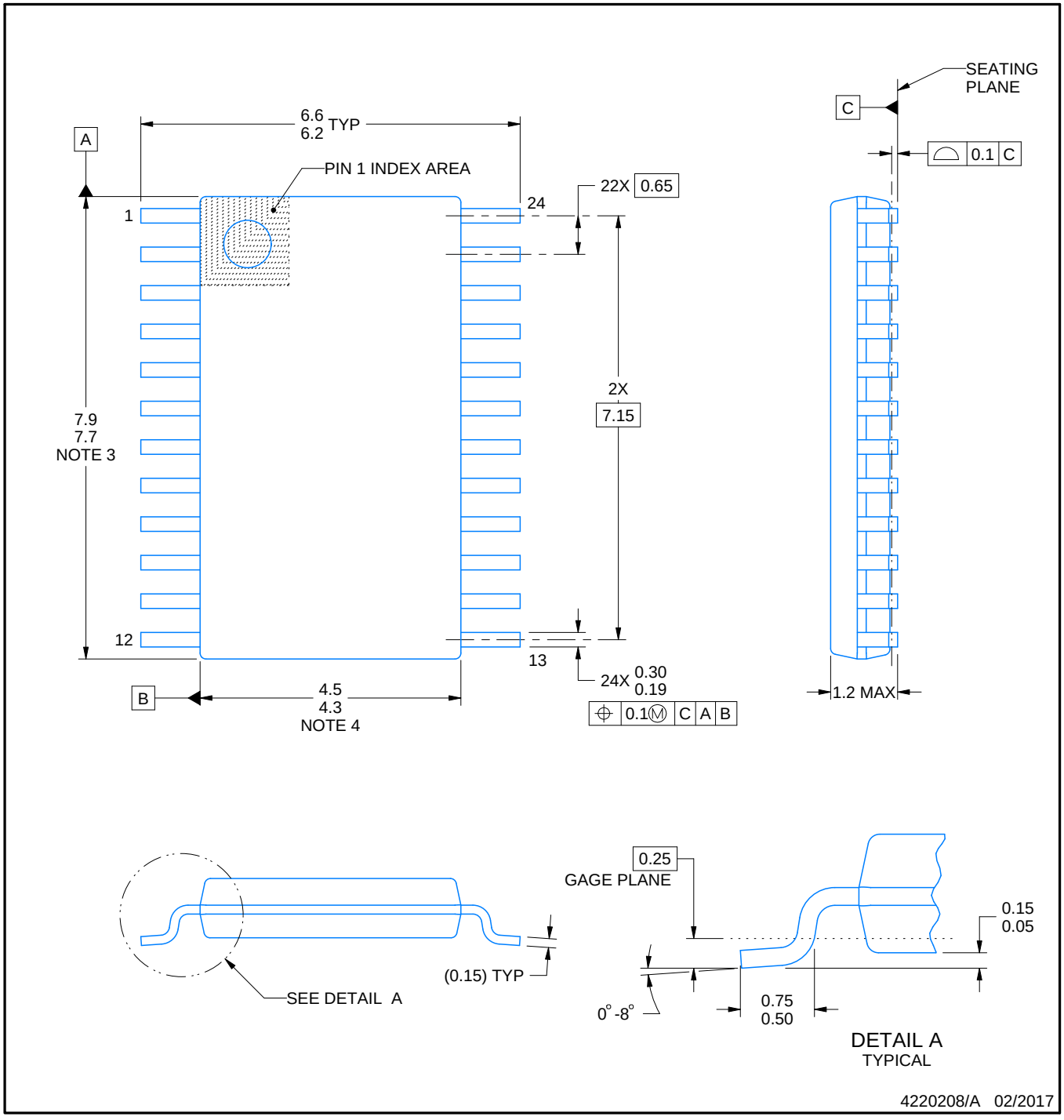
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

PACKAGE OUTLINE

PW0024A

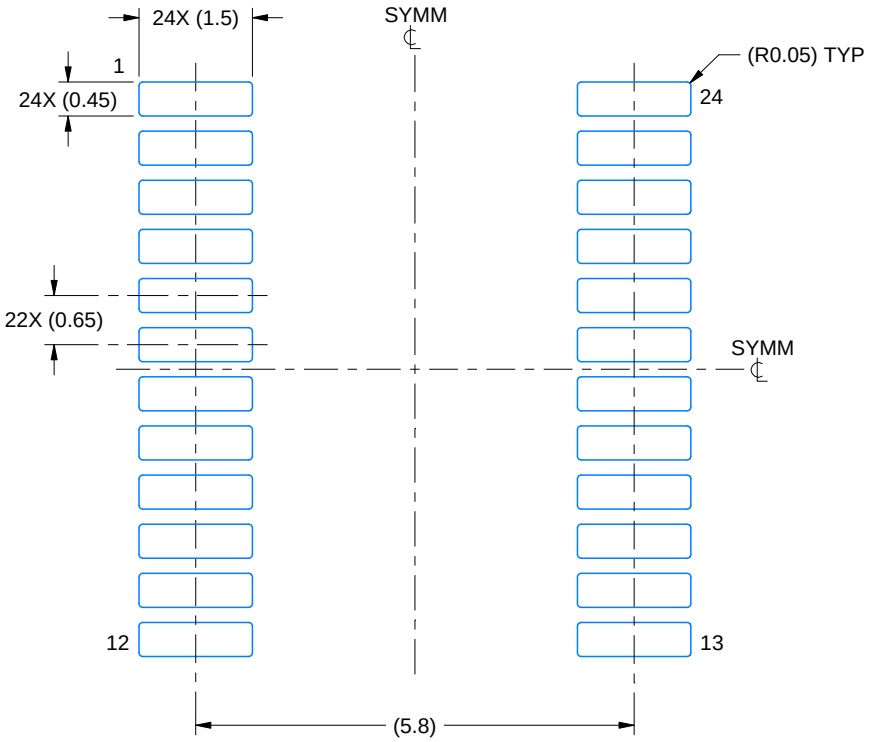
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

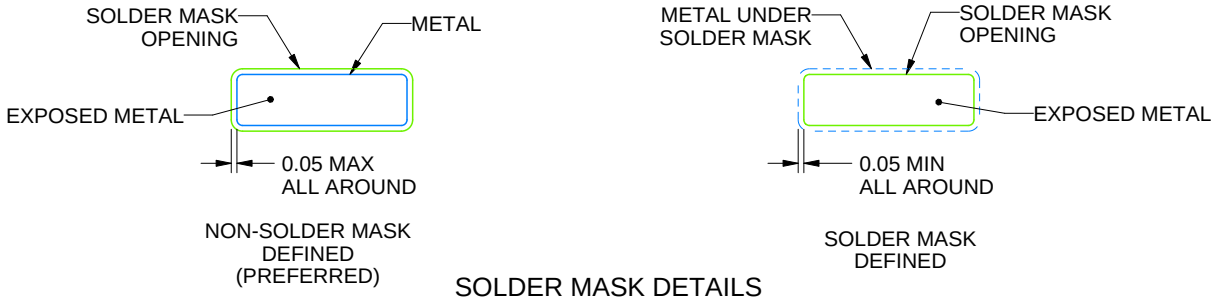


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

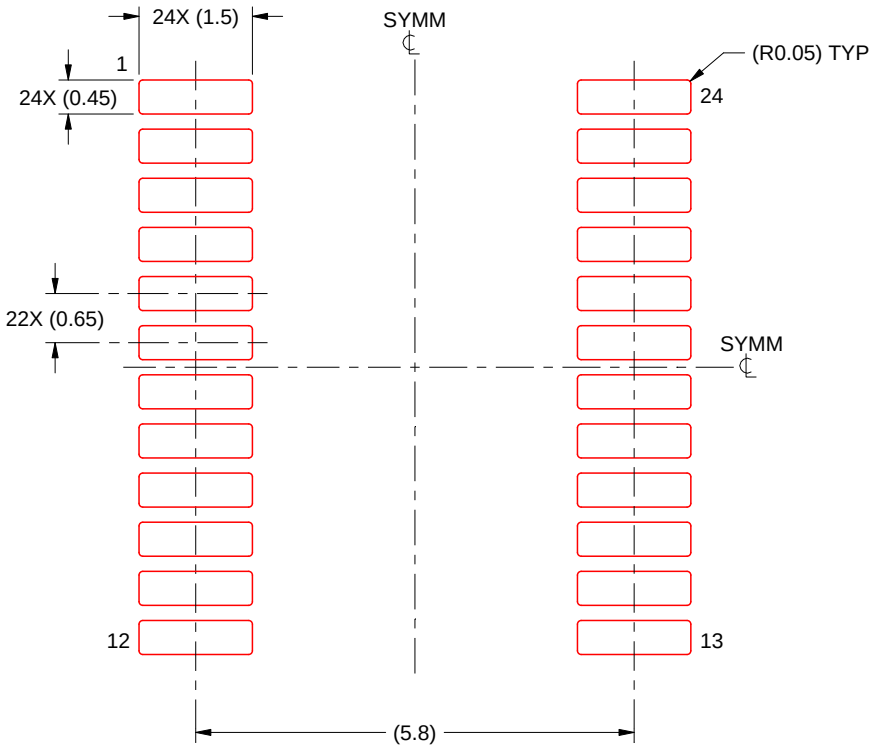


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



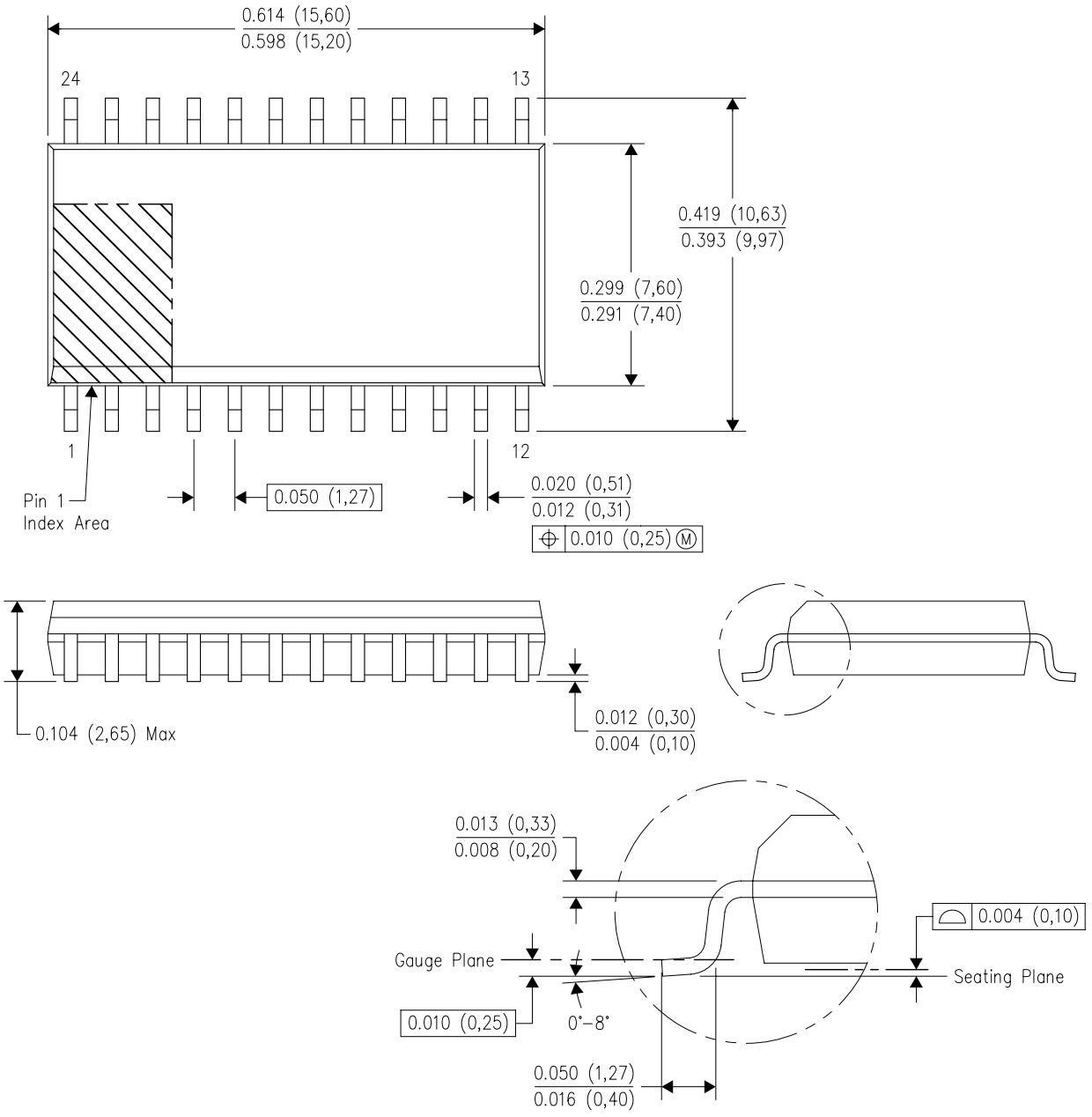
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



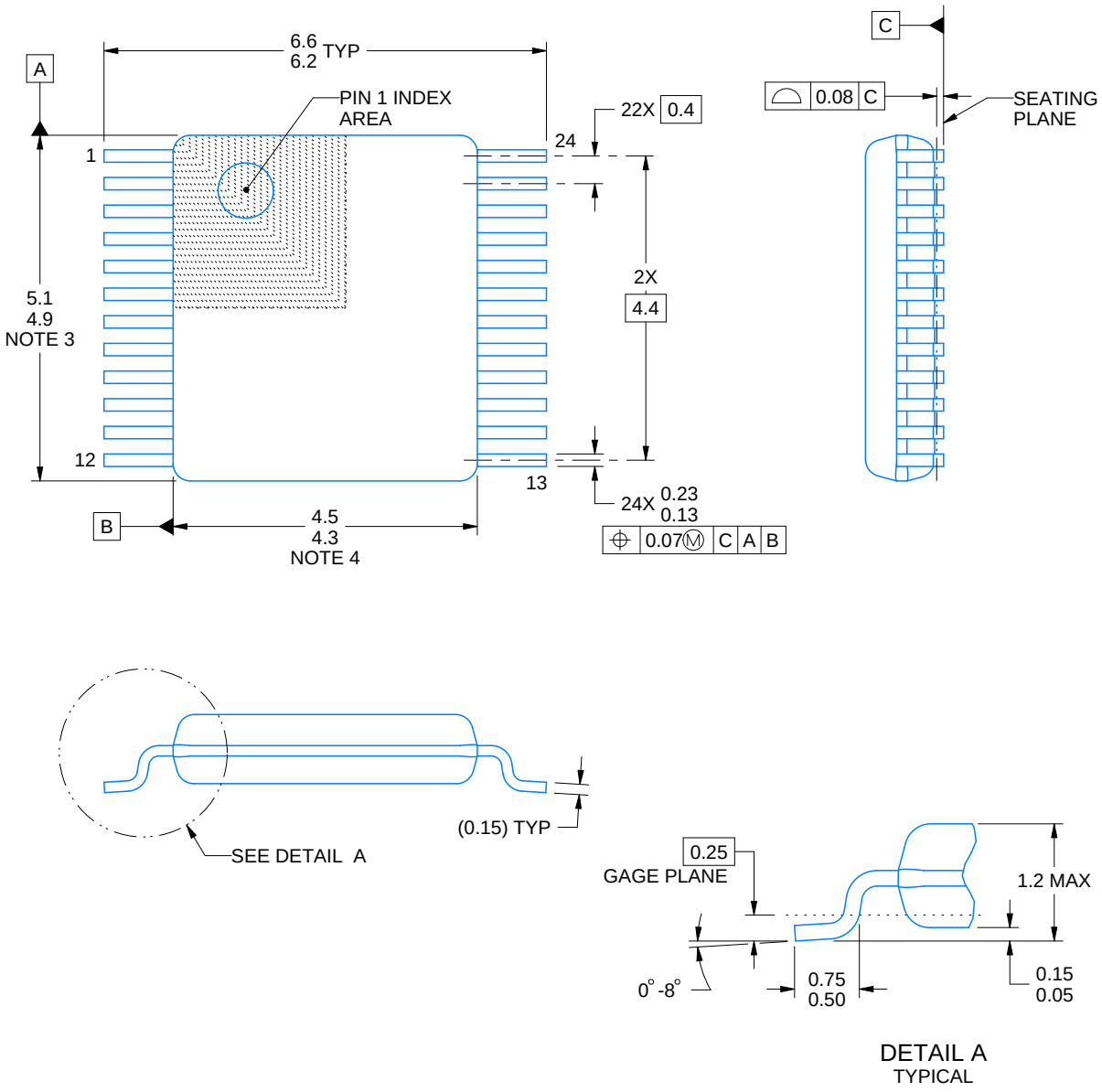
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

PACKAGE OUTLINE

DGV0024A

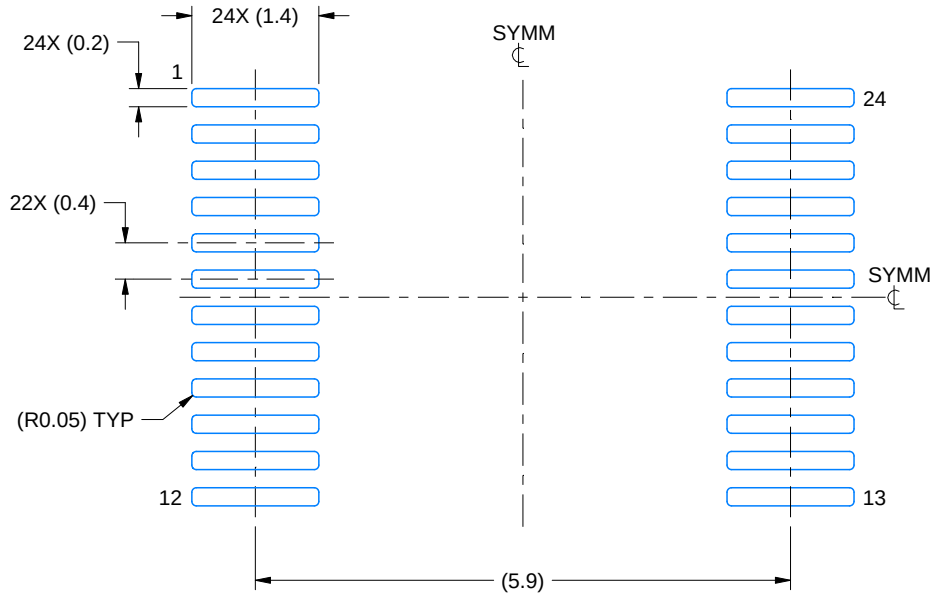
TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

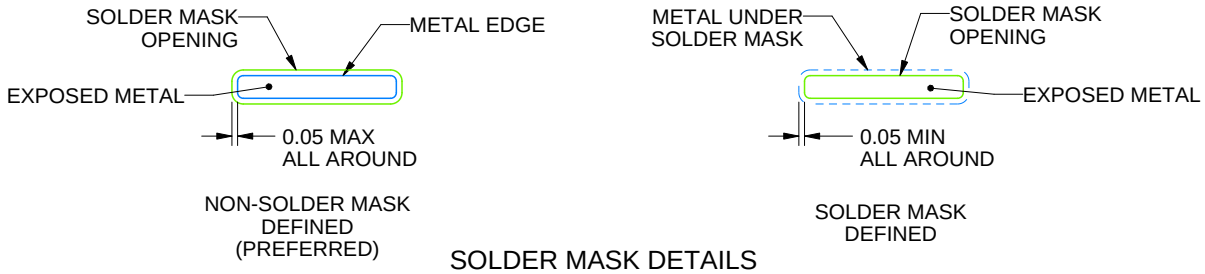


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

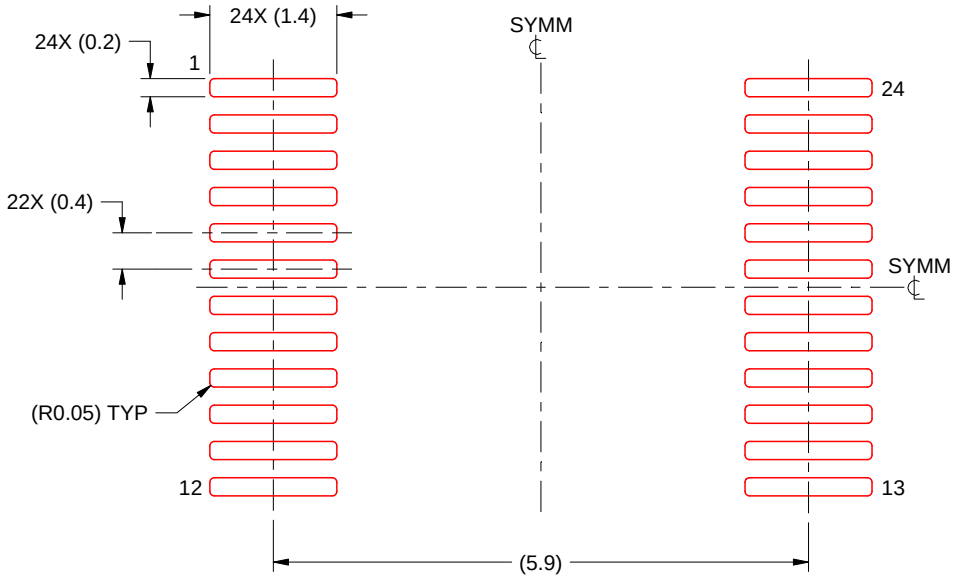


SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4229221/A 12/2022

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月