SN74CBTLV3245A 低电压八通道 FET 总线开关

1 特性

- 标准 '245 型引脚排列
- 两个端口之间具有 5Ω 开关连接
- 支持在数据 I/O 端口进行轨到轨开关
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)

应用

- 数据中心和企业计算
- 宽带固定线路接入
- 楼宇自动化
- 有线网络
- 电机驱动器

2 说明

SN74CBTLV3245A 器件在标准 '245 器件引脚排列中提供 8 位高速总线开关功能。此开关具有低导通状态电阻，可以最短传播延迟建立连接。

该器件配置成一个 8 位开关。当输出使能 ($\overline{OE}$) 为低电平时，8 位总线开关打开，端口 A 连接到端口 B。当 $\overline{OE}$ 为高电平时，开关断开，并且在两个端口之间存在高阻抗状态。

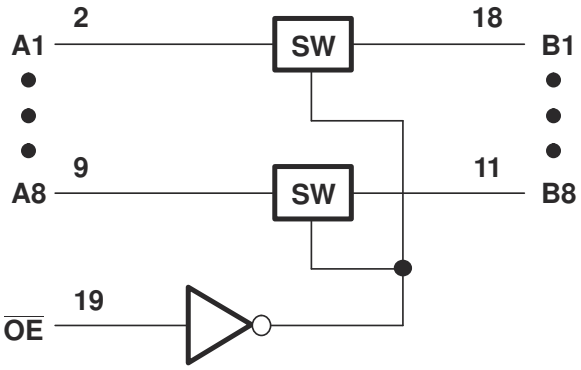
该器件专用于使用 I_{off} 的局部断电应用。I_{off} 特性确保在器件断电时，破坏性电流不会通过器件回流。该器件可在关断时提供隔离。

为了在上电或下电期间保持高阻抗状态，$\overline{OE}$ 必须通过一个上拉电阻器连接至 V_{CC}；该电阻器的最小阻值由驱动器的电流灌入能力来决定。

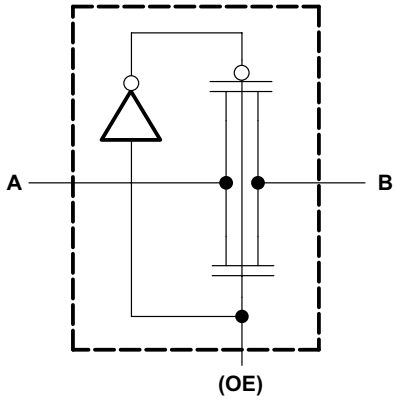
封装信息 (1)

器件型号	封装	封装尺寸(2)
SN74CBTLV3245A	DBQ（SSOP，20）	8.65mm × 3.90mm
	PW（TSSOP，20）	6.50mm × 4.40mm
	RGY（VQFN，20）	4.50mm × 3.50mm
	DW（SOIC，20）	12.80mm × 7.50mm
	DGV（TVSOP，20）	5.00mm × 4.40mm
	DGS（VSSOP，20）	5.10mm × 3.00mm
	RKS（VQFN，20）	4.50mm × 2.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）



每个 FET 开关的简化版原理图

内容

3 引脚配置和功能

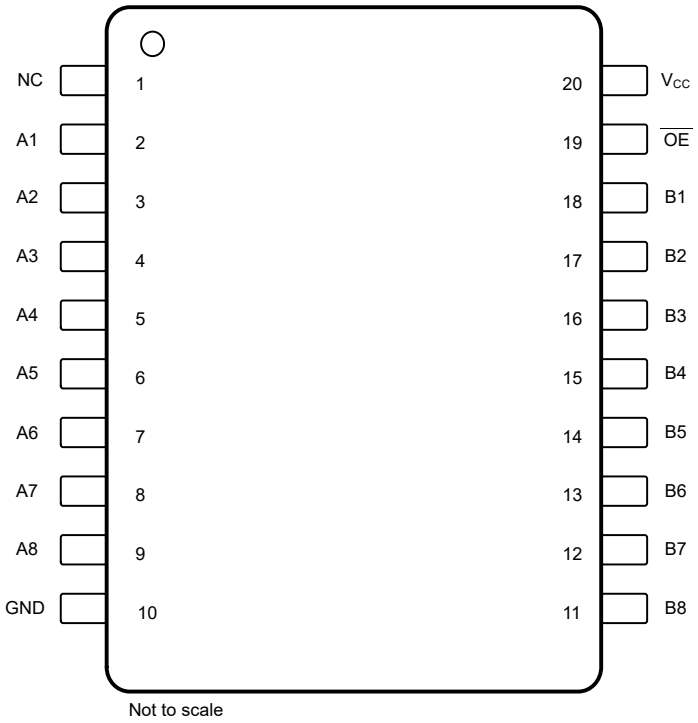


图 3-1. DBQ、DGV、DW、DGS 和 PW 封装 20 引脚 SSOP、TVSOP、SOIC、VSSOP 和 TSSOP（顶视图）

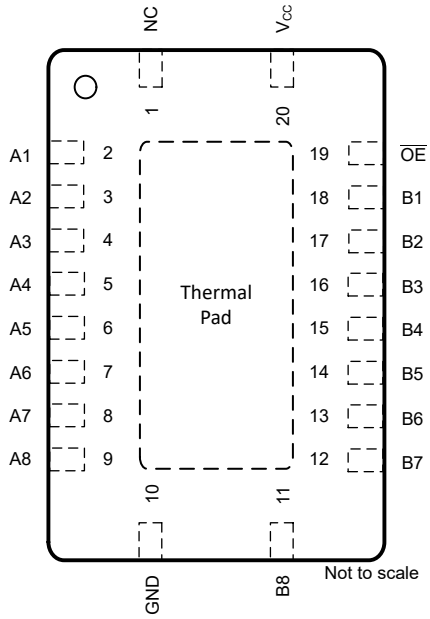


图 3-2. RGY、RKS 封装 20 引脚 VQFN（顶视图）

表 3-1. 引脚功能

引脚		类型(1)	说明
名称	编号		
NC	1	I/O	无内部连接。可短接到 GND 或保持悬空
A1	2	I/O	输入/输出引脚
A2	3	I/O	输入/输出引脚
A3	4	I/O	输入/输出引脚
A4	5	I/O	输入/输出引脚
A5	6	I/O	输入/输出引脚
A6	7	I/O	输入/输出引脚
A7	8	I/O	输入/输出引脚
A8	9	I/O	输入/输出引脚
GND	10	GND	接地引脚
B8	11	I/O	输入/输出引脚
B7	12	I/O	输入/输出引脚
B6	13	I/O	输入/输出引脚
B5	14	I/O	输入/输出引脚
B4	15	I/O	输入/输出引脚
B3	16	I/O	输入/输出引脚
B2	17	I/O	输入/输出引脚
B1	18	I/O	输入/输出引脚
$\overline{OE}$	19	I	输出使能，低电平有效
V_{CC}	20	PWR	电压源引脚

(1) I = 输入，O = 输出，PWR = 电源

4 规格

4.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	4.6	V
V_I	输入电压范围(2)		-0.5	4.6	V
	连续通道电流			128	mA
I_{IK}	输入钳位电流	$V_{I/O}$ < 0		-50	mA
T_{stg}	贮存温度范围		-65	150	°C

(1) 超出*绝对最大额定值*运行可能会对器件造成永久损坏。*绝对最大额定值*并不表示器件在这些条件下或在*建议的工作条件*以外的任何其他条件下能够正常运行。如果超出*建议运行条件*但在*绝对最大额定值*范围内使用，器件可能不会完全正常运行，这可能影响器件的可靠性、功能和性能并缩短器件寿命。
(2) 如果遵守输入和输出钳位电流额定值，则可能会超过输入和输出负电压额定值。

4.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±2000	V

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。

4.3 热性能信息

热指标 [1]		SN74CBTLV3245A							单位
		PW (TSSOP)	RKS(VQFN)	DGS(VSSOP)	DBQ(SSOP)	RGY(VQFN)	DW(SOIC)	DGV(TVSOP)	
		20 引脚	20 引脚	20 引脚	20 引脚	20 引脚	20 引脚	20 引脚	
$R_{\theta JA}$	结至环境热阻	105.9	71.8	120.5	100.9	80.8	58	92	°C/W

4.4 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压		2.3	3.6	V
V_{IH}	高电平控制输入电压	V_{CC} = 2.3V 至 2.7V	1.7		V
		V_{CC} = 2.7V 至 3.6V	2		
V_{IL}	低电平控制输入电压	V_{CC} = 2.3V 至 2.7V		0.7	V
		V_{CC} = 2.7V 至 3.6V		0.8	
T_A	自然通风条件下的工作温度	PKG = DBQ、DGV、DW、PW、RGY	-40	85	°C
T_A	自然通风条件下的工作温度	PKG = RKS、DGS	-40	125	°C

(1) 器件所有的未使用控制输入必须保持在 V_{CC} 或 GND 以保证器件正常运行。请参阅 TI 应用笔记，*CMOS 输入缓慢或悬空的影响*，文献编号 SCBA004。

4.5 电气特性 - 仅限 DBQ、DGV、DW、PW 和 RGY

在自然通风条件下的建议运行温度范围（-40°C 至 85°C）内测得（除非另有说明）

参数		测试条件			最小值	典型值 (1)	最大值	单位
V_{IK}	控制输入	V_{CC} = 3V，	I_I = -18mA				-1.2	V
	数据输入						-0.8	
I_I		V_{CC} = 3.6V，	V_I = V_{CC} 或 GND				±60	μA
I_{off}		V_{CC} = 0，	V_I 或 V_O = 0V 至 3.6V				40	μA
I_{CC}		V_{CC} = 3.6V，	I_O = 0，	V_I = V_{CC} 或 GND			20	μA
ΔI_{CC} (2)	控制输入	V_{CC} = 3.6V，	一个输入为 3V，	其他输入电压为 V_{CC} 或 GND			300	μA
C_i	控制输入	V_I = 3V 或 0V				4		pF
$C_{io(OFF)}$		V_O = 3V 或 0V，	$\overline{OE}$ = V_{CC}			9		pF
r_{on} (3)		V_{CC} = 2.3V，V_{CC} = 2.5V 时的典型值	V_I = 0	I_O = 64mA		5	8	Ω
				I_O = 24mA		5	8	
			V_I = 1.7V，	I_O = 15mA		27	40	
		V_{CC} = 3V	V_I = 0	I_O = 64mA		5	7	
				I_O = 24mA		5	7	
			V_I = 2.4V，	I_O = 15mA		10	15	

(1) 所有典型值均在 V_{CC} = 3.3V（除非另外注明）、T_A = 25°C 时测得。
(2) 这是每个输入在指定电压电平（而不是 V_{CC} 或 GND 下）的电源电流增加情况。
(3) 在通过开关的指示电流下，由 A 和 B 端子之间的压降测量。导通状态电阻由两个（A 或 B）端子的较低电压决定。

4.6 电气特性 - 仅限 RKS 和 DGS 封装

在自然通风条件下的建议运行温度范围（-40°C 至 125°C）内测得（除非另有说明）

参数		测试条件			最小值	典型值 (1)	最大值	单位
V_{IK}	控制输入	V_{CC} = 3V，	I_I = -18mA				-1.2	V
	数据输入						-0.8	
I_I		V_{CC} = 3.6V，	V_I = V_{CC} 或 GND				±60	μA
I_{off}		V_{CC} = 0，	V_I 或 V_O = 0V 至 3.6V				40	μA
I_{CC}		V_{CC} = 3.6V，	I_O = 0，	V_I = V_{CC} 或 GND			20	μA
ΔI_{CC} (2)	控制输入	V_{CC} = 3.6V，	一个输入为 3V，	其他输入电压为 V_{CC} 或 GND			300	μA
C_i	控制输入	V_I = 3V 或 0V				4		pF
$C_{io(OFF)}$		V_O = 3V 或 0V，	$\overline{OE}$ = V_{CC}			9		pF
r_{on} (3)		V_{CC} = 2.3V，V_{CC} = 2.5V 时的典型值	V_I = 0	I_O = 64mA		5	10	Ω
				I_O = 24mA		5	10	
			V_I = 1.7V，	I_O = 15mA		27	40	
		V_{CC} = 3V	V_I = 0	I_O = 64mA		5	9	
				I_O = 24mA		5	9	
			V_I = 2.4V，	I_O = 15mA		10	20	

4.7 开关特性 - 仅 DBQ、DGV、DW、PW 和 RGY

在自然通风条件下的建议运行温度范围（-40°C 至 85°C）内测得（除非另有说明）

参数	从（输入）	至（输出）	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		单位
			最小值	最大值	最小值	最大值	
t_{pd} (1)	A 或 B	B 或 A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A 或 B	1	6	1	4.7	ns
t_{dis}	$\overline{OE}$	A 或 B	1	6.1	1	6.4	ns

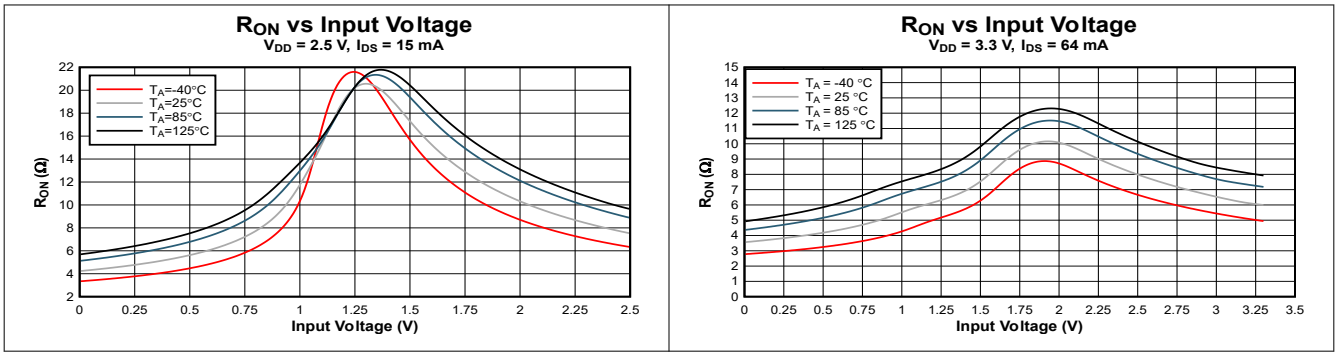
(1) 当由一个典型理想电压源（零输出阻抗）驱动时，传播延迟是使用此开关通态电阻典型值和额定负载电容计算得出的 RC 时间常数。

4.8 开关特性 - 仅限 RKS 和 DGS 封装

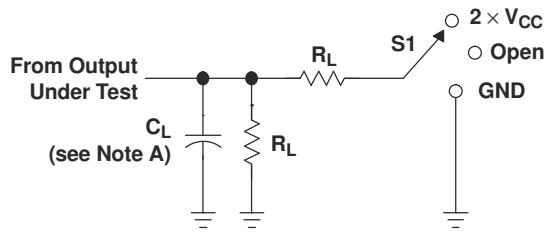
在自然通风条件下的建议运行温度范围（-40°C 至 125°C）内测得（除非另有说明）

参数	从（输入）	至（输出）	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		单位
			最小值	最大值	最小值	最大值	
t_{pd} (1)	A 或 B	B 或 A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A 或 B	1	8.5	1	7.8	ns
t_{dis}	$\overline{OE}$	A 或 B	1	6.8	1	5.8	ns

4.9 典型特性



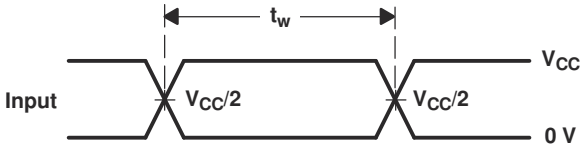
5 参数测量信息



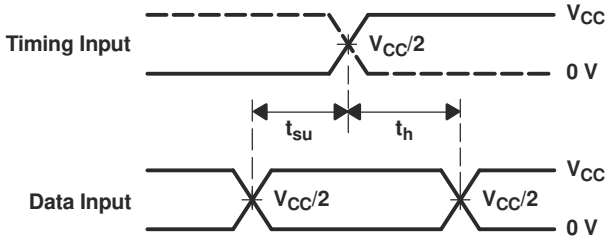
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND

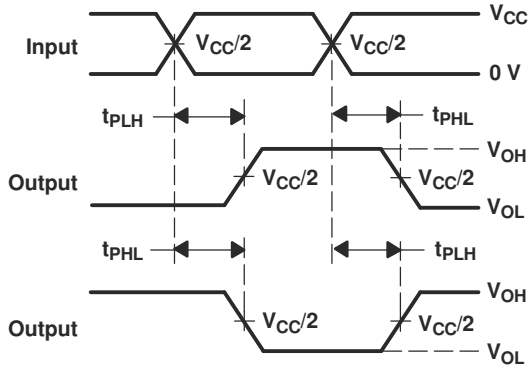
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V



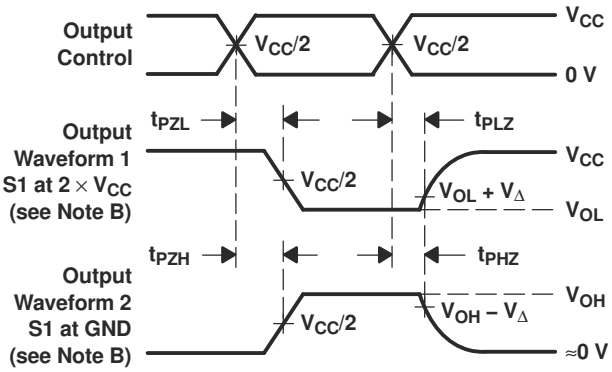
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 5-1. 负载电路和电压波形

6 详细说明

6.1 概述

6.2 功能方框图

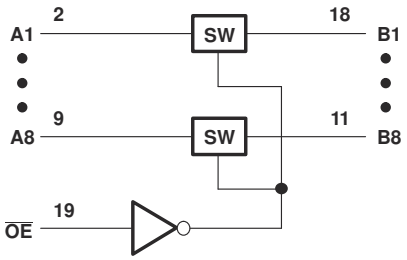


图 6-1. 逻辑图（正逻辑）

6.3 特性说明

6.4 器件功能模式

功能表

输入 $\overline{OE}$	功能
L	端口 A = 端口 B
H	断开

7 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 应用信息

SN74CBTLV3245A 可用于开关信号路径。此开关是双向开关，因此 A 和 B 引脚可用作输入或输出。一般情况下，在某一条信号路径在特定时间需要隔离时，才会使用该开关。

(1)

7.2 典型应用

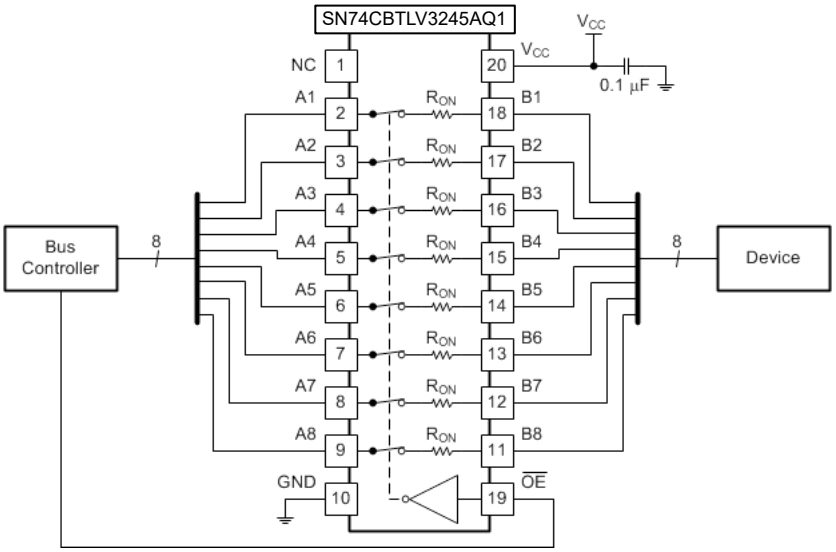


图 7-1. 典型应用原理图

7.2.1 设计要求

SN74CBTLV3245A 器件无需任何外部元件即可正常运行。TI 建议将数字控制引脚 (OE) 上拉至 VCC 或下拉至 GND，以避免引脚悬空可能导致的非预期开关状态。数字引脚悬空可能会导致过多的电流消耗。请参阅 CMOS 输入缓慢或悬空的影响。

7.2.2 详细设计过程

当 $\overline{OE}$ 为高电平时，总线处于有源状态。这意味着 A 和 B 引脚之间存在低阻抗路径。VCC 上的 0.1µF 电容器是去耦电容器，必须尽可能靠近器件放置。

7.3 电源相关建议

电源可以是 节 4.4 表中列出的最小和最大电源电压额定值之间的任何电压。

每个 V_{CC} 端子都必须具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1 µF 旁路电容器。如果多个引脚被标记为 V_{CC}，鉴于 V_{CC} 引脚在电路内部彼此相连，建议为每个 V_{CC} 引脚配备一个 0.01 µF 或 0.022 µF 电容器。若器件具备 V_{CC} 和 V_{DD} 等在不同电压水平运作的双电源引脚，为保证稳定，建议为每个电源引脚配备一个 0.1µF 旁路电容器。要抑制不同的噪声频率，请并联多个旁路电容器。值为 0.1 µF 和 1 µF 的电容器通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

7.4 布局

7.4.1 布局指南

反射和匹配问题与环路天线理论密切相关，但两者之间存在显著差异，故而需要独立于该理论框架外进行探讨。当 PCB 布线以 90° 角拐角时，会发生反射。反射的主要原因是布线宽度发生了变化。在拐角的顶点，布线宽度增加到原来宽度的 1.414 倍。这种增加会影响传输线特性，尤其是导致反射的布线的分布式电容和自感特性。并非所有 PCB 布线都是直线，因此某些布线必须拐角。图 7-2 展示了渐入佳境的圆角技术。只有最后一个示例（理想）保持恒定的布线宽度并能够更大限度地减少反射。

7.4.2 布局示例

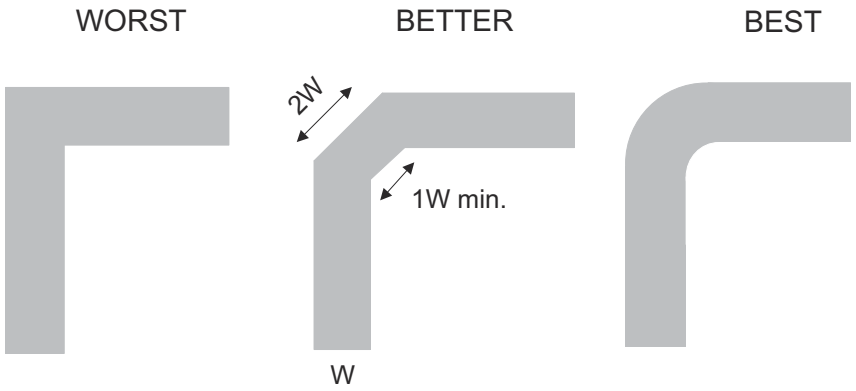


图 7-2. 布线示例

8 器件和文档支持

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (August 2005) to Revision N (May 2026)	Page
• 将文档更新为新的 TI 数据表格式 - 未对现有规格做出更改。	1
• 删除了“订购信息”表	1
• 添加了应用部分、器件信息部分、引脚配置和功能部分、ESD 等级表、特性说明部分、器件功能模式、应用和实现部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。	1
• 更新了“热性能额定值”。	6
• 添加了具有 125°C 适应能力的新封装	6
• 针对 RKS 和 DGS 封装添加了“电气和开关特性”部分。	7
• 添加了“典型特性”	8
• 添加了机械、封装和可订购信息部分。	13

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

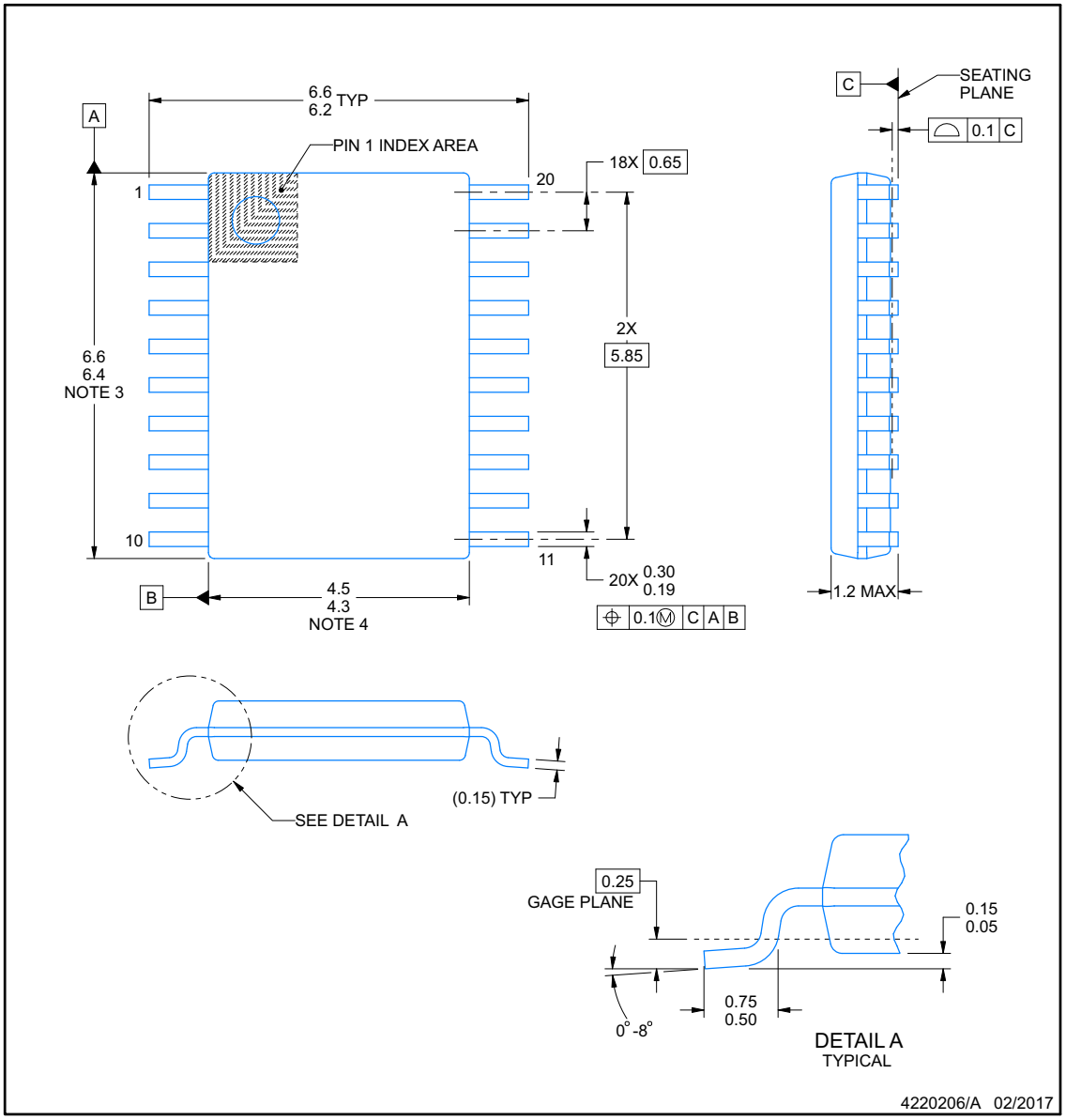
10.1 机械数据

PACKAGE OUTLINE

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

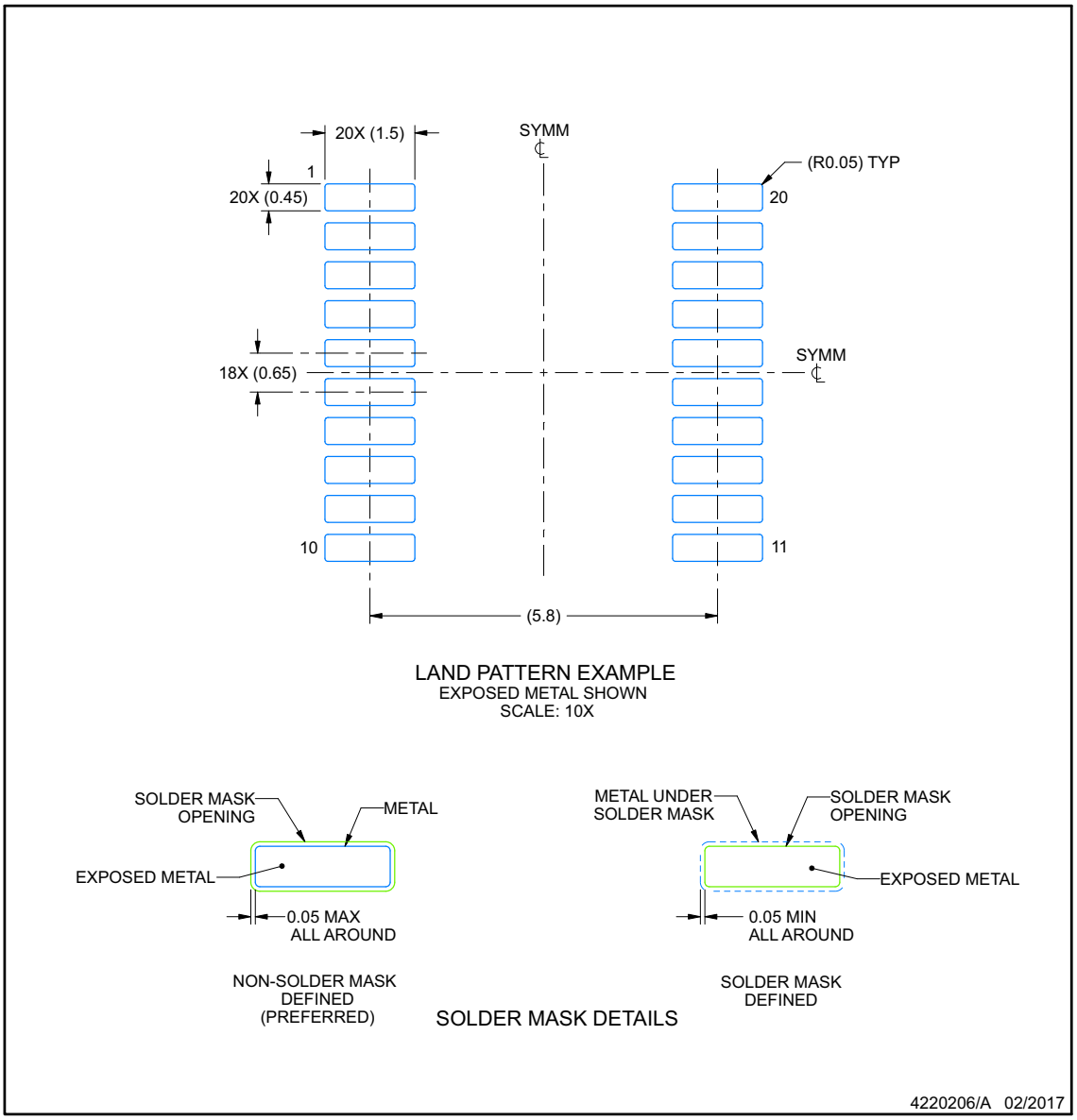
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



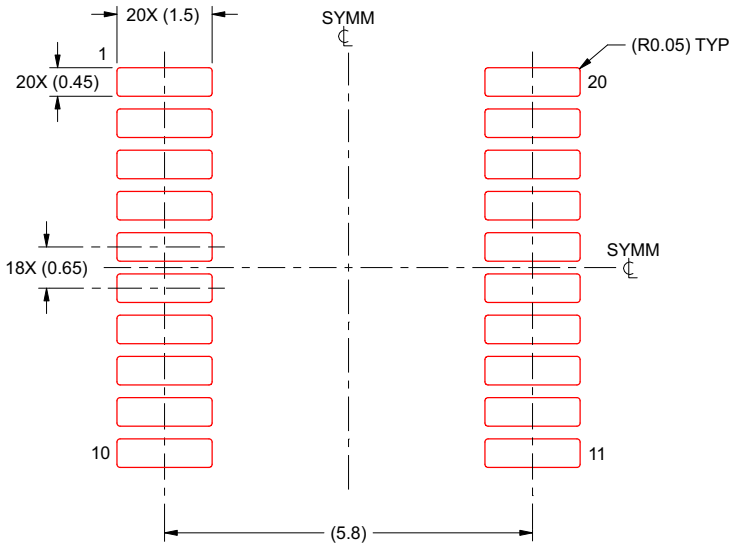
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

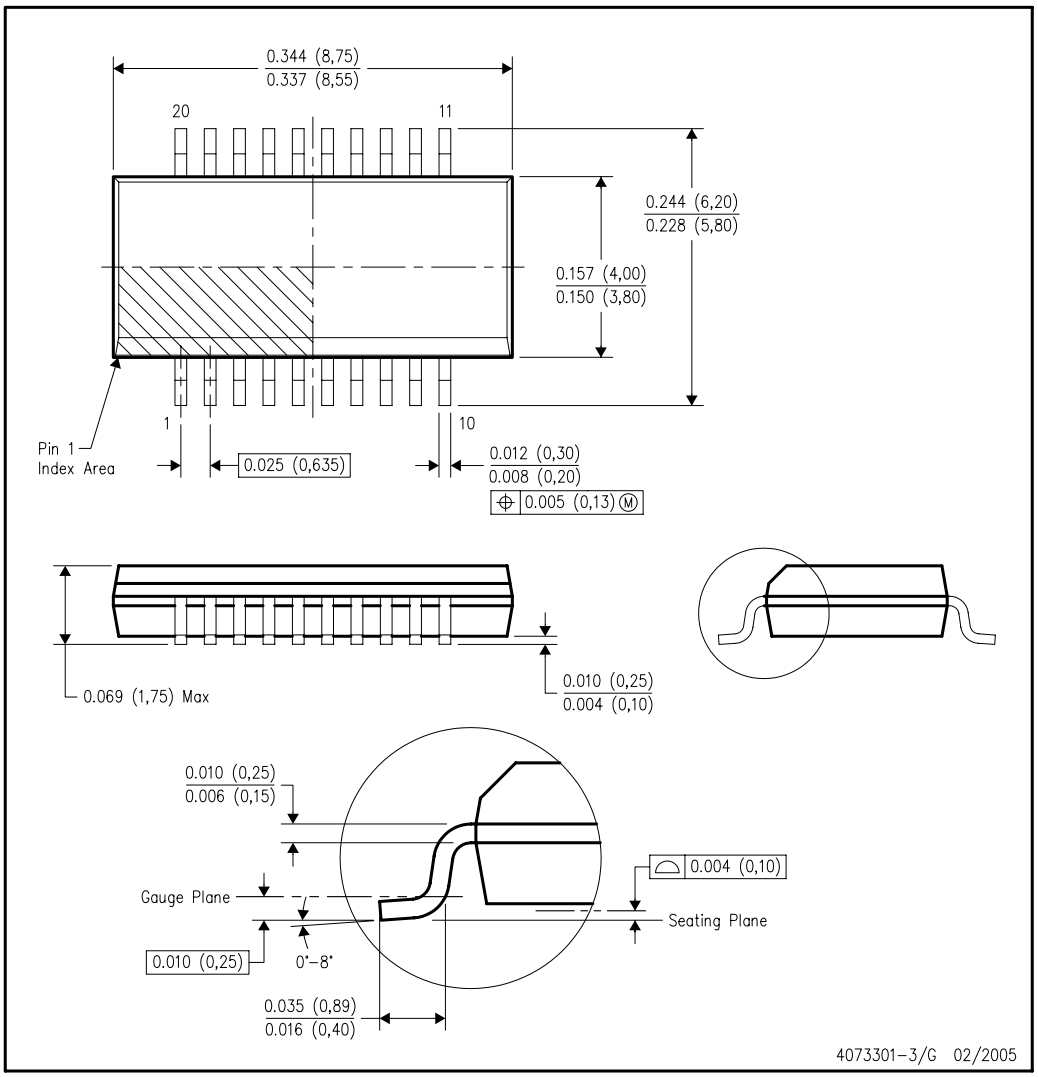
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



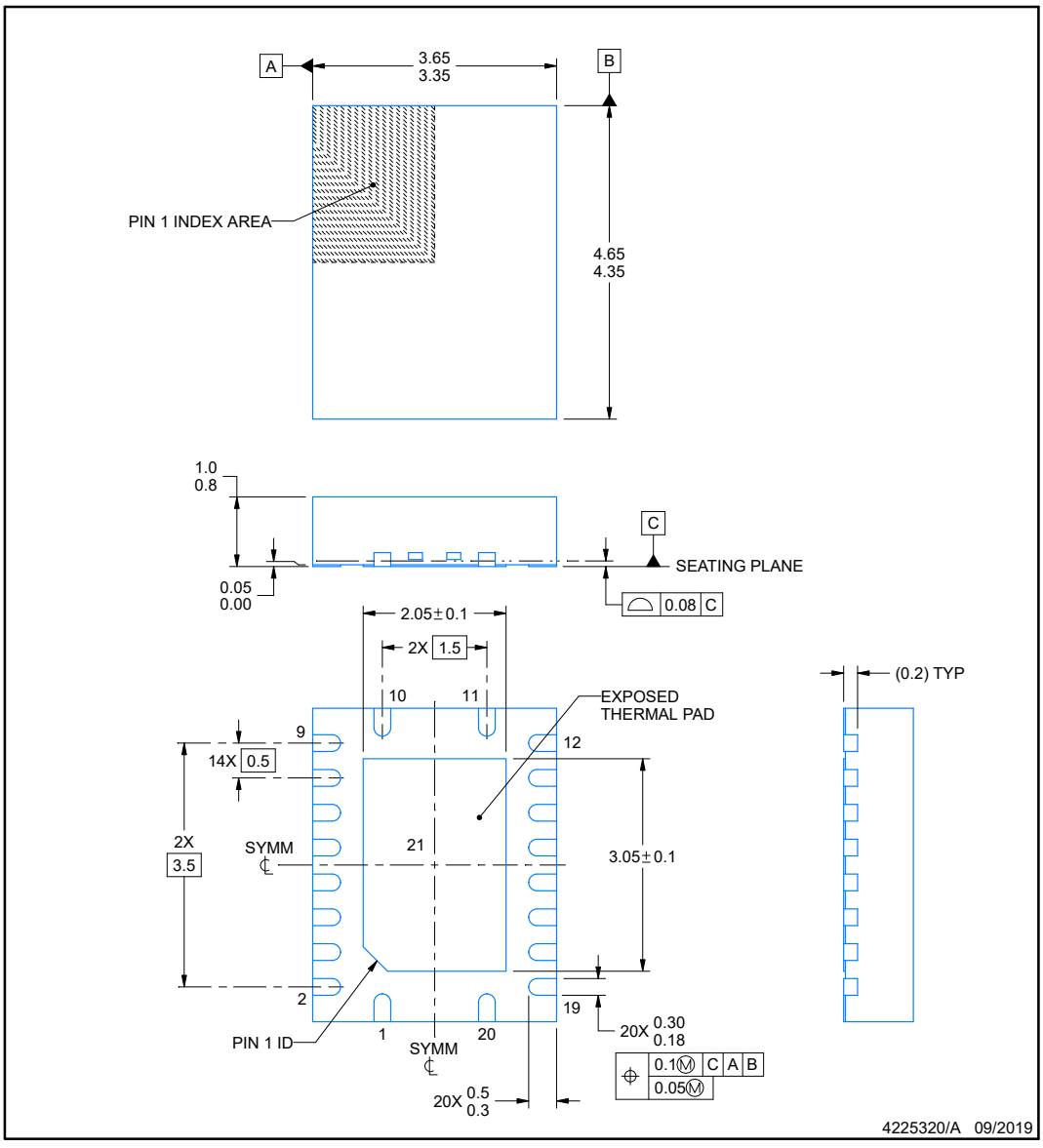
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

RGY0020A

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



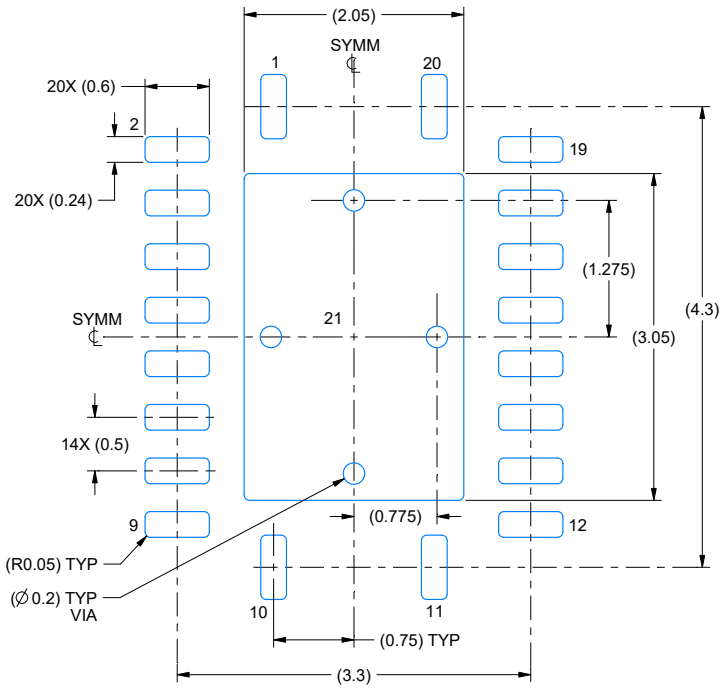
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

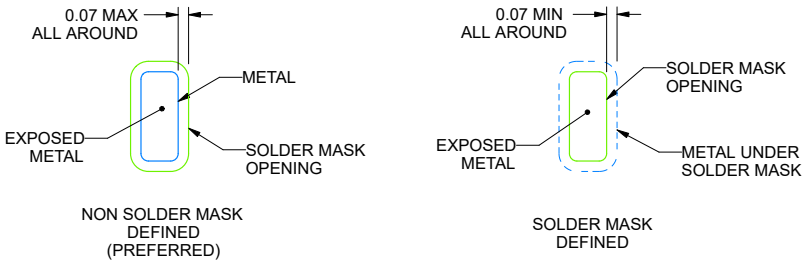
EXAMPLE BOARD LAYOUT

RGY0020A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

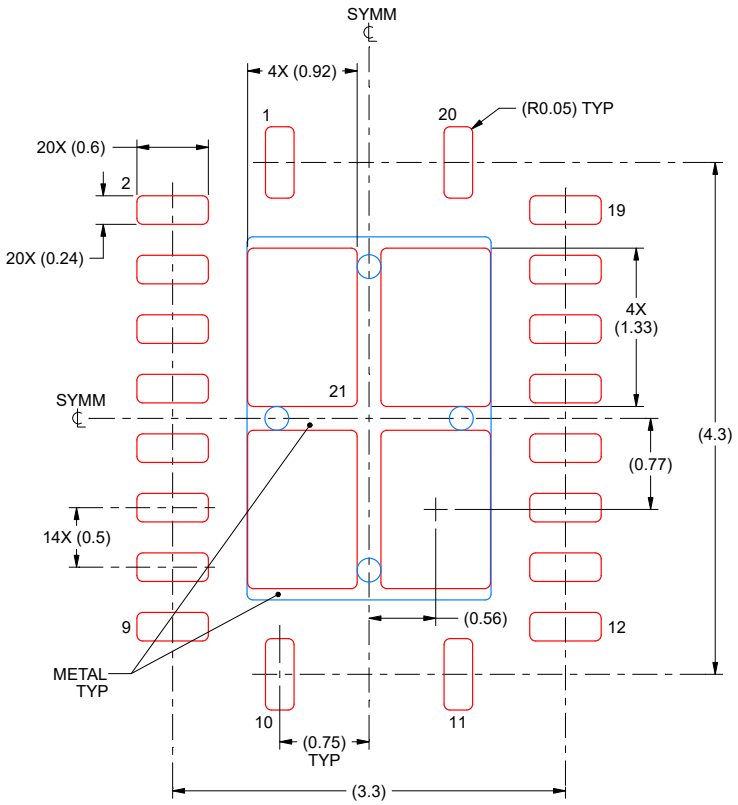
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0020A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

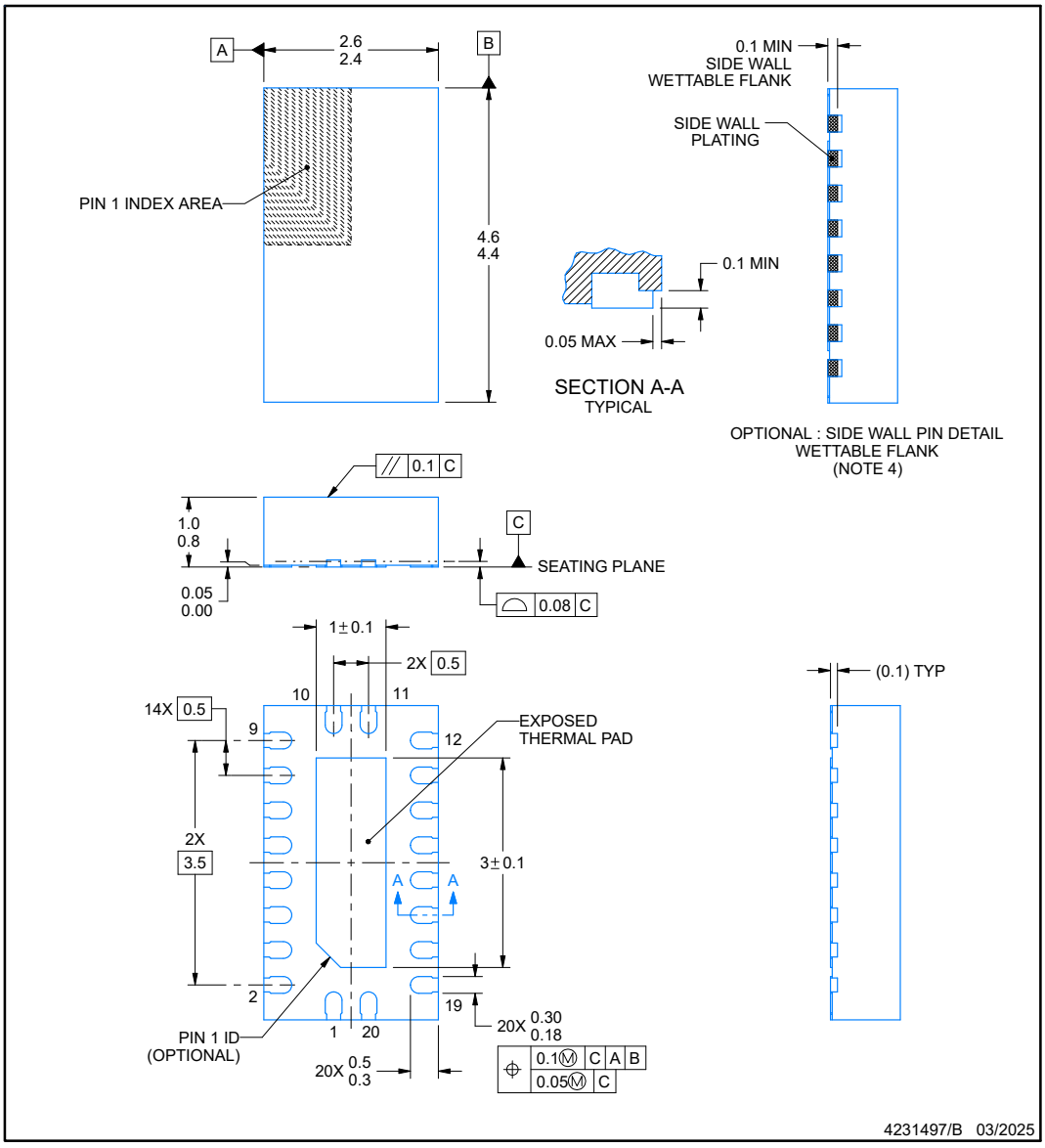
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RKS0020C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



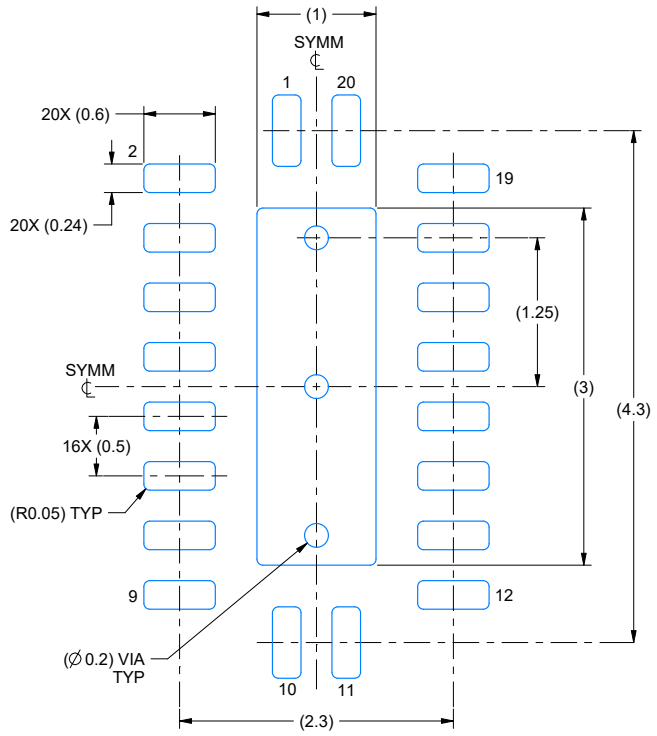
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1mm solder wetting on pins side wall. Available for wettable flank version only

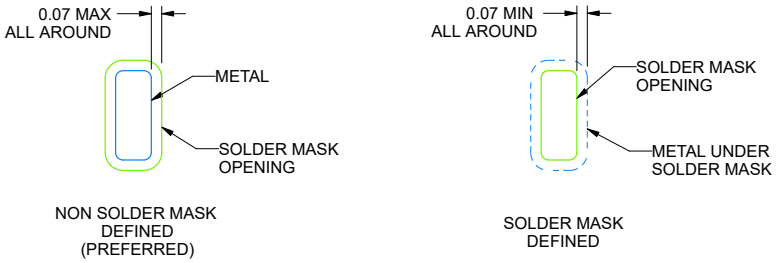
EXAMPLE BOARD LAYOUT

RKS0020C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4231497/B 03/2025

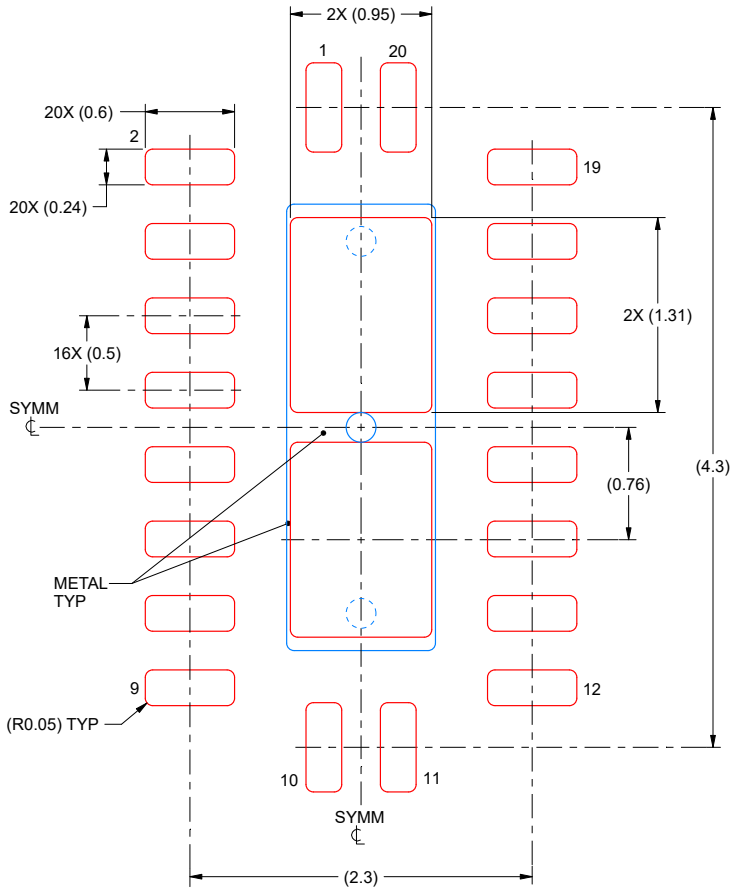
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

RKS0020C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4231497/B 03/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CBTLV3245ADGVRG4	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL245A
74CBTLV3245ADGVRG4.B	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL245A
74CBTLV3245ADWG4	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3245A
74CBTLV3245APWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL245A
74CBTLV3245APWRG4.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL245A
74CBTLV3245ARGYRG4	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL245A
74CBTLV3245ARGYRG4.A	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL245A
74CBTLV3245ARGYRG4.B	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL245A
SN74CBTLV3245ADBQR	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTLV3245A
SN74CBTLV3245ADBQR.A	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTLV3245A
SN74CBTLV3245ADBQR.B	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTLV3245A
SN74CBTLV3245ADGVR	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL245A
SN74CBTLV3245ADGVR.B	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL245A
SN74CBTLV3245ADW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3245A
SN74CBTLV3245ADW.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3245A
SN74CBTLV3245ADWE4	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3245A
SN74CBTLV3245ADWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3245A
SN74CBTLV3245ADWR.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3245A
SN74CBTLV3245APW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	CL245A
SN74CBTLV3245APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	CL245A
SN74CBTLV3245APWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL245A
SN74CBTLV3245APWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL245A
SN74CBTLV3245ARGYR	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	CL245A
SN74CBTLV3245ARGYR.A	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL245A
SN74CBTLV3245ARGYR.B	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL245A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74CBTLV3245A :

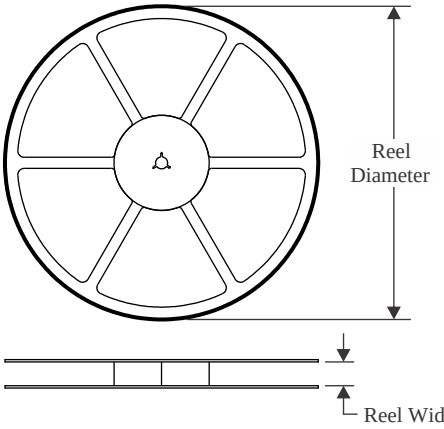
- Automotive : SN74CBTLV3245A-Q1

NOTE: Qualified Version Definitions:

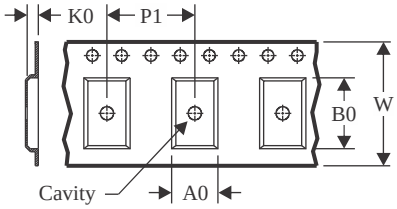
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

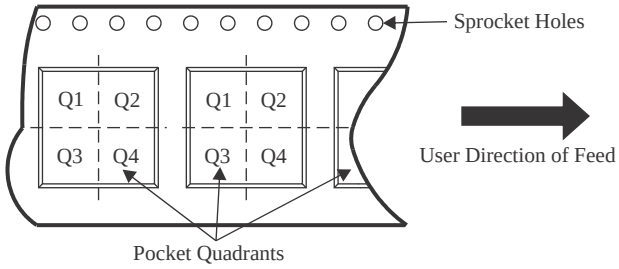


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

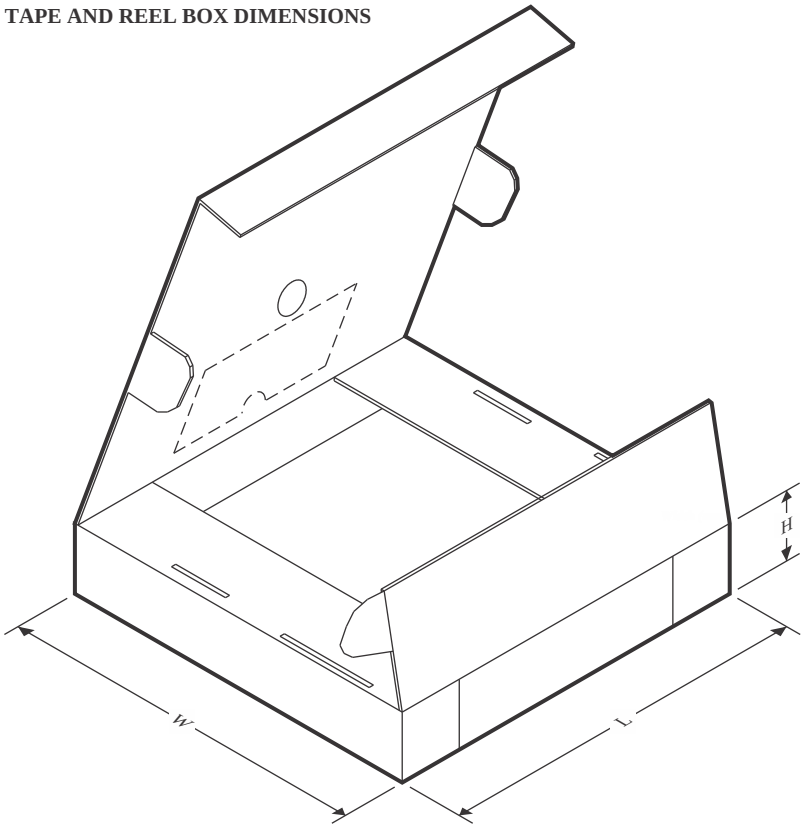
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBTLV3245ADGVRG4	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
74CBTLV3245APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
74CBTLV3245ARGYRG4	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
SN74CBTLV3245ADBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTLV3245ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3245ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74CBTLV3245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74CBTLV3245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74CBTLV3245ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

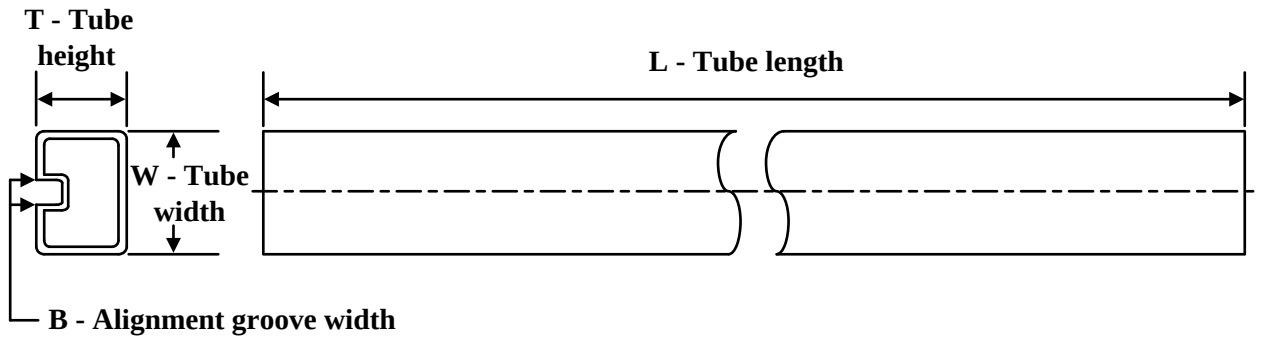
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBTLV3245ADGVRG4	TVSOP	DGV	20	2000	353.0	353.0	32.0
74CBTLV3245APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
74CBTLV3245ARGYRG4	VQFN	RGY	20	3000	353.0	353.0	32.0
SN74CBTLV3245ADBQR	SSOP	DBQ	20	2500	353.0	353.0	32.0
SN74CBTLV3245ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74CBTLV3245ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74CBTLV3245APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74CBTLV3245APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74CBTLV3245ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

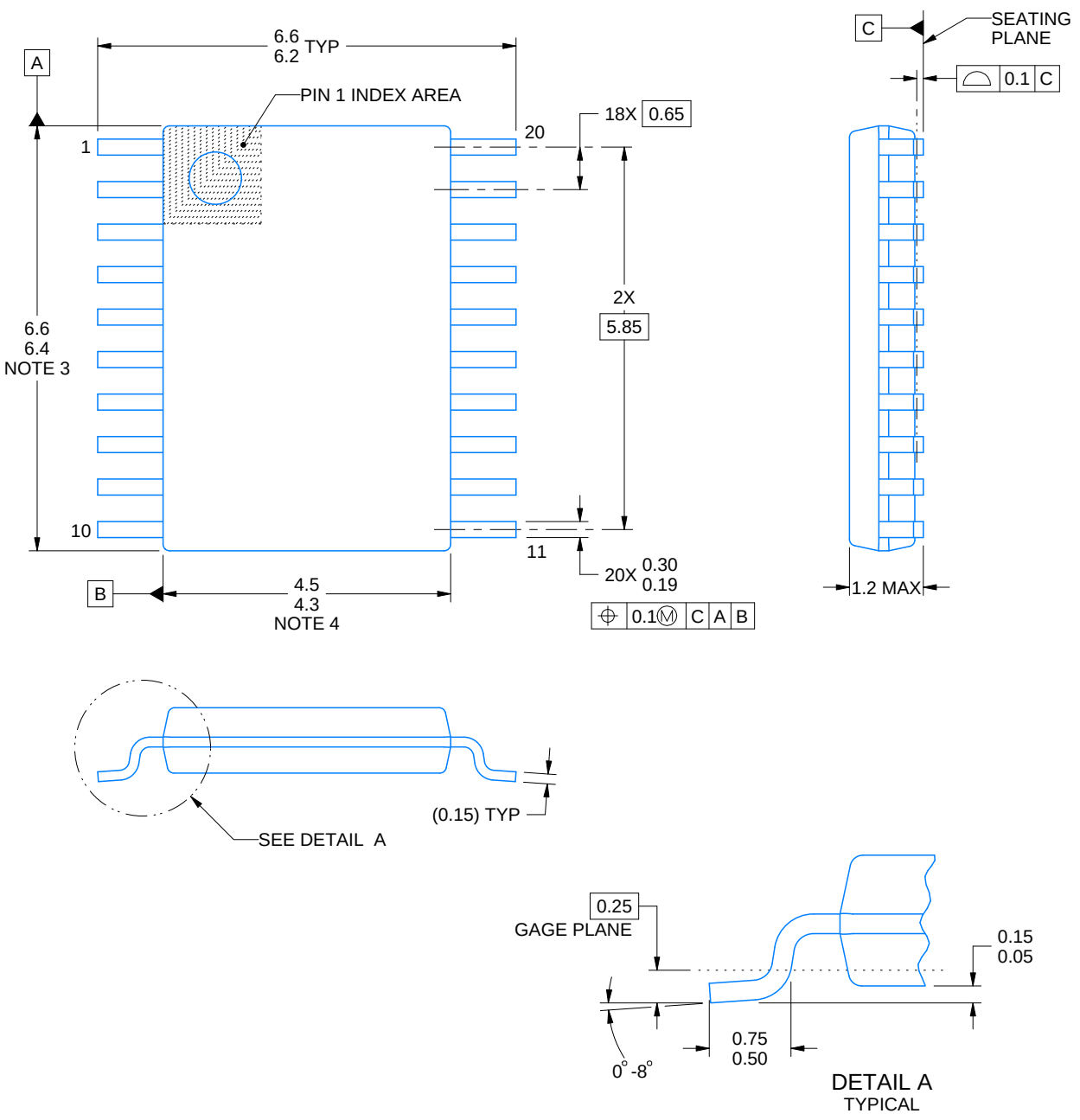
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
74CBTLV3245ADWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CBTLV3245ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CBTLV3245ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CBTLV3245ADWE4	DW	SOIC	20	25	507	12.83	5080	6.6

PACKAGE OUTLINE

PW0020A

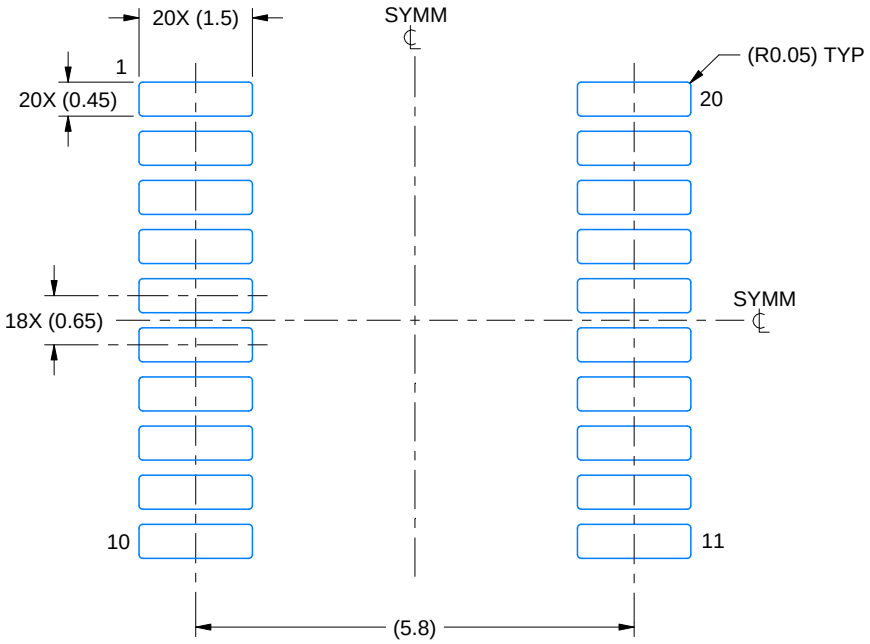
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



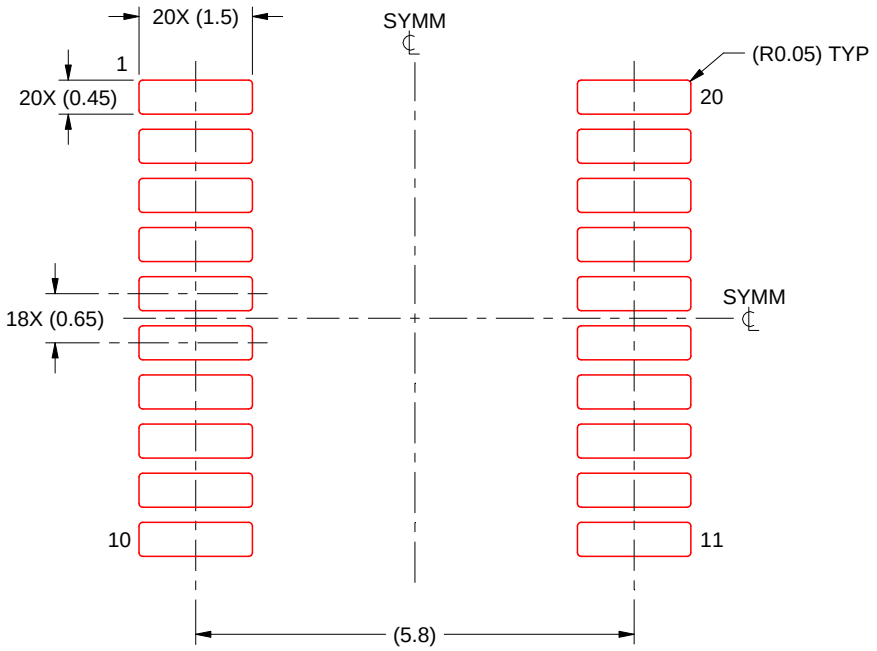
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



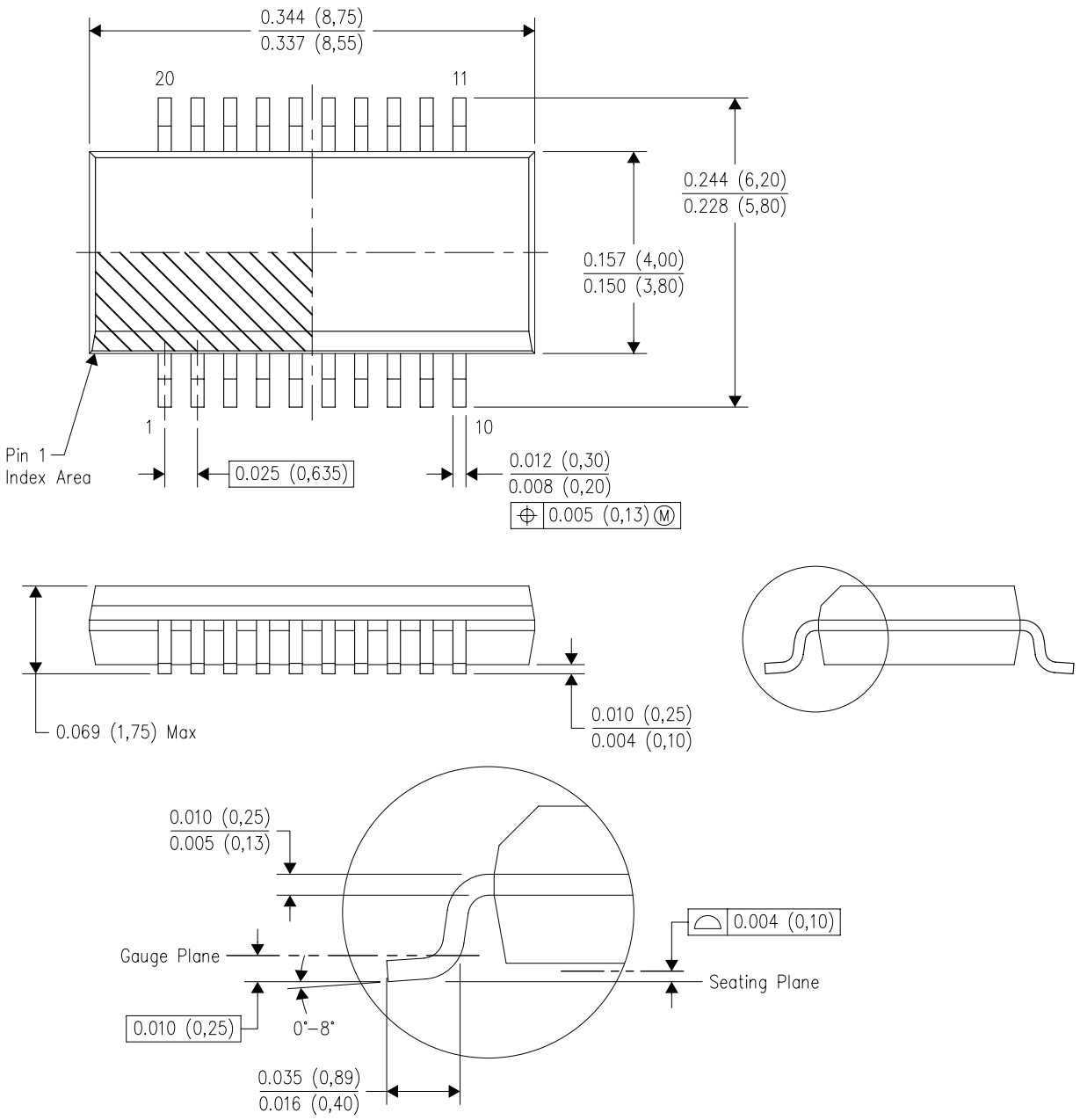
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

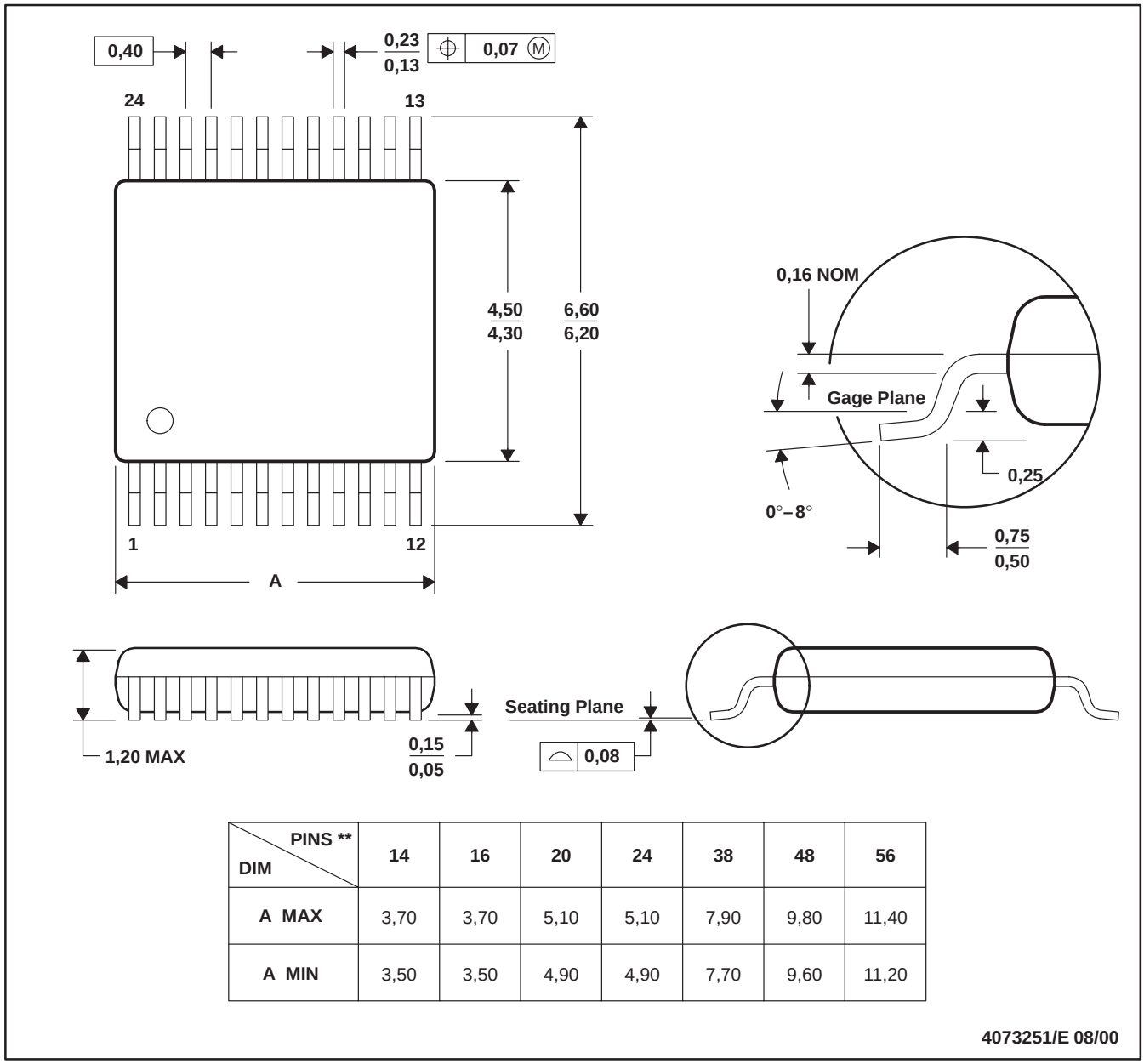
DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

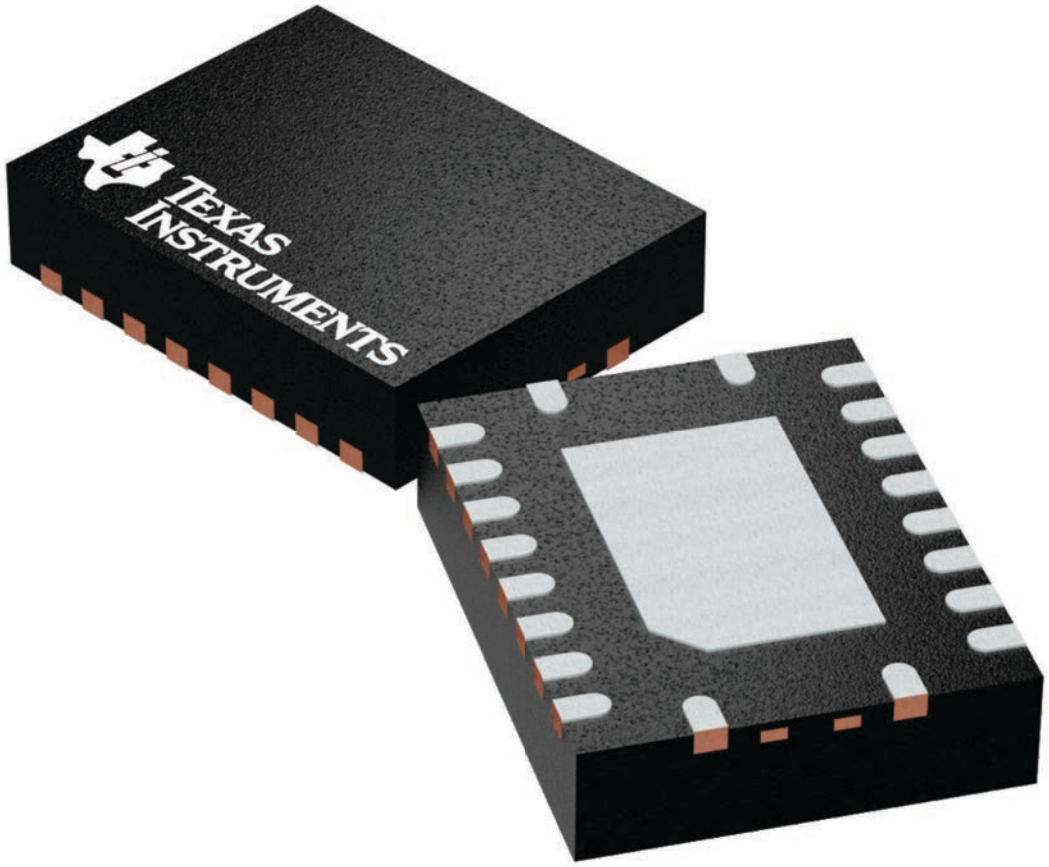
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



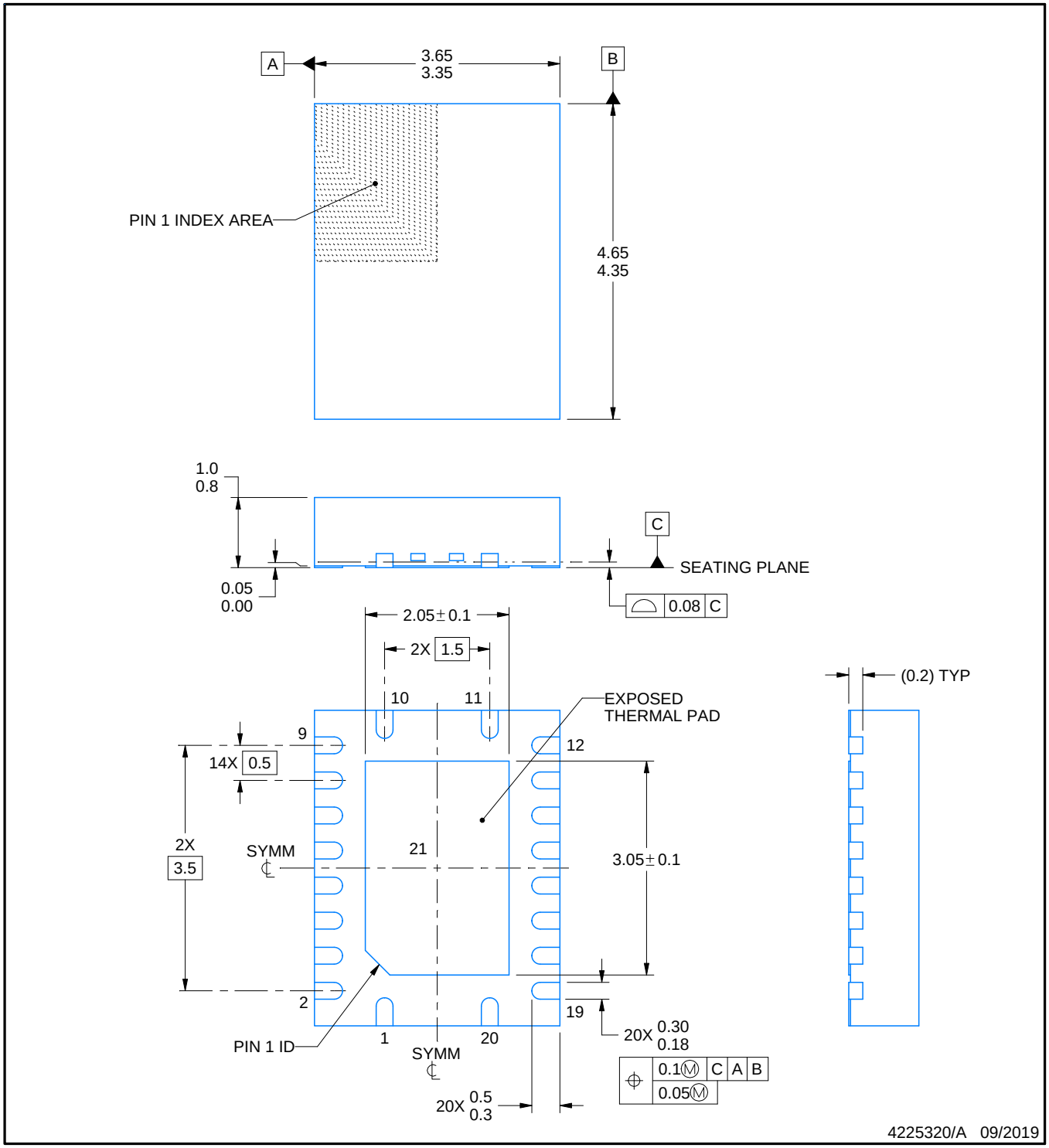
4225264/A

PACKAGE OUTLINE

RGY0020A

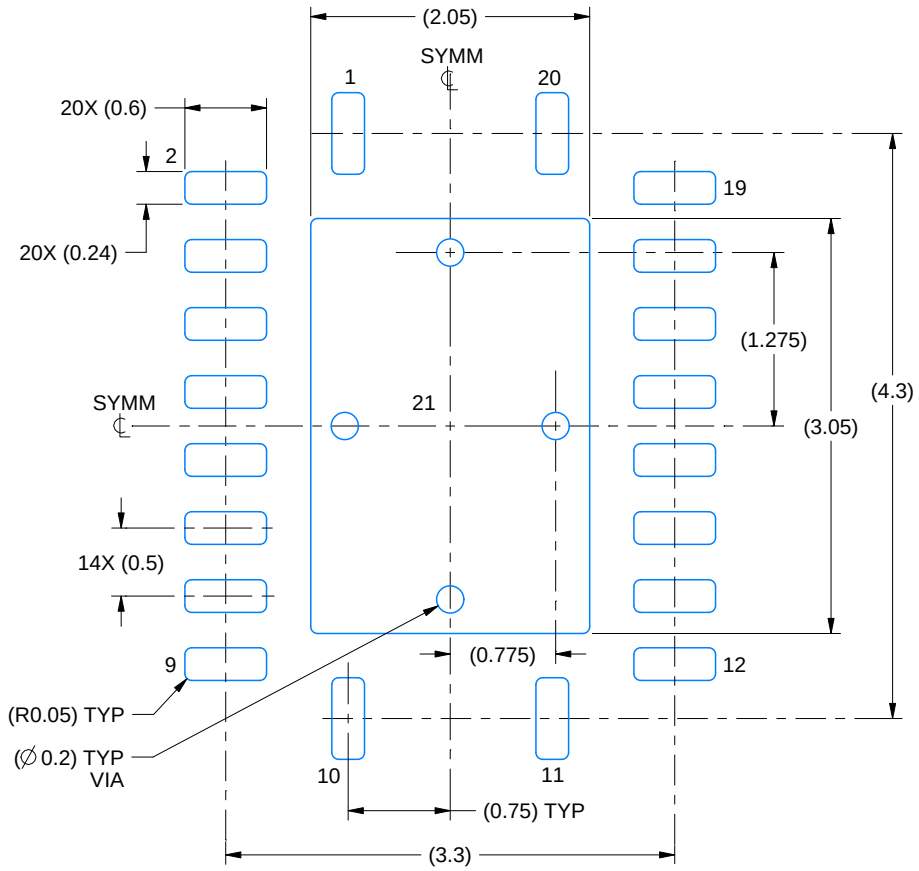
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

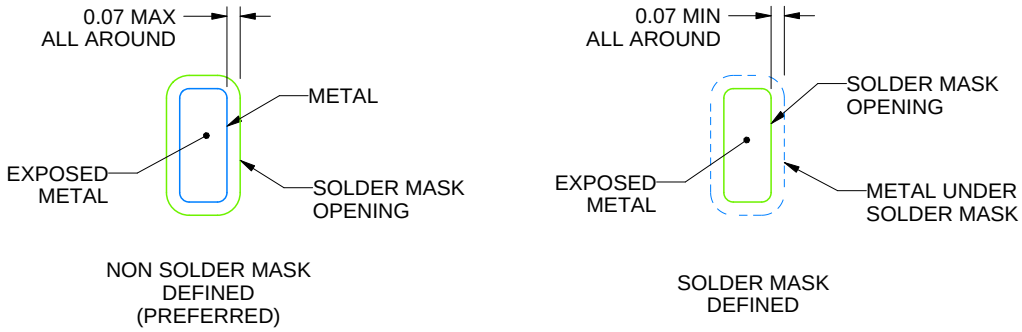


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

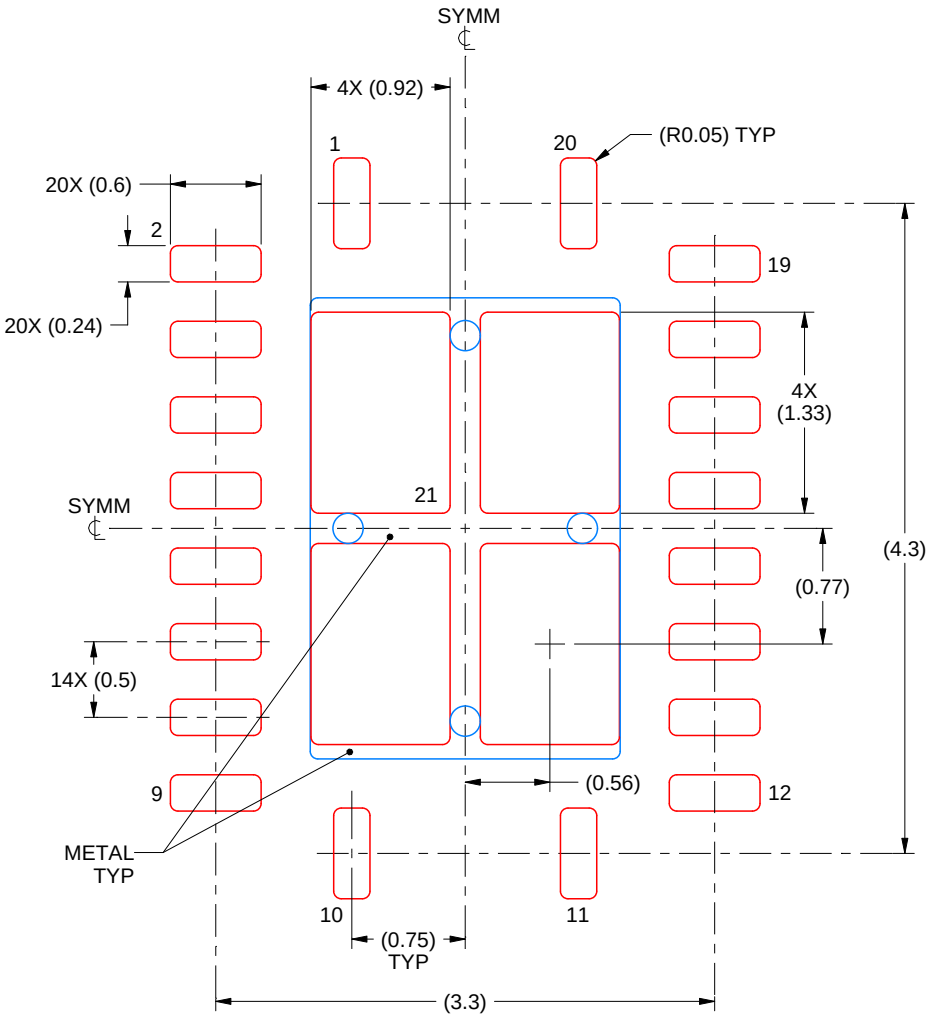


SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



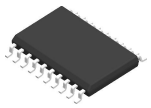
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

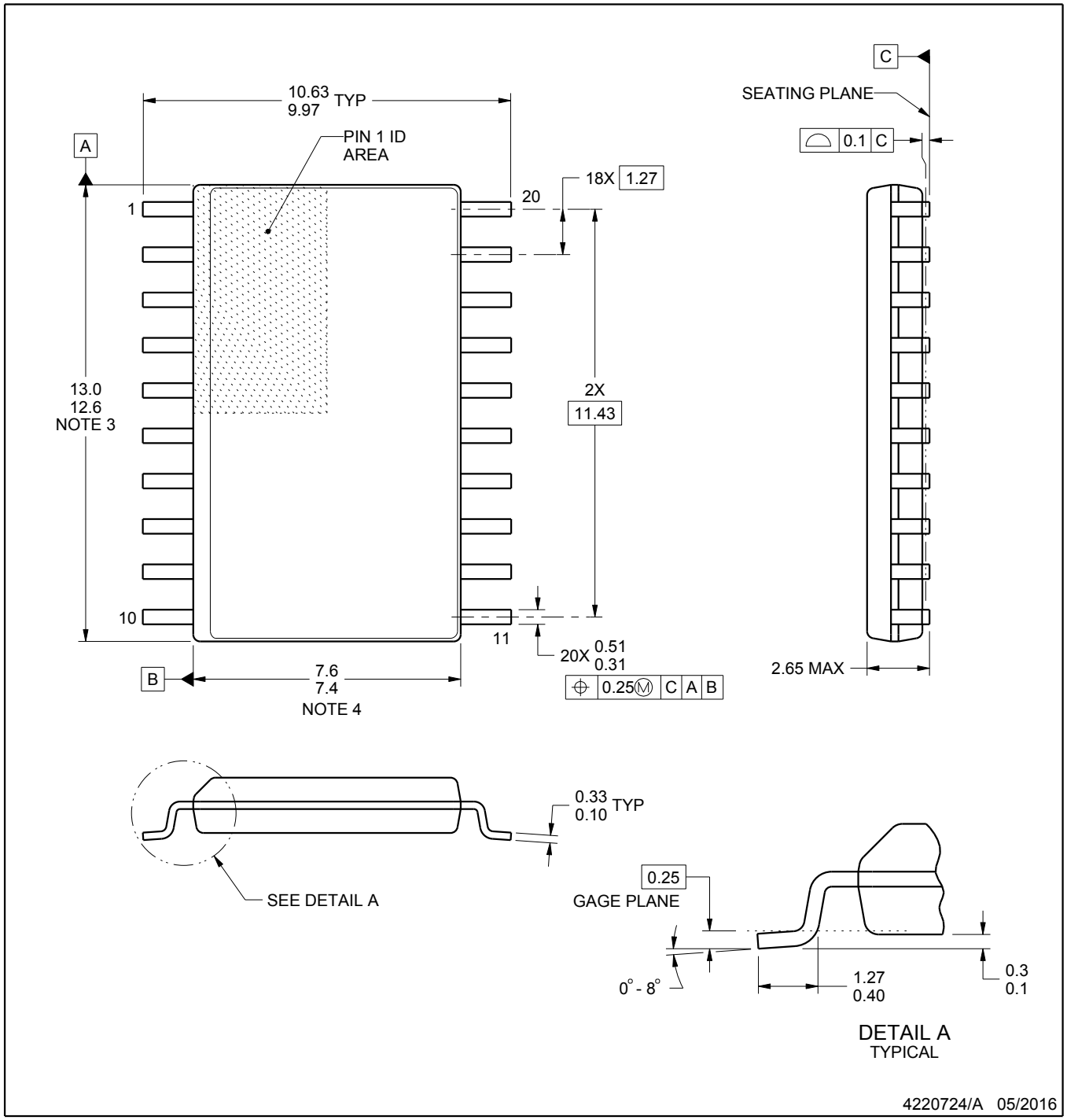


PACKAGE OUTLINE

DW0020A

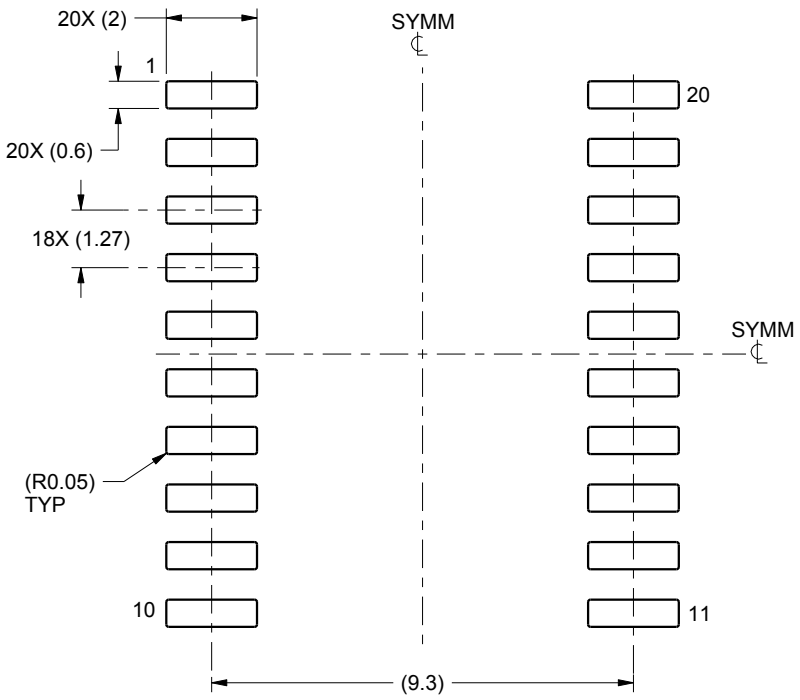
SOIC - 2.65 mm max height

SOIC

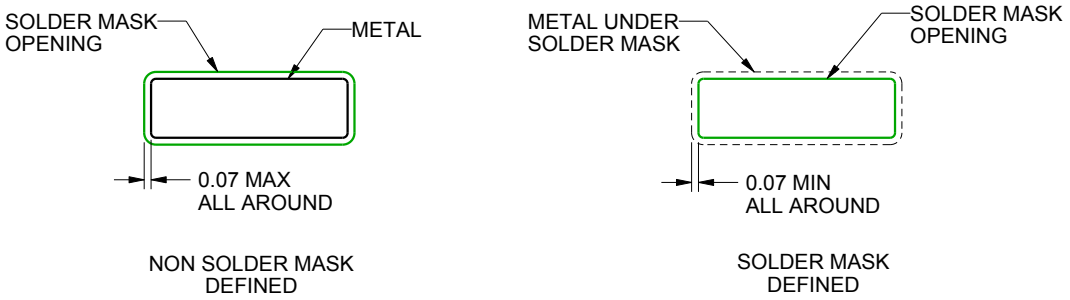


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

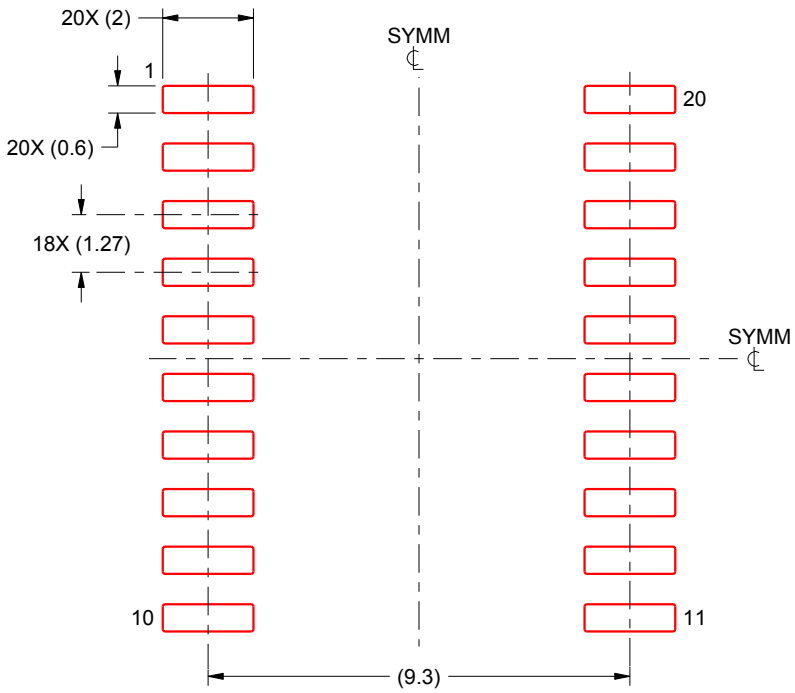


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月