SN74CB3Q3245 8-Bit FET Bus Switch 2.5V/3.3V Low-Voltage High-Bandwidth Bus Switch

1 Features

- High-Bandwidth Data Path (up to 500MHz)
- Equivalent to IDTQS3VH384 Device
- 5V Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4Ω Typ)
- Rail-to-Rail Switching on Data I/O Ports
  - 0 to 5V Switching With 3.3V V_{CC}
  - 0 to 3.3V Switching With 2.5V V_{CC}
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5pF Typ)
- Fast Switching Frequency ($f_{\overline{OE}}$ = 20MHz Max)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 1mA Typical)
- V_{CC} Operating Range From 2.3V to 3.6V
- Data I/Os Support 0 to 5V Signaling Levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)
- Control Inputs Can Be Driven by TTL or 5V/3.3V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000V Human-Body Model (A114B, Class II)
  - 1000V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

2 Description

The SN74CB3Q3245 device is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3245 device provides an optimized interface device designed for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3245 device is organized as an 8-bit bus switch with a single output-enable ($\overline{OE}$) input. When $\overline{OE}$ is low, the bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the bus switch is OFF and a high-impedance state exists between the A and B ports.

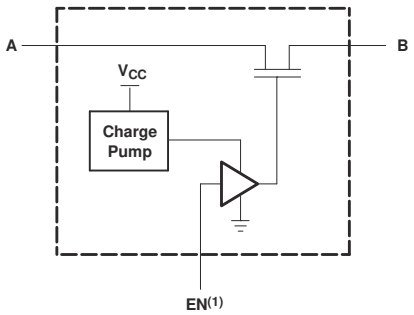
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when the device is powered down. The device has isolation during power off.

To verify the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN74CB3Q3245	DBQ (SSOP, 20)	8.65mm × 3.90mm
	DGV (TVSOP, 20)	5.00mm × 4.40mm
	PW (TSSOP, 20)	6.50mm × 4.40mm
	RGY (VQFN, 20)	4.50mm × 3.50mm

(1) For all available packages, see Section 8.



(1) EN is the internal enable signal applied to the switch.

Simplified Schematic, Each FET Switch (SW)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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3 Pin Configuration and Functions

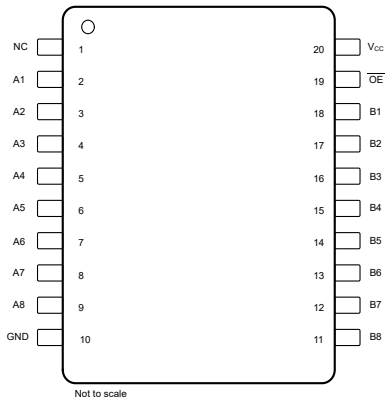


Figure 3-1. DBQ, DGV, or PW Package, SOP 20-Pins (Top View)

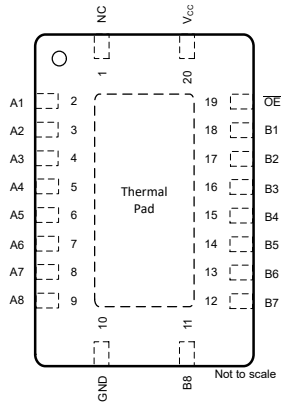


Figure 3-2. RGY Package, VQFN 20-Pins (Top View)

Table 3-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
N.C.	1		No internal connection. Can be shorted to GND or left floating
A1	2	I/O	Input/output pin
A2	3	I/O	Input/output pin
A3	4	I/O	Input/output pin
A4	5	I/O	Input/output pin
A5	6	I/O	Input/output pin
A6	7	I/O	Input/output pin
A7	8	I/O	Input/output pin
A8	9	I/O	Input/output pin
GND	10	P	Ground (0V) reference
B8	11	I/O	Input/output pin
B7	12	I/O	Input/output pin
B6	13	I/O	Input/output pin
B5	14	I/O	Input/output pin
B4	15	I/O	Input/output pin
B3	16	I/O	Input/output pin
B2	17	I/O	Input/output pin
B1	18	I/O	Input/output pin
$\overline{OE}$	19	I	Output Enable, active low
V_{CC}	20	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD and GND.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

Table 3-2. Function Table

INPUTS	FUNCTION
$\overline{OE}$	
L	A port = B port
H	Disconnect

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
I_{IO}	ON-state switch current(5)			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance	DBQ package(6)		68	°C/W
		DGV package(6)		92	
		GQN package(6)		78	
		PW package(6)		83	
		RGY package(7)		37	
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* can cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device can not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.
(7) The package thermal impedance is calculated in accordance with JESD 51-5.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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4.3 Recommended Operating Conditions

	(1)		MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3V to 2.7V	1.7	5.5	V
		V_{CC} = 2.7V to 3.6V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3V to 2.7V	0	0.7	V
		V_{CC} = 2.7V to 3.6V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to verify proper device operation. See also the *Implications of Slow or Floating CMOS Inputs* application note.

4.4 Thermal Information

THERMAL METRIC(1)		SN74CB3Q3245				UNIT
		DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.04	115.29	100.43	71.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.05	53.21	44.99	68	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.25	73.71	62.48	46.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.01	12.58	9.33	19.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.55	73.12	62.00	46.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	31.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{IK}		V_{CC} = 3.6V,	I_I = –18mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6V,	V_{IN} = 0 to 5.5V				±1	µA
I_{OZ}(3)		V_{CC} = 3.6V,	V_O = 0 to 5.5V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		1	2	mA
ΔI_{CC}(4)	Control inputs	V_{CC} = 3.6V,	One input at 3V,	Other inputs at V_{CC} or GND			30	µA
I_{CCD}(5)	Per control input	V_{CC} = 3.6V, Control input switching at 50% duty cycle	A and B ports open,			0.3	0.45	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3V,	V_{IN} = 5.5V, 3.3V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5V, 3.3V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5V, 3.3V, or 0		9	11	pF
r_{on}(6)		V_{CC} = 2.3V, TYP at V_{CC} = 2.5V	V_I = 0,	I_O = 30mA		4	8	Ω
			V_I = 1.7V,	I_O = –15mA		4.5	9	
		V_{CC} = 3V	V_I = 0,	I_O = 30mA		4	6	
			V_I = 2.4V,	I_O = –15mA		4	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

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(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 4-2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

4.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Test Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$(1)	$\overline{OE}$	A or B		10		20	MHz
t_{pd}(2)	A or B	B or A		0.12		0.20	ns
t_{en}	$\overline{OE}$	A or B	1.5	11	1.5	14	ns
t_{dis}	$\overline{OE}$	A or B	1	16	1	13	ns

(1) Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5V, $R_L \geq 1M\Omega$, C_L = 0)
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

4.7 Typical Characteristics

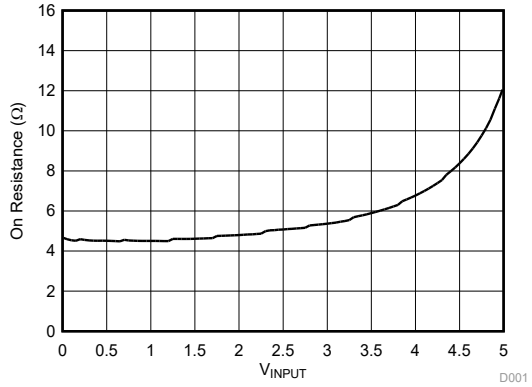


Figure 4-1. Typical r_{on} vs V_I

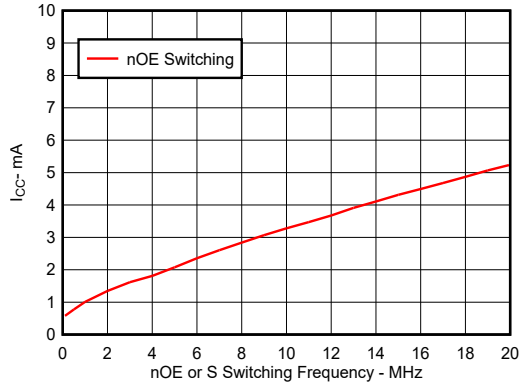
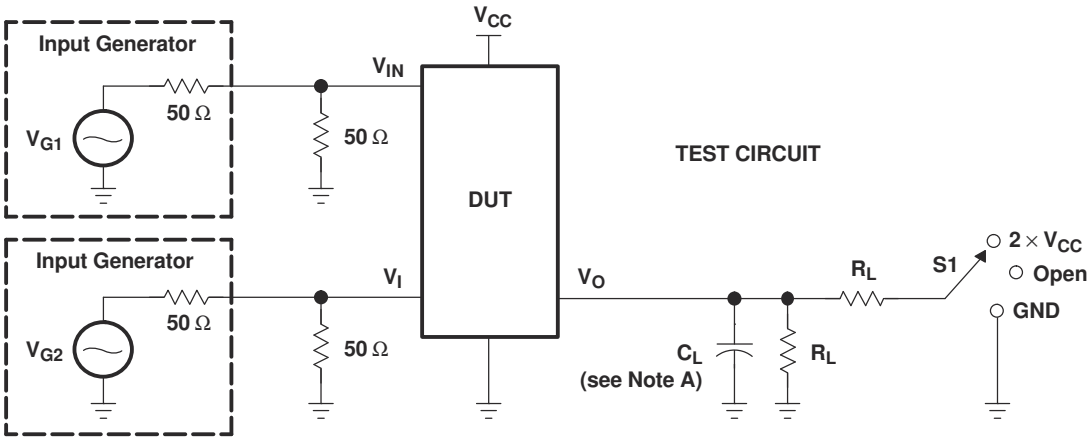


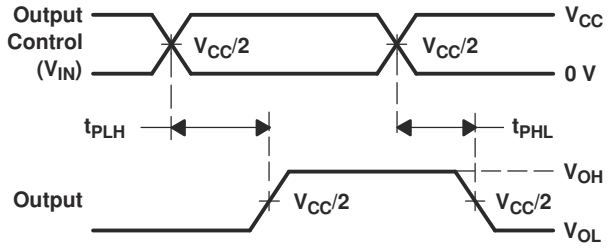
Figure 4-2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency

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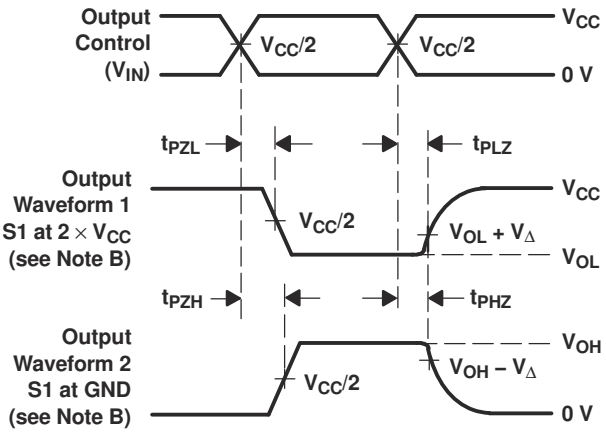
5 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Test Circuit and Voltage Waveforms

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6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2026) to Revision D (October 2026)	Page
• Added Pin Configuration and Functions	3
• Updated Thermal Information	5

Changes from Revision B (March 2005) to Revision C (August 2026)	Page
• Deleted the GQN package from the document	1
• Updated the number formatting for tables, figures, and cross-references throughout the document	1
• Removed Ordering Information table.	1
• Added the ESD Ratings table	4
• Added the *Thermal Information* table and moved $R_{\theta JA}$ values to the table	5
• Updated the maximum *Per input control* parameter in the *Electrical Characteristics* table from 0.35 to 0.45	5
• Updated the maximum V_{CC} rating for t_{en} and t_{dis} in the *Switching Characteristics* table	6

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8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CB3Q3245DBQR	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3Q3245
SN74CB3Q3245DBQR.B	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3Q3245
SN74CB3Q3245DGVR	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU245
SN74CB3Q3245DGVR.B	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU245
SN74CB3Q3245DGVRG4	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU245
SN74CB3Q3245DGVRG4.B	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU245
SN74CB3Q3245PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	BU245
SN74CB3Q3245PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU245
SN74CB3Q3245PWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU245
SN74CB3Q3245RGYR	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU245
SN74CB3Q3245RGYR.B	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU245

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

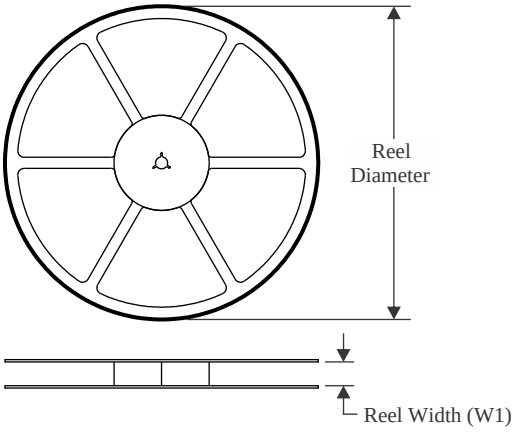
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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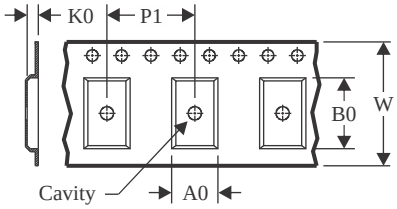
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

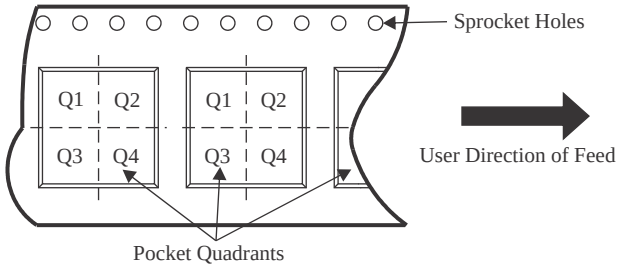


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

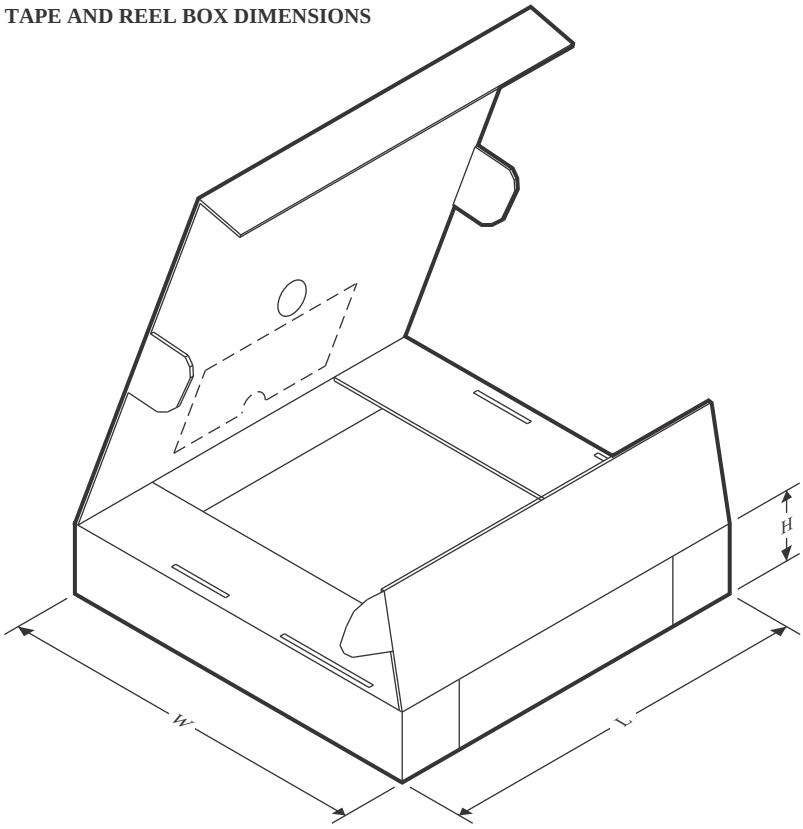
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3245DBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3Q3245DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3245DGVRG4	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74CB3Q3245RGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

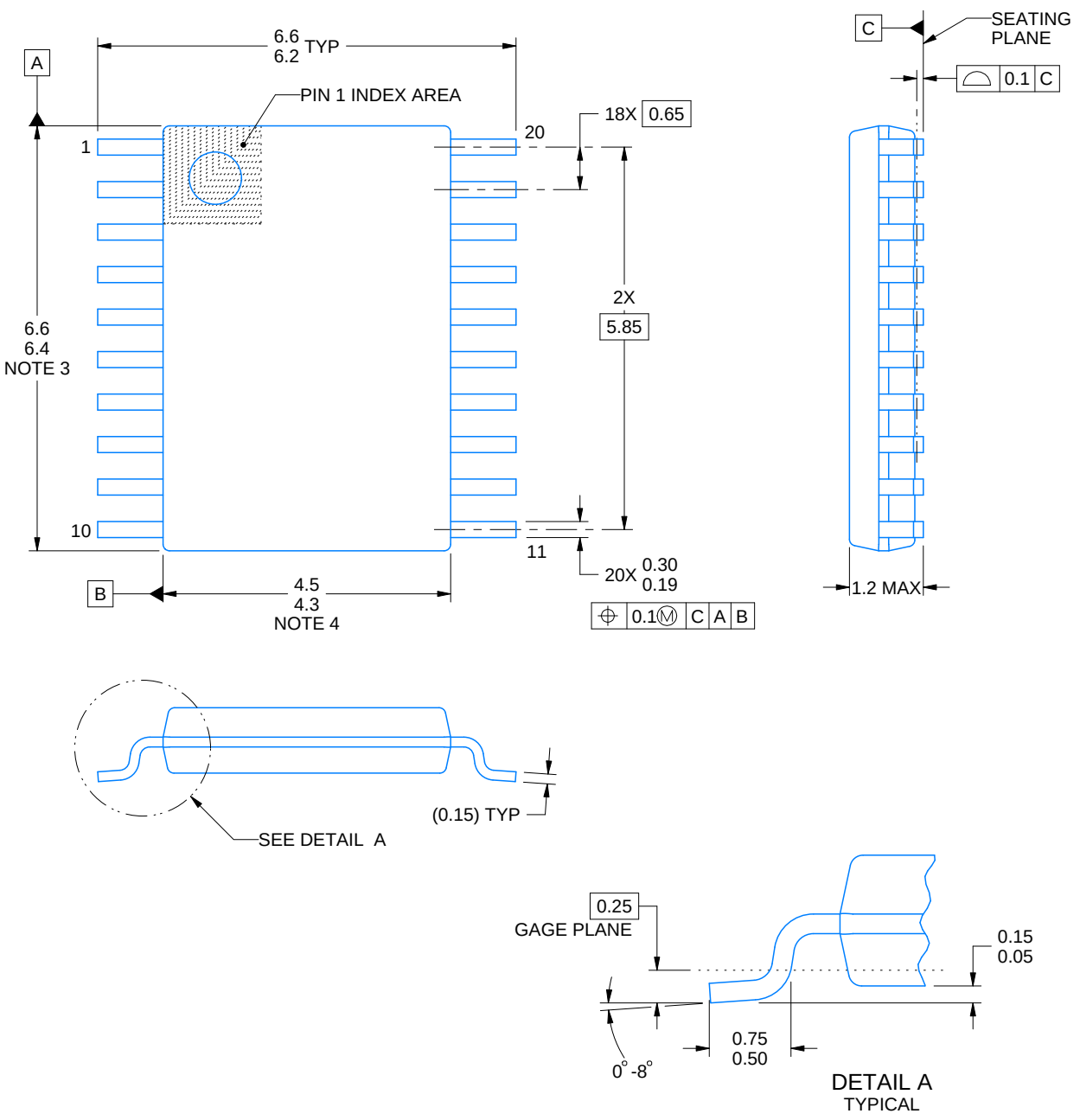
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3245DBQR	SSOP	DBQ	20	2500	353.0	353.0	32.0
SN74CB3Q3245DGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74CB3Q3245DGVRG4	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74CB3Q3245PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74CB3Q3245RGYR	VQFN	RGY	20	3000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0020A

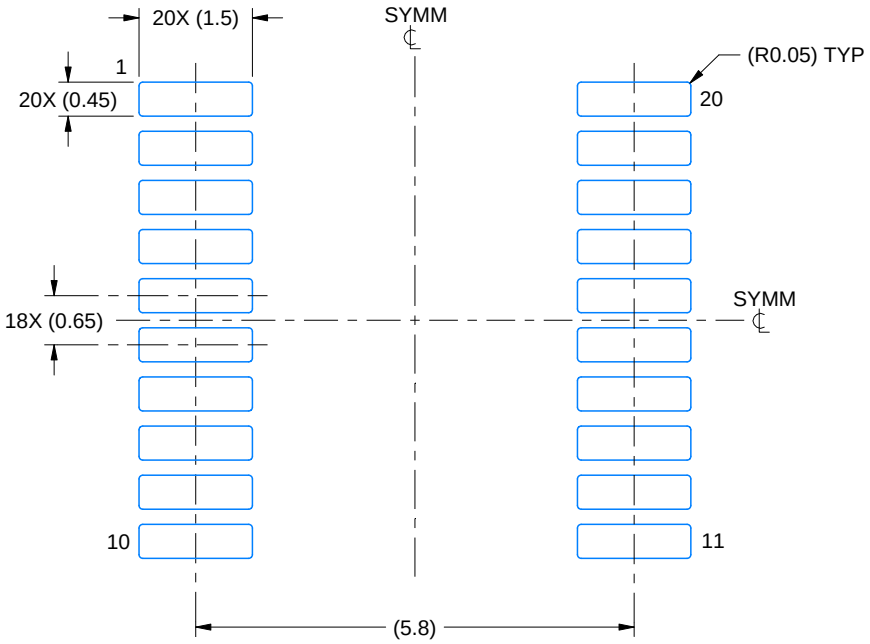
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

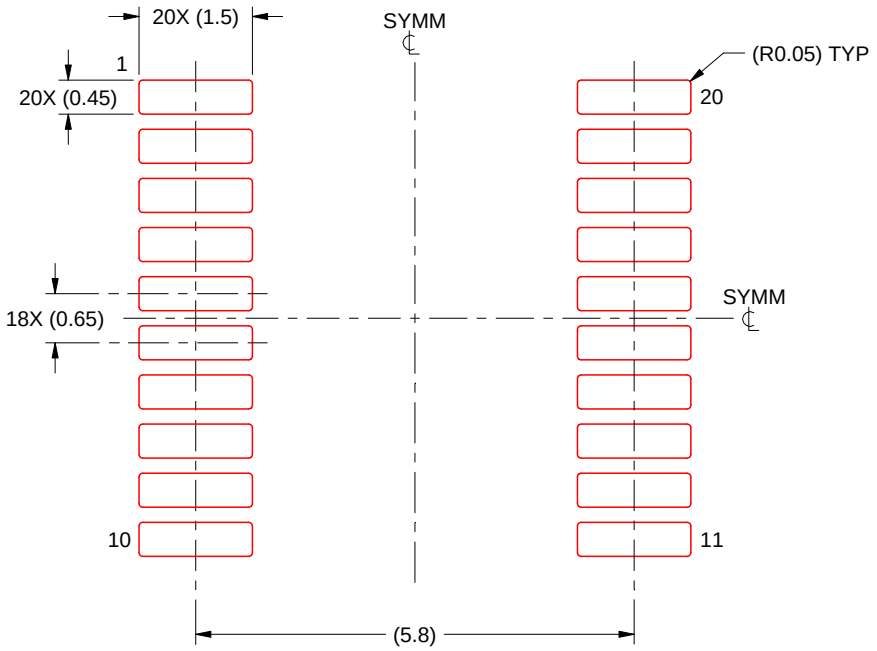


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



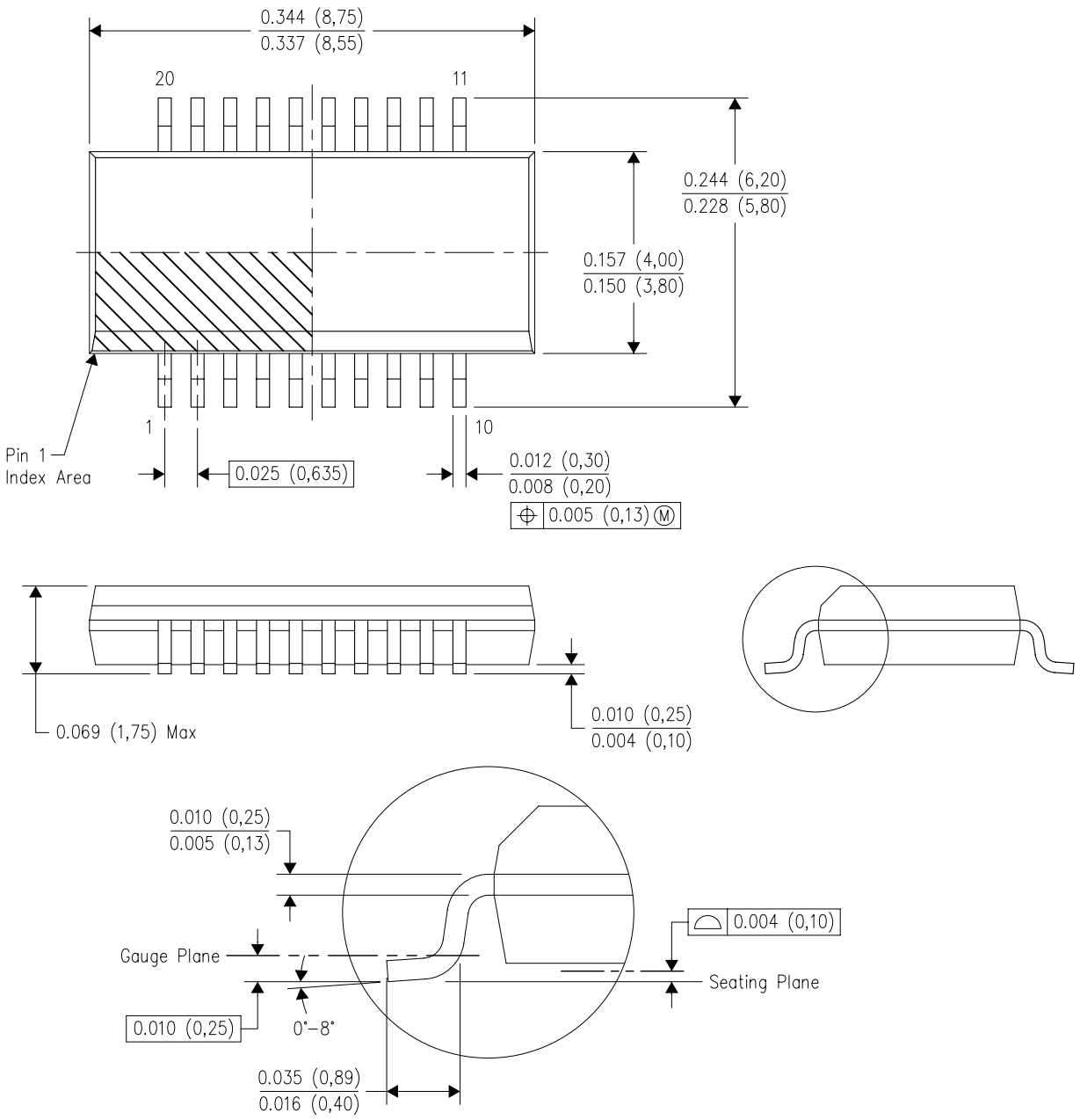
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

GENERIC PACKAGE VIEW

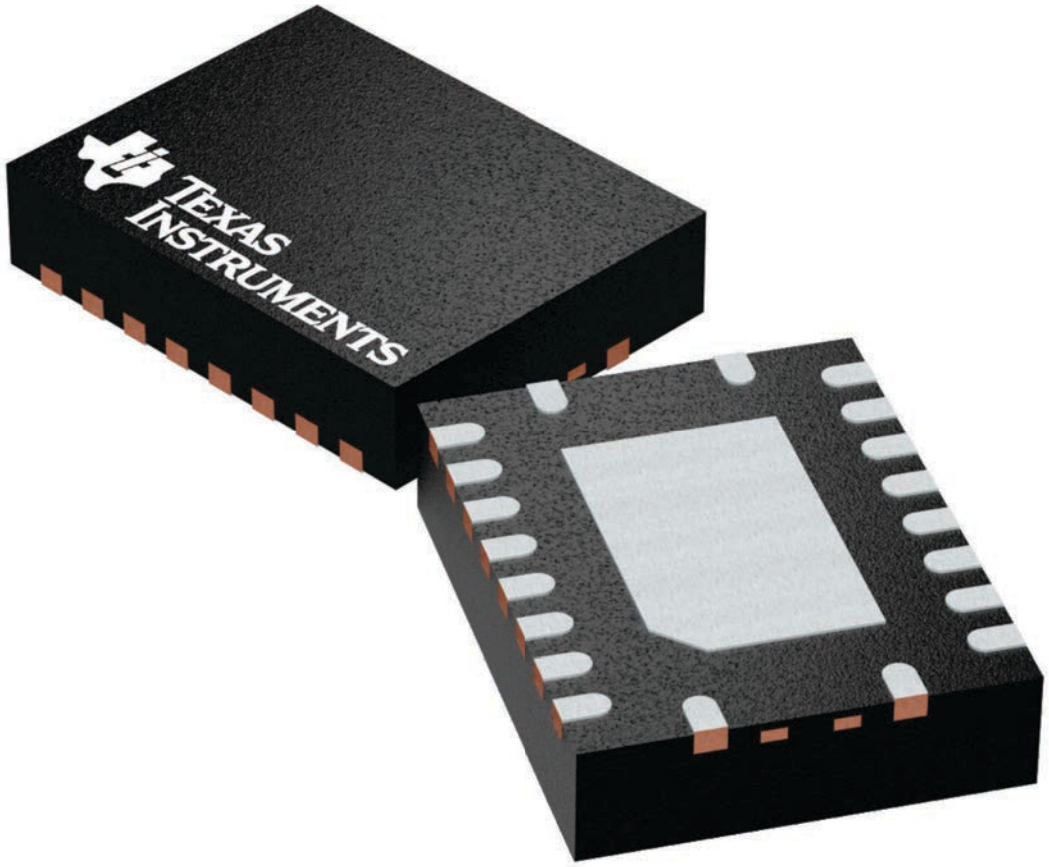
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A

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