# SN74AVCH2T45 具有可配置电平转换和三态输出的 2 位 2 电源总线收发器

## 1 特性

- 采用德州仪器 (TI) NanoFree™ 封装
- $V_{CC}$ 隔离
- 2 轨设计
- I/O 可承受 4.6V 的电压
- 局部省电模式运行
- 总线保持数据输入
- 最大数据速率
  - 500Mbps（1.8V 至 3.3V）
  - 320Mbps（< 1.8V 至 3.3V）
  - 320Mbps（电平转换至 2.5V 或 1.8V）
  - 280Mbps（电平转换至 1.5V）
  - 240Mbps（电平转换至 1.2V）
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求

## 2 应用

- 智能手机
- 服务器
- 台式计算机和笔记本电脑
- 其他便携式设备

## 3 说明

这款 2 位同相总线收发器使用两个独立的可配置电源轨。A 端口用于跟踪 $V_{CCA}$，可支持 1.2V 至 3.6V 范围内的任何电源电压。B 端口用于跟踪 $V_{CCB}$，可支持 1.2V 至 3.6V 范围内的任何电源电压。因此可在 1.2V、1.5V、1.8V、2.5V 和 3.3V 电压节点之间进行通用的低压双向转换和电平转换。

SN74AVCH2T45 旨在实现两条数据总线间的异步通信。方向控制（DIR 引脚）输入的逻辑电平会激活 B 端口或 A 端口输出。当 B 端口输出被激活时，此器件将数据从 A 总线发送到 B 总线，而当 A 端口输出被激活时，此器件将数据从 B 总线发送到 A 总线。SN74AVCH2T45 具备有源总线保持电路会将未使用或未驱动的输入保持在有效逻辑状态。TI 不建议在总线保持电路上使用上拉或下拉电阻。

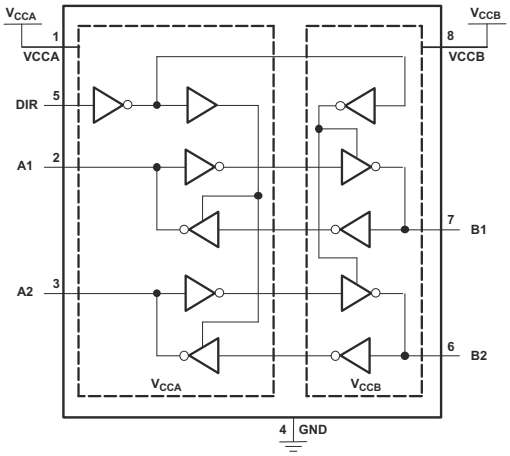
该器件专用于使用 $I_{off}$ 的局部断电应用。$I_{off}$ 电路可禁用输出，以防在器件断电时电流回流对器件造成损坏。$V_{CC}$ 隔离特性可确保当任一 $V_{CC}$ 输入接地时，两个输出都处于高阻抗状态。上电侧的总线保持电路始终保持有效状态。

有源总线保持电路会将未使用或未驱动的输入保持在有效逻辑状态。NanoFree 封装技术是 IC 封装概念的一项重大突破，它将硅晶片用作封装。

**封装信息**

| 器件型号 | 封装 (1) | 封装尺寸 (2) |
|---|---|---|
| SN74AVCH2T45 | DCT（SSOP，8） | 2.95mm × 4.00mm |
| | DCU（VSSOP，8） | 3.10mm × 2.00mm |
| | YZP（DSBGA，8） | 1.89mm × 0.89mm |

(1) 有关更多信息，请参阅节 11
(2) 封装尺寸（长 × 宽）为标称值并包括引脚（如适用）




逻辑图（正逻辑）

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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# 4 Pin Configurations and Functions

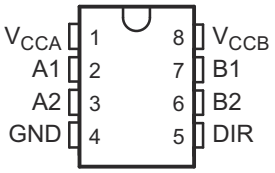


**图 4-1. DCT and DCU Packages 8-Pin SSOP and VSSOP Top View**

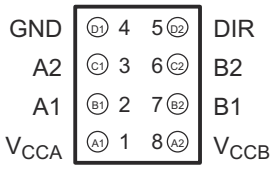


**图 4-2. YZP Package 8-Pin DSBGA Bottom View**

**表 4-1. Pin Functions**

| PIN | | | DESCRIPTION |
|---|---|---|---|
| NAME | SSOP, VSSOP | DSBGA | |
| VCCA | 1 | A1 | Supply Voltage A |
| VCCB | 8 | A2 | Supply Voltage B |
| GND | 4 | D1 | Ground |
| A1 | 2 | B1 | Output or input depending on state of DIR. Output level depends on $V_{CCA}$. |
| A2 | 3 | C1 | Output or input depending on state of DIR. Output level depends on $V_{CCA}$. |
| B1 | 7 | B2 | Output or input depending on state of DIR. Output level depends on $V_{CCB}$. |
| B2 | 6 | C2 | Output or input depending on state of DIR. Output level depends on $V_{CCB}$. |
| DIR | 5 | D2 | Direction Pin, Connect to GND or to VCCA. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ $V_{CCB}$ | Supply voltage | | – 0.5 | 4.6 | V |
| $V_I$ | Input voltage[2] | I/O ports (A port) | – 0.5 | 4.6 | V |
| | | I/O ports (B port) | – 0.5 | 4.6 | |
| | | Control inputs | – 0.5 | 4.6 | |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state[2] | A port | – 0.5 | 4.6 | V |
| | | B port | – 0.5 | 4.6 | |
| $V_O$ | Voltage range applied to any output in the high or low state[2] [3] | A port | – 0.5 | $V_{CCA}$ + 0.5 | V |
| | | B port | – 0.5 | $V_{CCB}$ + 0.5 | |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | – 50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | – 50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CCA}$, $V_{CCB}$, or GND | | | ±100 | mA |
| $T_J$ | Junction temperature | | – 40 | 150 | °C |
| $T_{stg}$ | Storage temperature | | – 65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *节 5.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±8000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 | |
| | | Machine Model (MM), Per JEDEC specification JESD22-A115-A | ±200 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.


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## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[3] [4] [5]

| | | | $V_{CCI}$ [1] | $V_{CCO}$ [2] | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | | 1.2 | | 3.6 | V |
| $V_{CCB}$ | Supply voltage | | | | 1.2 | | 3.6 | V |
| $V_{IH}$ | High-level input voltage | Data inputs[4] | 1.2V to 1.95V | | $V_{CCI}$ [1] × 0.65 | | | V |
| | | | 1.95V to 2.7V | | 1.6 | | | |
| | | | 2.7V to 3.6V | | 2 | | | |
| $V_{IL}$ | Low-level input voltage | Data inputs[4] | 1.2V to 1.95V | | | | $V_{CCI}$ [1] × 0.35 | V |
| | | | 1.95V to 2.7V | | | | 0.7 | |
| | | | 2.7V to 3.6V | | | | 0.8 | |
| $V_{IH}$ | High-level input voltage | DIR (referenced to $V_{CCA}$)[5] | 1.2V to 1.95V | | $V_{CCA}$ × 0.65 | | | V |
| | | | 1.95 V to 2.7V | | 1.6 | | | |
| | | | 2.7V to 3.6V | | 2 | | | |
| $V_{IL}$ | Low-level input voltage | DIR (referenced to $V_{CCA}$)[5] | 1.2V to 1.95V | | | | $V_{CCA}$ × 0.35 | V |
| | | | 1.95V to 2.7V | | | | 0.7 | |
| | | | 2.7V to 3.6V | | | | 0.8 | |
| $V_I$ | Input voltage | | | | 0 | | 3.6 | V |
| $V_O$ | Output voltage | Active state | | | 0 | | $V_{CCO}$ [2] | V |
| | | 3-state | | | 0 | | 3.6 | |
| $I_{OH}$ | High-level output current | | | 1.2V | | | –3 | mA |
| | | | | 1.4V to 1.6V | | | –6 | |
| | | | | 1.65V to 1.95V | | | –8 | |
| | | | | 2.3V to 2.7V | | | –9 | |
| | | | | 3V to 3.6V | | | –12 | |
| $I_{OL}$ | Low-level output current | | | 1.2V | | | 3 | mA |
| | | | | 1.4V to 1.6V | | | 6 | |
| | | | | 1.65V to 1.95V | | | 8 | |
| | | | | 2.3V to 2.7V | | | 9 | |
| | | | | 3V to 3.6V | | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | | | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | | | –40 | | 85 | °C |

(1) $V_{CCI}$ is the voltage associated with the input port supply VCCA or VCCB.
(2) $V_{CCO}$ is the voltage associated with the output port supply VCCA or VCCB.
(3) All unused data inputs of the device must be held at $V_{CCI}$ or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.
(4) For $V_{CCI}$ values not specified in the data sheet, $V_{IH}$ min = $V_{CCI}$ × 0.7V, $V_{IL}$ max = $V_{CCI}$ × 0.3V.
(5) For $V_{CCI}$ values not specified in the data sheet, $V_{IH}$ min = $V_{CCA}$ × 0.7V, $V_{IL}$ max = $V_{CCA}$ × 0.3V.

## 5.4 Thermal Information

| THERMAL METRIC [1] | | SN74AVCH2T45 | | | UNIT |
|---|---|---|---|---|---|
| | | DCT (SSOP) | DCU (VSSOP) | YZP (DSBGA) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 183.1 | 246.9 | 105.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 101.5 | 95.2 | 1.6 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 111.0 | 158.4 | 10.8 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 27.6 | 34.1 | 3.1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 109.2 | 157.5 | 10.8 | |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[5] [6]

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | $V_{CCB}$ | $T_A$ = 25°C | | | – 40°C to 85°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ [7] | | $I_{OH}$ = – 100 µA | $V_I = V_{IH}$ | 1.2V to 3.6V | 1.2V to 3.6V | | | | $V_{CCO}$ – 0.2 | | | V |
| | | $I_{OH}$ = – 3mA | | 1.2V | 1.2V | | 0.95 | | | | | |
| | | $I_{OH}$ = – 6mA | | 1.4V | 1.4V | | | | 1.05 | | | |
| | | $I_{OH}$ = – 8mA | | 1.65V | 1.65V | | | | 1.2 | | | |
| | | $I_{OH}$ = – 9mA | | 2.3V | 2.3V | | | | 1.75 | | | |
| | | $I_{OH}$ = – 12mA | | 3V | 3V | | | | 2.3 | | | |
| $V_{OL}$ [7] | | $I_{OL}$ = 100 µA | $V_I = V_{IL}$ | 1.2V to 3.6V | 1.2V to 3.6V | | | | | | 0.2 | V |
| | | $I_{OL}$ = 3mA | | 1.2V | 1.2V | | 0.15 | | | | | |
| | | $I_{OL}$ = 6mA | | 1.4V | 1.4V | | | | | | 0.35 | |
| | | $I_{OL}$ = 8mA | | 1.65V | 1.65V | | | | | | 0.45 | |
| | | $I_{OL}$ = 9mA | | 2.3V | 2.3V | | | | | | 0.55 | |
| | | $I_{OL}$ = 12mA | | 3V | 3V | | | | | | 0.7 | |
| $I_I$ [7] | DIR input | $V_I = V_{CCA}$ or GND | | 1.2V to 3.6V | 1.2V to 3.6V | | ±0.025 | ±0.25 | | | ±1 | µA |
| $I_{BHL}$ [1] | | $V_I$ = 0.42V | | 1.2V | 1.2V | | 25 | | | | | µA |
| | | $V_I$ = 0.49V | | 1.4V | 1.4V | | | | 15 | | | |
| | | $V_I$ = 0.58V | | 1.65V | 1.65V | | | | 25 | | | |
| | | $V_I$ = 0.7V | | 2.3V | 2.3V | | | | 45 | | | |
| | | $V_I$ = 0.8V | | 3.3V | 3.3V | | | | 100 | | | |
| $I_{BHH}$ [2] | | $V_I$ = 0.78V | | 1.2V | 1.2V | | – 25 | | | | | µA |
| | | $V_I$ = 0.91V | | 1.4V | 1.4V | | | | – 15 | | | |
| | | $V_I$ = 1.07V | | 1.65V | 1.65V | | | | – 25 | | | |
| | | $V_I$ = 1.6V | | 2.3V | 2.3V | | | | – 45 | | | |
| | | $V_I$ = 2V | | 3.3V | 3.3V | | | | – 100 | | | |
| $I_{BHLO}$ [3] | | $V_I$ = 0 to $V_{CC}$ | | 1.2V | 1.2V | | 50 | | | | | µA |
| | | | | 1.6V | 1.6V | | | | 125 | | | |
| | | | | 1.95V | 1.95V | | | | 200 | | | |
| | | | | 2.7V | 2.7V | | | | 300 | | | |
| | | | | 3.6V | 3.6V | | | | 500 | | | |
| $I_{BHHO}$ [4] | | $V_I$ = 0 to $V_{CC}$ | | 1.2V | 1.2V | | – 50 | | | | | µA |
| | | | | 1.6V | 1.6V | | | | – 125 | | | |
| | | | | 1.95V | 1.95V | | | | – 200 | | | |
| | | | | 2.7V | 2.7V | | | | – 300 | | | |
| | | | | 3.6V | 3.6V | | | | – 500 | | | |


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over recommended operating free-air temperature range (unless otherwise noted)(5) (6)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | $T_A$ = 25°C | | | – 40°C to 85°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_{off}$ (8) | A port | $V_I$ or $V_O$ = 0 to 3.6V | 0V | 0V to 3.6V | | ±0.1 | ±1 | | | ±5 | µA |
| | B port | | 0V to 3.6V | 0V | | ±0.1 | ±1 | | | ±5 | |
| $I_{OZ}$ (8) | B port | $V_O$ = $V_{CCO}$ or GND, $V_I$ = $V_{CCI}$ or GND | 0V | 3.6V | | ±0.5 | ±2.5 | | | ±5 | |
| | A port | | 3.6V | 0V | | ±0.5 | ±2.5 | | | ±5 | µA |
| $I_{CCA}$ (8) | | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0 | 1.2V to 3.6V | 1.2V to 3.6V | | | | | | 10 | µA |
| | | | 0V | 3.6V | | | | | | – 2 | |
| | | | 3.6V | 0V | | | | | | 10 | |
| $I_{CCB}$ (8) | | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0 | 1.2V to 3.6V | 1.2V to 3.6V | | | | | | 10 | µA |
| | | | 0V | 3.6V | | | | | | 10 | |
| | | | 3.6V | 0V | | | | | | – 2 | |
| $I_{CCA}$ + $I_{CCB}$ | | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0 | 1.2V to 3.6V | 1.2V to 3.6V | | | | | | 20 | µA |
| $C_i$ | Control inputs | $V_I$ = 3.3V or GND | 3.3V | 3.3V | | 2.5 | | | | | pF |
| $C_{io}$ | A or B port | $V_I$ = 3.3 V or GND | 3.3V | 3.3V | | 6 | | | | | pF |

(1) The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ maximum. $I_{BHL}$ should be measured after lowering $V_{IN}$ to GND and then raising it to $V_{IL}$ maximum.
(2) The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH}$ mininum. $I_{BHH}$ should be measured after raising $V_{IN}$ to $V_{CC}$ and then lowering it to $V_{IH}$ minimum.
(3) An external driver must source at least $I_{BHLO}$ to switch this node from low to high.
(4) An external driver must sink at least $I_{BHHO}$ to switch this node from high to low.
(5) $V_{CCO}$ is the voltage associated with the output port supply VCCA or VCCB.
(6) $V_{CCI}$ is the voltage associated with the input port supply VCCA or VCCB.
(7) $V_{OH}$: Output High Voltage; $V_{OL}$: Output Low Voltage; $I_I$: Control Input Current.
(8) $I_{off}$: Partial Power Down Output current; $I_{OZ}$: Hi-Z Output Current; $I_{CCA}$: Supply A Current; $I_{CCB}$: Supply B Current.

## 5.6 Switching Characteristics: $V_{CCA}$ = 1.2V

over recommended operating free-air temperature range, $V_{CCA}$ = 1.2V (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.2V | $V_{CCB}$ = 1.5V | $V_{CCB}$ = 1.8V | $V_{CCB}$ = 2.5V | $V_{CCB}$ = 3.3V | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | TYP | |
| $t_{PLH}$ (2) | A | B | 3.1 | 2.6 | 2.4 | 2.2 | 2.2 | ns |
| $t_{PHL}$ (2) | | | 3.1 | 2.6 | 2.4 | 2.2 | 2.2 | |
| $t_{PLH}$ (2) | B | A | 3.4 | 3.1 | 3 | 2.9 | 2.9 | ns |
| $t_{PHL}$ (2) | | | 3.4 | 3.1 | 3 | 2.9 | 2.9 | |
| $t_{PHZ}$ (2) | DIR | A | 5.2 | 5.2 | 5.1 | 5 | 4.8 | ns |
| $t_{PLZ}$ (2) | | | 5.2 | 5.2 | 5.1 | 5 | 4.8 | |
| $t_{PHZ}$ (2) | DIR | B | 5 | 4 | 3.8 | 2.8 | 3.2 | ns |
| $t_{PLZ}$ (2) | | | 5 | 4 | 3.8 | 2.8 | 3.2 | |
| $t_{PZH}$ (2) (1) | DIR | A | 8.4 | 7.1 | 6.8 | 5.7 | 6.1 | ns |
| $t_{PZL}$ (2) (1) | | | 8.4 | 7.1 | 6.8 | 5.7 | 6.1 | |
| $t_{PZH}$ (2) (1) | DIR | B | 8.3 | 7.8 | 7.5 | 7.2 | 7 | ns |
| $t_{PZL}$ (2) (1) | | | 8.3 | 7.8 | 7.5 | 7.2 | 7 | |

(1) The enable time is a calculated value derived using the formula shown in the 节 8.2.2.2.1 section.
(2) $t_{PLH}$: Low-to-high Propagation Delay; $t_{PHL}$: High-to-Low Propagation Delay; $t_{PHZ}$: High-to-Hi-Z Propagation Delay; $t_{PLZ}$: Low-to-Hi-Z Propagation Delay; $t_{PZH}$: Hi-Z-to-High Propagation Delay; $t_{PZL}$: Hi-Z-to-Low Propagation Delay

## 5.7 Switching Characteristics: $V_{CCA}$ = 1.5V

over recommended operating free-air temperature range, $V_{CCA}$ = 1.5V ± 0.1V (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.2V | $V_{CCB}$ = 1.5V ± 0.1V | | $V_{CCB}$ = 1.8V ± 0.15V | | $V_{CCB}$ = 2.5V ± 0.2V | | $V_{CCB}$ = 3.3V ± 0.3V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ (2) | A | B | 2.8 | 0.7 | 5.4 | 0.5 | 4.6 | 0.4 | 3.7 | 0.3 | 3.5 | ns |
| $t_{PHL}$ (2) | | | 2.8 | 0.7 | 5.4 | 0.5 | 4.6 | 0.4 | 3.7 | 0.3 | 3.5 | |
| $t_{PLH}$ (2) | B | A | 2.7 | 0.8 | 5.4 | 0.7 | 5.2 | 0.6 | 4.9 | 0.5 | 4.7 | ns |
| $t_{PHL}$ (2) | | | 2.7 | 0.8 | 5.4 | 0.7 | 5.2 | 0.6 | 4.9 | 0.5 | 4.7 | |
| $t_{PHZ}$ (2) | DIR | A | 3.9 | 1.3 | 8.5 | 1.3 | 7.8 | 1.1 | 7.7 | 1.4 | 7.6 | ns |
| $t_{PLZ}$ (2) | | | 3.9 | 1.3 | 8.5 | 1.3 | 7.8 | 1.1 | 7.7 | 1.4 | 7.6 | |
| $t_{PHZ}$ (2) | DIR | B | 4.7 | 1.1 | 7 | 1.4 | 6.9 | 1.2 | 6.9 | 1.7 | 7.1 | ns |
| $t_{PLZ}$ (2) | | | 4.7 | 1.1 | 7 | 1.4 | 6.9 | 1.2 | 6.9 | 1.7 | 7.1 | |
| $t_{PZH}$ (2) (1) | DIR | A | 7.4 | | 12.4 | | 12.1 | | 11.8 | | 11.8 | ns |
| $t_{PZL}$ (2) (1) | | | 7.4 | | 12.4 | | 12.1 | | 11.8 | | 11.8 | |
| $t_{PZH}$ (2) (1) | DIR | B | 6.7 | | 13.9 | | 12.4 | | 11.4 | | 11.1 | ns |
| $t_{PZL}$ (2) (1) | | | 6.7 | | 13.9 | | 12.4 | | 11.4 | | 11.1 | |

(1) The enable time is a calculated value derived using the formula shown in the 节 *8.2.2.2.1* section.
(2) $t_{PLH}$: Low-to-high Propagation Delay; $t_{PHL}$: High-to-Low Propagation Delay; $t_{PHZ}$: High-to-Hi-Z Propagation Delay; $t_{PLZ}$: Low-to-Hi-Z Propagation Delay; $t_{PZH}$: Hi-Z-to-High Propagation Delay; $t_{PZL}$: Hi-Z-to-Low Propagation Delay


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## 5.8 Switching Characteristics: $V_{CCA}$ = 1.8V

over recommended operating free-air temperature range, $V_{CCA}$ = 1.8V ± 0.15V (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.2V | $V_{CCB}$ = 1.5V ± 0.1V | | $V_{CCB}$ = 1.8V ± 0.15V | | $V_{CCB}$ = 2.5V ± 0.2V | | $V_{CCB}$ = 3.3V ± 0.3V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ (2) | A | B | 2.7 | 0.5 | 5.2 | 0.4 | 4.3 | 0.2 | 3.4 | 0.2 | 3.1 | ns |
| $t_{PHL}$ (2) | | | 2.7 | 0.5 | 5.2 | 0.4 | 4.3 | 0.2 | 3.4 | 0.2 | 3.1 | |
| $t_{PLH}$ (2) | B | A | 2.4 | 0.7 | 4.7 | 0.5 | 4.4 | 0.5 | 4 | 0.4 | 3.8 | ns |
| $t_{PHL}$ (2) | | | 2.4 | 0.7 | 4.7 | 0.5 | 4.4 | 0.5 | 4 | 0.4 | 3.8 | |
| $t_{PHZ}$ (2) | DIR | A | 3.7 | 1.3 | 8.1 | 0.7 | 6.9 | 1.4 | 5.3 | 1.1 | 5.2 | ns |
| $t_{PLZ}$ (2) | | | 3.7 | 1.3 | 8.1 | 0.7 | 6.9 | 1.4 | 5.3 | 1.1 | 5.2 | |
| $t_{PHZ}$ (2) | DIR | B | 4.4 | 1.3 | 5.8 | 1.3 | 5.9 | 0.8 | 5.7 | 1.5 | 5.9 | ns |
| $t_{PLZ}$ (2) | | | 4.4 | 1.3 | 5.8 | 1.3 | 5.9 | 0.8 | 5.7 | 1.5 | 5.9 | |
| $t_{PZH}$ (2) (1) | DIR | A | 6.8 | | 10.5 | | 10.3 | | 9.7 | | 9.7 | ns |
| $t_{PZL}$ (2) (1) | | | 6.8 | | 10.5 | | 10.3 | | 9.7 | | 9.7 | |
| $t_{PZH}$ (2) (1) | DIR | B | 6.4 | | 13.3 | | 11.2 | | 8.7 | | 8.3 | ns |
| $t_{PZL}$ (2) (1) | | | 6.4 | | 13.3 | | 11.2 | | 8.7 | | 8.3 | |

(1) The enable time is a calculated value derived using the formula shown in the 节 8.2.2.2.1 section.
(2) $t_{PLH}$: Low-to-high Propagation Delay; $t_{PHL}$: High-to-Low Propagation Delay; $t_{PHZ}$: High-to-Hi-Z Propagation Delay; $t_{PLZ}$: Low-to-Hi-Z Propagation Delay; $t_{PZH}$: Hi-Z-to-High Propagation Delay; $t_{PZL}$: Hi-Z-to-Low Propagation Delay

## 5.9 Switching Characteristics: $V_{CCA}$ = 2.5V

over recommended operating free-air temperature range, $V_{CCA}$ = 2.5V ± 0.2V (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.2V | $V_{CCB}$ = 1.5V ± 0.1V | | $V_{CCB}$ = 1.8V ± 0.15V | | $V_{CCB}$ = 2.5V ± 0.2V | | $V_{CCB}$ = 3.3V ± 0.3V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ (2) | A | B | 2.6 | 0.4 | 4.9 | 0.2 | 4 | 0.2 | 3 | 0.2 | 2.6 | ns |
| $t_{PHL}$ (2) | | | 2.6 | 0.4 | 4.9 | 0.2 | 4 | 0.2 | 3 | 0.2 | 2.6 | |
| $t_{PLH}$ (2) | B | A | 2.1 | 0.6 | 3.8 | 0.5 | 3.4 | 0.4 | 3 | 0.3 | 2.8 | ns |
| $t_{PHL}$ (2) | | | 2.1 | 0.6 | 3.8 | 0.5 | 3.4 | 0.4 | 3 | 0.3 | 2.8 | |
| $t_{PHZ}$ (2) | DIR | A | 2.4 | 0.7 | 7.9 | 0.8 | 6.4 | 0.8 | 5 | 0.5 | 4.3 | ns |
| $t_{PLZ}$ (2) | | | 2.4 | 0.7 | 7.9 | 0.8 | 6.4 | 0.8 | 5 | 0.5 | 4.3 | |
| $t_{PHZ}$ (2) | DIR | B | 3.8 | 1 | 4.3 | 0.6 | 4.3 | 0.5 | 4.2 | 1.1 | 4.1 | ns |
| $t_{PLZ}$ (2) | | | 3.8 | 1 | 4.3 | 0.6 | 4.3 | 0.5 | 4.2 | 1.1 | 4.1 | |
| $t_{PZH}$ (2) (1) | DIR | A | 5.9 | | 8.5 | | 7.7 | | 7.2 | | 6.9 | ns |
| $t_{PZL}$ (2) (1) | | | 5.9 | | 8.5 | | 7.7 | | 7.2 | | 6.9 | |
| $t_{PZH}$ (2) (1) | DIR | B | 5 | | 12.8 | | 10.4 | | 8 | | 6.9 | ns |
| $t_{PZL}$ (2) (1) | | | 5 | | 12.8 | | 10.4 | | 8 | | 6.9 | |

(1) The enable time is a calculated value derived using the formula shown in the 节 8.2.2.2.1 section.
(2) $t_{PLH}$: Low-to-high Propagation Delay; $t_{PHL}$: High-to-Low Propagation Delay; $t_{PHZ}$: High-to-Hi-Z Propagation Delay; $t_{PLZ}$: Low-to-Hi-Z Propagation Delay; $t_{PZH}$: Hi-Z-to-High Propagation Delay; $t_{PZL}$: Hi-Z-to-Low Propagation Delay

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## 5.10 Switching Characteristics: $V_{CCA}$ = 3.3V

over recommended operating free-air temperature range, $V_{CCA}$ = 3.3V ± 0.3V (see 图 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.2V | $V_{CCB}$ = 1.5V ± 0.1V | | $V_{CCB}$ = 1.8V ± 0.15V | | $V_{CCB}$ = 2.5V ± 0.2V | | $V_{CCB}$ = 3.3V ± 0.3V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ (2) | A | B | 2.5 | 0.3 | 4.7 | 0.2 | 3.8 | 0.2 | 2.8 | 0.2 | 2.4 | ns |
| $t_{PHL}$ (2) | | | 2.5 | 0.3 | 4.7 | 0.2 | 3.8 | 0.2 | 2.8 | 0.2 | 2.4 | |
| $t_{PLH}$ (2) | B | A | 2.1 | 0.6 | 3.6 | 0.4 | 3.1 | 0.3 | 2.6 | 0.3 | 2.4 | ns |
| $t_{PHL}$ (2) | | | 2.1 | 0.6 | 3.6 | 0.4 | 3.1 | 0.3 | 2.6 | 0.3 | 2.4 | |
| $t_{PHZ}$ (2) | DIR | A | 2.9 | 1.1 | 8 | 1 | 6.5 | 1.3 | 4.7 | 1.2 | 4 | ns |
| $t_{PLZ}$ (2) | | | 2.9 | 1.1 | 8 | 1 | 6.5 | 1.3 | 4.7 | 1.2 | 4 | |
| $t_{PHZ}$ (2) | DIR | B | 3.4 | 0.5 | 6.6 | 0.3 | 5.6 | 0.3 | 4.6 | 1.1 | 4.2 | ns |
| $t_{PLZ}$ (2) | | | 3.4 | 0.5 | 6.6 | 0.3 | 5.6 | 0.3 | 4.6 | 1.1 | 4.2 | |
| $t_{PZH}$ (2) (1) | DIR | A | 5.5 | | 10.2 | | 8.7 | | 7.2 | | 6.6 | ns |
| $t_{PZL}$ (2) (1) | | | 5.5 | | 10.2 | | 8.7 | | 7.2 | | 6.6 | |
| $t_{PZH}$ (2) (1) | DIR | B | 5.4 | | 12.7 | | 10.3 | | 7.5 | | 6.4 | ns |
| $t_{PZL}$ (2) (1) | | | 5.4 | | 12.7 | | 10.3 | | 7.5 | | 6.4 | |

(1) The enable time is a calculated value derived using the formula shown in the 节 8.2.2.2.1 section.
(2) $t_{PLH}$: Low-to-high Propagation Delay; $t_{PHL}$: High-to-Low Propagation Delay; $t_{PHZ}$: High-to-Hi-Z Propagation Delay; $t_{PLZ}$: Low-to-Hi-Z Propagation Delay; $t_{PZH}$: Hi-Z-to-High Propagation Delay; $t_{PZL}$: Hi-Z-to-Low Propagation Delay

## 5.11 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ = $V_{CCB}$ = 1.2V | $V_{CCA}$ = $V_{CCB}$ = 1.5V | $V_{CCA}$ = $V_{CCB}$ = 1.8V | $V_{CCA}$ = $V_{CCB}$ = 2.5V | $V_{CCA}$ = $V_{CCB}$ = 3.3V | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | TYP | |
| $C_{pdA}$ (1) | A-port input, B-port output | $C_L$ = 0, f = 10MHz, $t_r$ (2) = $t_f$ (2) = 1ns | 3 | 3 | 3 | 3 | 4 | pF |
| | B-port input, A-port output | | 13 | 13 | 14 | 15 | 15 | |
| $C_{pdB}$ (1) | A-port input, B-port output | $C_L$ = 0, f = 10MHz, $t_r$ (2) = $t_f$ (2) = 1ns | 13 | 13 | 14 | 15 | 15 | pF |
| | B-port input, A-port output | | 3 | 3 | 3 | 3 | 4 | |

(1) Power dissipation capacitance per transceiver
(2) $t_r$: Rise time; $t_f$: Fall time


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## 5.12 Typical Characteristics

### *5.12.1 Typical Propagation Delay (A to B) vs Load Capacitance, $T_A$ = 25°C, $V_{CCA}$ = 1.8V*

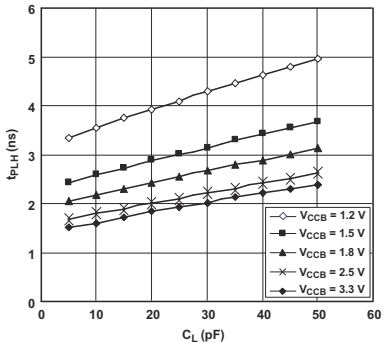



图 5-1. Typical A-to-B Propagation Delay, Low to High

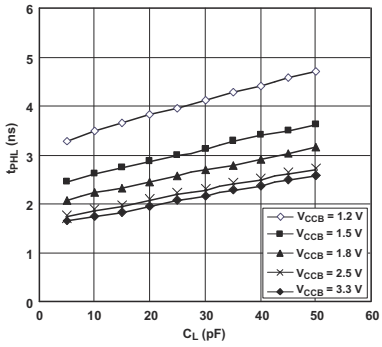



图 5-2. Typical A-to-B Propagation Delay, High to Low

### *5.12.2 Typical Propagation Delay (A to B) vs Load Capacitance, $T_A$ = 25°C, $V_{CCA}$ = 2.5V*

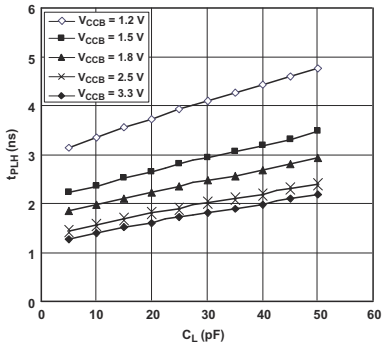



图 5-3. Typical A-to-B Propagation Delay, Low to High

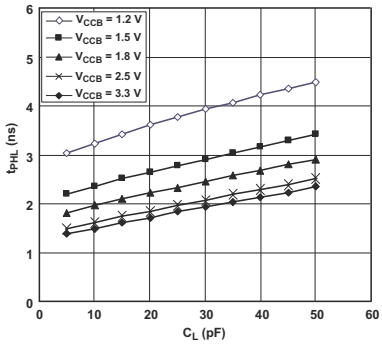



图 5-4. Typical A-to-B Propagation Delay, High to Low

### *5.12.3 Typical Propagation Delay (A to B) vs Load Capacitance, $T_A$ = 25°C, $V_{CCA}$ = 3.3V*

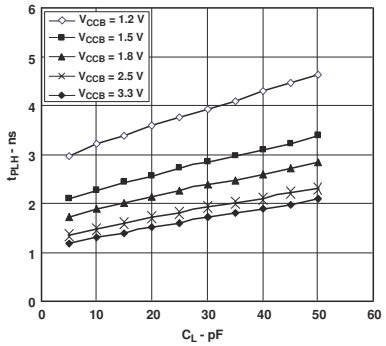



图 5-5. Typical A-to-B Propagation Delay, Low to High

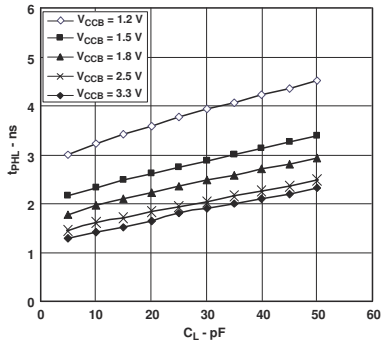
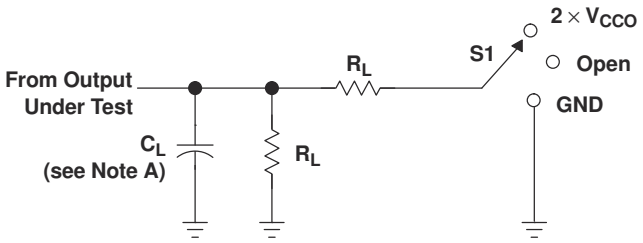



图 5-6. Typical A-to-B Propagation Delay, High to Low

# 6 Parameter Measurement Information

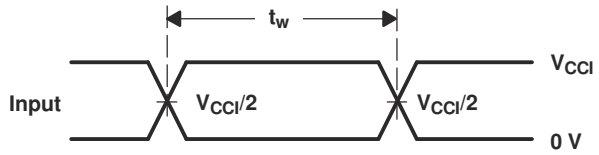
## 6.1



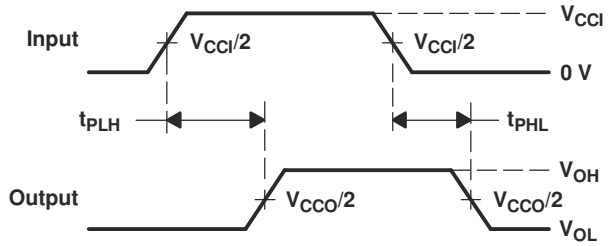

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CCO}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

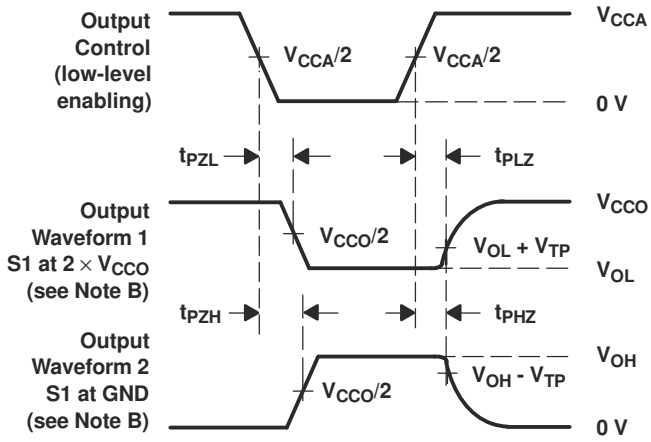
| $V_{CCO}$ | $C_L$ | $R_L$ | $V_{TP}$ |
|---|---|---|---|
| 1.2 V | 15 pF | 2 kΩ | 0.1 V |
| 1.5 V ± 0.1 V | 15 pF | 2 kΩ | 0.1 V |
| 1.8 V ± 0.15 V | 15 pF | 2 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | 15 pF | 2 kΩ | 0.15 V |
| 3.3 V ± 0.3 V | 15 pF | 2 kΩ | 0.3 V |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. $V_{CCI}$ is the $V_{CC}$ associated with the input port.
I. $V_{CCO}$ is the $V_{CC}$ associated with the output port.

**图 6-1. Load Circuit and Voltage Waveforms**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# 7 Detailed Description

## 7.1 Overview

This dual-bit non-inverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track $V_{CCA}$ and accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track $V_{CCB}$ and accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes.

The SN74AVCH2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR pin) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated.

The SN74AVCH2T45 features active bus-hold circuitry.

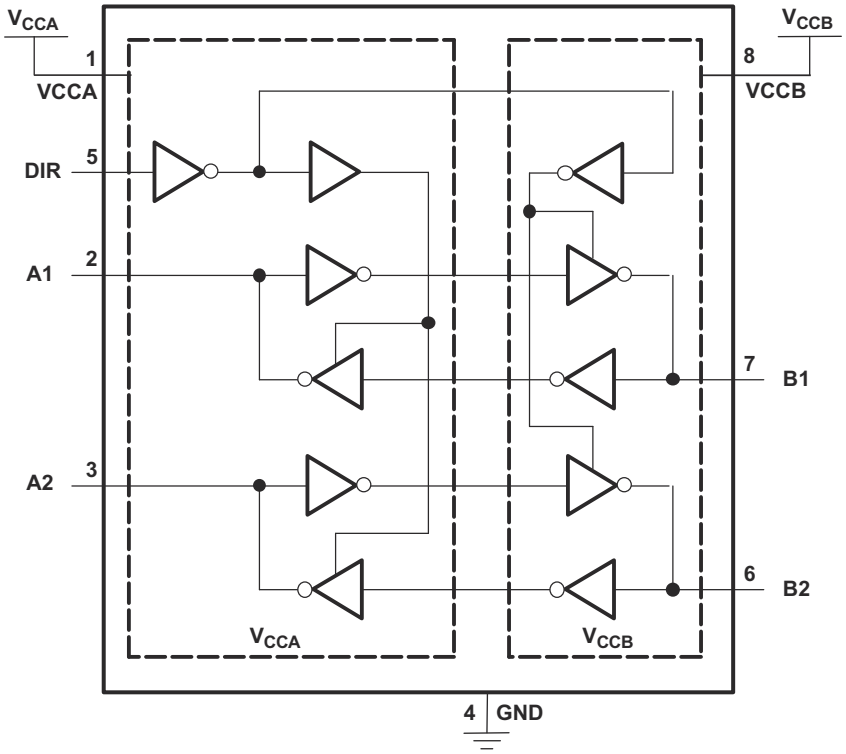
The DIR input is powered by supply voltage from VCCA.

This device is fully specified for partial-power-down applications using off output current ($I_{off}$). The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The $V_{CC}$ isolation feature ensures that if either VCC input is at GND, both ports are put in a high-impedance state. This will prevent a false high or low logic being presented at the output.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 VCC Isolation

The $V_{CC}$ isolation feature ensures that if either $V_{CCA}$ or $V_{CCB}$ are at GND, both ports will be in a high-impedance state ($I_{OZ}$ shown in the 节 7.2). This prevents false logic levels from being presented to either bus.

### 7.3.2 2-Rail Design

Fully configurable 2-rail design allows each port to operate over the full 1.2 V to 3.6 V power-supply range.

### 7.3.3 IO Ports are 4.6 V Tolerant

The IO ports are up to 4.6 V tolerant

### 7.3.4 Partial Power Down Mode

This device is fully specified for partial-power-down applications using off output current ($I_{off}$). The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 7.3.5 Bus Hold on Data Inputs

Active bus-hold circuitry holds unused or un-driven inputs at a valid logic state. TI does not recommend using pull-up or pull-down resistors with the bus-hold circuitry.

## 7.4 Device Functional Modes

**表 7-1. Function Table (Each Transceiver)**

| INPUT DIR | OPERATION |
|---|---|
| L | B data to A bus |
| H | A data to B bus |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# 8 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 8.1 Application Information

The SN74AVCH2T45 is used to shift IO voltage levels from one voltage domain to another. Each bus (bus A and bus B) have independent power supplies, and a direction pin is used to control the direction of data flow.

## 8.2 Typical Applications

### *8.2.1 Unidirectional Logic Level-Shifting Application*

图 8-1 is an example of the SN74AVCH2T45 circuit used in a unidirectional logic level-shifting application.

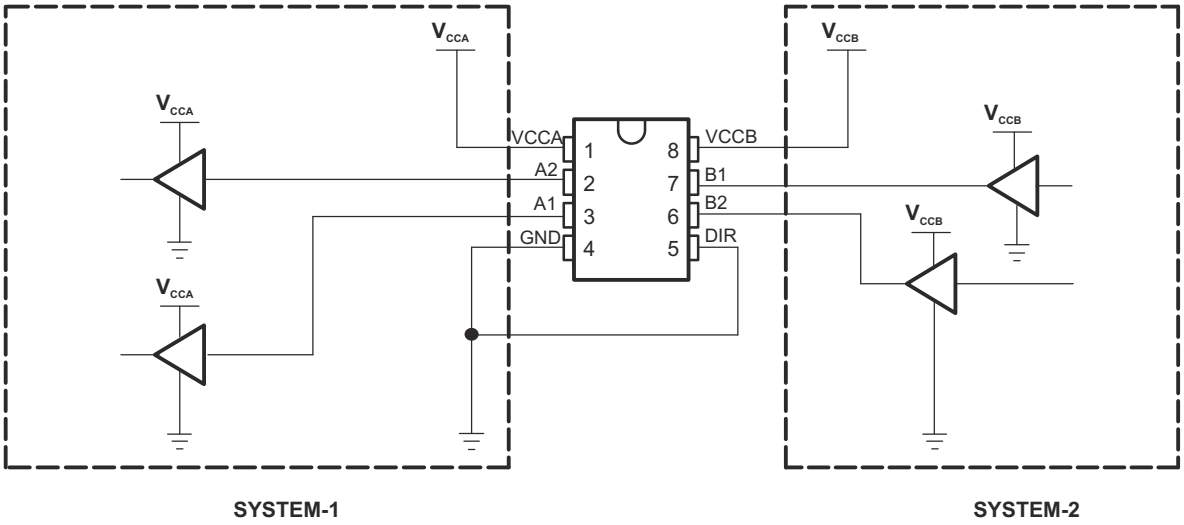


**图 8-1. Unidirectional Logic Level-Shifting Application**

#### 8.2.1.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Active bus-hold circuitry holds unused or un-driven inputs at a valid logic state. TI does not recommend using pull-up or pull-down resistors with the bus-hold circuitry.

#### 8.2.1.2 Detailed Design Procedure

表 8-1 lists the pins and pin descriptions of the SN74AVCH2T45 connections with SYSTEM-1 and SYSTEM-2.

表 8-1. SN74AVCH2T45 Pin Connections With SYSTEM-1 and SYSTEM-2

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | VCCA | SYSTEM-1 supply voltage (1.2V to 3.6V) |
| 2 | A1 | Output level depends on $V_{CCA}$. |
| 3 | A2 | Output level depends on $V_{CCA}$. |
| 4 | GND | Device GND |
| 5 | DIR | The GND (low-level) determines B-port to A-port direction. |
| 6 | B2 | Input threshold value depends on $V_{CCB}$. |
| 7 | B1 | Input threshold value depends on $V_{CCB}$. |
| 8 | VCCB | SYSTEM-2 supply voltage (1.2V to 3.6V) |

#### 8.2.1.3 Application Curve

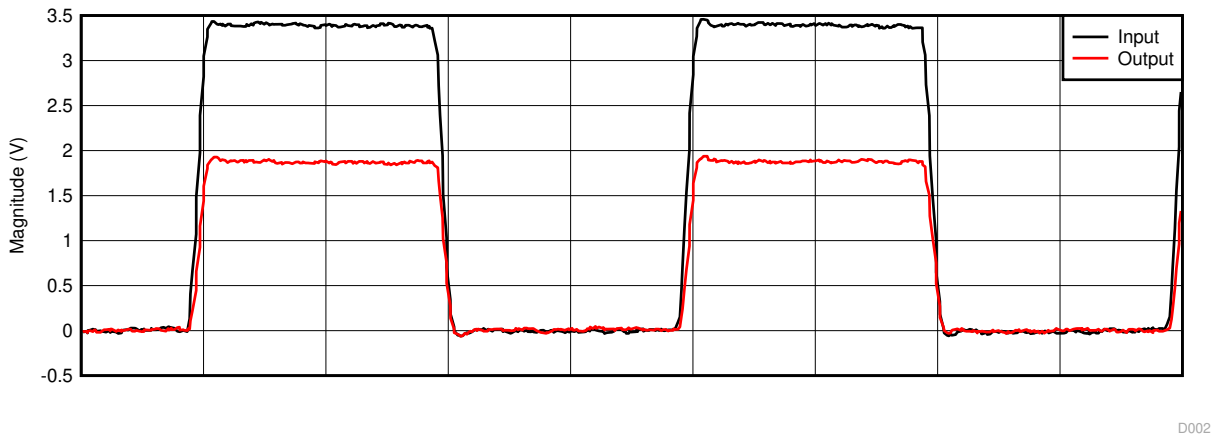


图 8-2. 3.3- to 1.8-V Level-Shifting With 1MHz Square Wave


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### 8.2.2 Bidirectional Logic Level-Shifting Application

图 8-3 shows the SN74AVCH2T45 used in a bidirectional logic level-shifting application. Because the SN74AVCH2T45 does not have an output-enable (OE) pin, system designers should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

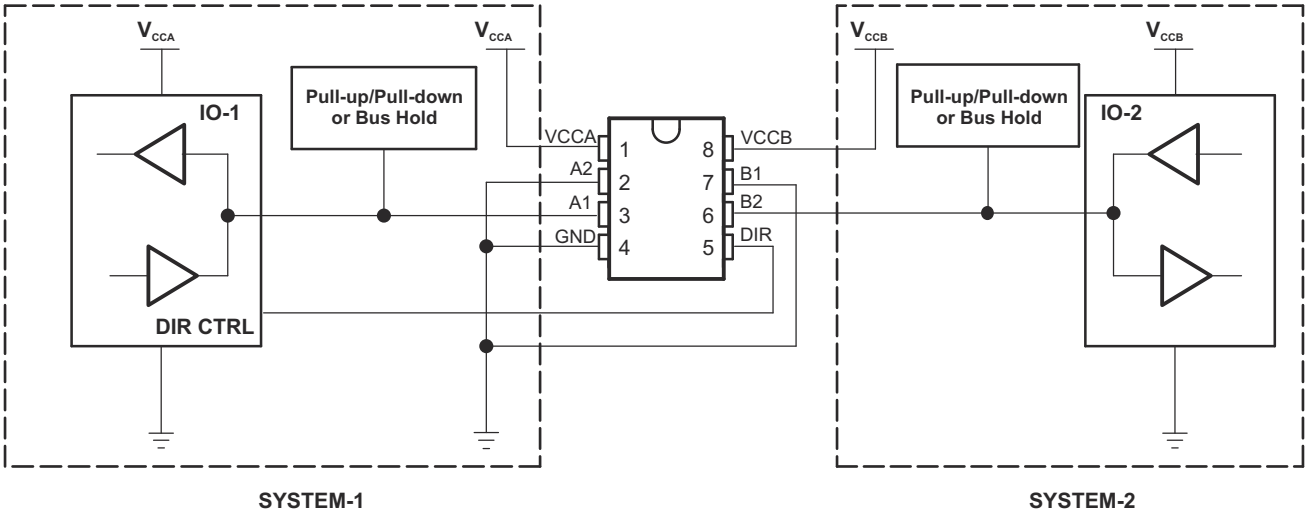


**图 8-3. Bidirectional Logic Level-Shifting Application**

#### 8.2.2.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Active bus-hold circuitry holds unused or un-driven inputs at a valid logic state. TI does not recommend using pull-up or pull-down resistors with the bus-hold circuitry.

#### 8.2.2.2 Detailed Design Procedure

表 8-2 lists a sequence that shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

**表 8-2. Data Transmission Sequence**

| STATE | DIR CTRL | IO-1 | IO-2 | DESCRIPTION |
|---|---|---|---|---|
| 1 | H | Output | Input | SYSTEM-1 data to SYSTEM-2 |
| 2 | H | Hi-Z | Hi-Z | SYSTEM-2 is getting ready to send data to SYSTEM-1. IO-1 and IO-2 are disabled.<br>The bus-line state depends on pull-up or pull-down.(1) |
| 3 | L | Hi-Z | Hi-Z | DIR bit is flipped. IO-1 and IO-2 still are disabled.<br>The bus-line state depends on pull-up or pull-down.(1) |
| 4 | L | Input | Output | SYSTEM-2 data to SYSTEM-1 |

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

#### *8.2.2.2.1 Enable Times*

Calculate the enable times for the SN74AVCH2T45 using the following formulas:

$$t_{PZH}\text{ (DIR to A)} = t_{PLZ}\text{ (DIR to B)} + t_{PLH}\text{ (B to A)} \quad (1)$$

$$t_{PZL}\text{ (DIR to A)} = t_{PHZ}\text{ (DIR to B)} + t_{PHL}\text{ (B to A)} \quad (2)$$

$$t_{PZH}\text{ (DIR to B)} = t_{PLZ}\text{ (DIR to A)} + t_{PLH}\text{ (A to B)} \quad (3)$$

$$t_{PZL}\text{ (DIR to B)} = t_{PHZ}\text{ (DIR to A)} + t_{PHL}\text{ (A to B)} \quad (4)$$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVCH2T45 initially is transmitting from A to B, the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

#### 8.2.2.3 Application Curve

Refer to *图 8-2*.

## 8.3 Power Supply Recommendations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up $V_{CCA}$.
3. $V_{CCB}$ can be ramped up along with or after $V_{CCA}$.

**表 8-3. Typical Total Static Power Consumption ($I_{CCA}$ + $I_{CCB}$)**

| $V_{CCB}$ | $V_{CCA}$ | | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | 0V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | |
| **0V** | 0 | < 0.5 | < 0.5 | < 0.5 | < 0.5 | < 0.5 | μA |
| **1.2V** | < 0.5 | < 1 | < 1 | < 1 | < 1 | 1 | |
| **1.5V** | < 0.5 | < 1 | < 1 | < 1 | < 1 | 1 | |
| **1.8V** | < 0.5 | < 1 | < 1 | < 1 | < 1 | < 1 | |
| **2.5V** | < 0.5 | 1 | < 1 | < 1 | < 1 | < 1 | |
| **3.3V** | < 0.5 | 1 | < 1 | < 1 | < 1 | < 1 | |

## 8.4 Layout

### *8.4.1 Layout Guidelines*

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB pin and GND pin.
- Short trace lengths should be used to avoid excessive loading.


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### 8.4.2 Layout Example

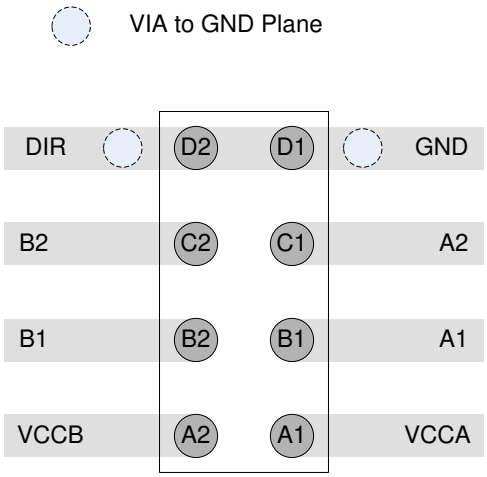


**图 8-4. Layout Example for YZP Package**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004

## 9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

## 9.4 Trademarks

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## 9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 9.6 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |


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## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

**Changes from Revision H (April 2015) to Revision I (February 2025)** **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 ..... 1
- Updated DCT and DCU *Thermal Information* ..... 6
- Added the *Receiving Notifications of Documentation Updates*, *Support Resources*, *Electrostatic Discharge Caution*, and *Glossary* sections ..... 20

**Changes from Revision G (April 2015) to Revision H (April 2015)** **Page**

- 添加了其他应用 ..... 1
- Updated Overview section. ..... 13
- Updated Layout Guidelines section. ..... 18

**Changes from Revision F (November 2007) to Revision G (February 2015)** **Page**

- 添加了 *ESD 等级表*、*特性说明* 部分、*器件功能模式*、*应用和实现* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ..... 1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 74AVCH2T45DCTTE4 | Last Time Buy | Production | SSOP (DCT) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2 Z |
| SN74AVCH2T45DCTR | Last Time Buy | Production | SSOP (DCT) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | ET2 Z |
| SN74AVCH2T45DCTR.A | Last Time Buy | Production | SSOP (DCT) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2 Z |
| SN74AVCH2T45DCTR.B | Last Time Buy | Production | SSOP (DCT) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2 Z |
| SN74AVCH2T45DCTRG4 | Active | Production | SSOP (DCT) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2 Z |
| SN74AVCH2T45DCTRG4.A | Active | Production | SSOP (DCT) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2 Z |
| SN74AVCH2T45DCTRG4.B | Active | Production | SSOP (DCT) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2 Z |
| SN74AVCH2T45DCTT | Last Time Buy | Production | SSOP (DCT) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2 Z |
| SN74AVCH2T45DCTT.B | Last Time Buy | Production | SSOP (DCT) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2 Z |
| SN74AVCH2T45DCUR | Active | Production | VSSOP (DCU) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | (ET2R, T2) EZ |
| SN74AVCH2T45DCUR.A | Active | Production | VSSOP (DCU) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | (ET2R, T2) EZ |
| SN74AVCH2T45DCUR.B | Active | Production | VSSOP (DCU) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | (ET2R, T2) EZ |
| SN74AVCH2T45DCURG4 | Active | Production | VSSOP (DCU) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2R |
| SN74AVCH2T45DCURG4.A | Active | Production | VSSOP (DCU) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2R |
| SN74AVCH2T45DCURG4.B | Active | Production | VSSOP (DCU) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ET2R |
| SN74AVCH2T45DCUT | Active | Production | VSSOP (DCU) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (ET2R, T2) EZ |
| SN74AVCH2T45DCUT.B | Active | Production | VSSOP (DCU) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (ET2R, T2) EZ |
| SN74AVCH2T45YZPR | Active | Production | DSBGA (YZP) \| 8 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TFN |
| SN74AVCH2T45YZPR.B | Active | Production | DSBGA (YZP) \| 8 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TFN |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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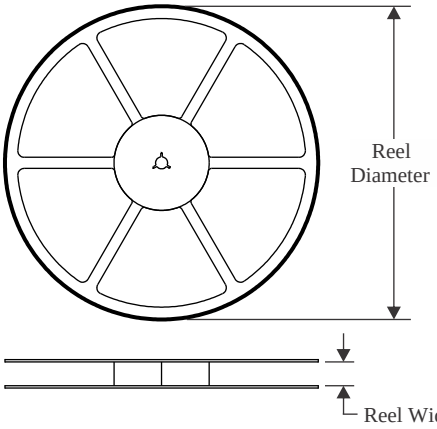
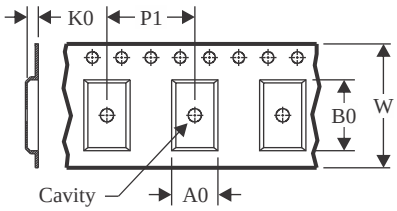
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

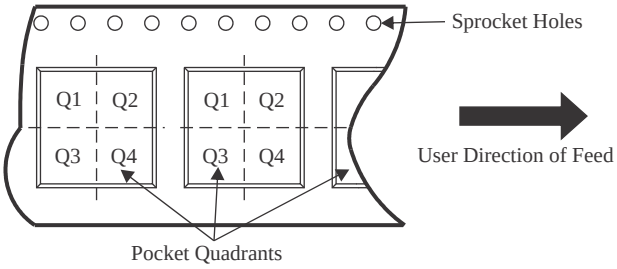



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

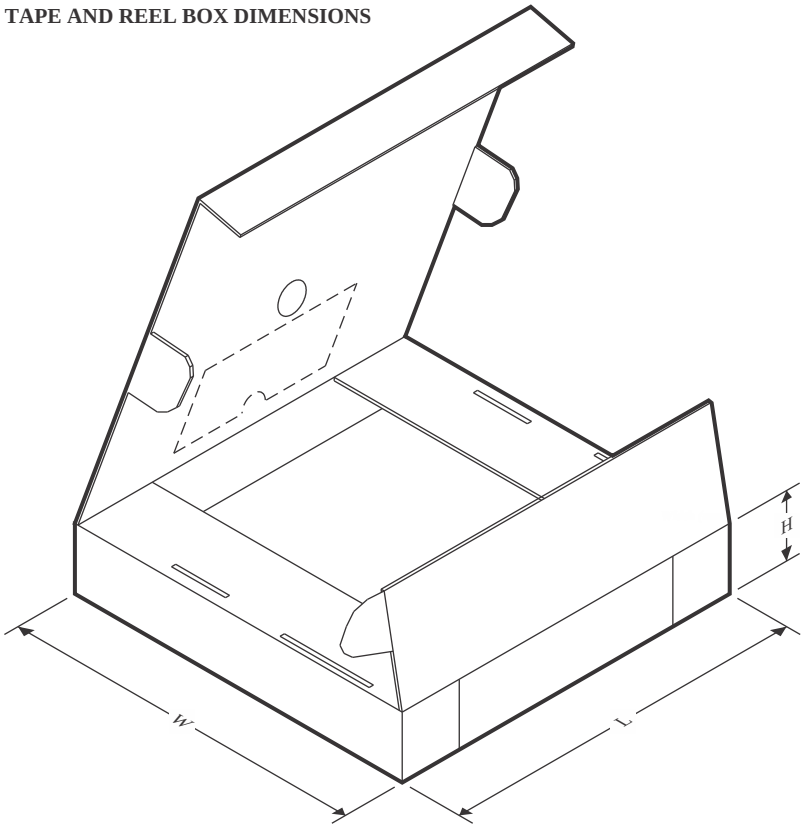
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

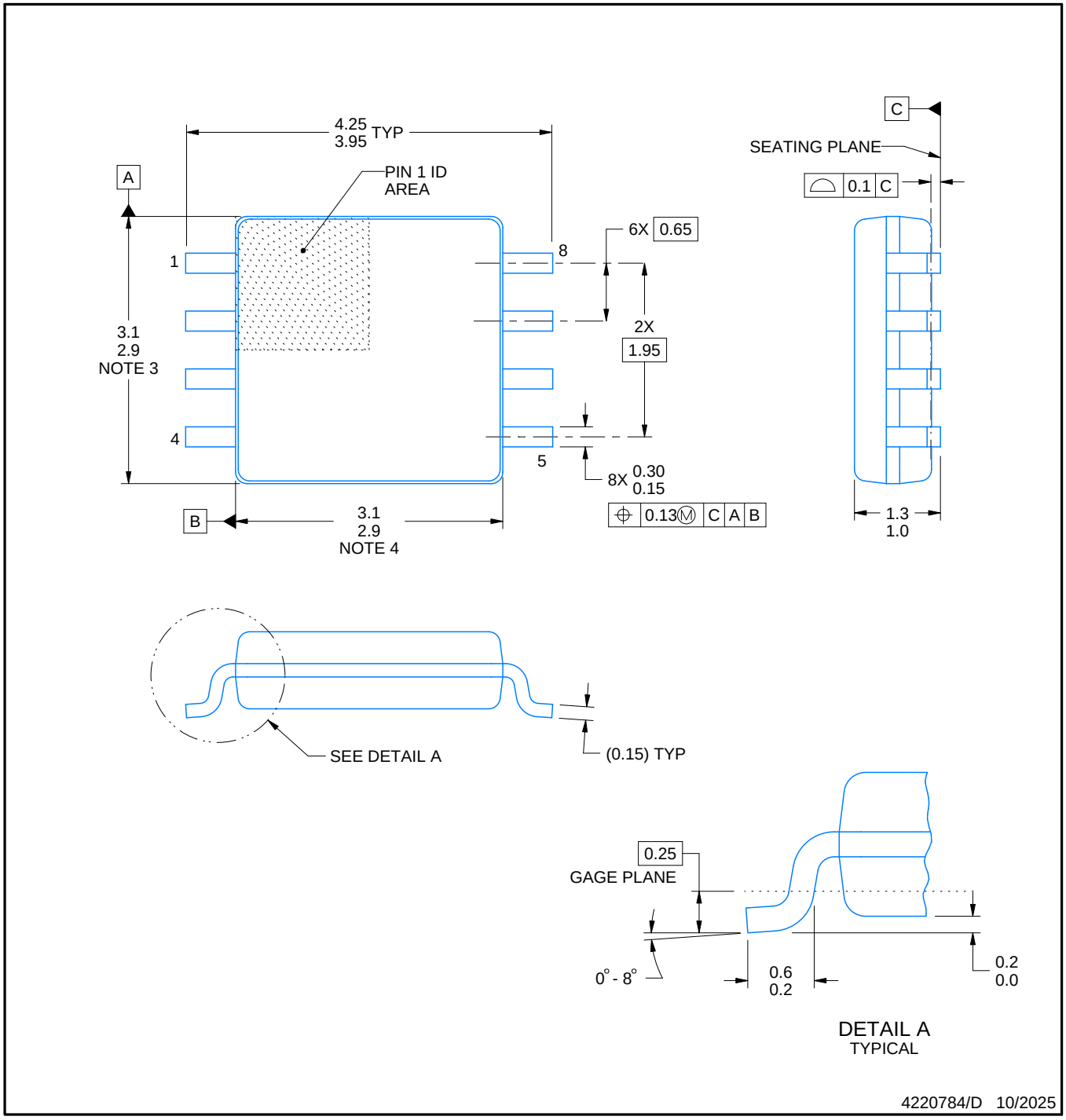
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AVCH2T45DCTR | SSOP | DCT | 8 | 3000 | 180.0 | 12.4 | 3.15 | 4.35 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74AVCH2T45DCTR | SSOP | DCT | 8 | 3000 | 177.8 | 12.4 | 3.45 | 4.4 | 1.45 | 4.0 | 12.0 | Q3 |
| SN74AVCH2T45DCTR | SSOP | DCT | 8 | 3000 | 180.0 | 13.0 | 3.35 | 4.5 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74AVCH2T45DCTRG4 | SSOP | DCT | 8 | 3000 | 177.8 | 12.4 | 3.45 | 4.4 | 1.45 | 4.0 | 12.0 | Q3 |
| SN74AVCH2T45DCTRG4 | SSOP | DCT | 8 | 3000 | 180.0 | 13.0 | 3.35 | 4.5 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74AVCH2T45DCTT | SSOP | DCT | 8 | 250 | 177.8 | 12.4 | 3.45 | 4.4 | 1.45 | 4.0 | 12.0 | Q3 |
| SN74AVCH2T45DCTT | SSOP | DCT | 8 | 250 | 180.0 | 13.0 | 3.35 | 4.5 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74AVCH2T45DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74AVCH2T45DCUR | VSSOP | DCU | 8 | 3000 | 178.0 | 9.0 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74AVCH2T45DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 9.0 | 2.25 | 3.4 | 1.0 | 4.0 | 8.0 | Q3 |
| SN74AVCH2T45DCURG4 | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74AVCH2T45DCURG4 | VSSOP | DCU | 8 | 3000 | 178.0 | 9.0 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74AVCH2T45YZPR | DSBGA | YZP | 8 | 3000 | 178.0 | 9.2 | 1.02 | 2.02 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



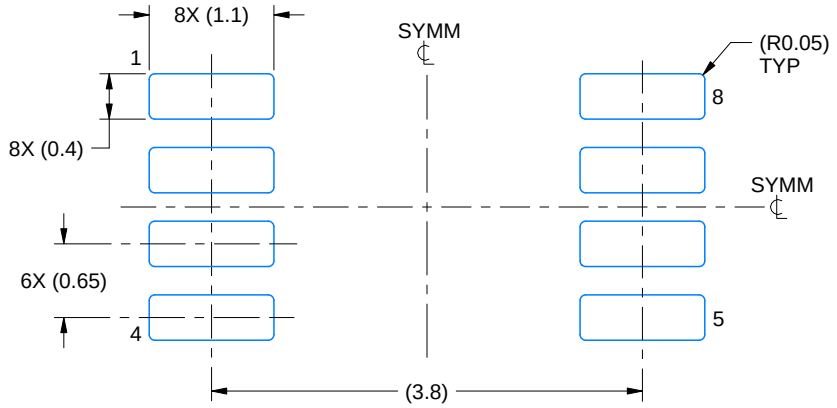

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AVCH2T45DCTR | SSOP | DCT | 8 | 3000 | 190.0 | 190.0 | 30.0 |
| SN74AVCH2T45DCTR | SSOP | DCT | 8 | 3000 | 183.0 | 183.0 | 20.0 |
| SN74AVCH2T45DCTR | SSOP | DCT | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| SN74AVCH2T45DCTRG4 | SSOP | DCT | 8 | 3000 | 183.0 | 183.0 | 20.0 |
| SN74AVCH2T45DCTRG4 | SSOP | DCT | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| SN74AVCH2T45DCTT | SSOP | DCT | 8 | 250 | 183.0 | 183.0 | 20.0 |
| SN74AVCH2T45DCTT | SSOP | DCT | 8 | 250 | 182.0 | 182.0 | 20.0 |
| SN74AVCH2T45DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AVCH2T45DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AVCH2T45DCUR | VSSOP | DCU | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| SN74AVCH2T45DCURG4 | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AVCH2T45DCURG4 | VSSOP | DCU | 8 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AVCH2T45YZPR | DSBGA | YZP | 8 | 3000 | 220.0 | 220.0 | 35.0 |

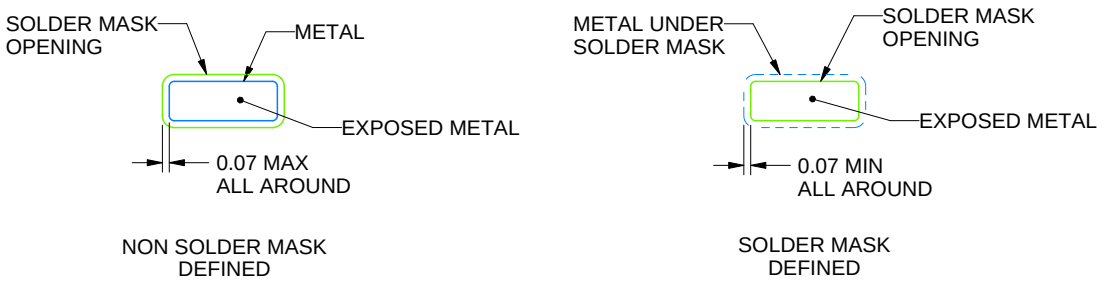



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

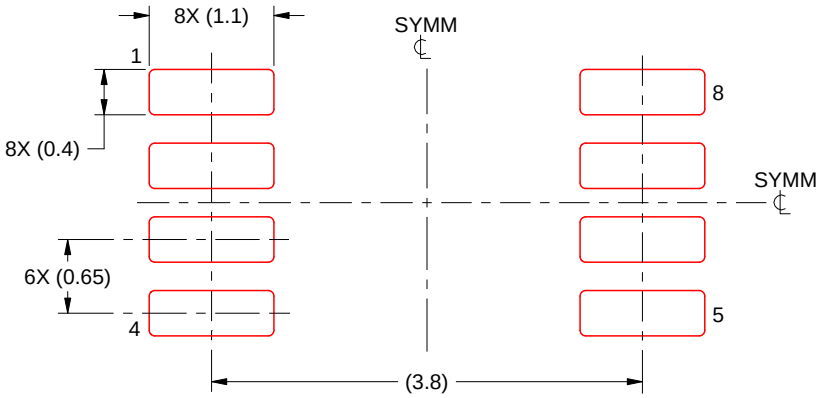



SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

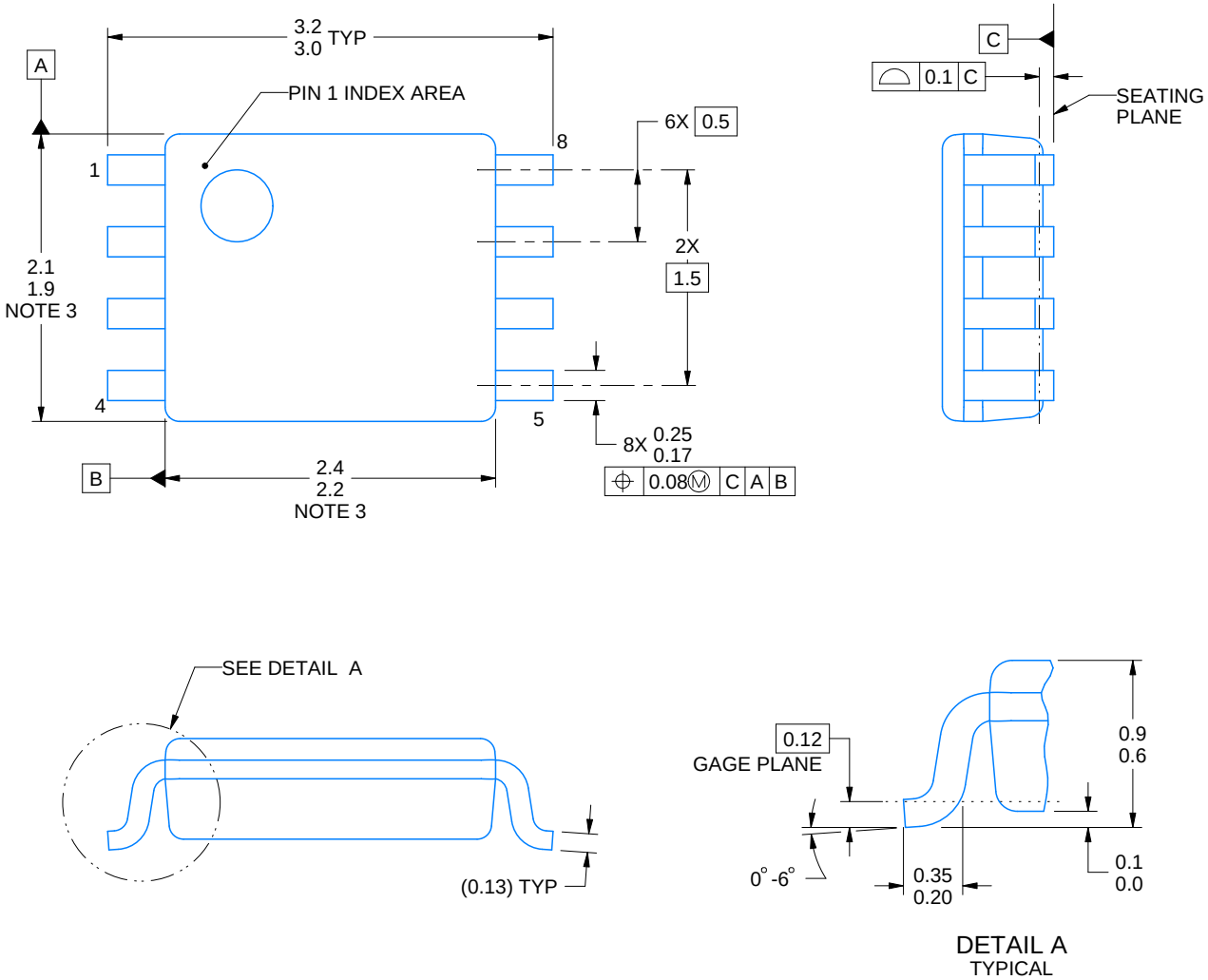
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# DCU0008A

# PACKAGE OUTLINE

## VSSOP - 0.9 mm max height

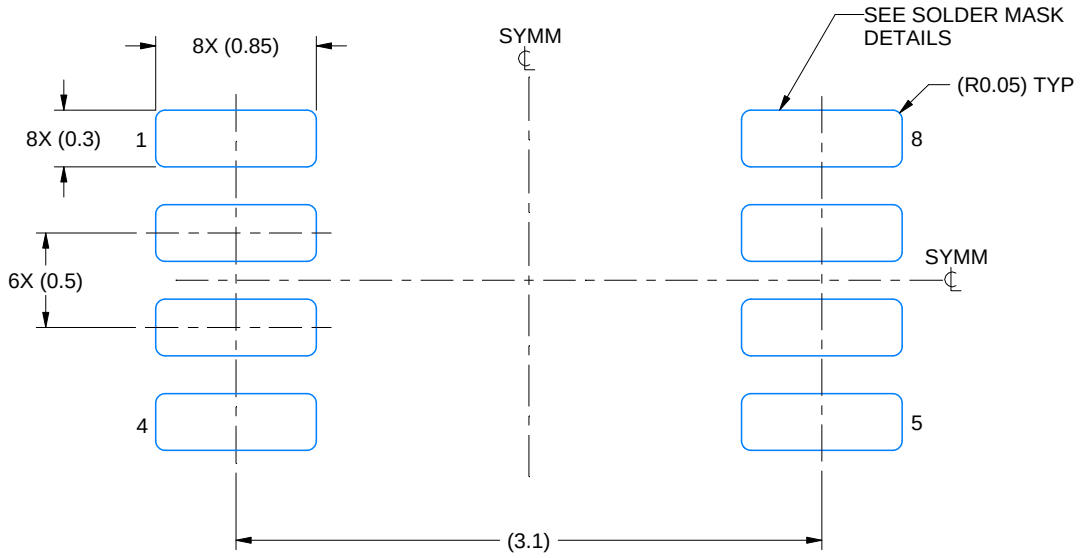
SMALL OUTLINE PACKAGE



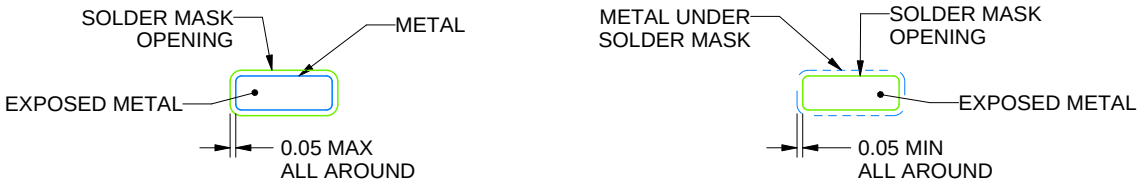

4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

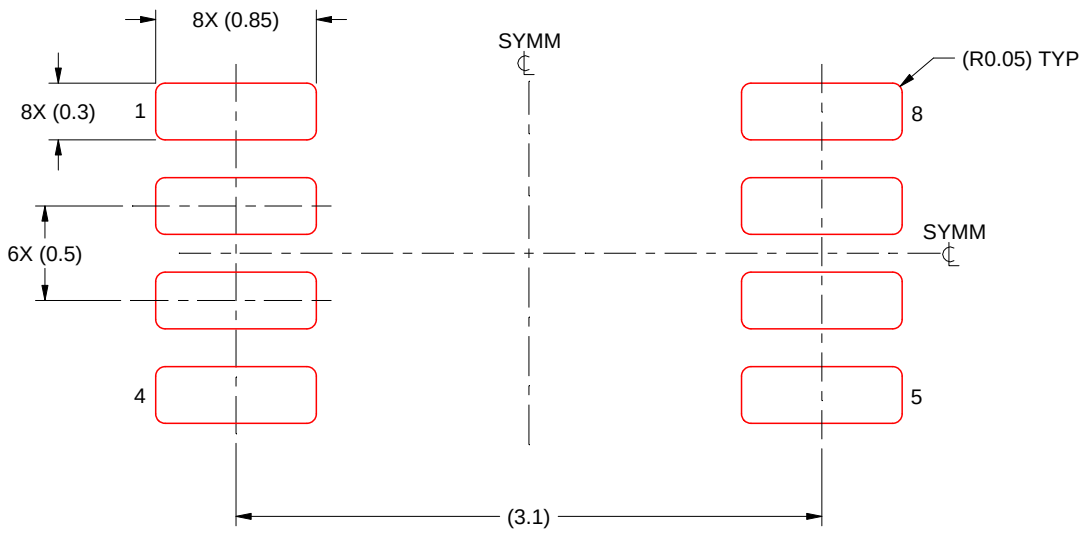



SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

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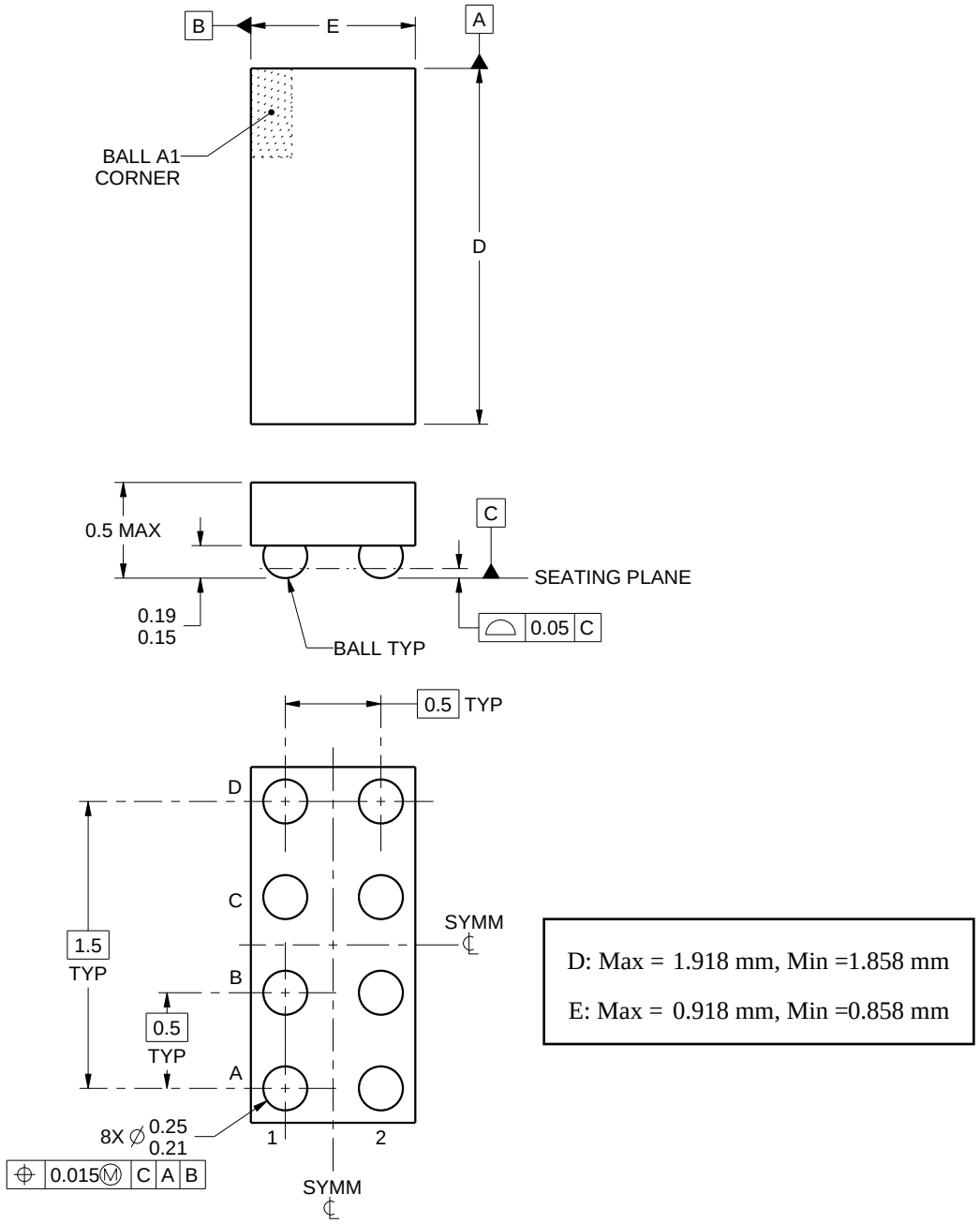
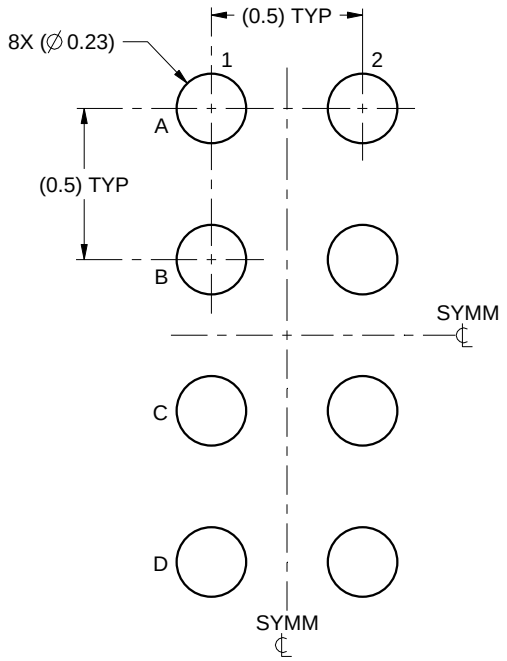
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

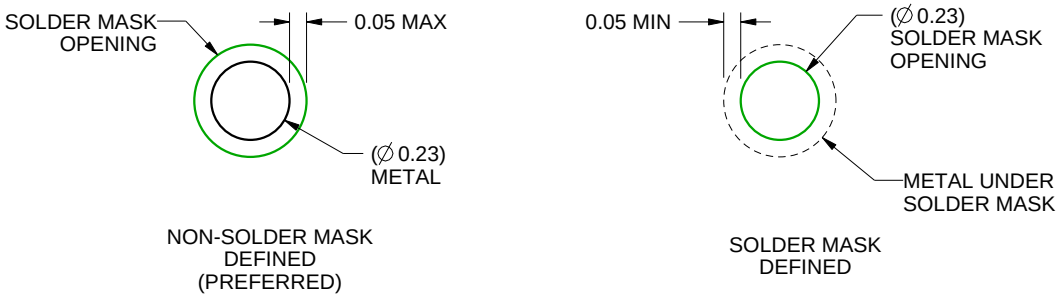



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:40X




SOLDER MASK DETAILS
NOT TO SCALE

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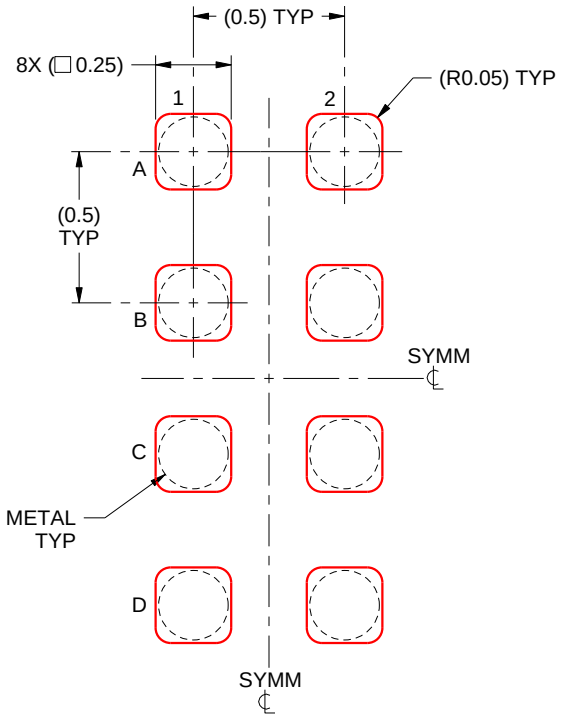
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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