SN74AUP1G32 低功耗单路双输入正或门

1 特性

- 采用间距为 0.5mm 的超小型 0.64mm^2 封装 (DPW)
- 低静态功耗
  （I_{CC} = 0.9 μA，最大值）
- 低动态功耗
  （C_{pd} = 4.3pF，3.3V 时的典型值）
- 低输入电容（C_I = 1.5pF，典型值）
- 低噪声 – 过冲和下冲
  低于 V_{CC} 的 10%
- I_{off} 支持带电插入、局部断电模式和后驱动保护
- 输入迟滞在 V_{hys} = 250mV（3.3V 时的典型值）输入下
  可实现缓慢的输入转换和更好的开关噪声抗扰度
- 宽工作 V_{CC} 范围为 0.8V 至 3.6V
- 针对 3.3V 运行进行了优化
- 3.6V 耐压 I/O 支持混合模式的信号操作
- 3.3V 时，t_{pd} = 4.6ns（最大值）
- 适用于点到点应用
- 闩锁性能超过 100mA，
  符合 JESD 78 II 类规范的要求
- ESD 性能测试符合 JESD 22 标准
  - 2000V 人体放电模型
    （A114-B，II 类）
  - 1000V 带电器件模型 (C101)

2 应用

- ATCA 解决方案
- 主动噪声消除 (ANC)
- 数据表末尾条形码扫描仪
- 血压监护仪
- CPAP 呼吸机
- 线缆解决方案
- DLP 3D 机器视觉、高光谱成像、光纤网络和光谱分析
- 电子书
- 嵌入式 PC
- 现场变送器：温度或湿度传感器
- 指纹生物识别
- HVAC：暖通空调
- 网络附加存储 (NAS)
- 服务器主板和 PSU
- 软件定义无线电 (SDR)
- 电视：高清电视 (HDTV)、LCD 电视和数字电视
- 视频通信系统
- 无线数据存取卡、耳机、键盘、鼠标和 LAN 卡
- X 射线：行李扫描仪、医疗和牙科

3 说明

此单路双输入正或门以正逻辑执行布尔函数 $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
SN74AUP1G32	SOT (5)	1.60mm × 1.20mm
	USON (6)	1.45mm × 1.00mm
	X2SON (4)	0.80mm × 0.80mm
	DSBGA (6)	1.19mm × 0.79mm
	DSBGA (5)	1.41mm × 0.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision J (September 2019) to Revision K (May 2020) — **Page**

- Corrected DPW package image description to "DPW Package X2SON 5-pins (Transparent Top View)" 3
- Updated DPW package image 3

Changes from Revision I (June 2014) to Revision J (September 2019) — **Page**

- Changed format of Pin Configuration images to allow for HTML search function 3
- Corrected YFP package pin descriptors in the Pin Functions table 3
- Added Thermal Information for the DPW package 5

Changes from Revision H (August 2012) to Revision I (June 2014) — **Page**

- 将文档更新为新的 TI 数据表格式 1
- 删除了“订购信息”表 1
- 添加了“应用” 1
- Added Handling Ratings table 4
- Added Thermal Information table 5
- Added Typical Characteristics 8

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5 Pin Configuration and Functions

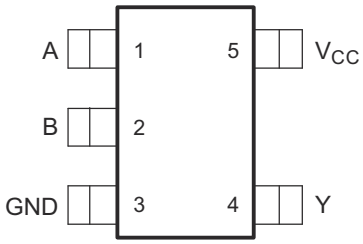


图 5-1. DBV Package SOT 5-pin (Top View)

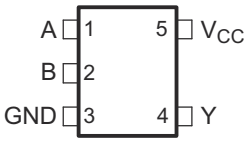


图 5-2. DRL Package SOT 5-pin (Top View)

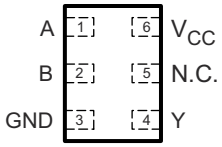
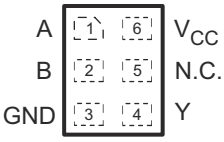


图 5-3. DSF Package SON 6-pin (Transparent Top View)



N.C. - No internal connection

图 5-4. DRY Package SON 6-pin (Transparent Top View)

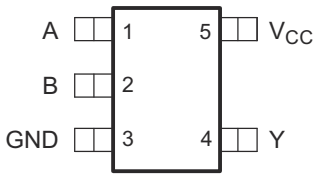


图 5-5. DCK Package SC70 5-pin (Top View)

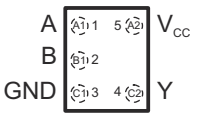
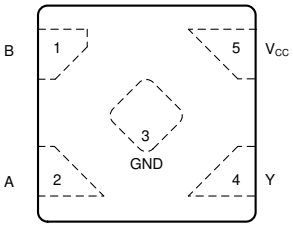


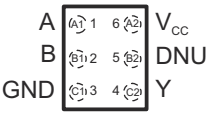
图 5-6. YZP Package DSBGA 5-balls (Transparent Top View)



Not to scale

See mechanical drawings at the end of the data sheet for all package dimensions

图 5-7. DPW Package X2SON 5-pins (Transparent Top View)



DNU - Do Not Use

图 5-8. YFP Package DSBGA 6-balls (Transparent Top View)

Pin Functions

PIN						I/O	DESCRIPTION
NAME	DRL, DCK, DBV	DPW	DRY, DSF	YZP	YFP		
A	1	2	1	A1	A1	I	Input A
B	2	1	2	B1	B1	I	Input B
GND	3	3	3	C1	C1	–	Ground
Y	4	4	4	C2	C2	O	Output Y
V_{CC}	5	5	6	A2	A2	–	Power Pin

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	4.6	V
V_I	Input voltage range(2)		– 0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		– 0.5	4.6	V
V_O	Voltage range applied to any output in the high or low state(2)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		– 50	mA
I_{OK}	Output clamp current	V_O < 0		– 50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		– 65	125	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

see (1)			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		– 20	μA
		V_{CC} = 1.1 V		– 1.1	mA
		V_{CC} = 1.4 V		– 1.7	
		V_{CC} = 1.65 V		– 1.9	
		V_{CC} = 2.3 V		– 3.1	
		V_{CC} = 3 V		– 4	

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see (1)			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
$\Delta t/\Delta v$	Input transition rise and fall rate	V_{CC} = 0.8 V to 1.95 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		DBV	DCK	DRL	DSF	DRY	DPW	UNIT
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard data sheet value)	271.4	338.4	349.7	407.1	554.9	492.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (standard data sheet value)	213.5	110.6	120.5	232.0	385.4	232.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (standard data sheet value)	108.2	118.8	171.4	306.9	388.2	355.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter (standard data sheet value)	89.3	3.0	10.8	40.3	159.0	37.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter (standard data sheet value)	107.6	117.8	169.4	306.0	384.1	353.9	°C/W
$\psi_{JC(bot)}$	Junction-to-case (bottom) thermal resistance (standard data sheet value)	–	–	–	–	–	147.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OH}	I_{OH} = –20 µA	0.8 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V
	I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
	I_{OH} = –1.7 mA	1.4 V	1.11			1.03		
	I_{OH} = –1.9 mA	1.65 V	1.32			1.3		
	I_{OH} = –2.3 mA	2.3 V	2.05			1.97		
	I_{OH} = –3.1 mA		1.9			1.85		
	I_{OH} = –2.7 mA	3 V	2.72			2.67		
	I_{OH} = –4 mA		2.6			2.55		
V_{OL}	I_{OL} = 20 µA	0.8 V to 3.6 V			0.1		0.1	V
	I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
	I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
	I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
	I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
	I_{OL} = 3.1 mA				0.44		0.45	
	I_{OL} = 2.7 mA	3 V			0.31		0.33	
	I_{OL} = 4 mA				0.44		0.45	
I_I A or B input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	µA
I_{off}	V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	µA
ΔI_{off}	V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	µA
I_{CC}	V_I = GND or (V_{CC} to 3.6 V), I_O = 0	0.8 V to 3.6 V			0.5		0.9	µA
ΔI_{CC}	V_I = V_{CC} – 0.6 V(1), I_O = 0	3.3 V			40		50	µA
C_i	V_I = V_{CC} or GND	0 V		1.5				pF
		3.6 V		1.5				
C_o	V_O = GND	0 V		3				pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

6.6 Switching Characteristics, C_L = 5 pF

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1 and 图 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		18				ns
			1.2 V ± 0.1 V	2.6	7.3	13.5	2.1	16.8	
			1.5 V ± 0.1 V	1.4	5.2	9.1	0.9	11	
			1.8 V ± 0.15 V	1	4.2	7	0.5	8.8	
			2.5 V ± 0.2 V	1	3	4.7	0.5	6	
			3.3 V ± 0.3 V	1	2.4	3.7	0.5	4.6	

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6.7 Switching Characteristics, C_L = 10 pF

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1 and 图 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		21				ns
			1.2 V ± 0.1 V	1.5	8.5	15.4	1	18.4	
			1.5 V ± 0.1 V	1	6.2	10.4	0.5	12	
			1.8 V ± 0.15 V	1	5	8.1	0.5	9.6	
			2.5 V ± 0.2 V	1	3.6	5.5	0.5	6.6	
			3.3 V ± 0.3 V	1	2.9	4.4	0.5	5	

6.8 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1 and 图 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		24				ns
			1.2 V ± 0.1 V	3.6	9.9	17	3.1	21.1	
			1.5 V ± 0.1 V	2.3	7.2	11.5	1.8	13.9	
			1.8 V ± 0.15 V	1.6	5.8	9.1	1.1	11.2	
			2.5 V ± 0.2 V	1	4.3	6.2	0.5	7.8	
			3.3 V ± 0.3 V	1	3.4	5	0.5	6.2	

6.9 Switching Characteristics, C_L = 30 pF

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1 and 图 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		32.8				ns
			1.2 V ± 0.1 V	4.9	13.1	21.6	4.4	26.7	
			1.5 V ± 0.1 V	3.4	9.5	14.6	2.9	17.6	
			1.8 V ± 0.15 V	2.5	7.7	11.4	2	14.1	
			2.5 V ± 0.2 V	1.8	5.7	7.9	1.3	9.9	
			3.3 V ± 0.3 V	1.5	4.7	6.4	1	7.8	

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4.1	pF
			1.2 V ± 0.1 V	4.1	
			1.5 V ± 0.1 V	4.1	
			1.8 V ± 0.15 V	4.1	
			2.5 V ± 0.2 V	4.2	
			3.3 V ± 0.3 V	4.3	

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6.11 Typical Characteristics

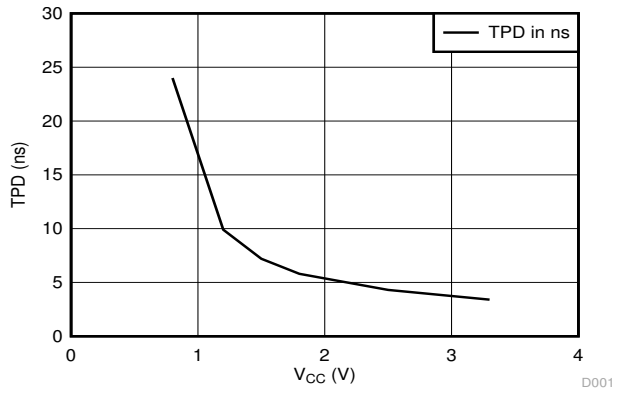


图 6-1. TPD vs V_{CC}, 15 pF Load

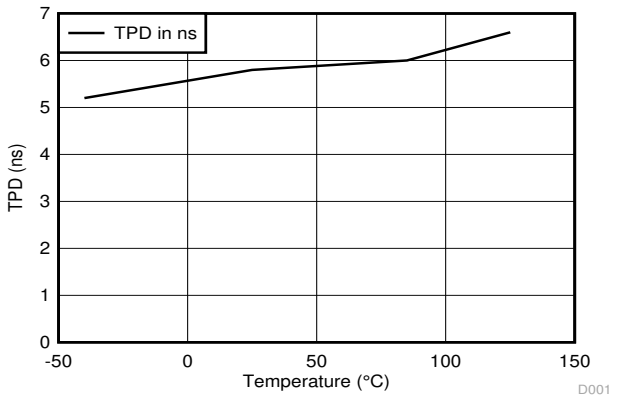
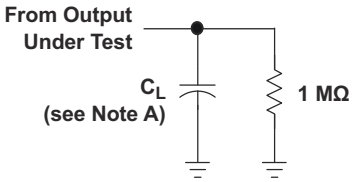


图 6-2. Temperature 1.8 V, 15 pF Load

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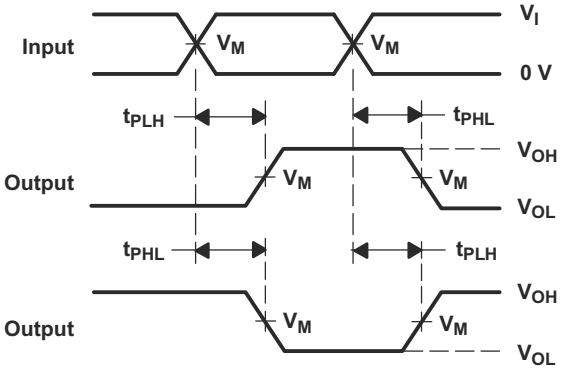
7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Width

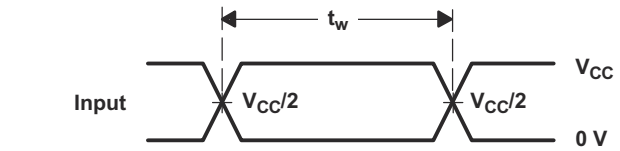


LOAD CIRCUIT

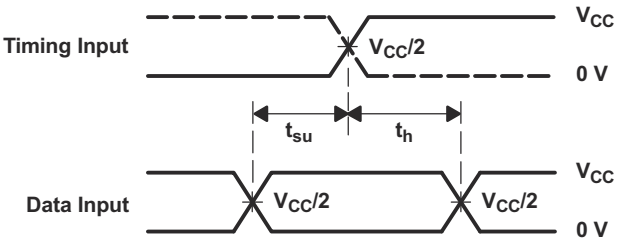
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION



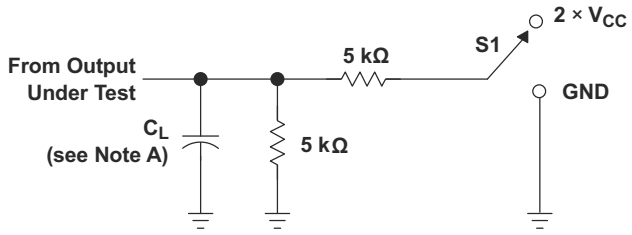
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r and t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

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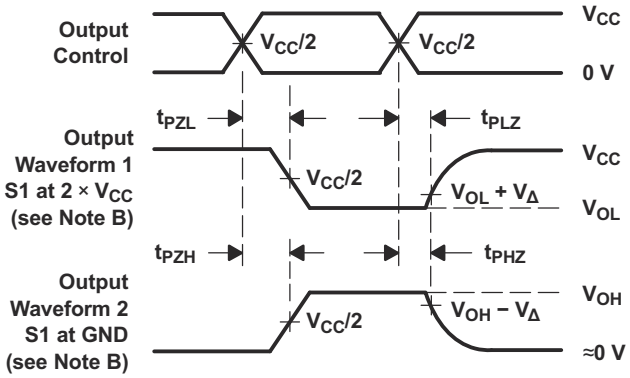
7.2 Enable and Disable Times



TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	2 × V_{CC} GND

LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_D	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
C. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, Z_O = 50 Ω, t_r and t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

图 7-2. Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

This single 2-input positive-OR gate that operates from 0.8 V to 3.6 V and performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The AUP family of devices has quiescent power consumption less than 1 µA and comes in the ultra small DPW package. The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating V_{CC} range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V
- Low noise due to slower edge rates

8.4 Device Functional Modes

表 8-1. Function Table

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	H

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9 Application and Implementation

备注

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9.1 Application Information

The AUP family is TI's premier solution to the industry’s low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire VCC range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

The AUP family of single gate logic makes excellent translators for the new lower voltage Micro- processors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

9.2 Typical Application

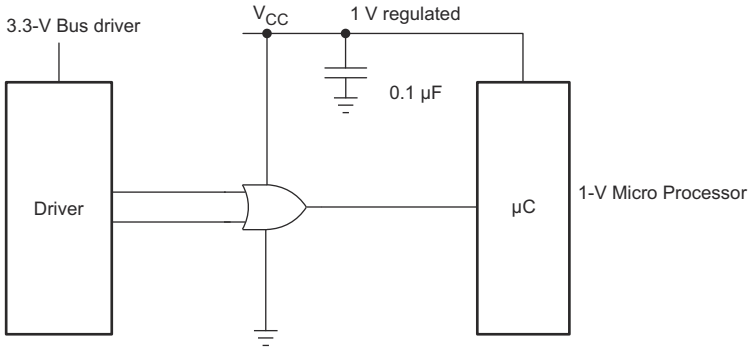


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

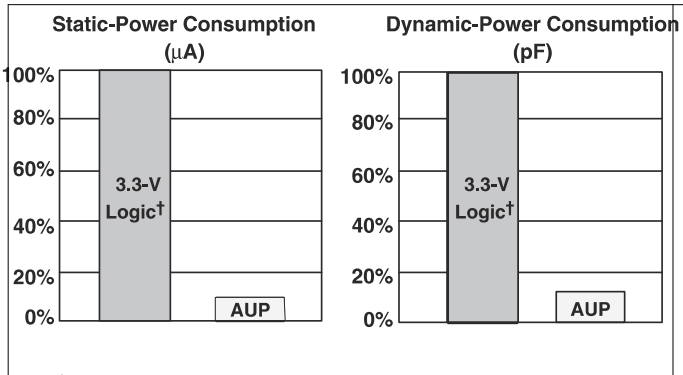
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

9.2.2 Detailed Design Procedure

1. Recommended Input conditions
   - Rise time and fall time specifications. See ($\Delta t/\Delta V$) in *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC}
2. Recommend output conditions
   - Load currents should not exceed 20 mA on the output and 50 mA total for the part
   - Outputs should not be pulled above V_{CC}

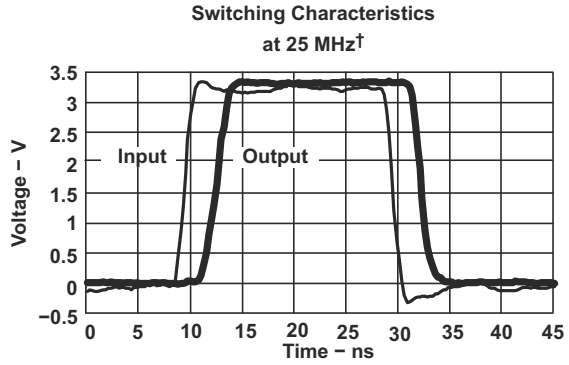
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9.2.3 Application Curves



† Single, dual, and triple gates.

图 9-2. AUP – The Lowest-Power Family



† AUP1G08 data at C_L = 15 pF

图 9-3. Excellent Signal Integrity

10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended and if there are multiple V_{CC} terminals then .01 μF or .022 μF is recommended for each power terminal. It is ok to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

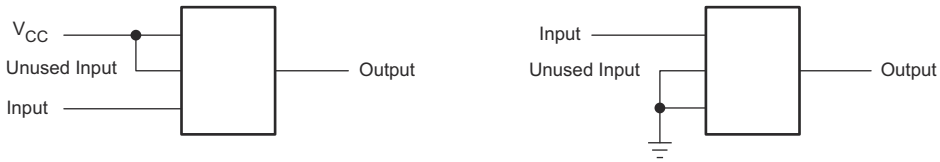
11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O’s so they also cannot float when disabled.

11.2 Layout Example



12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

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12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP1G32DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R
SN74AUP1G32DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(HG5, HGF, HGK, HGR)
SN74AUP1G32DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(HG5, HGF, HGK, HGR)
SN74AUP1G32DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HG5, HGR)
SN74AUP1G32DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HG5, HGR)
SN74AUP1G32DCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG5
SN74AUP1G32DCKTG4.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG5
SN74AUP1G32DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F4
SN74AUP1G32DPWR.B	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F4
SN74AUP1G32DRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HG7, HGR)
SN74AUP1G32DRLR.B	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HG7, HGR)
SN74AUP1G32DRY2	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DRY2.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DRYRG4	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DRYRG4.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSF2	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSF2.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSFRG4	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG
SN74AUP1G32DSFRG4.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP1G32YFPR	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	HGN
SN74AUP1G32YFPR.B	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HGN
SN74AUP1G32YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HGN
SN74AUP1G32YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HGN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

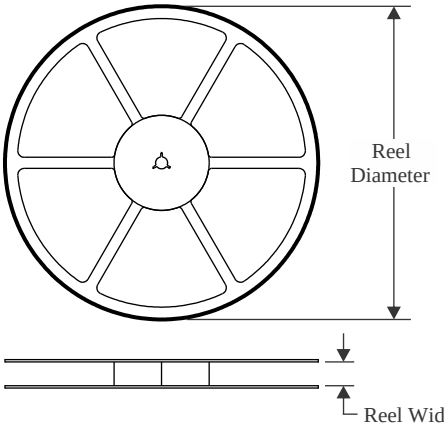
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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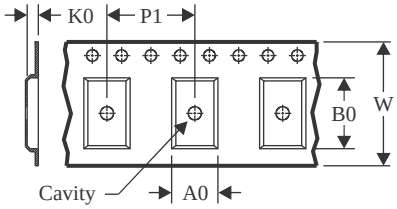
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

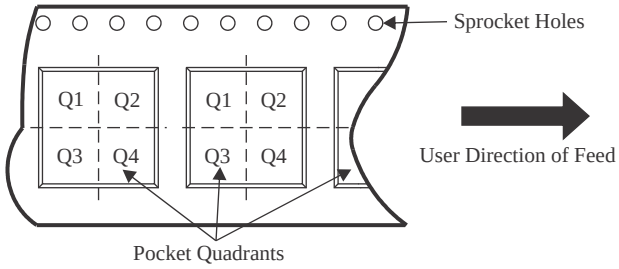


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

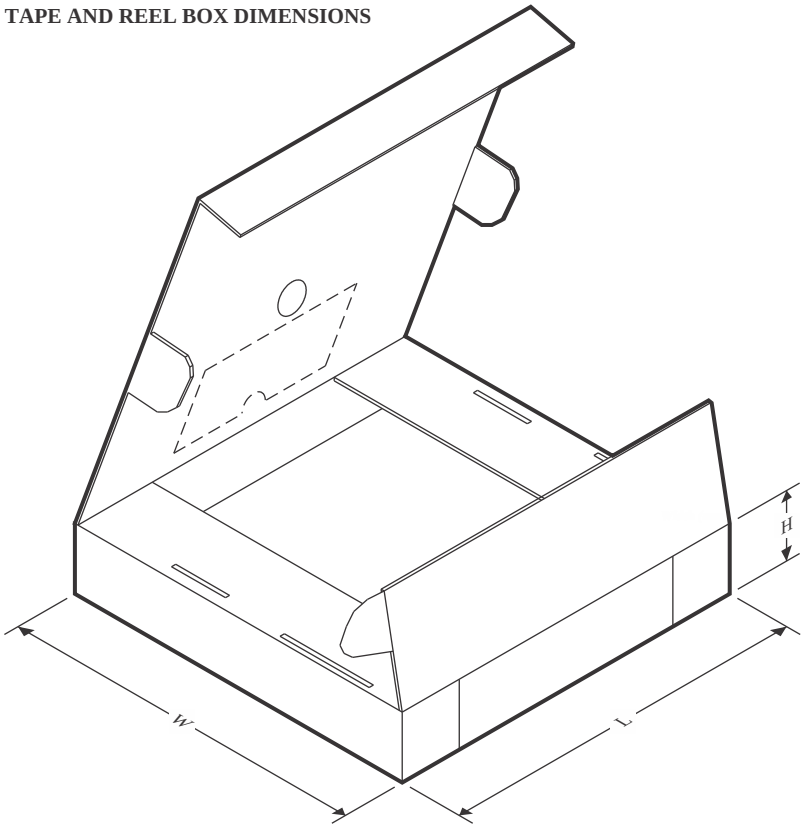


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G32DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G32DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G32DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G32DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUP1G32DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G32DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74AUP1G32DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G32DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G32DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G32DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G32DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G32DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G32DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74AUP1G32DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G32DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1G32DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G32DSF2	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP1G32DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP1G32DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP1G32DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G32DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G32DSFRG4	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G32YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G32YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AUP1G32DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AUP1G32DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74AUP1G32DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G32DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74AUP1G32DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AUP1G32DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74AUP1G32DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G32DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G32DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G32DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G32DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G32DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	184.0	184.0	19.0
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G32DRY2	SON	DRY	6	5000	184.0	184.0	19.0

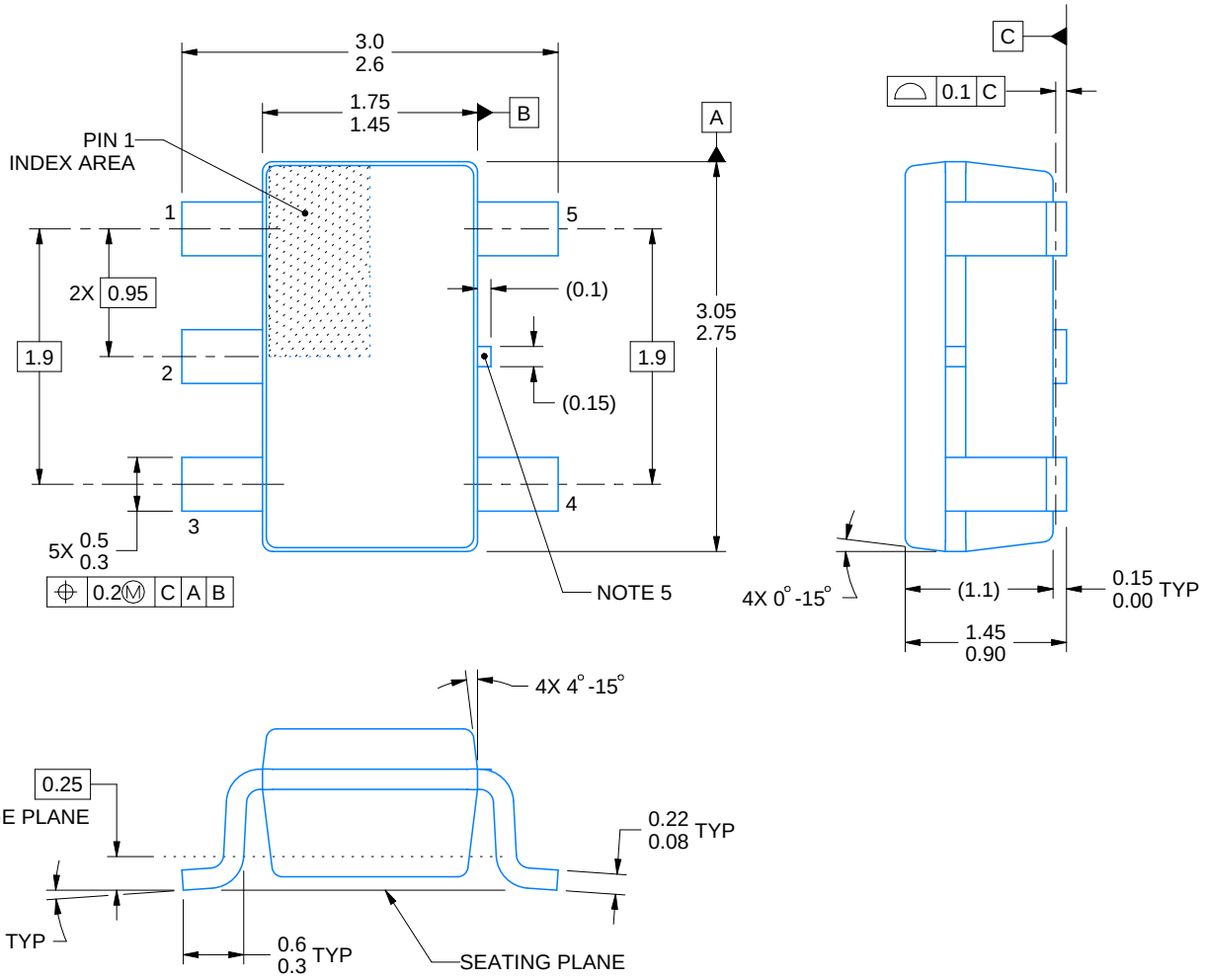
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G32DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G32DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1G32DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G32DSF2	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G32DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G32DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP1G32DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G32DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G32DSFRG4	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G32YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G32YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

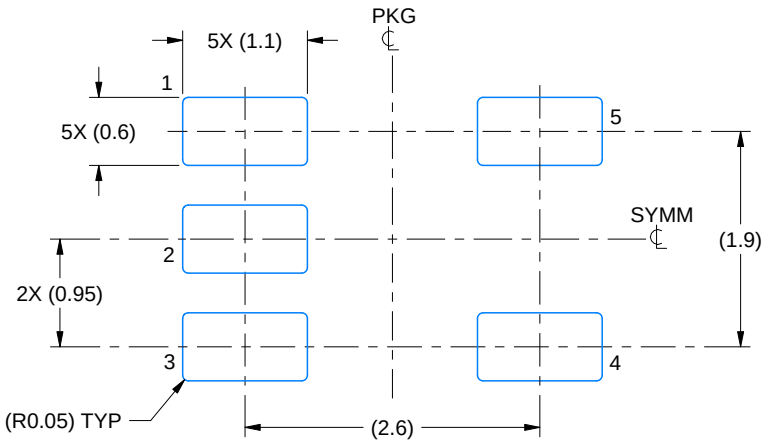
SMALL OUTLINE TRANSISTOR



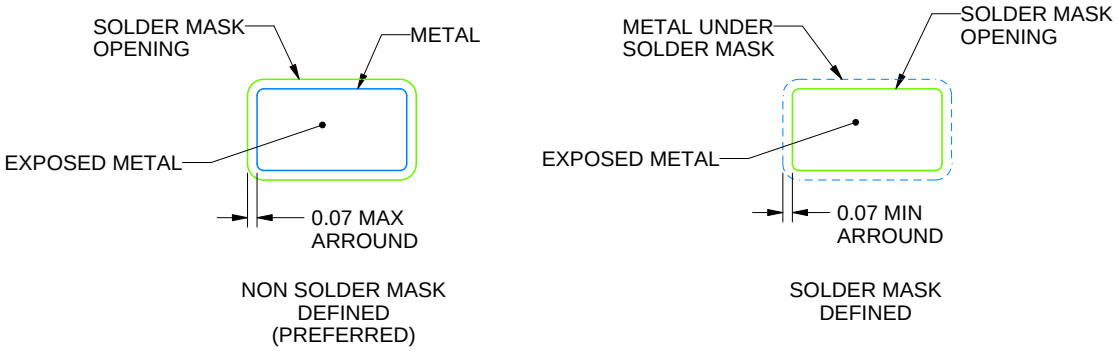
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

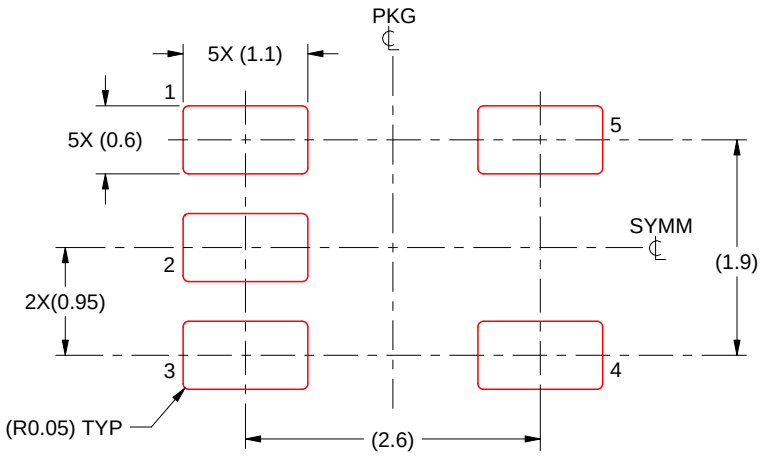


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

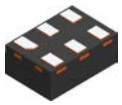
DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

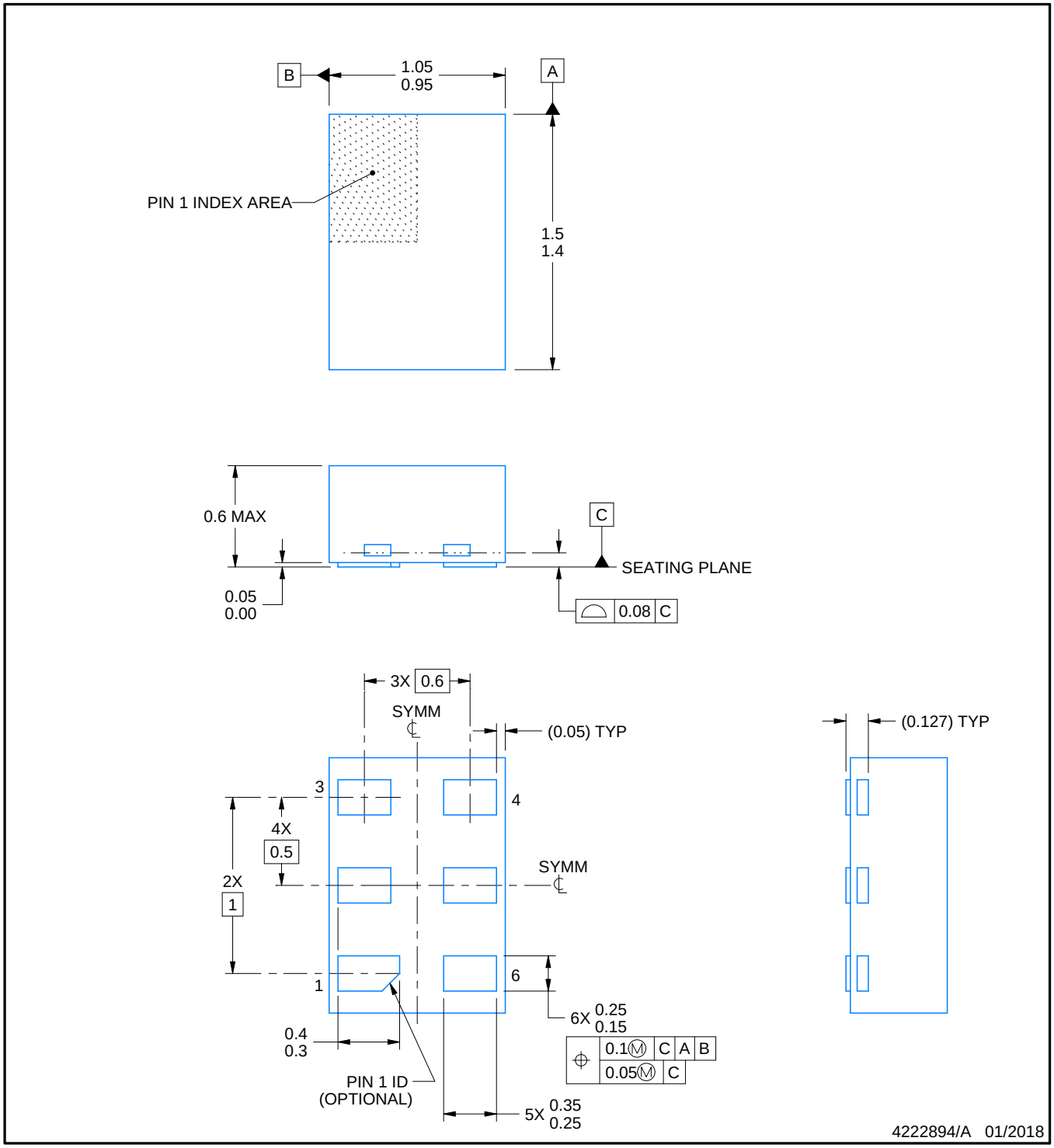
DRY0006A



PACKAGE OUTLINE

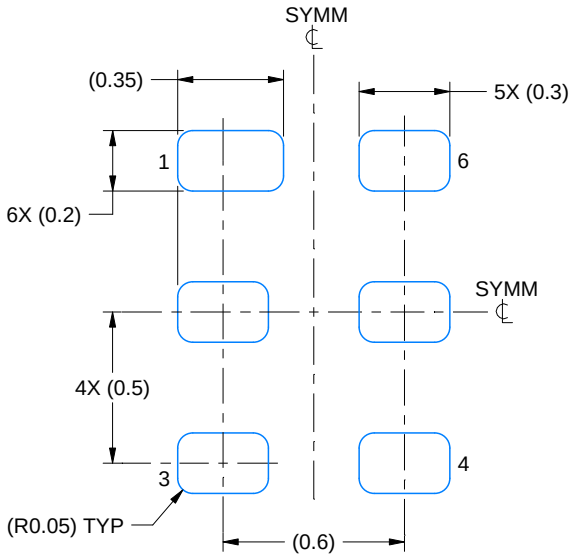
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

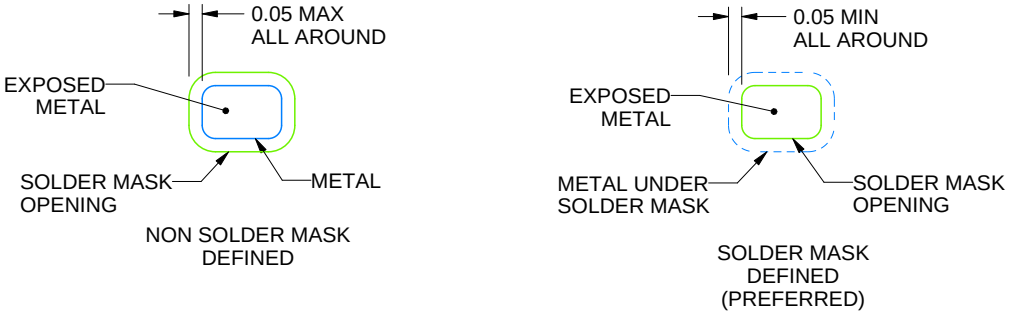


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

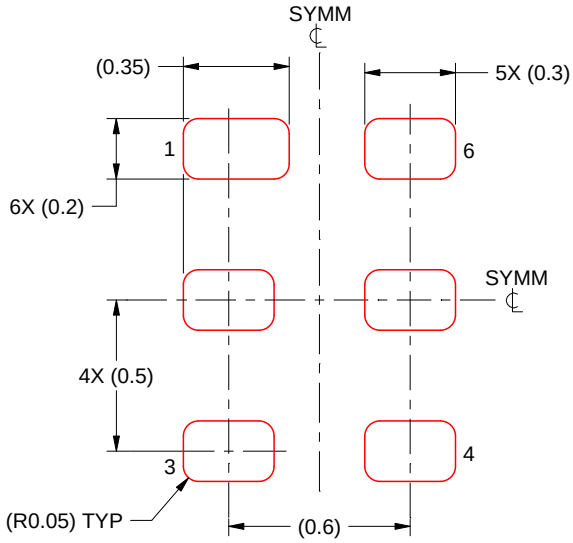
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

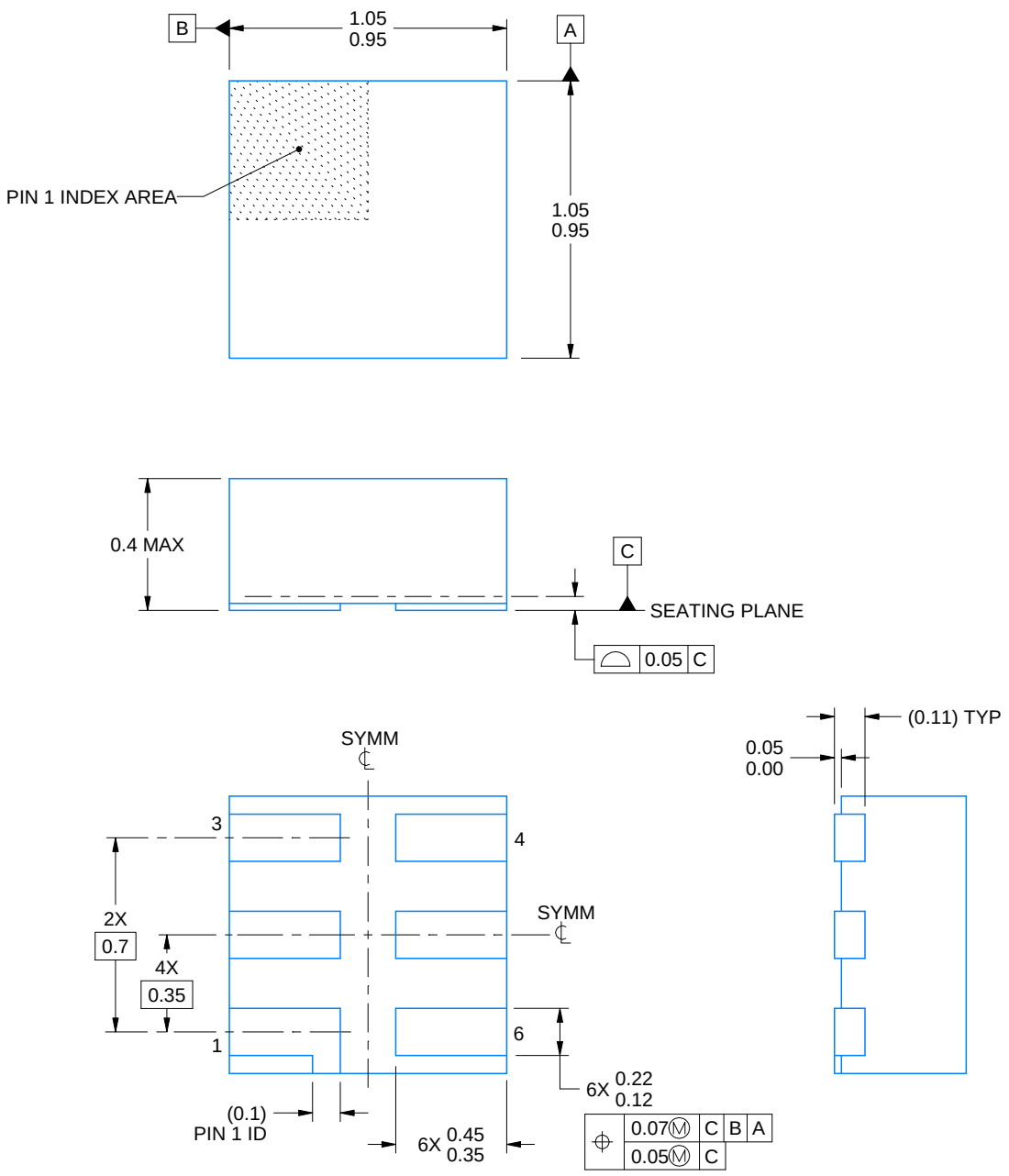
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

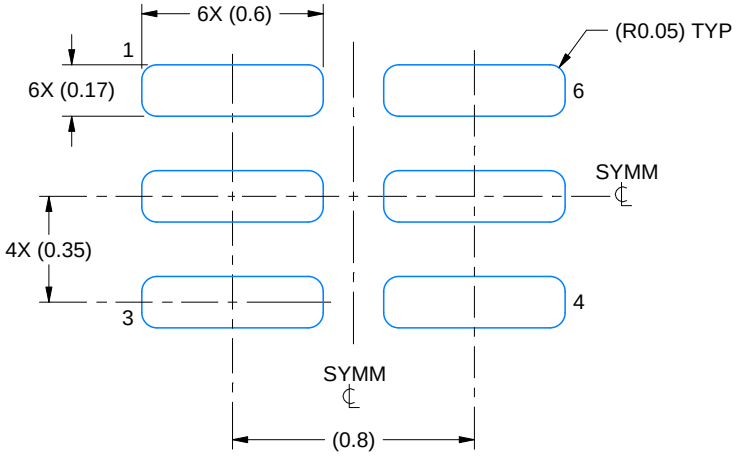
PLASTIC SMALL OUTLINE - NO LEAD



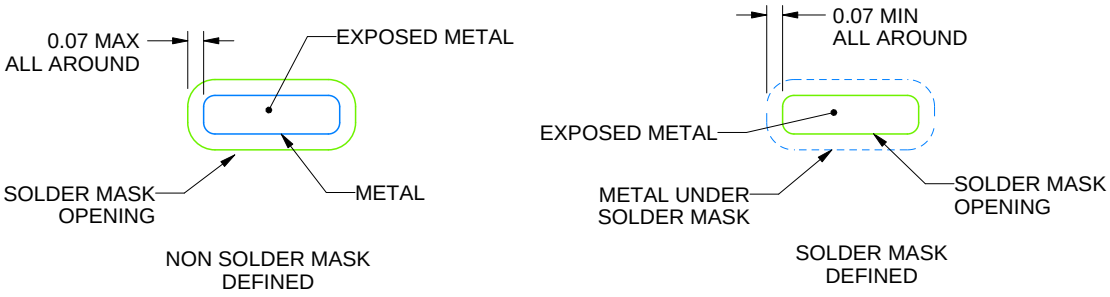
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

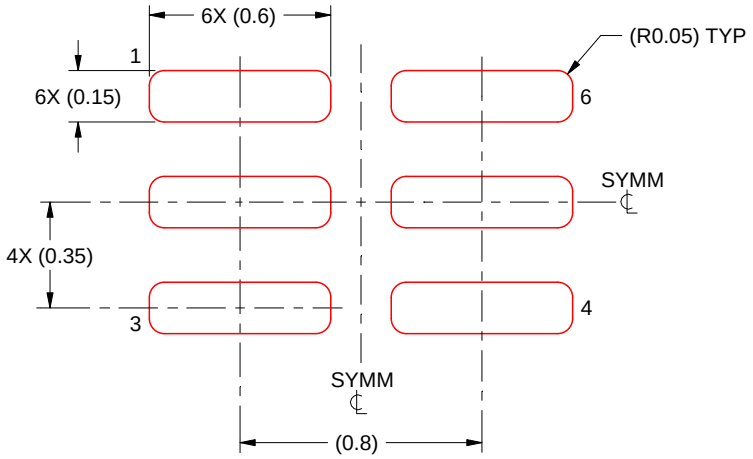
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

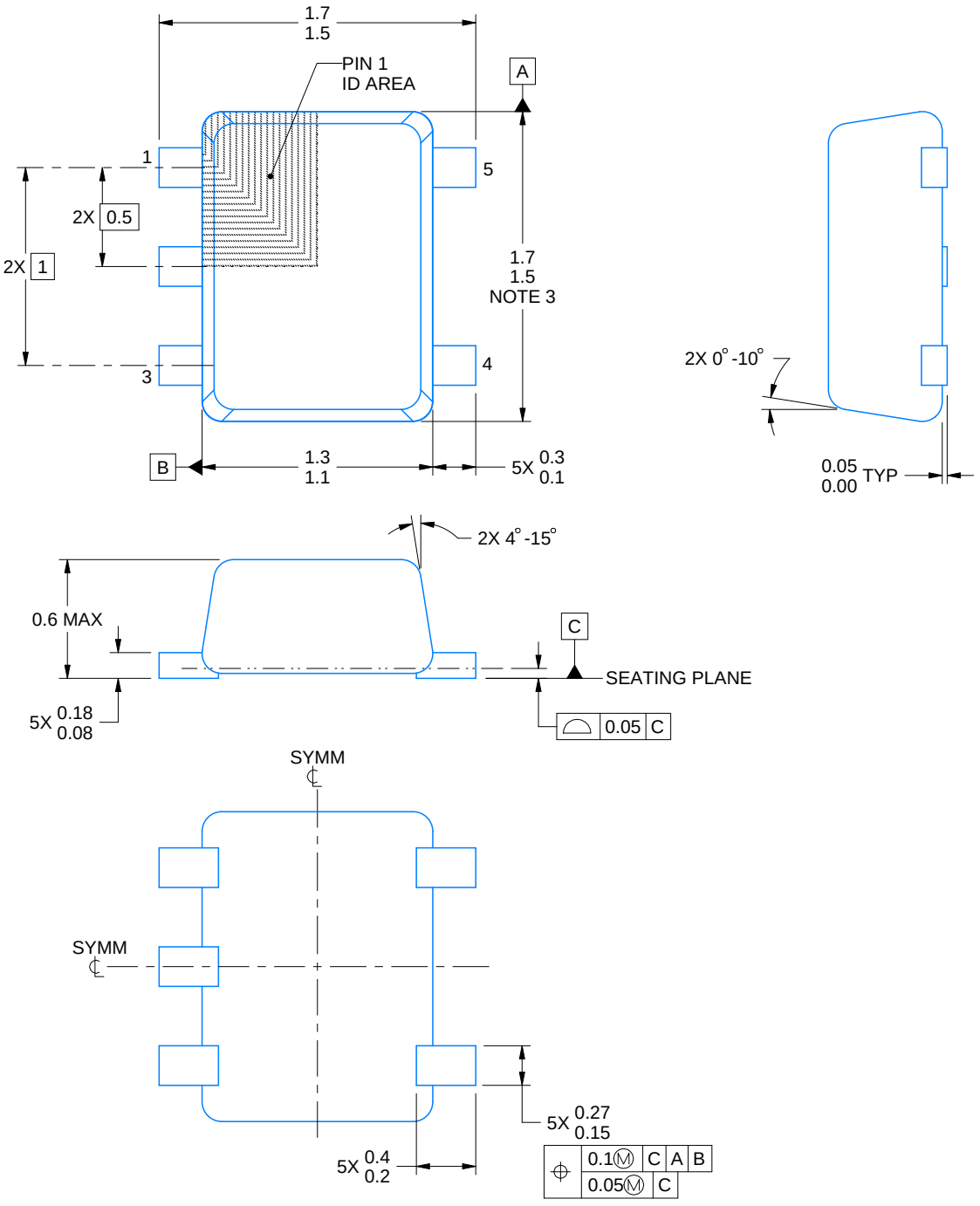
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

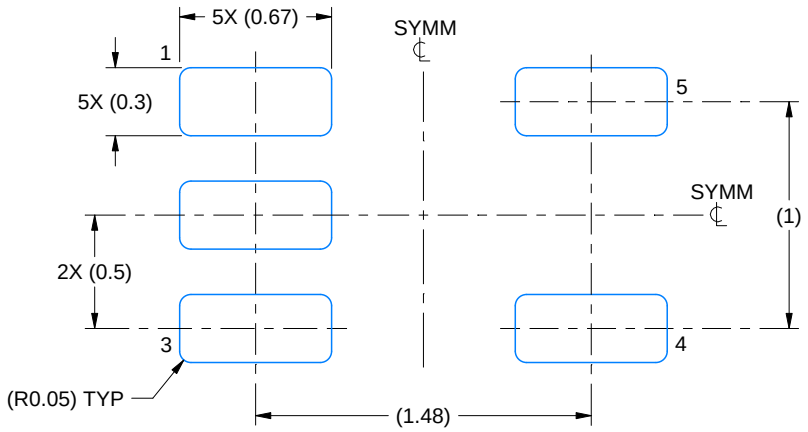
PLASTIC SMALL OUTLINE



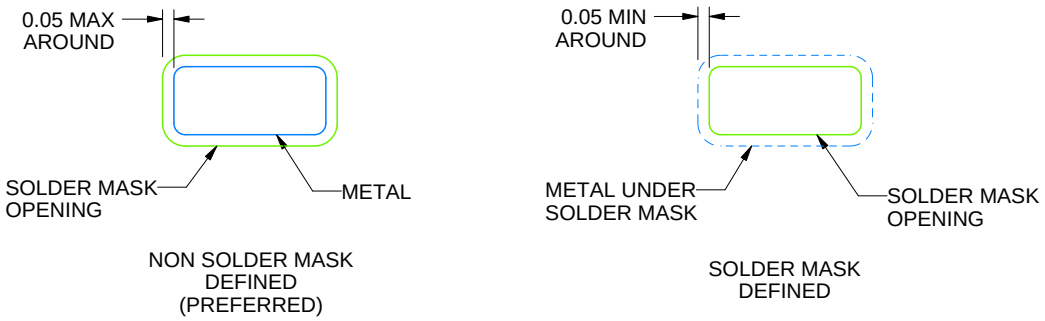
4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

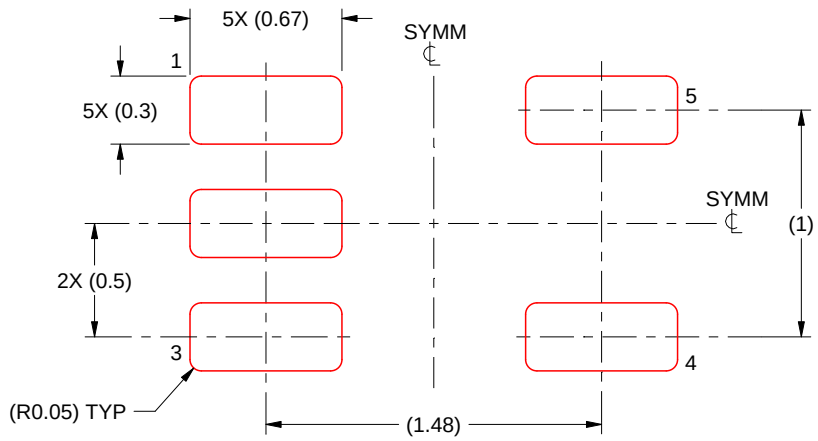


SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

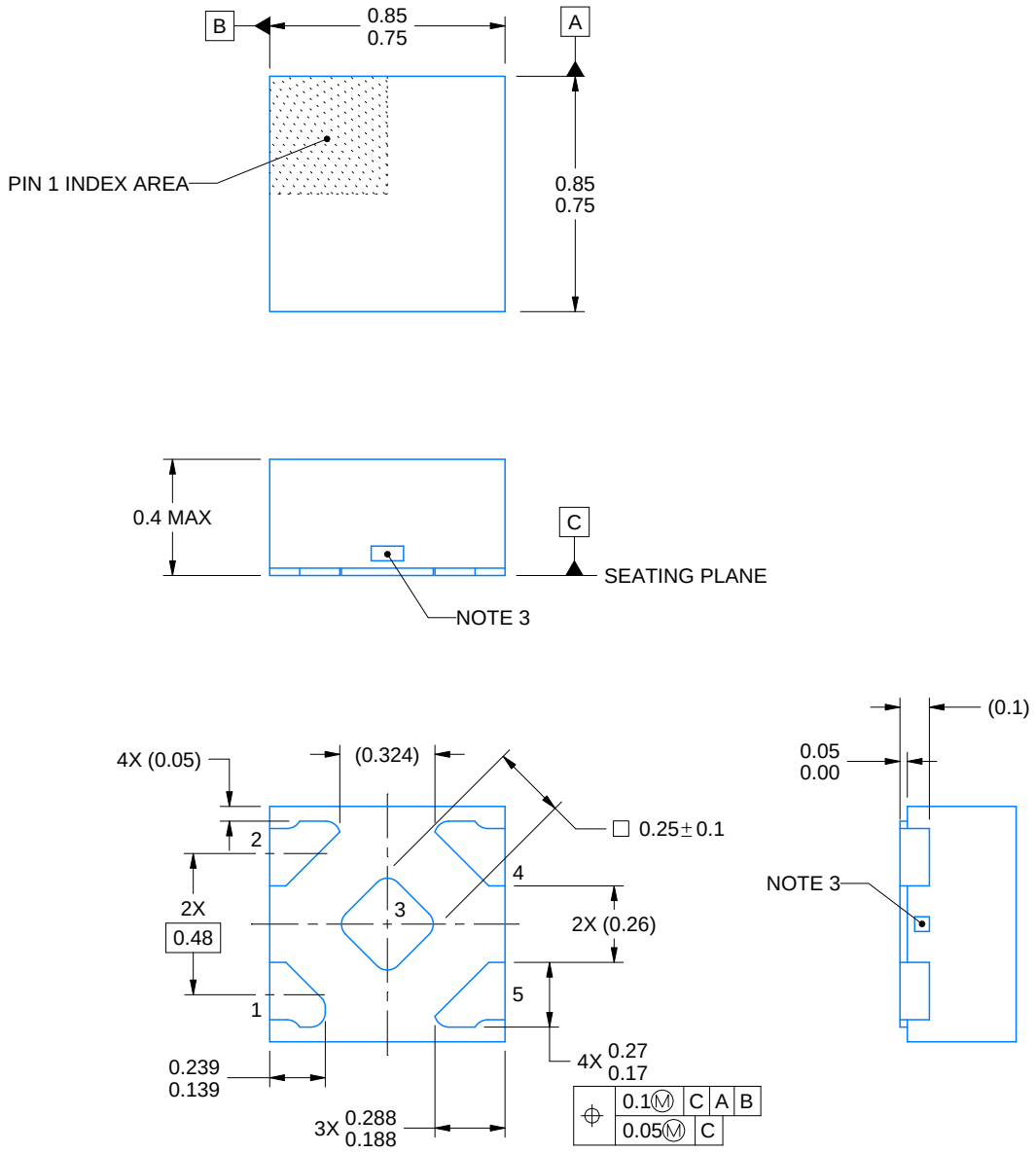
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

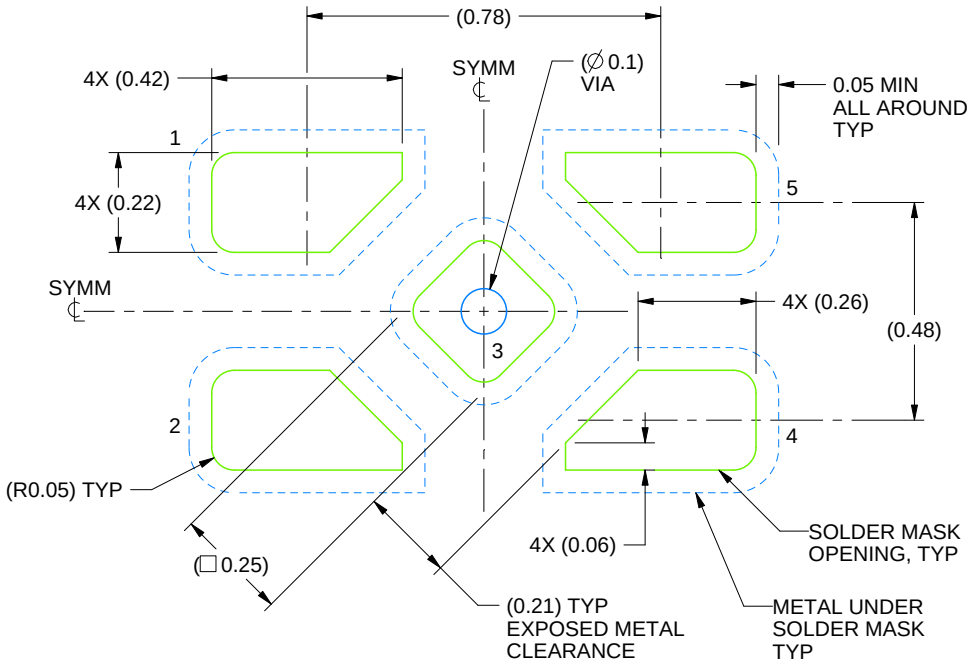
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

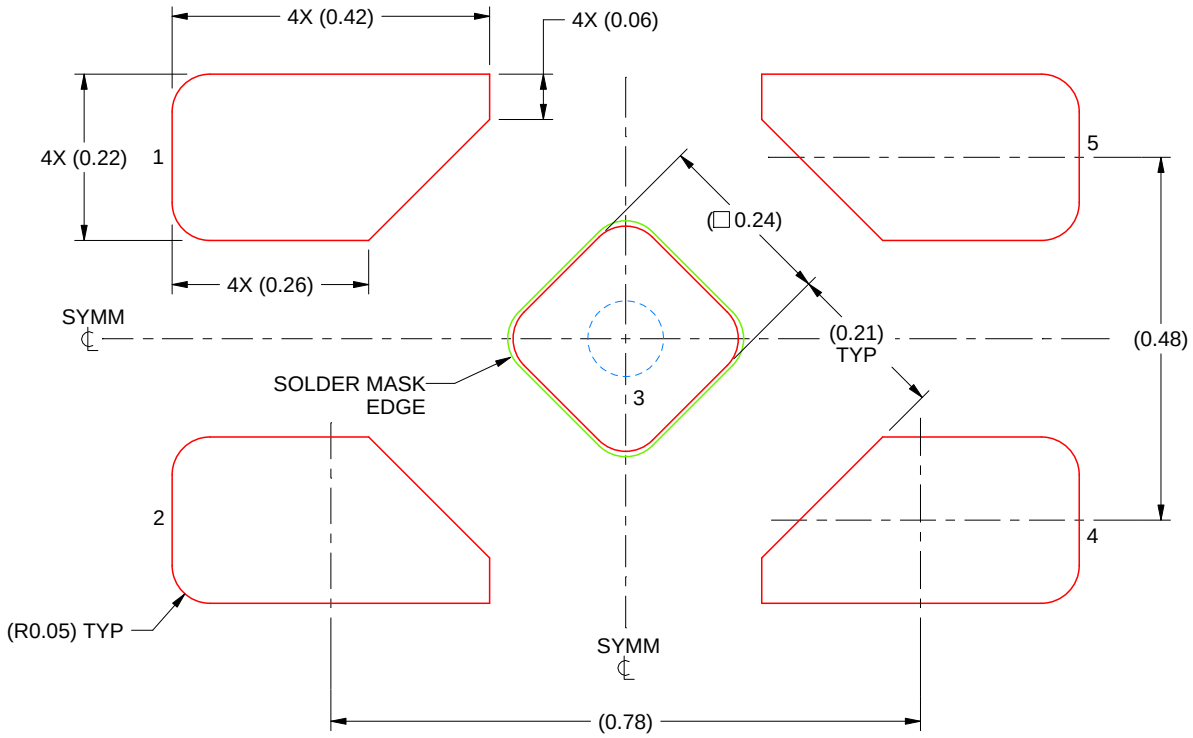
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

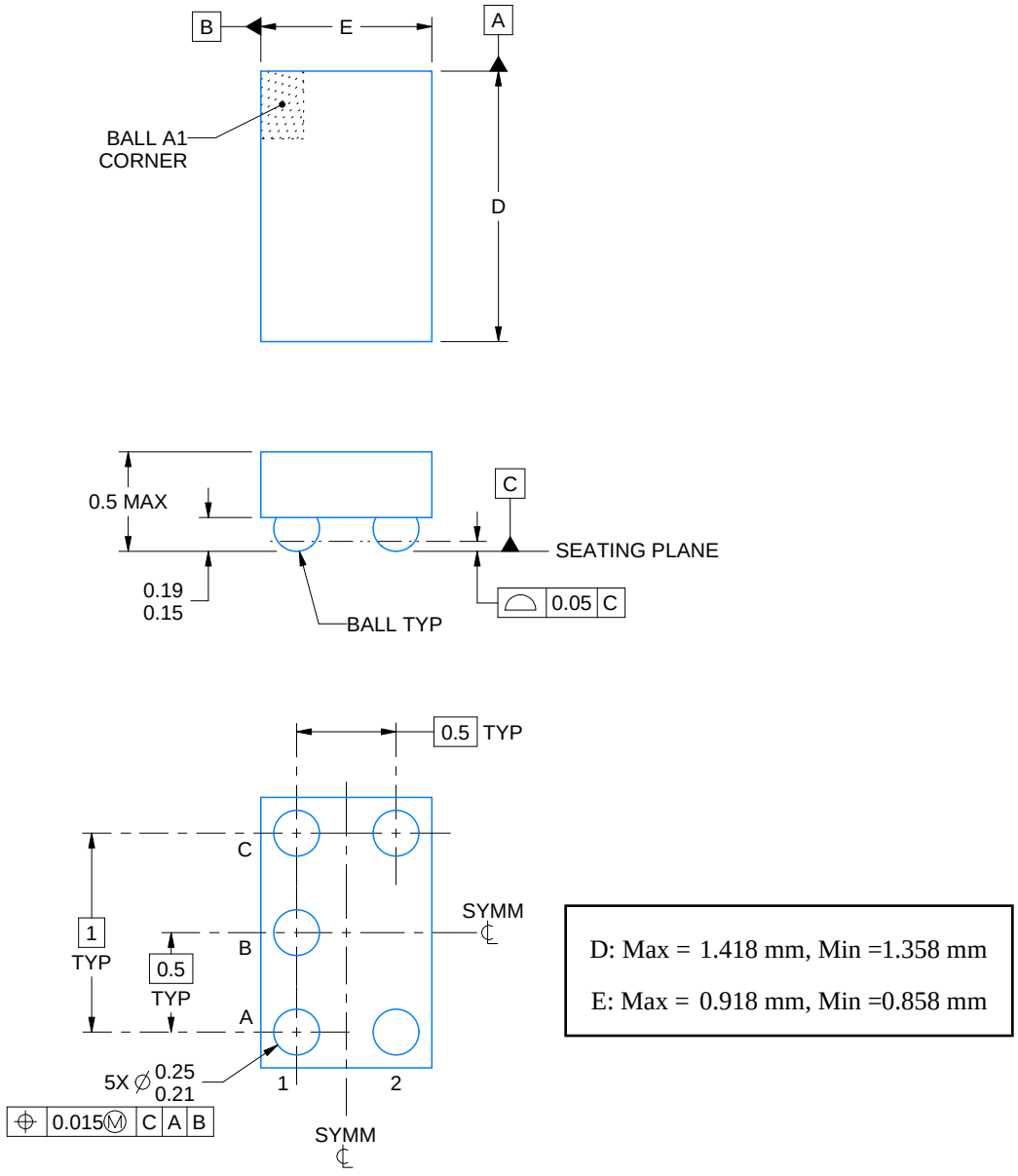
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



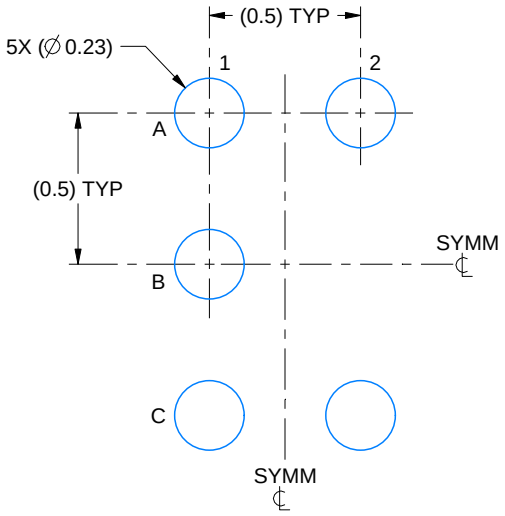
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

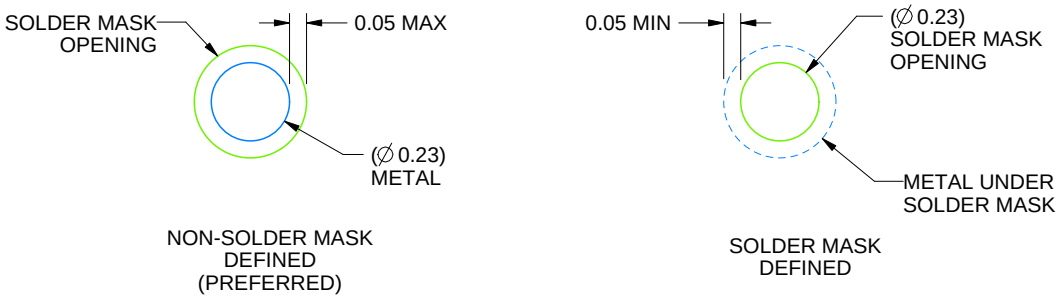
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

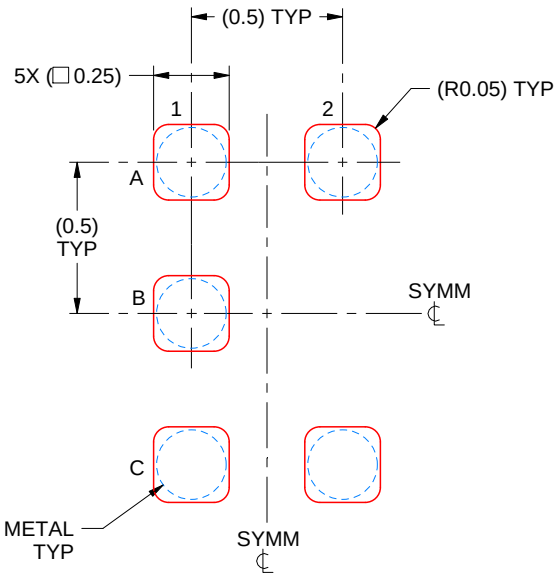


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

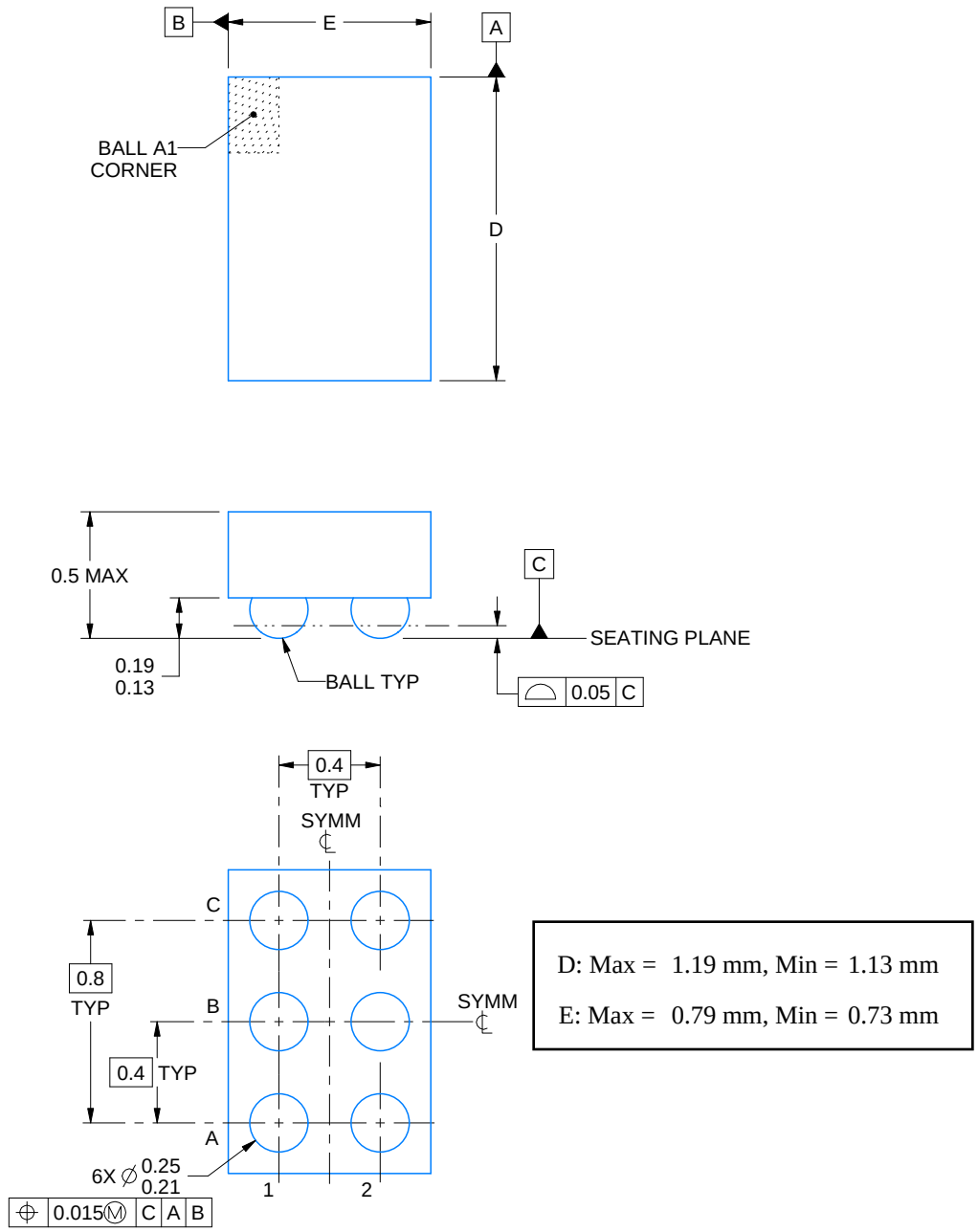
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

YFP0006

DSBGA - 0.5 mm max height

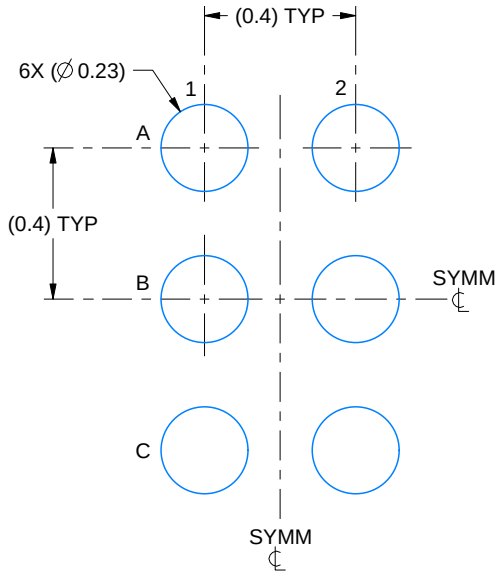
DIE SIZE BALL GRID ARRAY



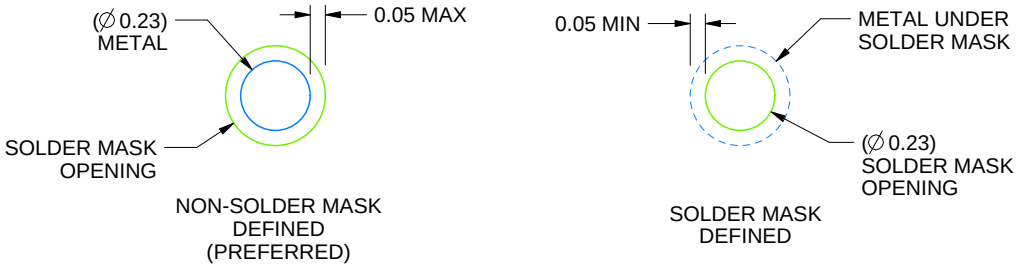
4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X

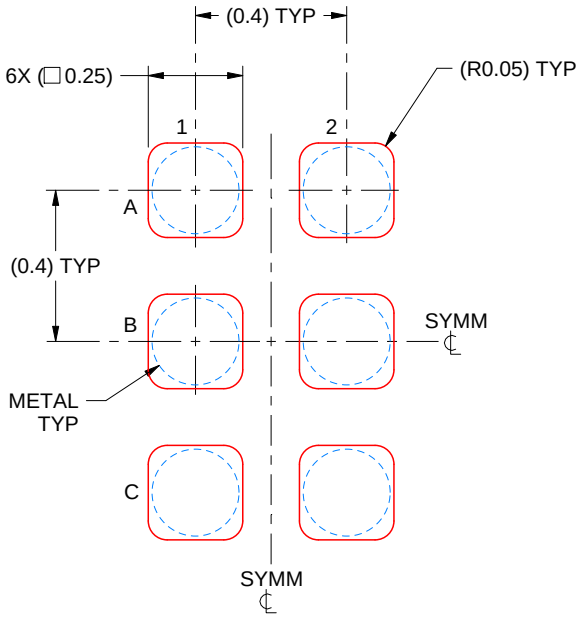


SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

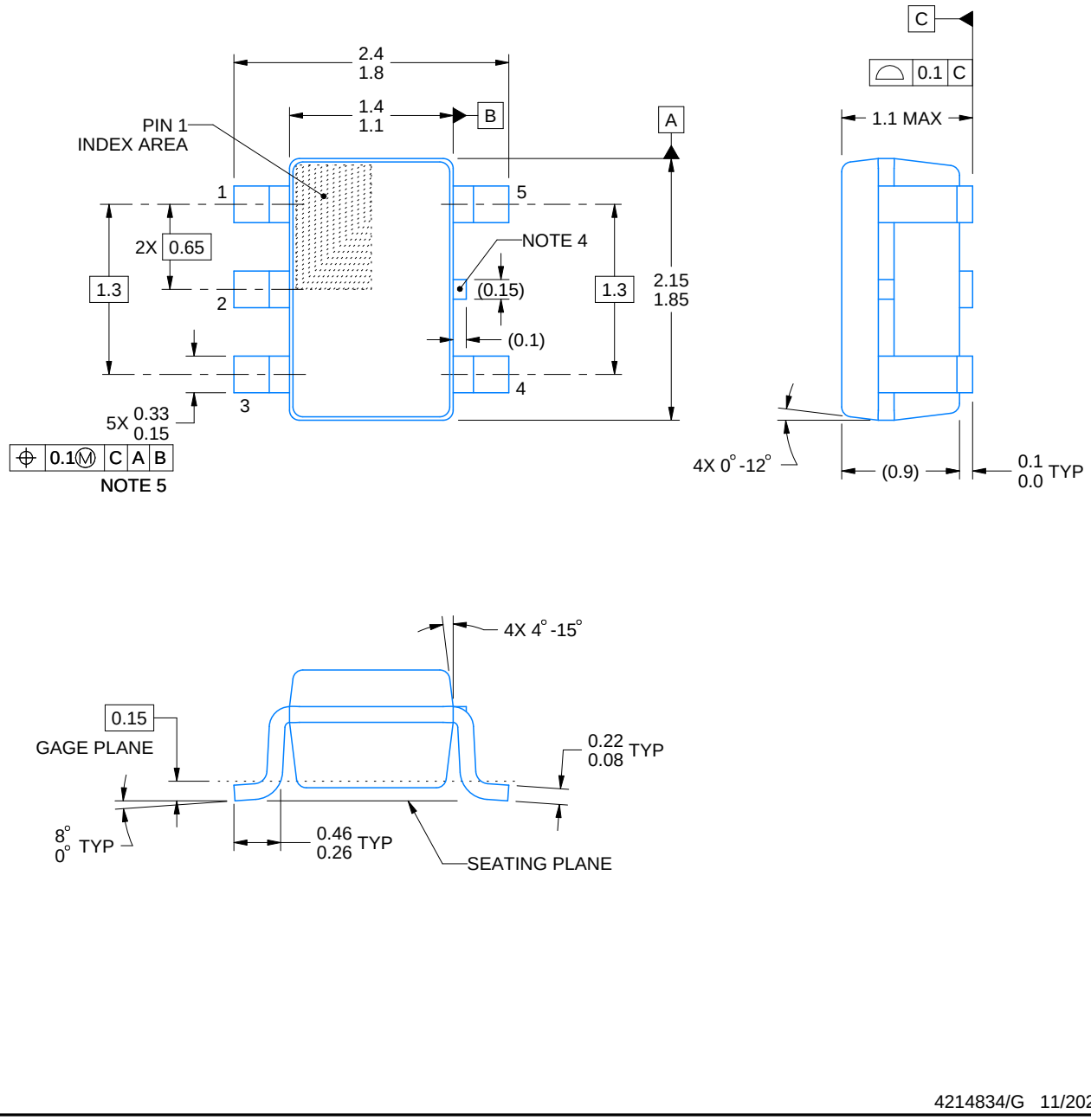
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

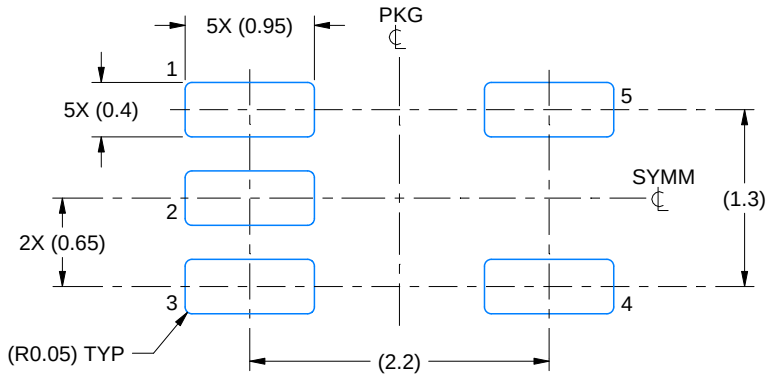
SMALL OUTLINE TRANSISTOR



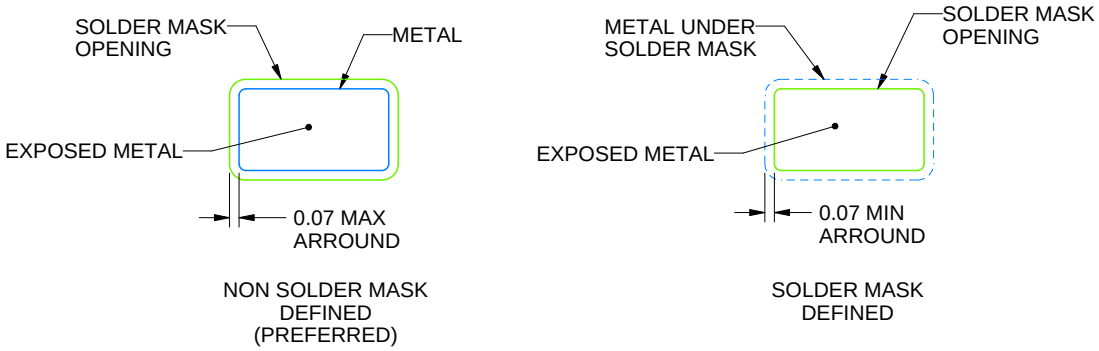
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

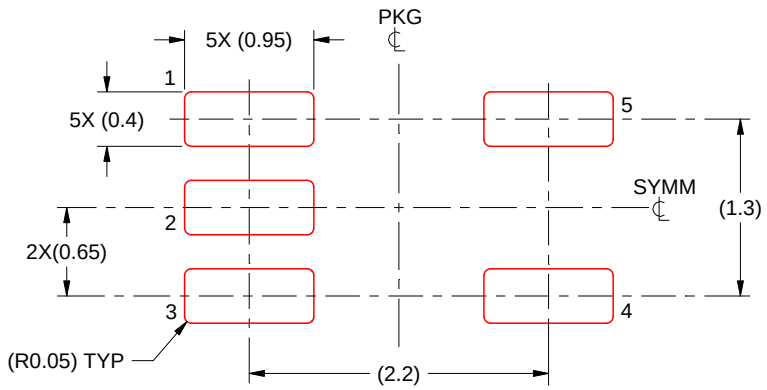


SOLDER MASK DETAILS

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NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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