

SN74AHC595-Q1 具有三态输出寄存器的汽车类 8 位移位寄存器

1 特性

- 符合汽车应用要求
- 工作范围为 2V 至 5.5V V_{CC}
- 8 位串行输入、并行输出移位寄存器
- 移位寄存器具有直接清除功能

2 应用

- 启用或禁用数字信号
- 控制指示灯 LED
- 通信模块和系统控制器之间的转换

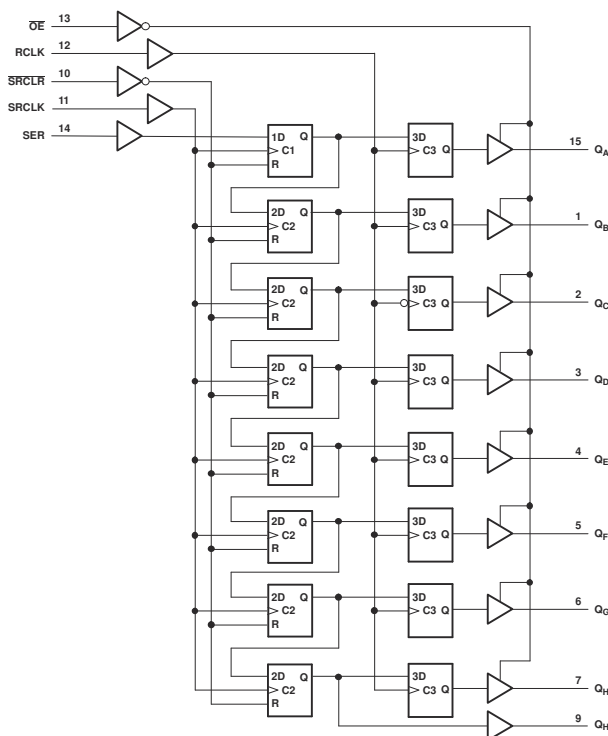
3 说明

SN74AHC595 包含一个可对 8 位 D 类存储寄存器进行馈送的 8 位串行输入、并行输出移位寄存器。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SN74AHC595-Q1	BQB (WQFN , 16)	3.5mm x 2.5mm	3.5mm x 2.5mm
	PW (TSSOP , 16)	5.00mm x 6.40mm	5.00mm x 4.4mm

- 如需了解更多信息，请参阅第 11 节。
- 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
- 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



逻辑图 (正逻辑)



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4 Pin Configuration and Functions

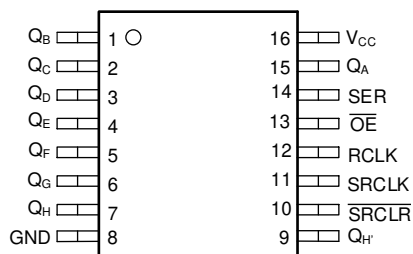


图 4-1. PW Package, 16-PIN TSSOP (Top View)

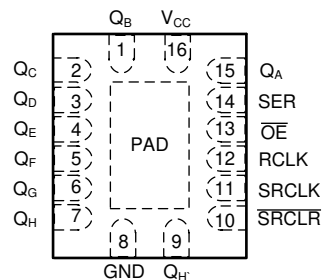


图 4-2. BQB Package, 16-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
Q _B	1	O	Q _B Output
Q _C	2	O	Q _C Output
Q _D	3	O	Q _D Output
Q _E	4	O	Q _E Output
Q _F	5	O	Q _F Output
Q _G	6	O	Q _G Output
Q _H	7	O	Q _H Output
GND	8	G	Ground Pin
Q _H '	9	O	Q _H ' Output
SRCLR	10	I	SRCLR Input
SRCLK	11	I	SRCLK Input
RCLK	12	I	RCLK Input
OE	13	I	Output Enable Pin. Active LOW
SER	14	I	SER Input
Q _A	15	O	Q _A Output
V _{CC}	16	P	Power Pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	- 0.5	7	V
V _I	Input voltage range ⁽²⁾	- 0.5	7	V
V _O	Output voltage range ⁽²⁾	- 0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current (V _I < 0)		- 20 mA	mA
I _{OK}	Output clamp current (V _O < 0 or V _O > V _{CC})		±20 mA	mA
I _O	Continuous output current (V _O = 0 to V _{CC})		±25 mA	mA
	Continuous current through V _{CC} or GND		±75 mA	mA
T _{stg}	Storage temperature range	- 65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 3 V	2.1		
		V _{CC} = 5.5 V	3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 3 V		0.9	
		V _{CC} = 5.5 V		1.65	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		- 50	μA
		V _{CC} = 3.3 V ± 0.3 V		- 4	mA
		V _{CC} = 5 V ± 0.5 V		- 8	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	μA
		V _{CC} = 3.3 V ± 0.3 V		4	mA
		V _{CC} = 5 V ± 0.5 V		8	
Δt / Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100	ns/V
		V _{CC} = 5 V ± 0.5 V		20	
T _A	Operating free-air temperature	I-suffix devices	- 40	85	°C
		Q-suffix devices	- 40	125	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾	BQB (WQFN)	PW (TSSOP)	UNIT
	16 PINS	16 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	91.8	135.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μA
I _{OZ}	Q _A - Q _H , V _I = V _{CC} or GND, V _O = V _{CC} or GND, $\overline{OE}$ = V _{IH} or V _{IL}	5.5 V			±0.25		±10	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	μA
C _i	V _I = V _{CC} or GND	5 V		3	10		10	pF
C _o	V _O = V _{CC} or GND	5 V		5.5				pF

5.5 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

V_{CC} = 3.3 V ± 0.3 V, over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

			T _A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t _w	Pulse duration	SRCLK high or low	5.5		6.5		ns
		RCLK high or low	5.5		6.5		
		SRCLR low	5		6		
t _{su}	Setup time	SER before SRCLK ↑	3.5		4.5		ns
		SRCLK ↑ before RCLK ↑ ⁽¹⁾	8		9.5		
		SRCLR low before RCLK ↑	8		10		
		SRCLR high (inactive) before SRCLK ↑	3		4		
t _h	Hold time	SER after SRCLK ↑	1.5		2.5		ns

- (1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.6 Timing Requirements, V_{CC} = 5 V ± 0.5 V

V_{CC} = 5 V ± 0.5 V, over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

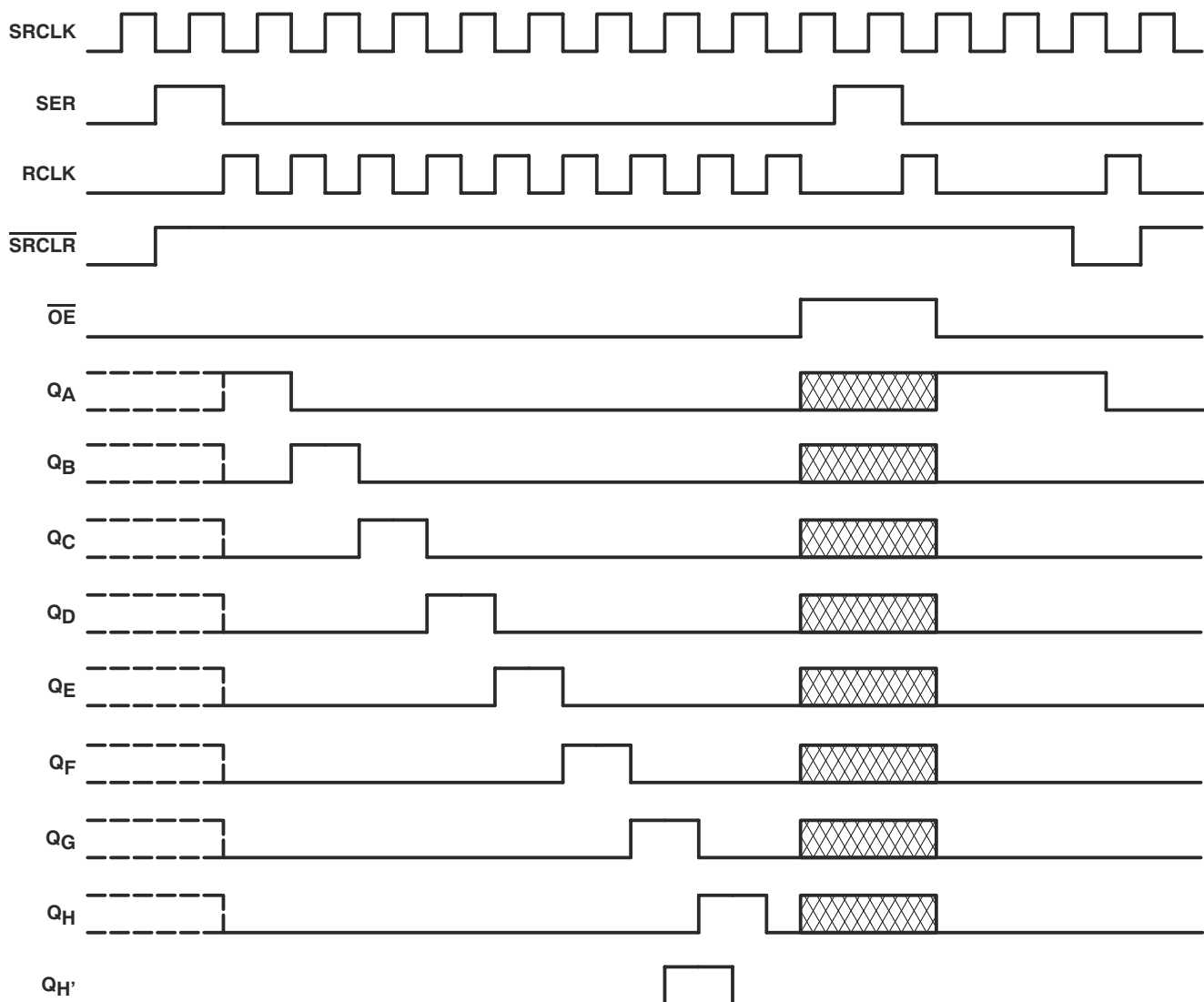
			T _A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t _w	Pulse duration	SRCLK high or low	5		6		ns
		RCLK high or low	5		6		
		SRCLR low	5.2		6.2		

$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
t_{su} Setup time	SER before SRCLK $\uparrow$	3		4		ns
	SRCLK $\uparrow$ before RCLK $\uparrow$ ⁽¹⁾	5		6		
	SRCLR low before RCLK $\uparrow$	5		6		
	SRCLR high (inactive) before SRCLK $\uparrow$	2.5		3.5		
t_h Hold time	SER after SRCLK $\uparrow$	2		3		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.7 Timing Diagrams



NOTE:  implies that the output is in 3-State mode.

5.8 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

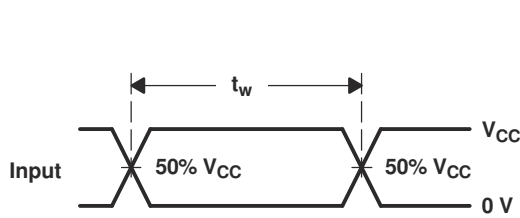
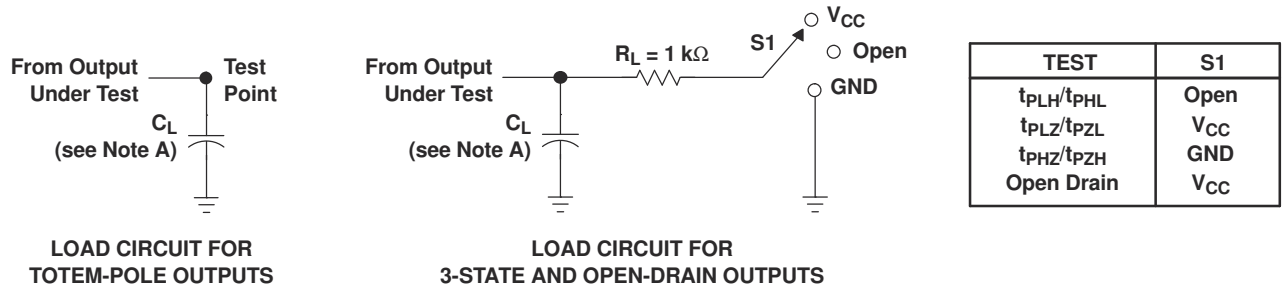
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{\max}$			$C_L = 50\text{ pF}$	55	105		40		MHz
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 50\text{ pF}$		7.9	15.4	1	20	ns
t_{PHL}					7.9	15.4	1	20	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$		9.2	16.5	1	21.5	ns
t_{PHL}					9.2	16.5	1	21.5	
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$		9	16.3	1	20.2	ns
t_{PZH}	$\overline{\text{OE}}$	$Q_A - Q_H$	$C_L = 50\text{ pF}$		7.8	15	1	20	ns
t_{PZL}					9.6	15	1	20	
t_{PHZ}	$\overline{\text{OE}}$	$Q_A - Q_H$	$C_L = 50\text{ pF}$		8.1	15.7	1	19.2	ns
t_{PLZ}					9.3	15.7	1	19.2	

5.9 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

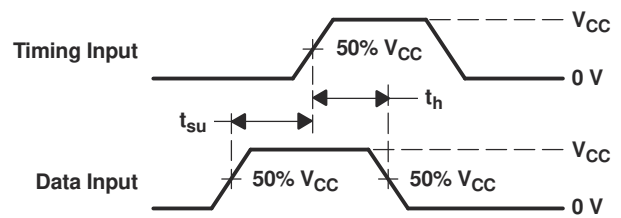
$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{\max}$			$C_L = 50\text{ pF}$	95	140		75		MHz
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 50\text{ pF}$		5.6	9.4	1	13.5	ns
t_{PHL}					5.6	9.4	1	13.5	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$		6.4	10.2	1	14.4	ns
t_{PHL}					6.4	10.2	1	14.4	
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$		6.4	10	1	14.1	ns
t_{PZH}	$\overline{\text{OE}}$	$Q_A - Q_H$	$C_L = 50\text{ pF}$		5.7	10.6	1	15	ns
t_{PZL}					6.8	10.6	1	15	
t_{PHZ}	$\overline{\text{OE}}$	$Q_A - Q_H$	$C_L = 50\text{ pF}$		3.5	10.3	1	14	ns
t_{PLZ}					3.4	10.3	1	14	

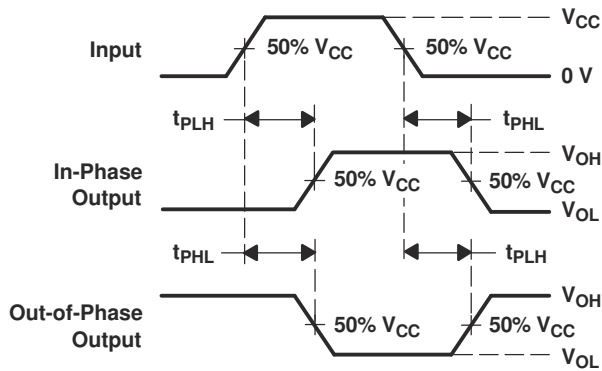
6 Parameter Measurement Information



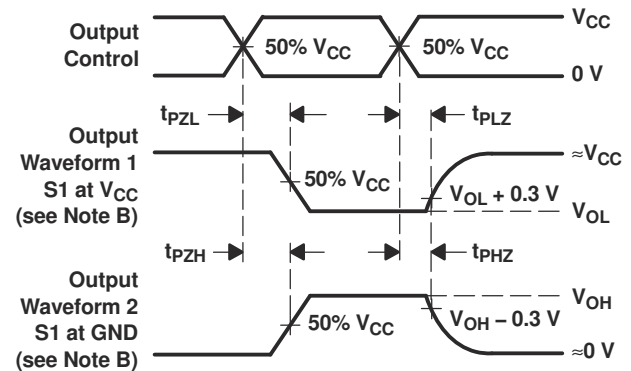
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
D. The outputs are measured one at a time, with one input transition per measurement.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AHC595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers.

The shift register has a direct overriding clear ($\overline{\text{SRCLR}}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{\text{OE}}$) input is high, all outputs, except QH' , are in the high-impedance state.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

7.2 Functional Block Diagram

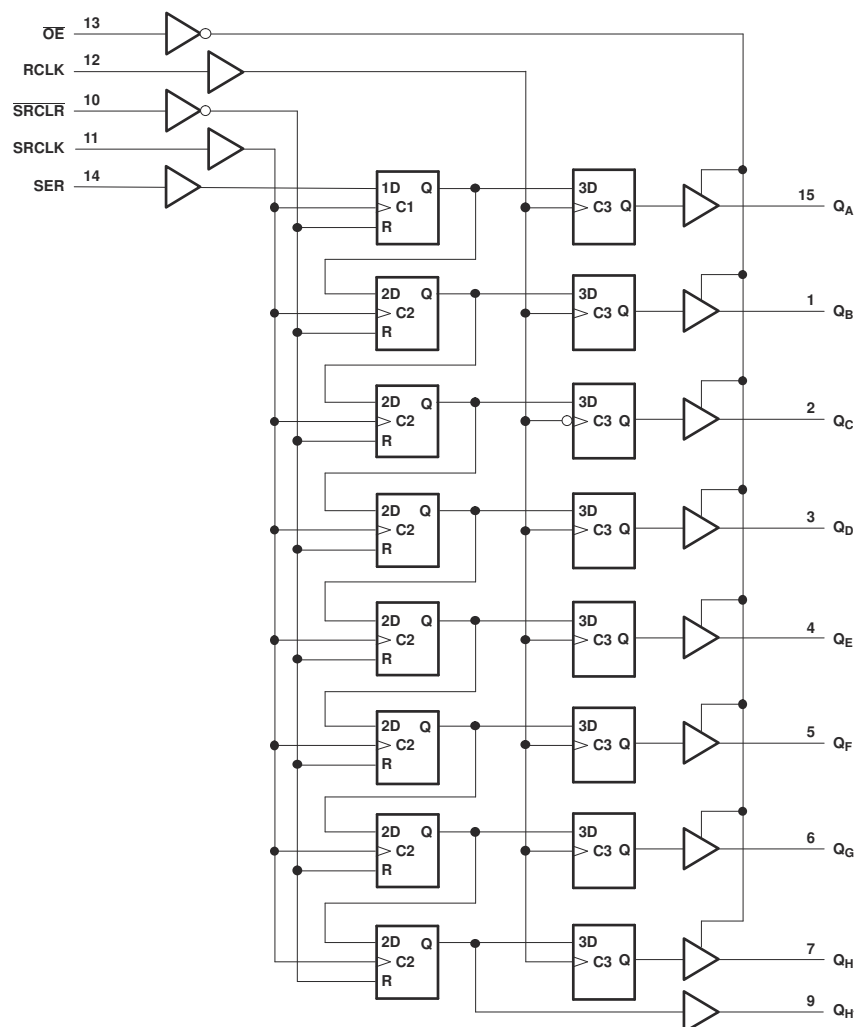


图 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	OE	
X	X	X	X	H	Outputs Q _A - Q _H are disabled.
X	X	X	X	L	Outputs Q _A - Q _H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored into the storage register.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.2.2 Layout Example

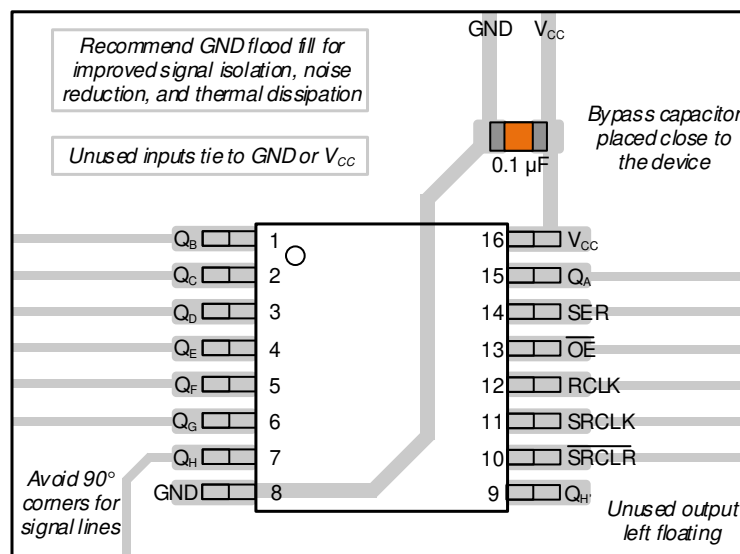


图 8-1. Example Layout for the SN74AHC595-Q1

9 Device and Documentation Support

9.1 Document Support (Analog)

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC595-Q1	Click here	Click here	Click here	Click here	Click here

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (March 2024) to Revision E (April 2024)	Page
• Updated thermal values for PW package from $R_{\theta JA} = 108$ to 135.9, all values in $^{\circ}\text{C}/\text{W}$	5

Changes from Revision C (November 2023) to Revision D (March 2024)	Page
• 向封装信息表、引脚配置和功能部分和热性能信息表中添加了 BQB 封装.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC595QPWRQ1	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595Q
SN74AHC595QPWRQ1.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595Q
SN74AHC595QWBQBRQ1	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH595Q
SN74AHC595QWBQBRQ1.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH595Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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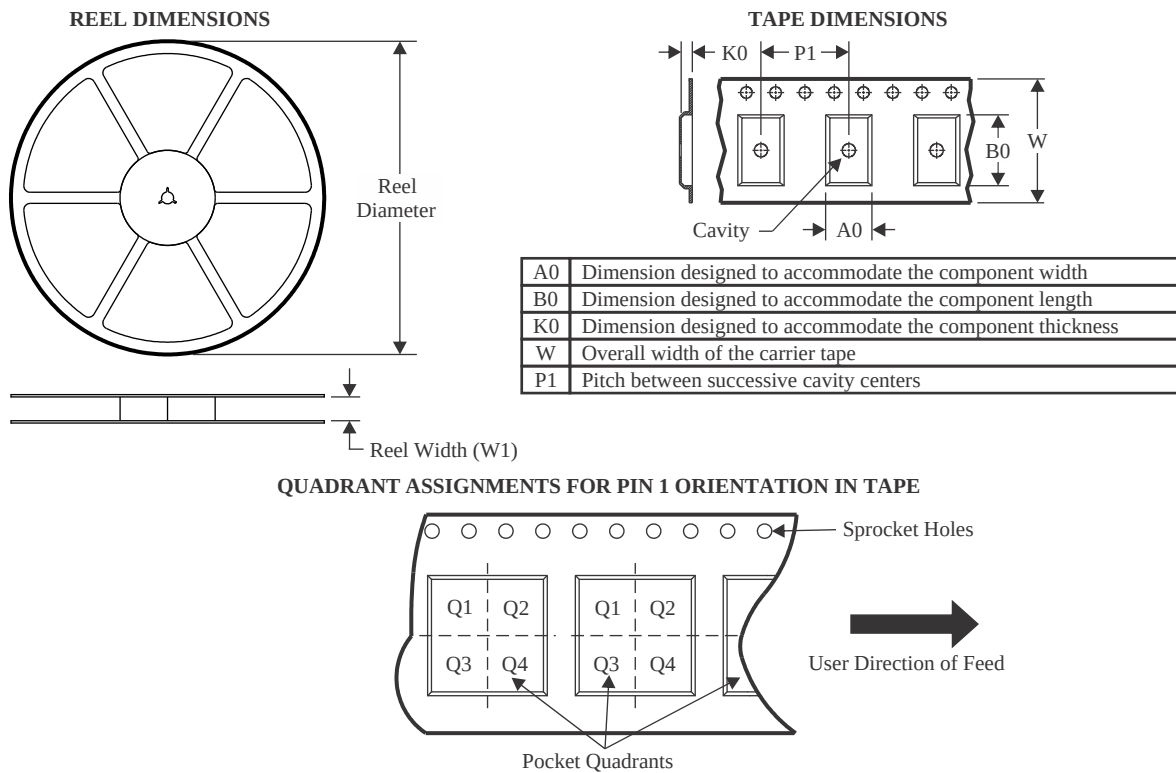
OTHER QUALIFIED VERSIONS OF SN74AHC595-Q1 :

- Catalog : [SN74AHC595](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

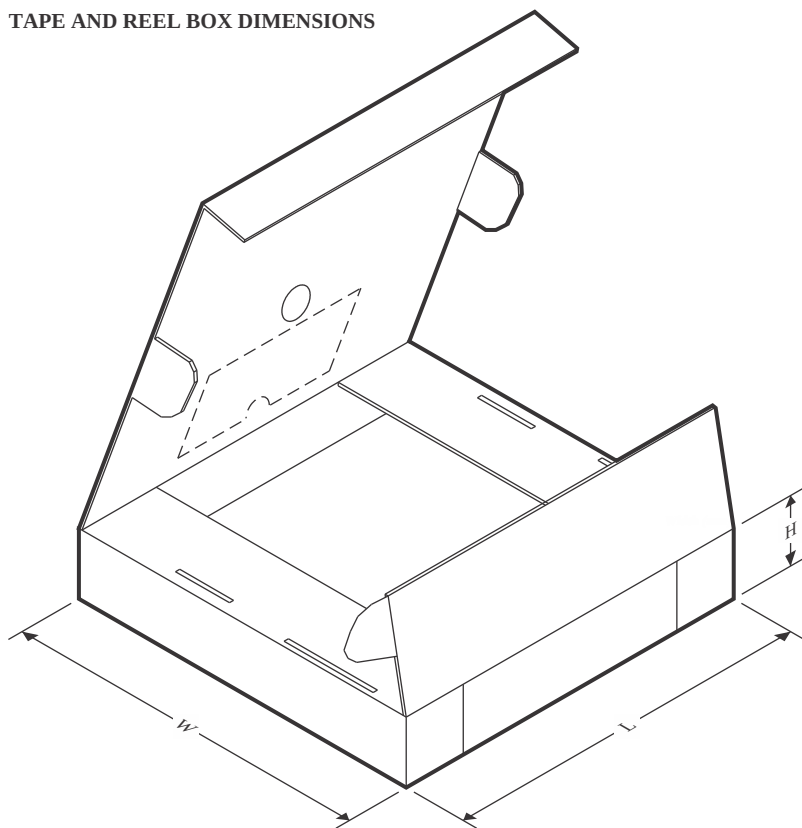
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC595QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC595QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC595QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHC595QWBQRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

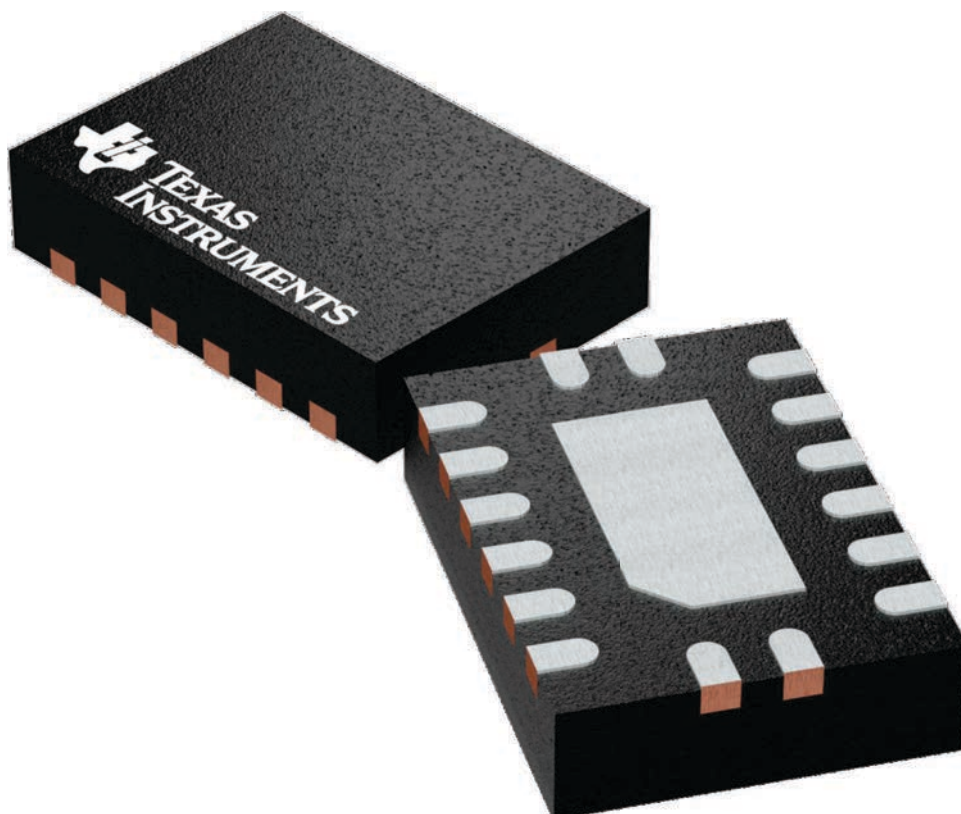
BQB 16

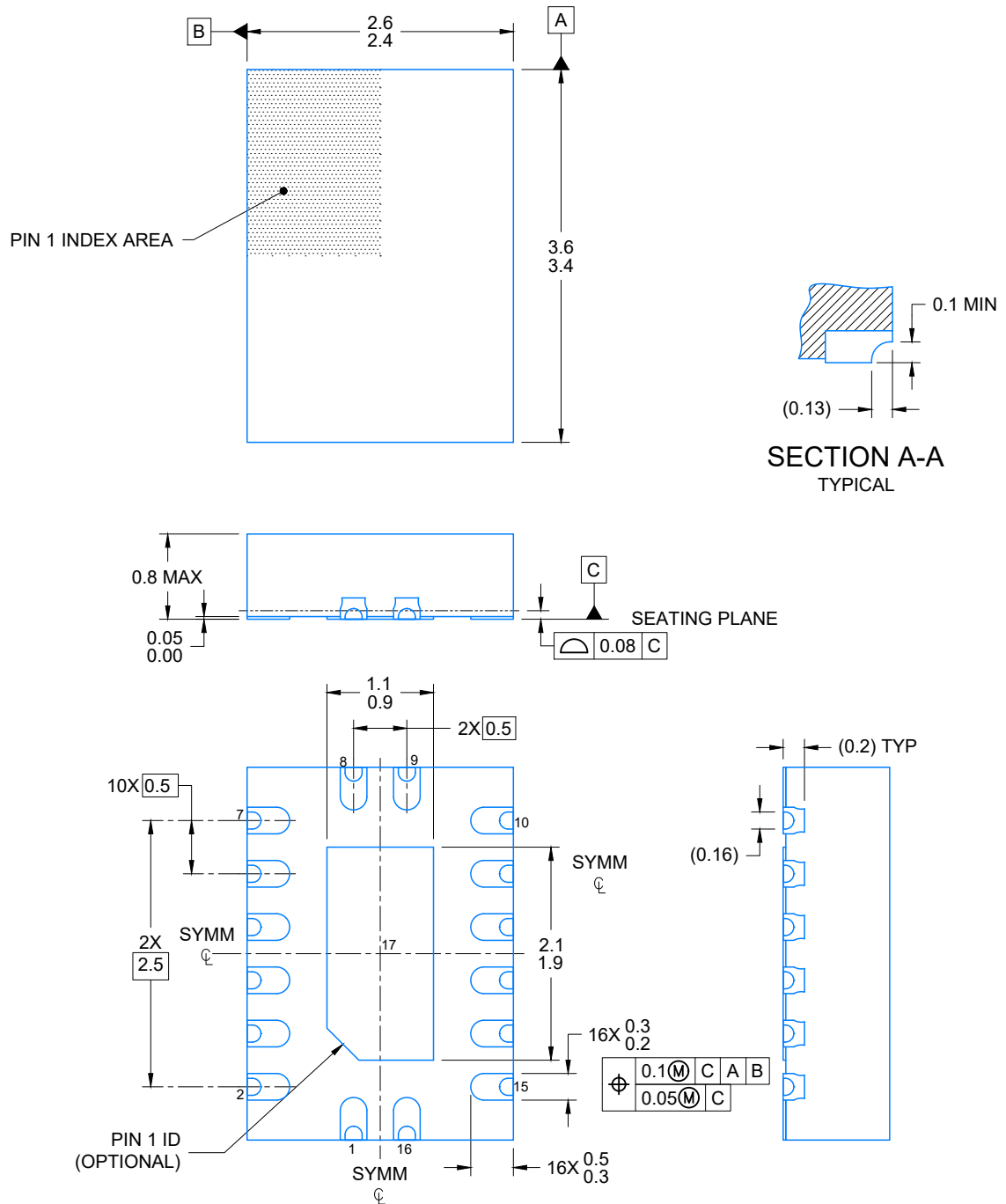
WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

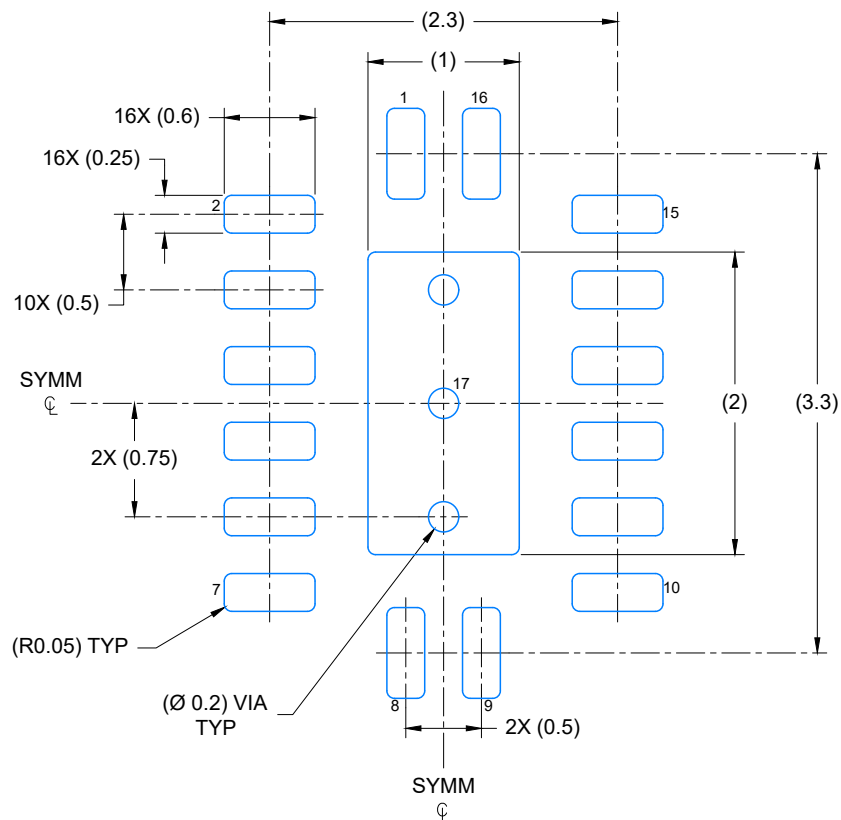




4226135/A 08/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

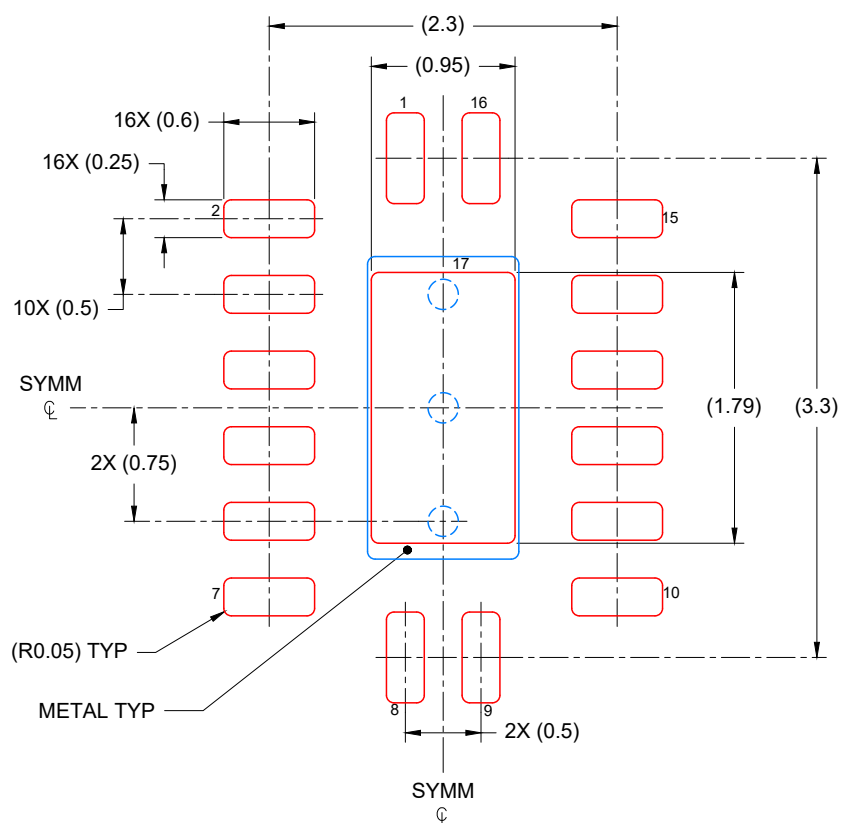


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



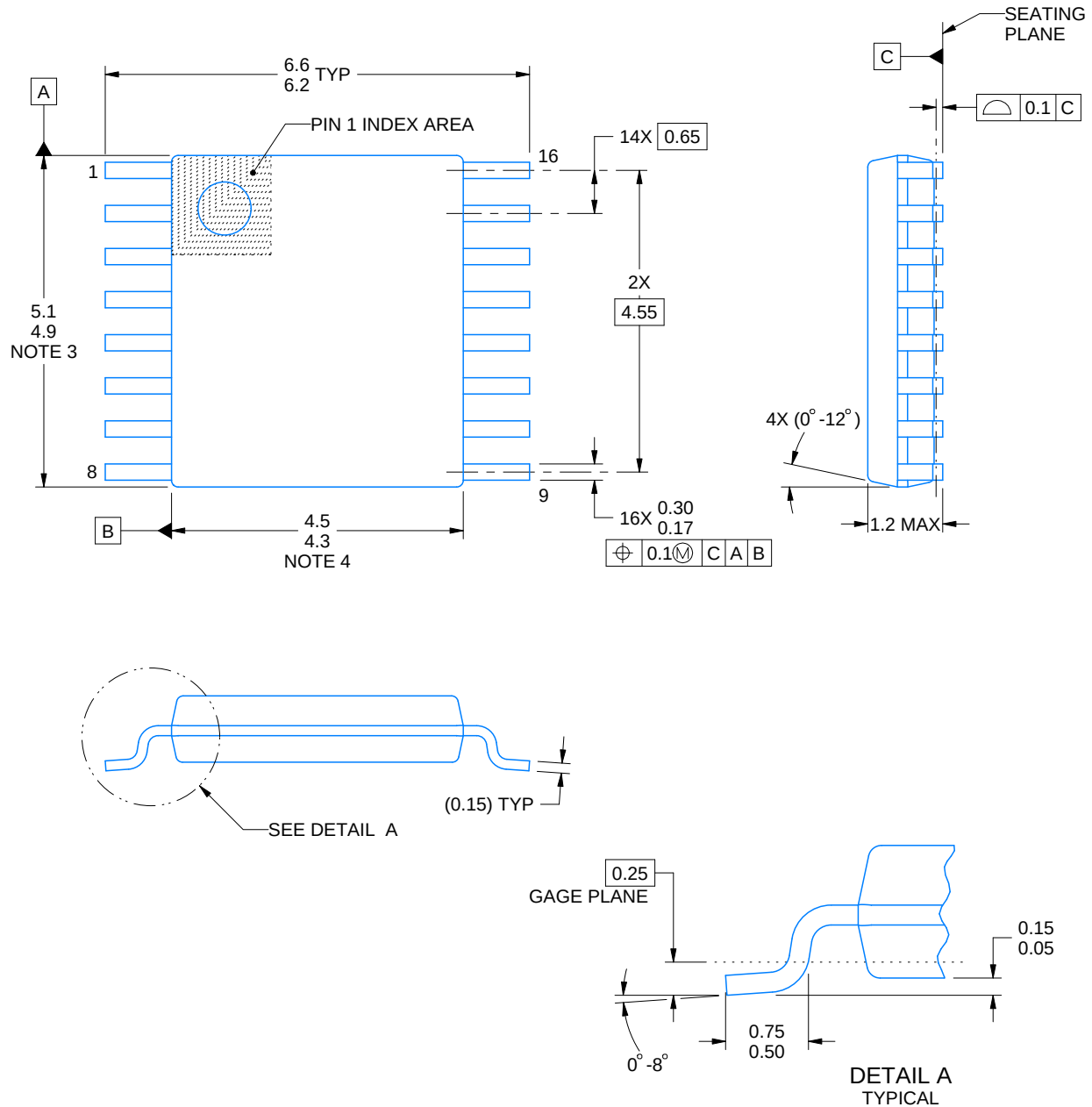
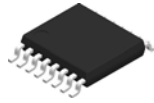
SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220204/B 12/2023

NOTES:

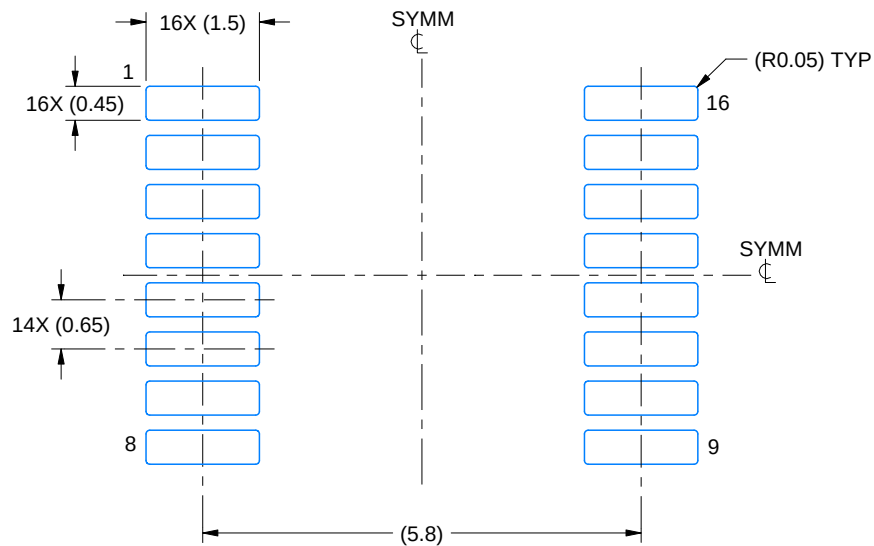
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

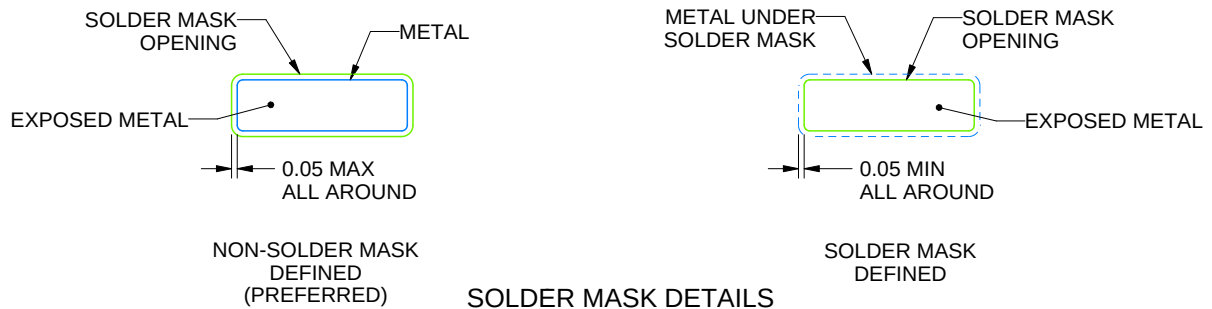
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

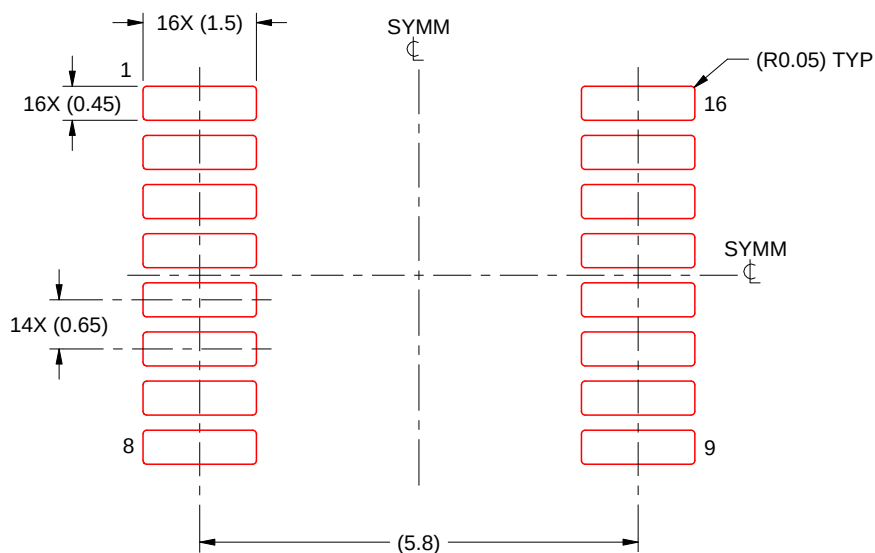
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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