SN74AHC32Q-Q1 汽车级四通道 2 输入正或门

1 特性

- 符合汽车应用要求
- 工作范围为 2V 至 5.5V V_{CC}
- 低功耗，I_{CC} 最大值为 10μA
- 5V 时，输出驱动为 ±8mA
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 启用或禁用数字信号
- 控制指示灯 LED
- 通信模块和系统控制器之间的转换

3 说明

SN74AHC32Q-Q1 器件是四路双输入正或门。这些器件执行布尔函数 $Y = \overline{A \times B}$ 或 Y = A + B。

封装信息

器件型号	封装(1)	封装尺寸(2)	封装尺寸(3)
SN74AHC32Q-Q1	BQA（WQFN，14）	3mm × 2.5mm	3mm × 2.5mm
	PW（TSSOP，14）	5mm × 6.4mm	5mm × 4.4mm
	D（SOIC，14）	8.7mm × 6mm	8.7mm × 3.9mm

(1) 更多相关信息，请参阅第 11 节。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 封装尺寸（长 × 宽）为标称值，不包括引脚。

逻辑图（正逻辑）

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Pin Configuration and Functions 3
5 Specifications 4
5.1 Absolute Maximum Ratings 4
5.2 ESD Ratings 4
5.3 Recommended Operating Conditions 5
5.4 Thermal Information 5
5.5 Electrical Characteristics 6
5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V 6
5.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V 6
5.8 Noise Characteristics 7
5.9 Operating Characteristics 7
6 Parameter Measurement Information 8
7 Detailed Description 9
7.1 Overview 9
7.2 Functional Block Diagram 9
7.3 Feature Description 9
7.3.1 Standard CMOS Inputs 9
7.3.2 Balanced CMOS Push-Pull Outputs 9
7.3.3 Clamp Diode Structure 9
7.4 Device Functional Modes 10
8 Application and Implementation 11
8.1 Application Information 11
8.2 Typical Application 11
8.2.1 Design Requirements 11
8.2.2 Detailed Design Procedure 13
8.2.3 Application Curves 13
8.3 Power Supply Recommendations 13
8.4 Layout 13
8.4.1 Layout Guidelines 13
8.4.2 Layout Example 14
9 Device and Documentation Support 15
9.1 Documentation Support (Analog) 15
9.1.1 Related Links 15
9.2 接收文档更新通知 15
9.3 支持资源 15
9.4 Trademarks 15
9.5 静电放电警告 15
9.6 术语表 15
10 Revision History 15
11 Mechanical, Packaging, and Orderable Information 16

Copyright © 2024 Texas Instruments Incorporated

4 Pin Configuration and Functions

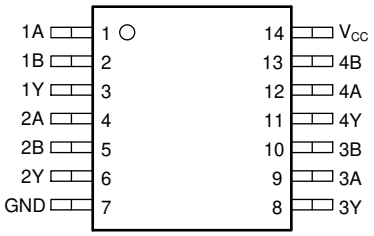


图 4-1. SN74AHC32 D or PW Package, 14-Pin (Top View)

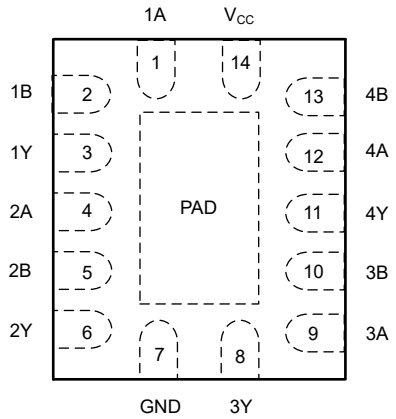


图 4-2. SN74AHC32 BQA Package, 14-Pin (Top View)

表 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	PIN No.		
1A	1	I	1A Input
1B	2	I	1B Input
1Y	3	O	1Y Output
2A	4	I	2A Input
2B	5	I	2B Input
2Y	6	O	2Y Output
3A	9	I	3A Input
3B	10	I	3B Input
3Y	8	O	3Y Output
4A	12	I	4A Input
4B	13	I	4B Input
4Y	11	O	4Y Output
GND	7	—	Ground Pin
V_{CC}	14	—	Power Pin
Thermal Pad[(2)]	–	–	Thermal Pad

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.
(2) BQA Package Only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		– 0.5	7	V
V_I [2]	Input voltage		– 0.5	7	V
V_O [2]	Output voltage		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0)		-20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Copyright © 2024 Texas Instruments Incorporated

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage[1]	V_{CC}= 2 V	1.5		V
		V_{CC}= 3V	2.1		
		V_{CC}= 5.5 V	3.85		
V_{IL}	Low-level Input voltage[1]	V_{CC}= 2 V		0.5	V
		V_{CC}= 3 V		0.9	
		V_{CC}= 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC}= 2 V		– 50	µA
		V_{CC}= 3.3 V ± 0.3 V		– 4	mA
		V_{CC}= 5 V ± 0.5 V		– 8	
I_{OL}	Low-level output current	V_{CC}= 2 V		50	µA
		V_{CC}= 3.3 V ± 0.3 V		4	mA
		V_{CC}= 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input Transition rise or fall rate	V_{CC}= 3.3 V ± 0.3 V		100	ns/V
		V_{CC}= 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		– 40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC[1]		SN74AHC32Q-Q1			UNIT
		D	PW	BQA	
		14	14	14	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.6	147.7	88.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C					NIT
			MIN	TYP	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 µA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OH} = 4 mA	3 V			0.36		0.5	
	I_{OH} = 8 mA	4.5 V			0.36		0.5	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	µA
C_i	V_I = V_{CC} or GND	5 V		2	10			pF

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		T_A = –40°C TO 125°C		UNIT
				TYP	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF	5.5	7.9	1	9.5	ns
t_{PHL}				5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF	8	11.4	1	13	ns
t_{PHL}				8	11.4	1	13	

5.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range(unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		T_A = –40°C TO 125°C		UNIT
				TYP	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF	3.8	5.5	1	6.5	ns
t_{PHL}				3.8	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF	5.3	7.5	1	8.5	ns
t_{PHL}				5.3	7.5	1	8.5	

Copyright © 2024 Texas Instruments Incorporated

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C[1]

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

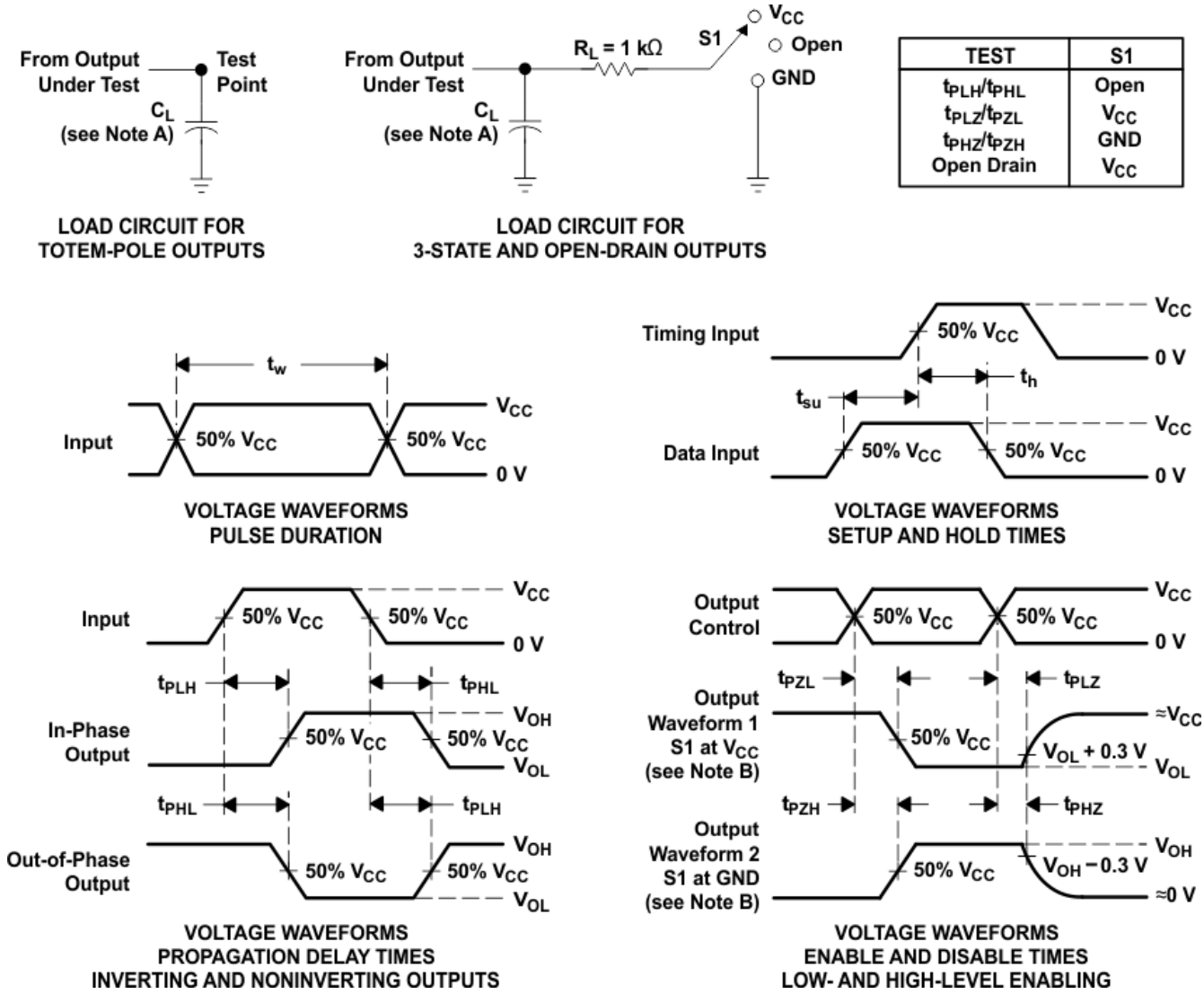
(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

6 Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω, t_r ⩽ 3 ns, t_f ⩽ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

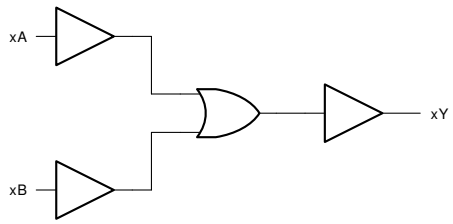
Copyright © 2024 Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The SN74AHC32Q-Q1 contains four independent 2-input OR Gates. Each gate performs the Boolean function Y = A + B in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10-kΩ resistor, however, is recommended and will typically meet all requirements.

7.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

7.3.3 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in 图 7-1.

> 小心
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

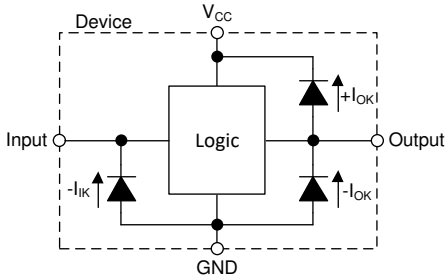


图 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

表 7-1 lists the functional modes of the SN74AHC32Q-Q1.

表 7-1. Function Table

INPUTS[(1)]		OUTPUT Y
A	B	
H	H	H
L	H	H
H	L	H
L	L	L

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

Copyright © 2024 Texas Instruments Incorporated

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, three 2-input OR gates are combined to produce a 4-input OR gate function as shown in 图 8-1. The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SN74AHC32Q-Q1 is used to directly control the Enable pin of a fan driver. The fan driver requires only one input signal to be HIGH before being enabled, and should be disabled in the event that all signals go LOW. The 4-input OR gate function combines the four individual overheat signals into a single active-high enable signal.

Temperature sensors can often be spread throughout a system rather than being in a centralized location. This would mean longer length traces or wires to pass signals through leading to slower edge transitions. This makes the SN74AHC32Q-Q1 useful for combining the incoming signals.

8.2 Typical Application

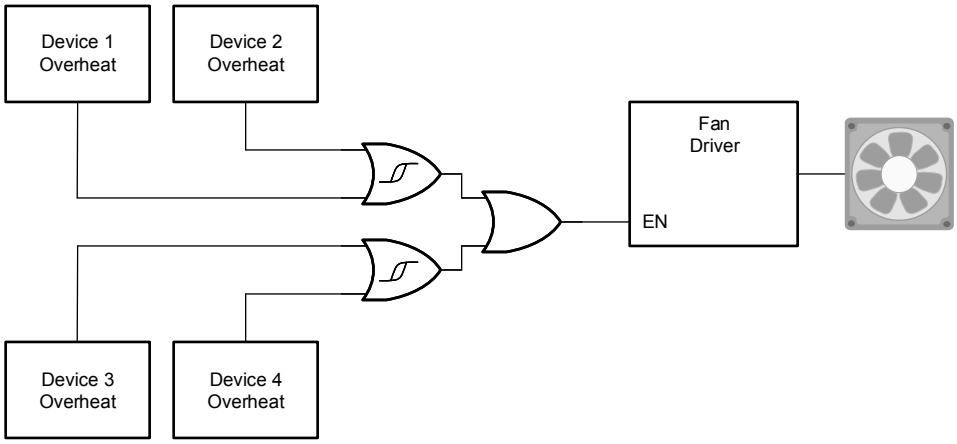


图 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHC32Q-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHC32Q-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74AHC32Q-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74AHC32Q-Q1 can drive a load with total resistance described by $R_L \geqslant V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

> 小心
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHC32Q-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74AHC32Q-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

Copyright © 2024 Texas Instruments Incorporated

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHC32Q-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Application Curves

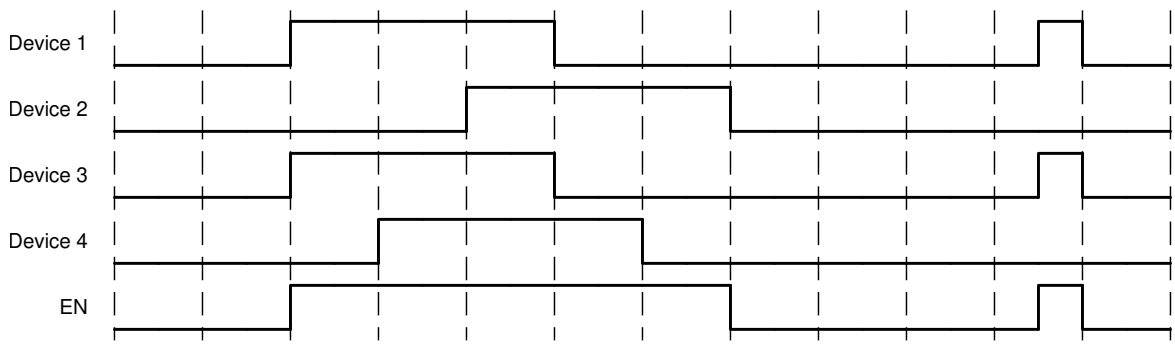


图 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Layout Example*.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

Copyright © 2024 Texas Instruments Incorporated

8.4.2 Layout Example

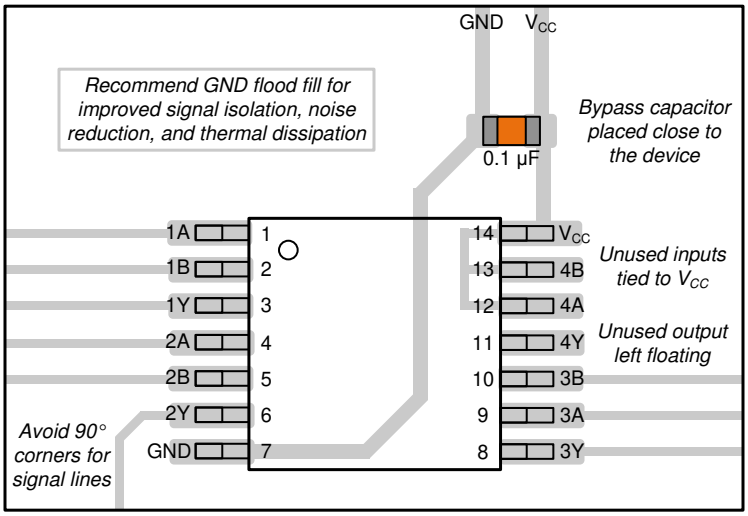


图 8-3. Example Layout for the SN74AHC32Q-Q1

Copyright © 2024 Texas Instruments Incorporated

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support (Analog)

9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC32Q-Q1	Click here	Click here	Click here	Click here	Click here

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (October 2023) to Revision D (February 2024) — **Page**

- Updated R θ JA values: D = 86 to 124.6, all values in °C/W 5

Changes from Revision B (June 2023) to Revision C (October 2023) — **Page**

- Updated R θ JA values: PW = 113 to 147.7, all values in °C/W 5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2024 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC32QDRG4Q1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC32Q
SN74AHC32QDRG4Q1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC32Q
SN74AHC32QDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC32Q
SN74AHC32QDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC32Q
SN74AHC32QPWRG4Q1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA32Q
SN74AHC32QPWRG4Q1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA32Q
SN74AHC32QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HA32Q
SN74AHC32QPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA32Q
SN74AHC32QWBQARQ1	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC32Q
SN74AHC32QWBQARQ1.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC32Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

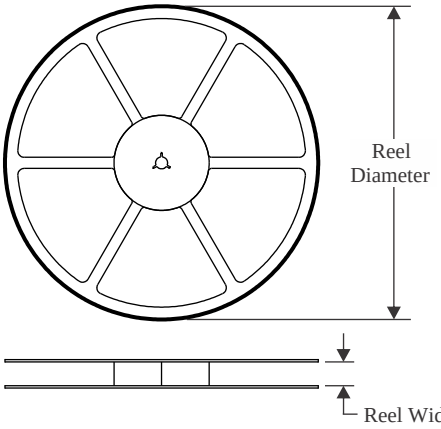
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

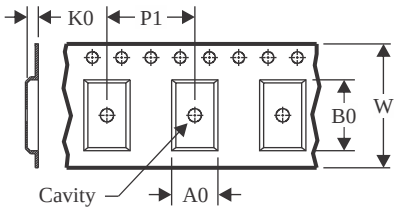
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

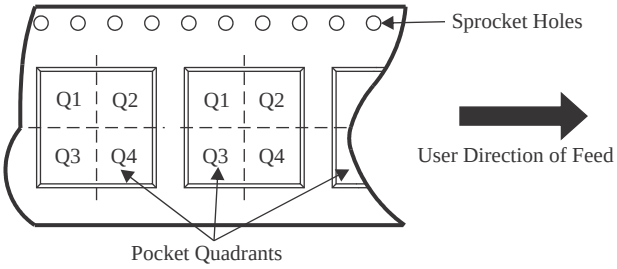


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

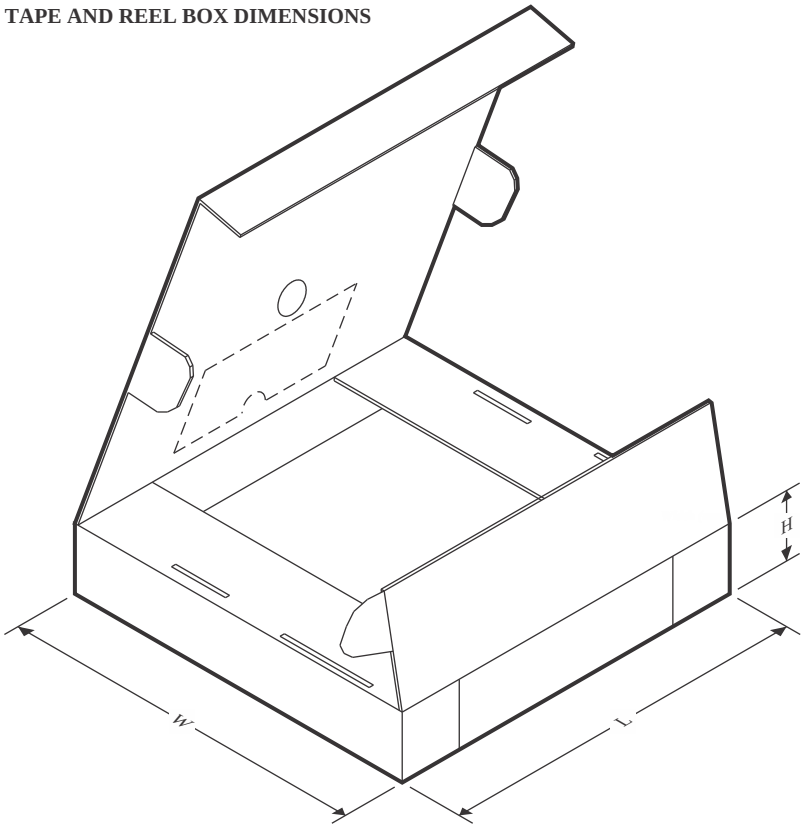
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

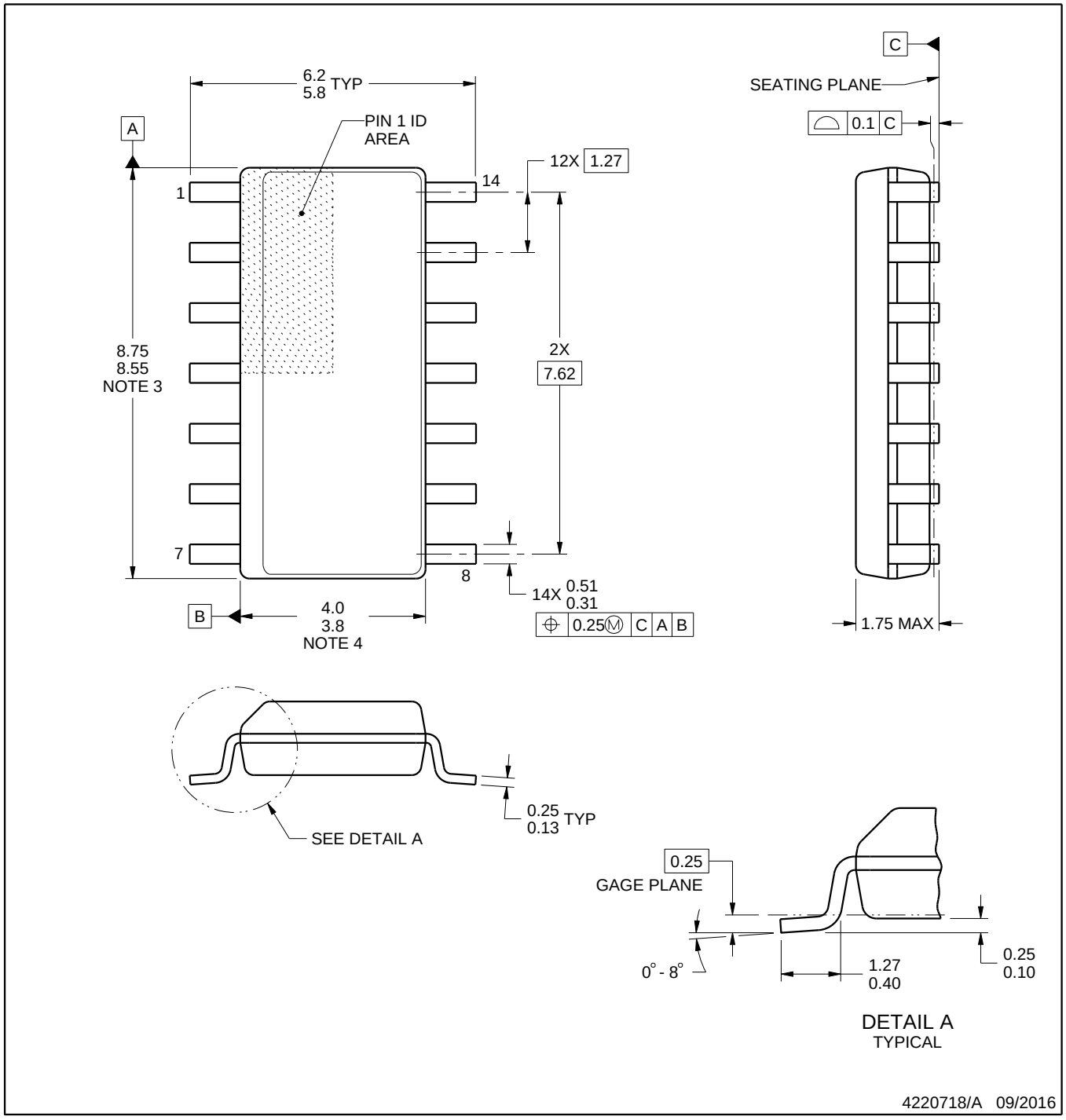
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC32QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC32QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC32QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC32QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC32QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC32QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



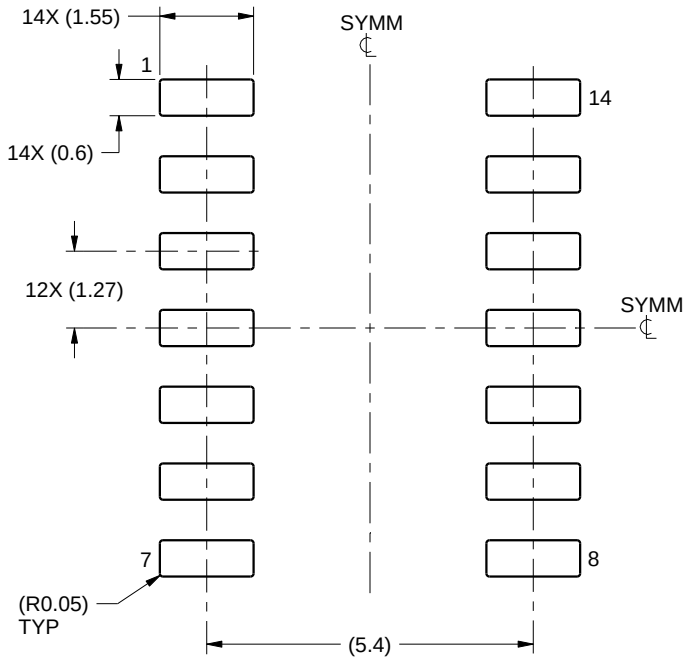
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC32QDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC32QPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC32QPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC32QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC32QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC32QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

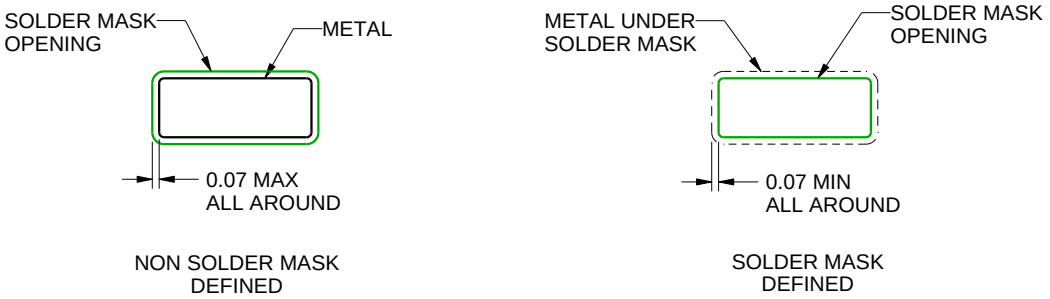


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

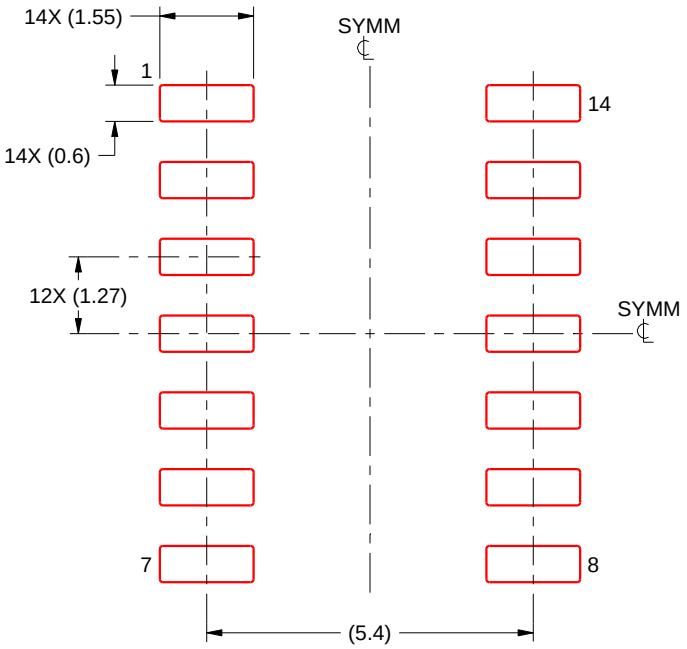


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

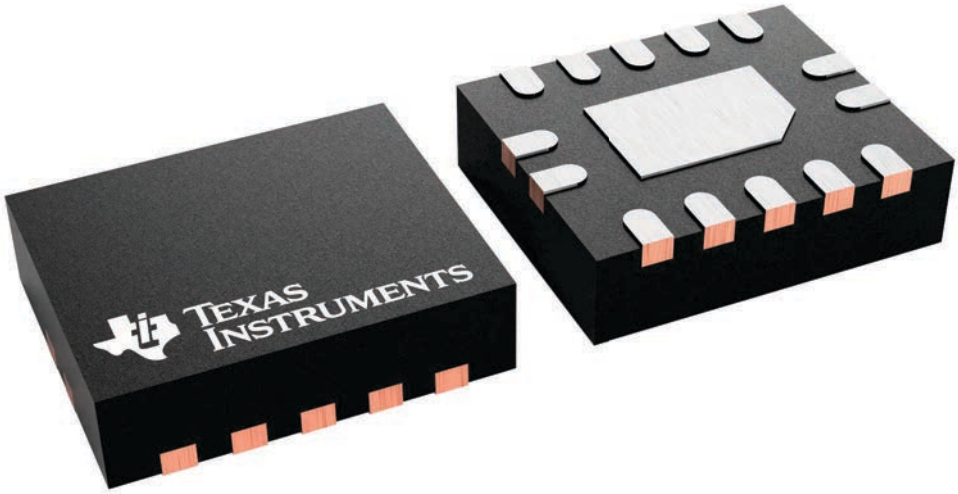
BQA 14

WQFN - 0.8 mm max height

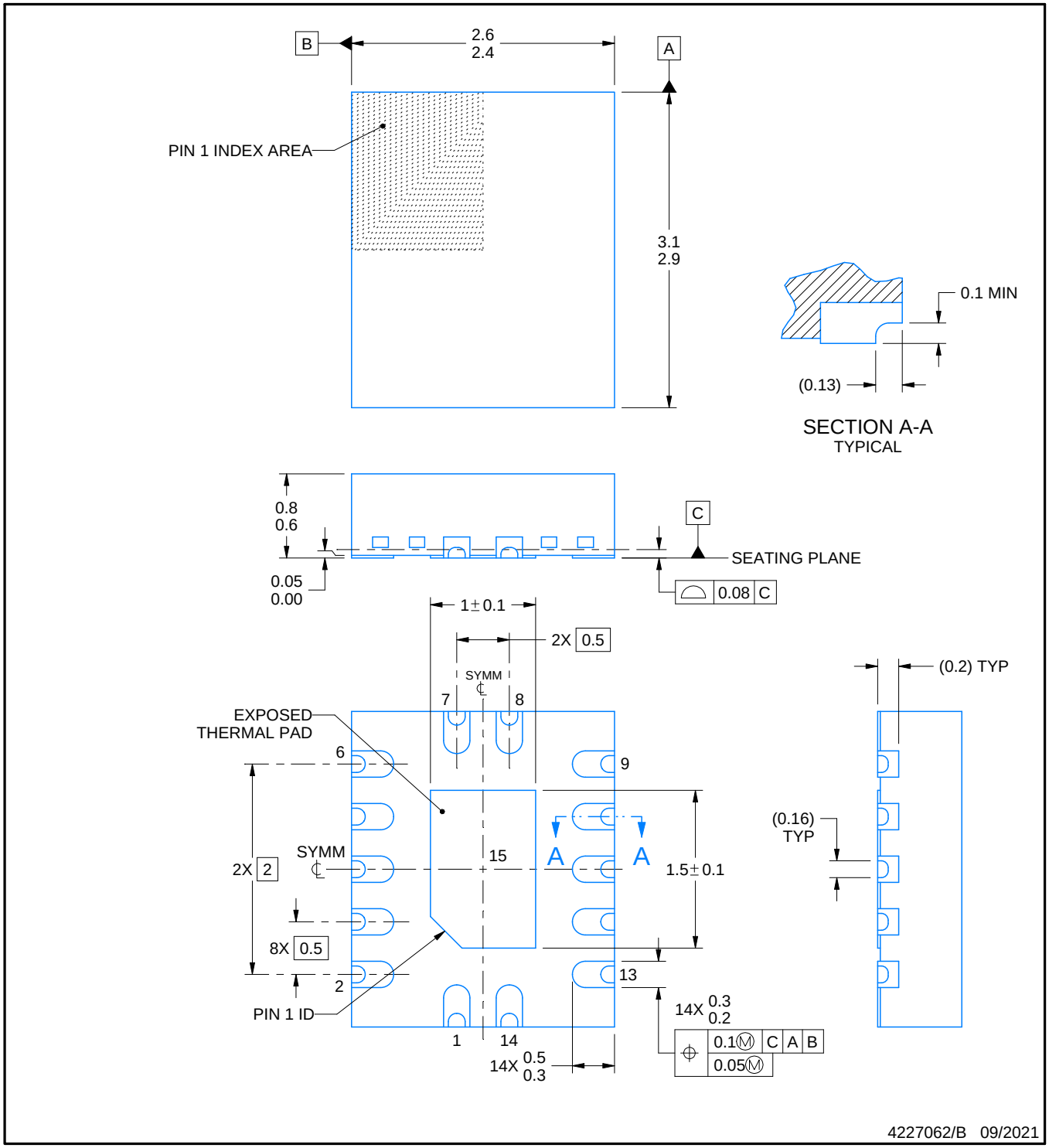
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

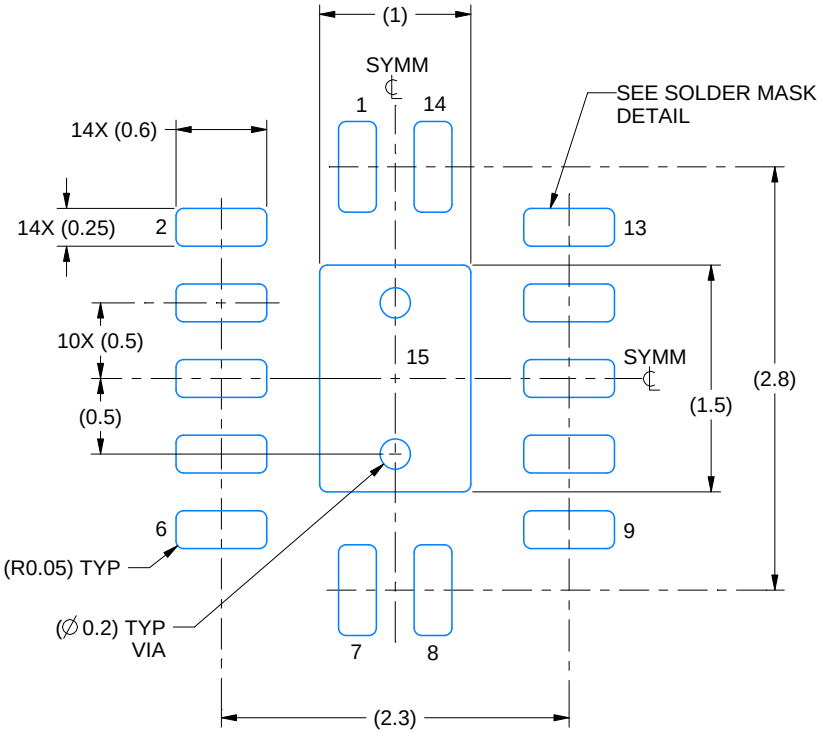


4227145/A

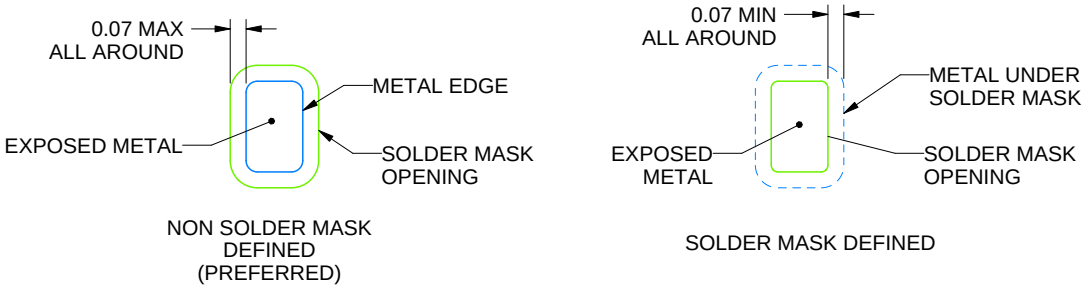


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

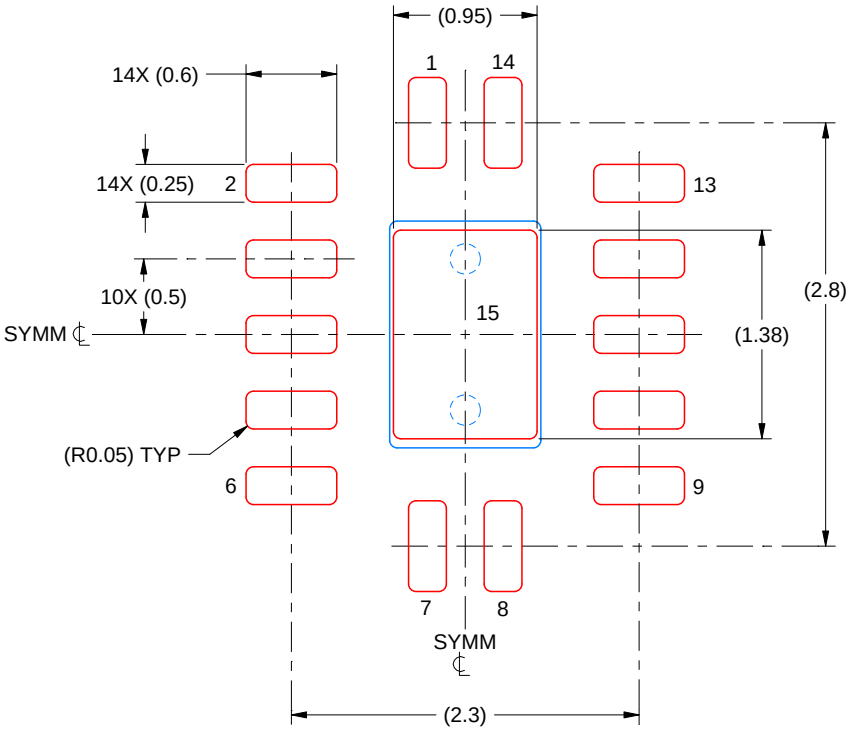


SOLDER MASK DETAILS

4227062/B 09/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

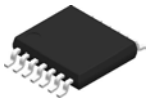
EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

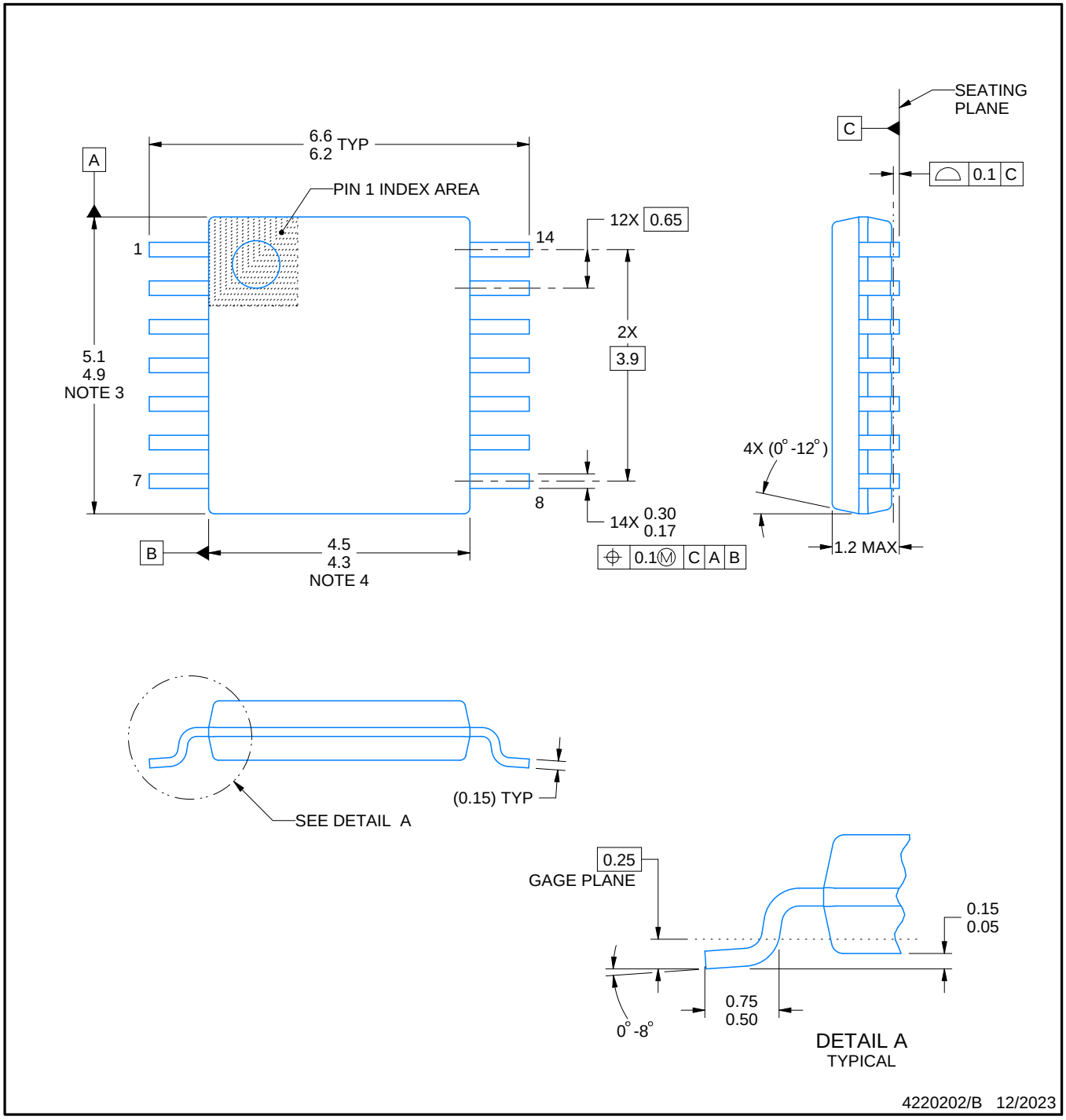
PW0014A



PACKAGE OUTLINE

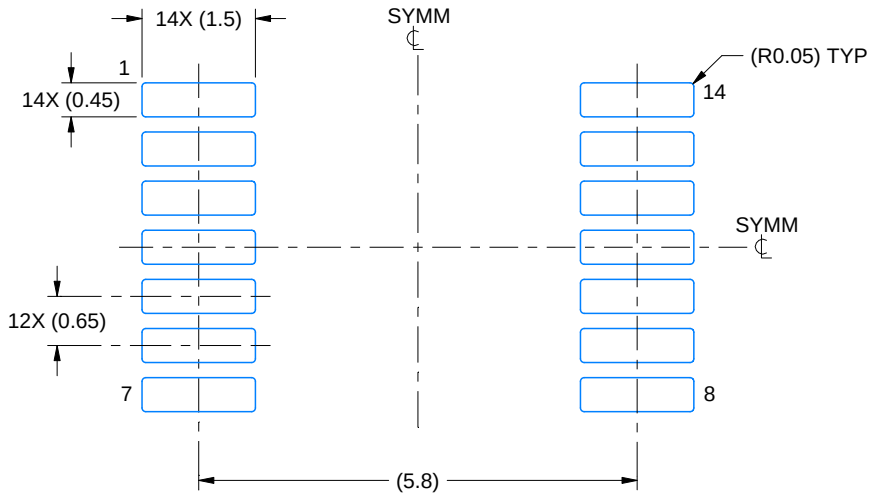
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

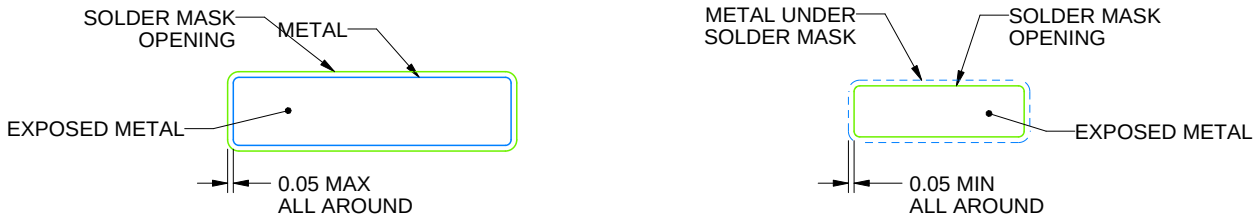


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

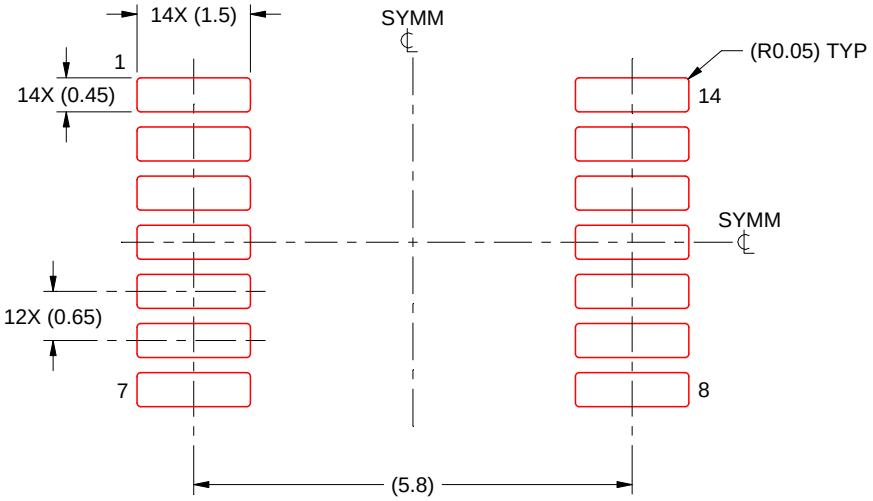
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月