

SNx4AHC240 具有三态输出的八通道缓冲器/驱动器

1 特性

- 低延迟, 4.3ns 典型值 (25°C , 5V)
- 闩锁性能超过 250mA , 符合 JESD 17 规范

2 应用

- 手持终端: 智能手机
- 网络交换机
- 健康与健身设备以及可穿戴设备

3 说明

这些八通道缓冲器/驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发送器的性能和密度。

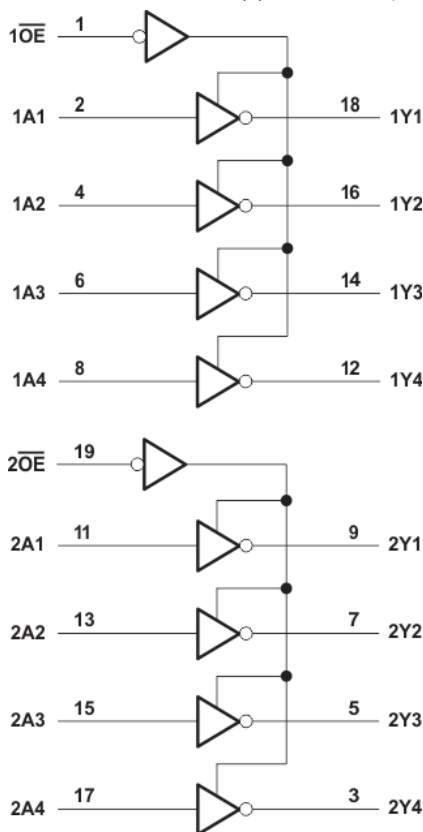
器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SN54AHC240	J (CDIP , 20)	24.2mm x 7.62mm	24.2mm x 6.92mm
	W (CFP , 20)	13.09mm x 8.13mm	13.09mm x 6.92mm
	FK (LCCC , 20)	8.89mm x 8.89mm	8.89mm x 8.89mm
SN74AHC240	N (PDIP , 20)	24.33mm x 9.4mm	25.40mm x 6.35mm
	DW (SOIC , 20)	12.80mm x 10.3mm	12.8mm x 7.5mm
	NS (SOP , 20)	12.60mm x 7.8mm	12.6mm x 5.30mm
	PW (TSSOP , 20)	6.50mm x 6.4mm	6.50mm x 4.40mm

(1) 有关更多信息, 请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用) 。

(3) 本体尺寸 (长 × 宽) 为标称值, 不包括引脚。



逻辑图 (正逻辑)



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4 引脚配置和功能

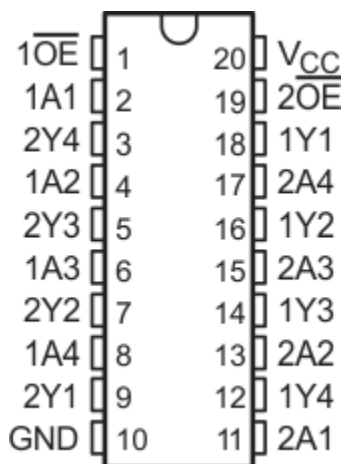


图 4-1. SN74AHC240-Q1 PW 封装 (顶视图)

引脚		类型 ⁽¹⁾	说明
名称	编号		
1OE	1	O	输出使能 1
1A1	2	I	1A1 输入
2Y4	3	O	2Y4 输出
1A2	4	I	1A2 输入
2Y3	5	O	2Y3 输出
1A3	6	I	1A3 输入
2Y2	7	O	2Y2 输出
1A4	8	I	1A4 输入
2Y1	9	O	2Y1 输出
GND	10	G	接地引脚
2A1	11	I	2A1 输入
1Y4	12	O	1Y4 输出
2A2	13	I	2A2 输入
1Y3	14	O	1Y3 输出
2A3	15	I	2A3 输入
1Y2	16	O	1Y2 输出
2A4	17	I	2A4 输入
1Y1	18	O	1Y1 输出
2OE	19	O	输出使能 2
VCC	20	P	电源引脚

(1) 信号类型：I = 输入，O = 输出，I/O = 输入或输出

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）⁽¹⁾

		最小值	最大值	单位
V_{CC}	电源电压范围	-0.5	7	V
V_I	输入电压范围 ⁽²⁾	-0.5	7	V
V_O	在高阻抗或断电状态对任一输出施加的电压范围 ⁽²⁾	-0.5	7	V
V_O	输出电压范围 ⁽²⁾	-0.5	$V_{CC}+0.5$	V
I_{IK}	输入钳位电流	$V_I < -0.5V$	-20	mA
I_{OK}	输出钳位电流	$V_O < -0.5V$ 或 $V_O > V_{CC} + 0.5V$	± 20	mA
I_O	持续输出电流	$V_O = 0$ 至 V_{CC}	± 25	mA
	通过 V_{CC} 或 GND 的持续输出电流		± 75	mA
T_{stg}	贮存温度	-65	150	°C

(1) 超出绝对最大额定值运行可能会对器件造成永久损坏。绝对最大额定值并不表示器件在这些条件下或在建议运行条件以外的任何其他条件下能够正常运行。如果在建议运行条件之外但在绝对最大额定值范围内短暂运行，器件可能不会受到损坏，但可能无法完全正常工作。以这种方式运行器件可能会影响器件的可靠性、功能和性能，并缩短器件寿命。

(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

5.2 ESD 等级

		值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准 ⁽¹⁾	± 2000 V

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）

规格	说明	条件	最小值	最大值	单位
V_{CC}	电源电压		2	5.5	V
V_{IH}	高电平输入电压	$V_{CC} = 2V$	1.5		V
		$V_{CC} = 3V$	2.1		
		$V_{CC} = 5.5V$	3.85		
V_{IL}	低电平输入电压	$V_{CC} = 2V$		0.5	V
		$V_{CC} = 3V$		0.9	
		$V_{CC} = 5.5V$		1.65	
V_I	输入电压		0	5.5	V
V_O	输出电压		0	V_{CC}	V
I_{OH}	高电平输出电流	$V_{CC} = 2V$		-50	μA
		$V_{CC} = 3.3V \pm 0.3V$		-4	mA
		$V_{CC} = 5V \pm 0.5V$		-8	mA
I_{OL}	低电平输出电流	$V_{CC} = 2V$		50	μA
		$V_{CC} = 3.3V \pm 0.3V$		4	mA
		$V_{CC} = 5V \pm 0.5V$		8	mA
$\Delta t/\Delta v$	输入转换上升或下降速率	$V_{CC} = 3.3V \pm 0.3V$		100	ns/V
		$V_{CC} = 5V \pm 0.5V$		20	ns/V
T_A	自然通风条件下的工作温度范围		-40	125	°C

5.4 热性能信息

热性能指标 ⁽¹⁾		DW	DB	DGV	N	NS	PW	单位
		20 引脚						
R _{θJA}	结至环境热阻 ⁽²⁾	81.1	70	92	69	60	116.8	°C/W

(1) 有关新旧热指标的更多信息，请参阅 *IC 封装热指标* 应用报告 [SPRA953](#)。

(2) 封装热阻抗根据 JESD 51-7 计算。

5.5 电气特性

在自然通风条件下的工作温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	$T_A = 25^{\circ}\text{C}$			-40°C 至 125°C			单位
			最小值	典型值	最大值	最小值	典型值	最大值	
V_{OH}	$I_{OH} = -50\ \mu\text{A}$	2V 至 5.5V	$V_{CC}-0.1$		V_{CC}	$V_{CC}-0.1$		V_{CC}	V
	$I_{OH} = -4\text{mA}$	3V	2.58			2.48			
	$I_{OH} = -8\text{mA}$	4.5V	3.94			3.8			
V_{OL}	$I_{OL} = 50\ \mu\text{A}$	2V 至 5.5V			0.1			0.1	V
	$I_{OL} = 4\text{mA}$	3V			0.36			0.44	
	$I_{OL} = 8\text{mA}$	4.5V			0.36			0.44	
I_I	$V_I = 5.5\text{V}$ 或 GND 并且 $V_{CC} = 0\text{V}$ 至 5.5V	0V 至 5.5V			± 0.1			± 1	μA
I_{OZ}	$V_O = V_{CC}$ 或 GND 且 $V_{CC} = 5.5\text{V}$	5.5V			± 0.25			± 5	μA
I_{CC}	$V_I = V_{CC}$ 或 GND, $I_O = 0$, $V_{CC} = 5.5\text{V}$	5.5V			4			40	μA
C_I	$V_I = V_{CC}$ 或 GND	5V		2	10			10	pF
C_O	$V_O = V_{CC}$ 或 GND	5V		5					pF
C_{PD}	空载, $F = 1\text{MHz}$	5V		15					pF

5.6 开关特性

$C_L = 50\text{pF}$ ；在自然通风条件下的工作温度范围内； $T_A = 25^{\circ}\text{C}$ 时测得的典型值（除非另有说明）。请参阅 [参数测量信息](#)

参数	从（输入）	到（输出）	负载电容	V_{CC}	$T_A = 25^{\circ}\text{C}$			-40°C 至 125°C			单位
					最小值	典型值	最大值	最小值	典型值	最大值	
t_{PLH}	A	Y	$C_L = 15\text{pF}$	2V			19.5		1	23	ns
t_{PHL}							19.5		1	23	ns
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 15\text{pF}$	2V			25.5		1	30	ns
t_{PZL}							25.5		1	30	ns
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 15\text{pF}$	2V			25.5		1	30	ns
t_{PLZ}							25.5		1	30	ns
t_{PLH}	A	Y	$C_L = 15\text{pF}$	3.3V		5.3	7.5		1	9	ns
t_{PHL}						5.3	7.5		1	9	ns
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 15\text{pF}$	3.3V		6.6	10.6		1	12.5	ns
t_{PZL}						6.6	10.6		1	12.5	ns
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 15\text{pF}$	3.3V		7.8	11.5		1	12.5	ns
t_{PLZ}						7.8	11.5		1	12.5	ns
t_{PLH}	A	Y	$C_L = 15\text{pF}$	5V		3.6	5.5		1	6.5	ns
t_{PHL}						3.6	5.5		1	6.5	ns

5.6 开关特性 (续)

$C_L = 50\text{pF}$ ；在自然通风条件下的工作温度范围内； $T_A = 25^\circ\text{C}$ 时测得的典型值（除非另有说明）。请参阅参数测量信息

参数	从 (输入)	到 (输出)	负载电容	V_{CC}	$T_A = 25^\circ\text{C}$			-40°C 至 125°C			单位
					最小值	典型值	最大值	最小值	典型值	最大值	
t_{PZH}	OE	Y	$C_L = 15\text{pF}$	5V	4.7	7.3		1		8.5	ns
t_{PZL}					4.7	7.3		1		8.5	ns
t_{PHZ}	OE	Y	$C_L = 15\text{pF}$	5V	5.2	7.2		1		8.5	ns
t_{PLZ}					5.2	7.2		1		8.5	ns
t_{PLH}	A	Y	$C_L = 50\text{pF}$	2V	26.5			1		30	ns
t_{PHL}					26.5			1		30	ns
t_{PZH}	OE	Y	$C_L = 50\text{pF}$	2V	32.5			1		36.5	ns
t_{PZL}					32.5			1		36.5	ns
t_{PHZ}	OE	Y	$C_L = 50\text{pF}$	2V	32			1		36.5	ns
t_{PLZ}					32			1		36.5	ns
t_{PLH}	A	Y	$C_L = 50\text{pF}$	3.3V	7.8	11		1		12.5	ns
t_{PHL}					7.8	11		1		12.5	ns
t_{PZH}	OE	Y	$C_L = 50\text{pF}$	3.3V	9.1	14.1		1		16	ns
t_{PZL}					9.1	14.1		1		16	ns
t_{PHZ}	OE	Y	$C_L = 50\text{pF}$	3.3V	10.3	14		1		16	ns
t_{PLZ}					10.3	14		1		16	ns
t_{PLH}	A	Y	$C_L = 50\text{pF}$	5V	5.1	7.5		1		8.5	ns
t_{PHL}					5.1	7.5		1		8.5	ns
t_{PZH}	OE	Y	$C_L = 50\text{pF}$	5V	6.2	9.3		1		10.5	ns
t_{PZL}					6.2	9.3		1		10.5	ns
t_{PHZ}	OE	Y	$C_L = 50\text{pF}$	5V	6.7	9.2		1		10.5	ns
t_{PLZ}					6.7	9.2		1		10.5	ns
$t_{sk(o)}$			$C_L = 50\text{pF}$	2V			2			2	ns
$t_{sk(o)}$			$C_L = 50\text{pF}$	3.3V			1.5			1.5	ns
$t_{sk(o)}$			$C_L = 50\text{pF}$	5V			1			1	ns

5.7 噪声特性

$V_{CC} = 5\text{V}$, $C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$

参数	说明	最小值	典型值	最大值	单位
$V_{OL(P)}$	安静输出, 最大动态 V_{OL}				V
$V_{OL(V)}$	安静输出, 最小动态 V_{OL}				V
$V_{OH(V)}$	安静输出, 最小动态 V_{OH}				V
$V_{IH(D)}$	高电平动态输入电压	3.5			V
$V_{IL(D)}$	低电平动态输入电压			1.5	V

5.8 典型特性

$T_A = 25^\circ\text{C}$ (除非另外注明)

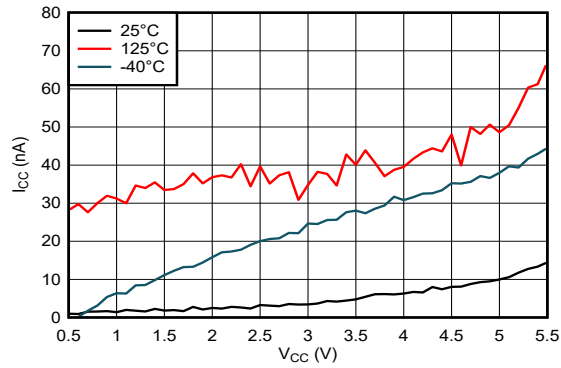


图 5-1. 电源电压两端的电源电流

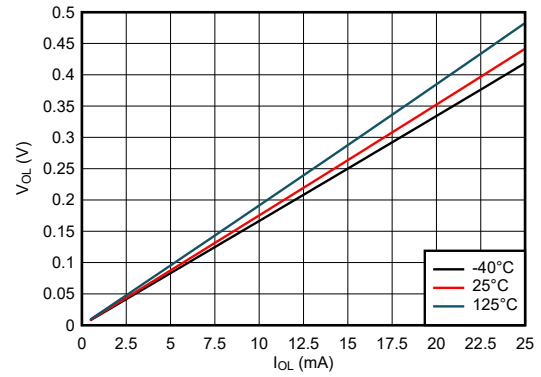


图 5-2. 低电平状态下输出电压与电流间的关系 (5V 电源)

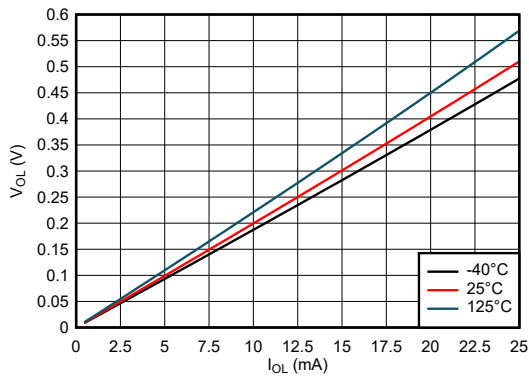


图 5-3. 低电平状态下输出电压与电流间的关系 (3.3V 电源)

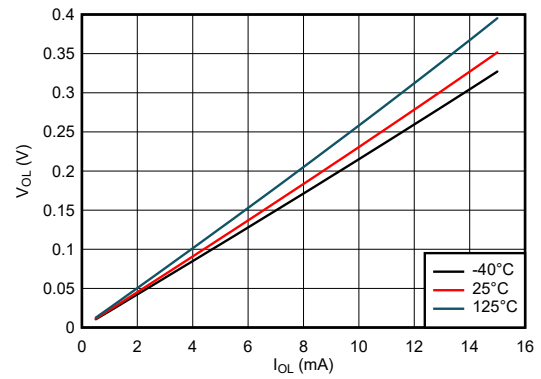
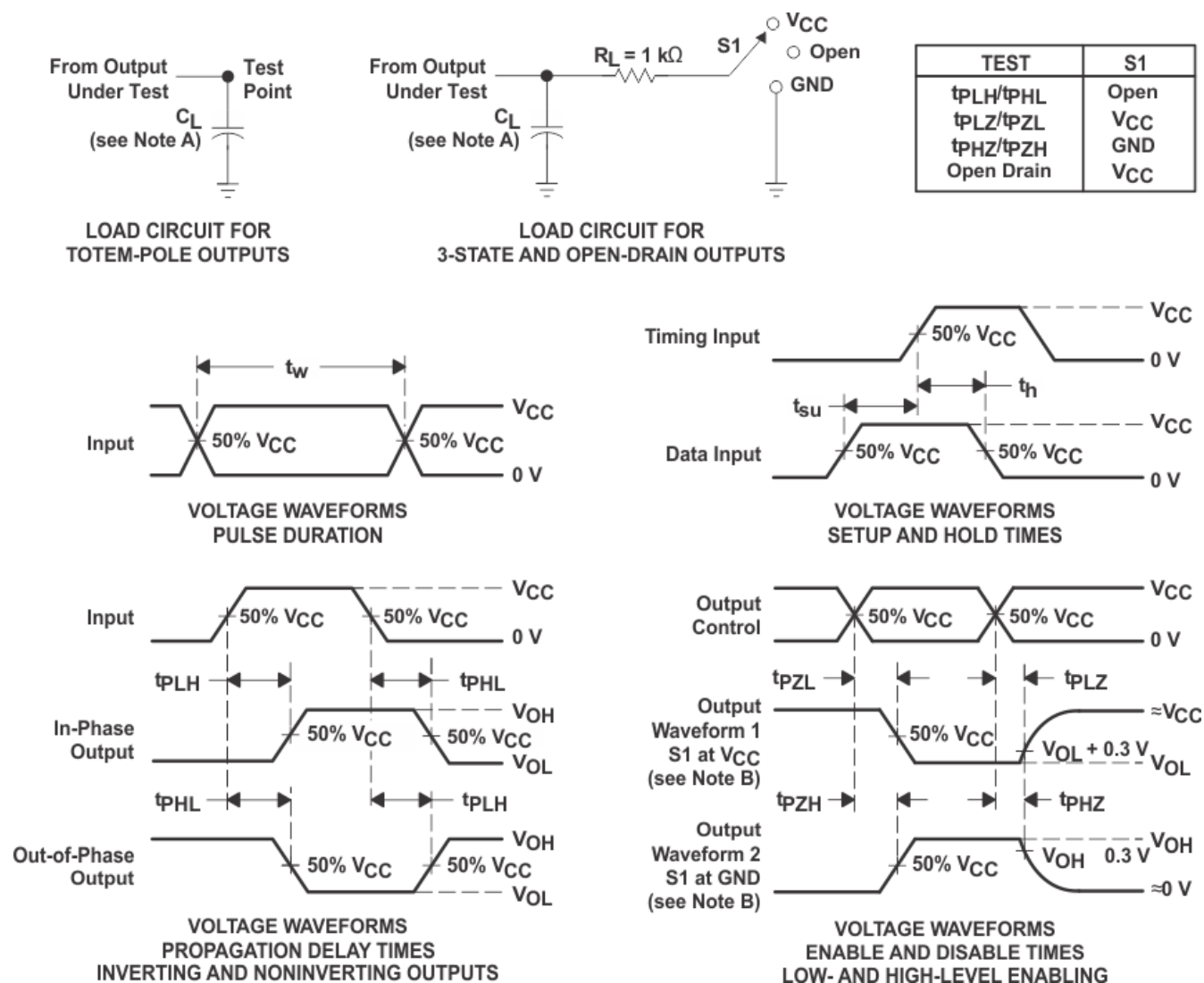


图 5-4. 低电平状态下输出电压与电流间的关系 (2.5V 电源)

6 参数测量信息



- A. C_L 包括探针和夹具电容。
- B. 波形 1 用于具有内部条件的输出，使得输出为低电平，除非被输出控制禁用。波形 2 用于具有内部条件的输出，使得输出为高电平，除非被输出控制禁用。
- C. 所有输入脉冲均由具有以下特性的发生器提供： $PRR \leq 1\text{ MHz}$ ， $Z_O = 50\Omega$ ， $t_r \leq 3\text{ ns}$ ， $t_f \leq 3\text{ ns}$ 。
- D. 一次测量一个输出，每次测量进行一次输入转换。E. 并非所有参数和波形都适用于所有器件。

图 6-1. 负载电路和电压波形

7 详细说明

7.1 概述

SNx4AHC240 器件配置为两个具有独立输出使能 ($\overline{OE}$) 输入的 4 位缓冲器/线路驱动器。当 $\overline{OE}$ 为低电平时，该器件将来自 A 输入的数据传输到 Y 输出。当 $\overline{OE}$ 为高电平时，输出处于高阻态。

要在上电或断电期间将器件置于高阻抗状态，应通过一个上拉电阻器将 $\overline{OE}$ 连接至 V_{CC} ；该电阻器的最小值由驱动器的电流灌入能力决定。

7.2 功能方框图

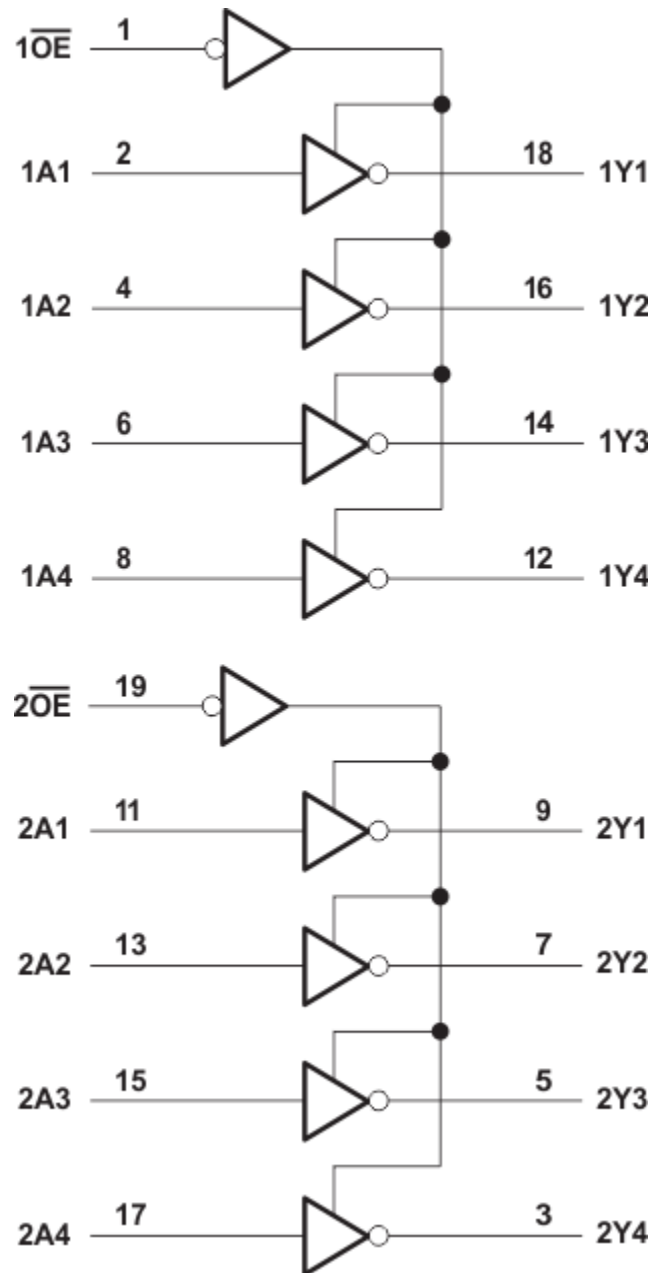


图 7-1. 逻辑图 (正逻辑)

7.3 特性说明

7.4 器件功能模式

表 7-1. 功能表
(每个缓冲器)

输入 ⁽¹⁾		输出 ⁽²⁾ Y
OE	A	
L	H	L
L	L	H
H	X	Z

- (1) H = 高电压电平, L = 低电压电平, X = 不用考虑
(2) H = 驱动为高电平, L = 驱动为低电平, Z = 高阻态

8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

SNx4AHC240 器件是一款高驱动 CMOS 器件，可用于需要保留或锁存数据的多种总线接口类型应用。它可以在 3.3V 下产生 24mA 驱动电流，因此非常适合驱动多个输出，也适用于高达 100MHz 的高速应用。输入可耐受 5.5V 电压，允许将其降压转换至 V_{CC} 。

8.2 典型应用

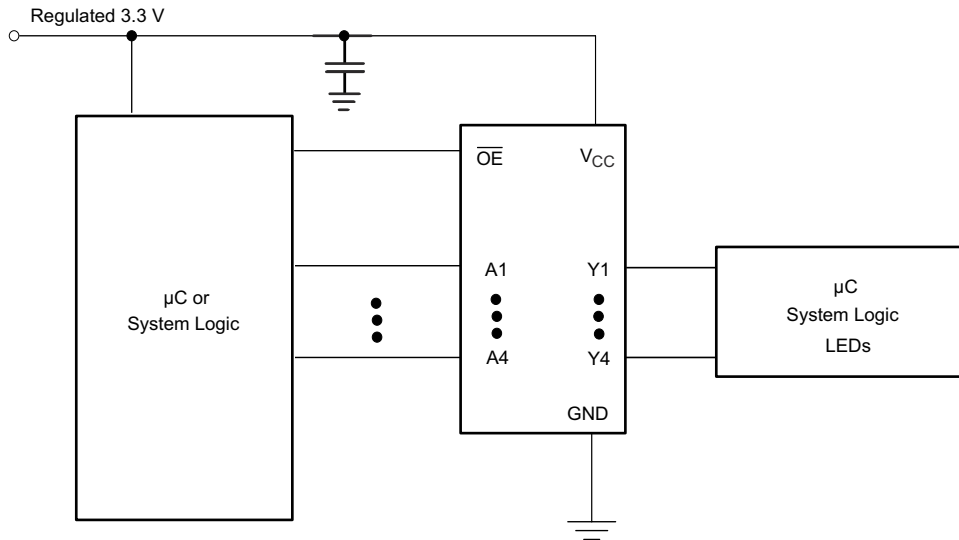


图 8-1. 典型应用图

8.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限制的电流。高驱动也会在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。

8.2.2 详细设计过程

1. 建议的输入条件
 - 上升时间和下降时间规格：请参阅 [建议运行条件](#) 表中的 $\Delta t / \Delta V$ 。
 - 指定的高电平和低电平：请参阅 [建议运行条件](#) 表中的 V_{IH} 和 V_{IL} 。
 - 输入具有过压容限，允许它们在任何有效 V_{CC} 下高达 5.5V。
2. 建议的输出条件
 - 每个输出的负载电流不应超过 25mA，该器件的总电流不应超过 50mA。
 - 输出不应被拉至高于 V_{CC} 。

8.2.3 应用曲线

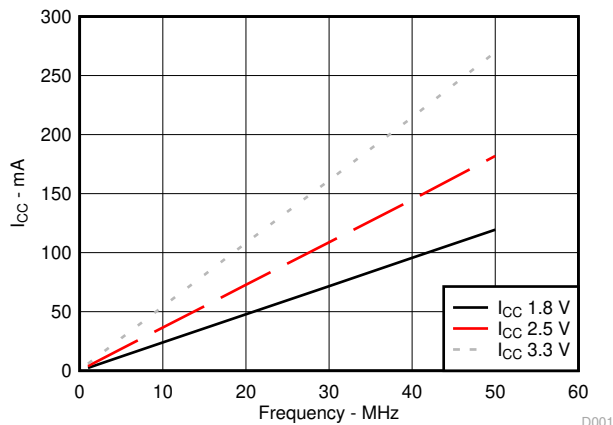


图 8-2. I_{CC} 与频率间的关系

8.3 电源相关建议

电源可以是 5.3 中最小和最大电源电压额定值之间的任意电压。

每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，TI 建议使用 $0.1\mu\text{F}$ 电容器；如果有多个 V_{CC} 端子，则 TI 建议为每个电源端子使用 $0.01\mu\text{F}$ 或 $0.022\mu\text{F}$ 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。 $0.1\mu\text{F}$ 和 $1\mu\text{F}$ 通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

8.4 布局

8.4.1 布局指南

当使用多位逻辑器件时，输入不应悬空。

在许多情况下，数字逻辑器件的功能或部分功能未被使用（例如，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时）。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的操作状态。以下是在所有情况下都必须遵守的规则。

数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。应为任何特定未使用输入应用的逻辑电平取决于器件的功能。通常，将这些输入连接到 GND 或 V_{CC} ，具体取决于哪种更合理或更方便。使输出悬空通常是可以接受的，除非该器件是收发器。如果该收发器有一个输出使能引脚，它会在置为有效时禁用该器件的输出部分。这不会禁用 I/O 的输入部分，因此输入在禁用后也不能悬空。

8.4.2 布局示例

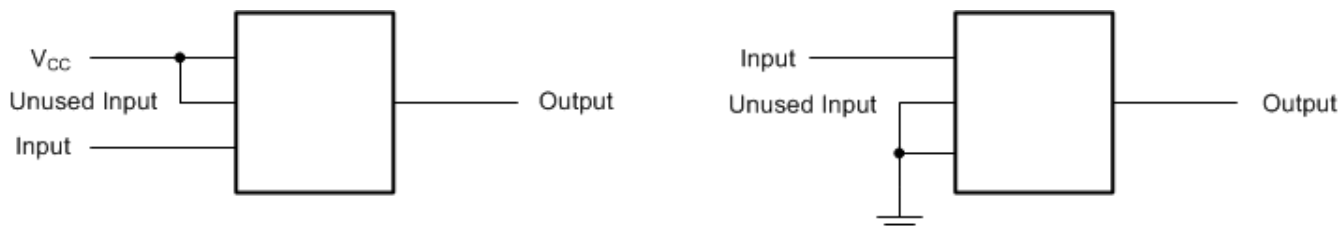


图 8-3. 布局建议

9 器件和文档支持

9.1 文档支持

9.1.1 相关文档

请参阅以下相关文档：

- 德州仪器 (TI)，[CMOS 输入缓慢变化或悬空的影响](#)
- 德州仪器 (TI)，[了解施密特触发](#)

9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

Changes from Revision I (April 2023) to Revision J (August 2024)	Page
--	------

- | | |
|---|---|
| • 向 器件信息 表中添加了封装尺寸和军用级封装..... | 1 |
| • 更新了 R _{θJA} 值：PW = 83 至 116.8，DW = 58 至 81.1，所有值均以 °C/W 为单位..... | 5 |

Changes from Revision H (July 2003) to Revision I (April 2023)	Page
--	------

- | | |
|--|---|
| • 添加了 封装信息表 、 引脚功能表 、 ESD 等级表 、 热性能信息表 、 器件功能模式 、“应用和实施”部分、 器件和文档支持 部分以及 机械、封装和可订购信息 部分..... | 1 |
|--|---|

11 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9680701Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9680701Q2A SNJ54AHC 240FK
5962-9680701QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680701QR A SNJ54AHC240J
5962-9680701QSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680701QS A SNJ54AHC240W
SN74AHC240DGSR	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240
SN74AHC240DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	AHC240
SN74AHC240DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240
SN74AHC240DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240
SN74AHC240N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHC240N
SN74AHC240N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHC240N
SN74AHC240NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240
SN74AHC240NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240
SN74AHC240PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	HA240
SN74AHC240PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA240
SN74AHC240PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA240
SN74AHC240RKSR	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240
SNJ54AHC240FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9680701Q2A SNJ54AHC 240FK
SNJ54AHC240FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9680701Q2A SNJ54AHC 240FK
SNJ54AHC240J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680701QR A SNJ54AHC240J

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHC240J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680701QR A SNJ54AHC240J
SNJ54AHC240W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680701QS A SNJ54AHC240W
SNJ54AHC240W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680701QS A SNJ54AHC240W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC240, SN74AHC240 :

- Catalog : [SN74AHC240](#)
- Automotive : [SN74AHC240-Q1](#), [SN74AHC240-Q1](#)
- Military : [SN54AHC240](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC240DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AHC240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC240NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC240RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC240DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AHC240DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC240NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHC240PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC240RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

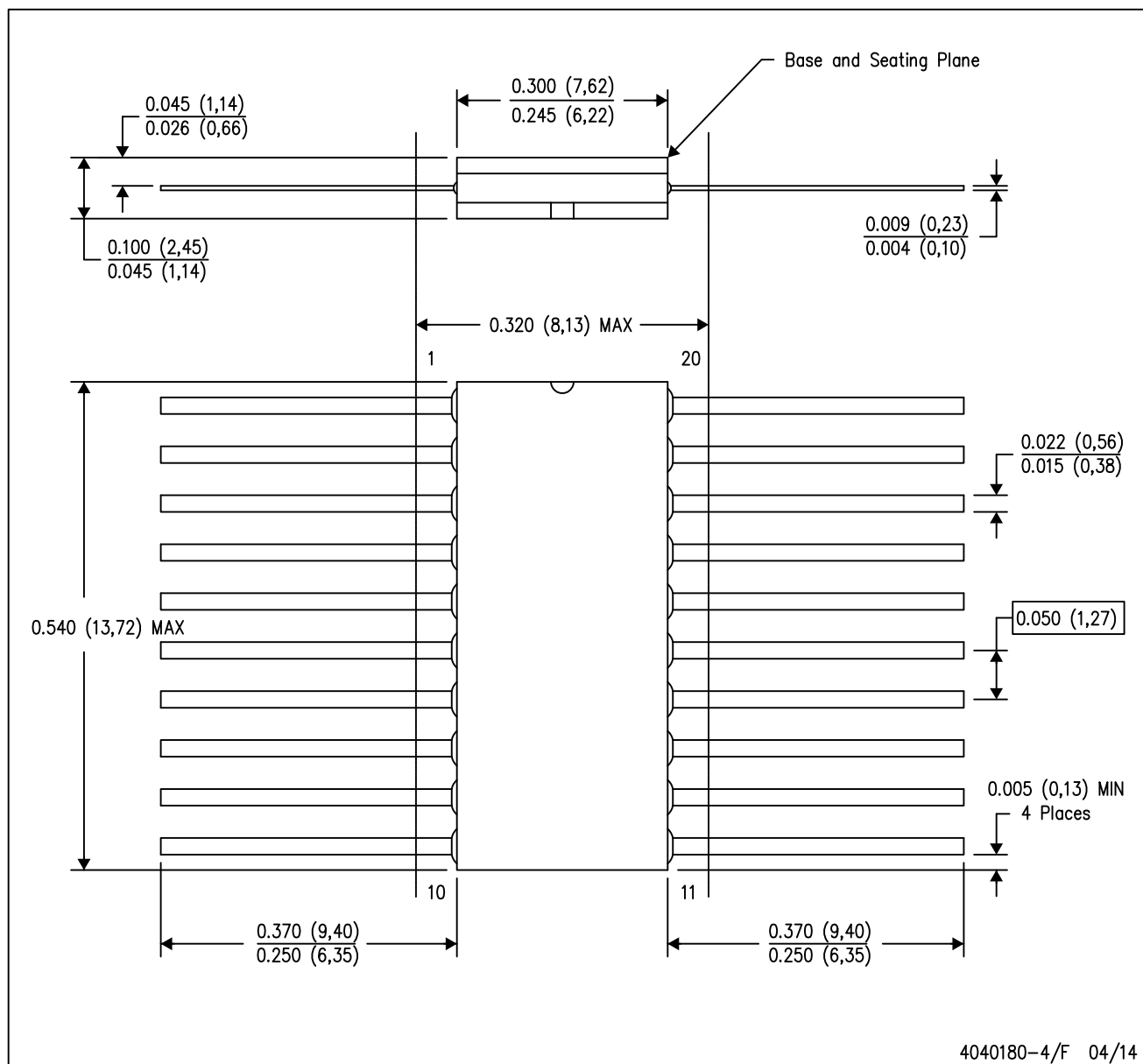
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9680701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9680701QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC240N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC240N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC240FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC240FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC240W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHC240W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

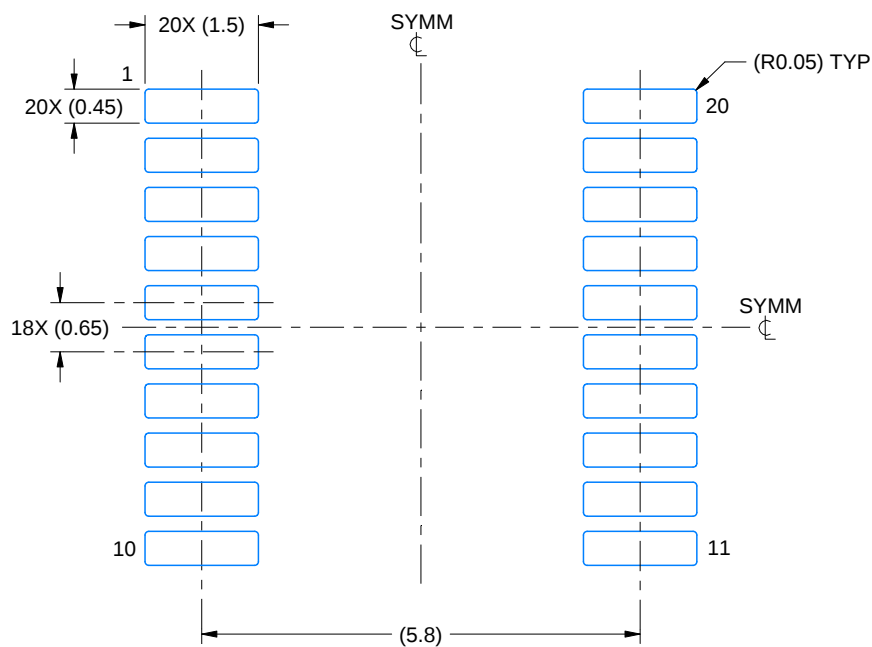


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

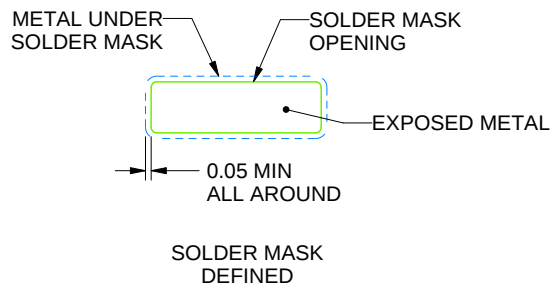
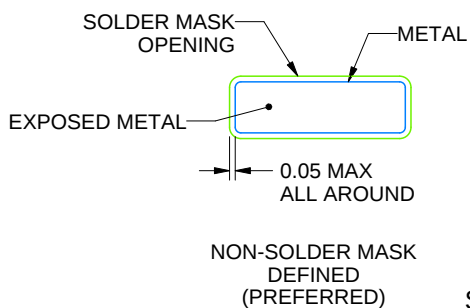
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

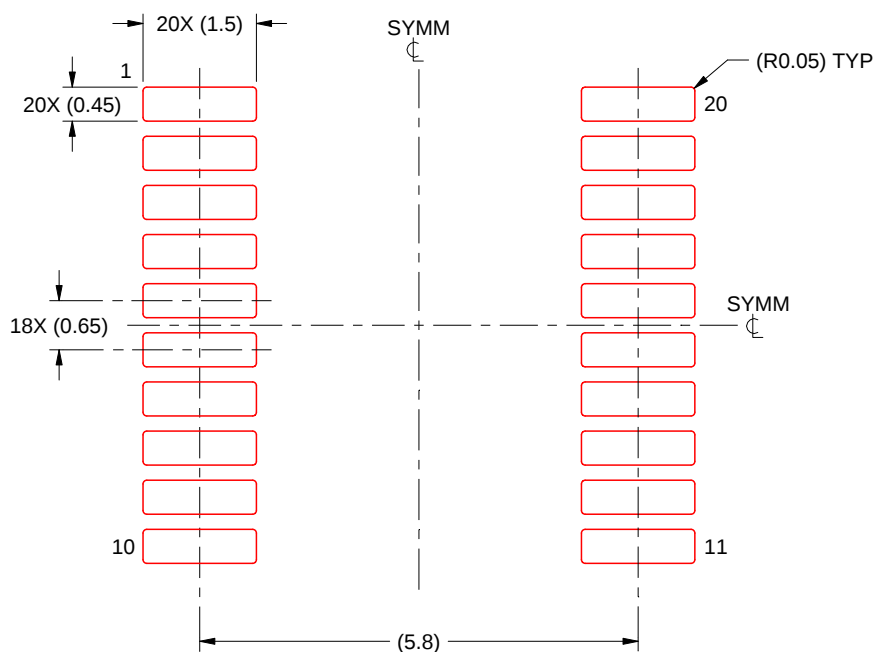
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

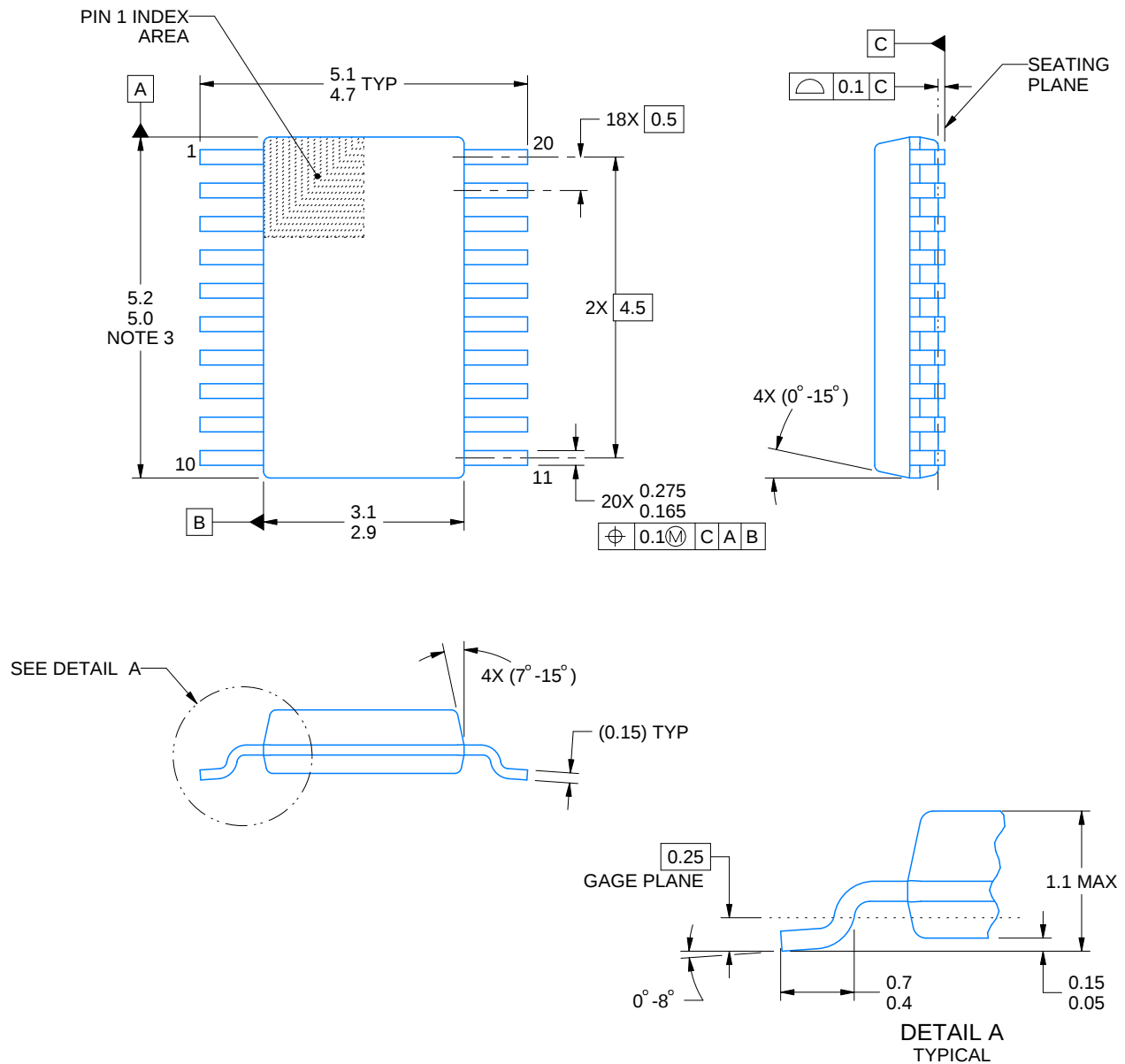


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4226367/A 10/2020

NOTES:

PowerPAD is a trademark of Texas Instruments.

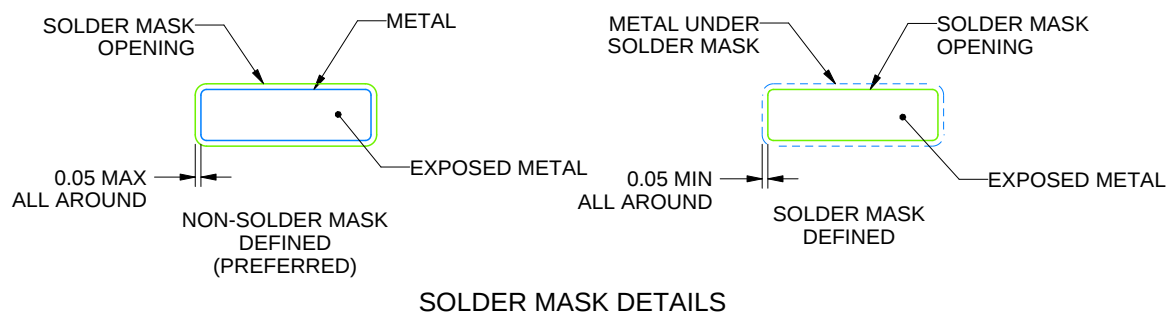
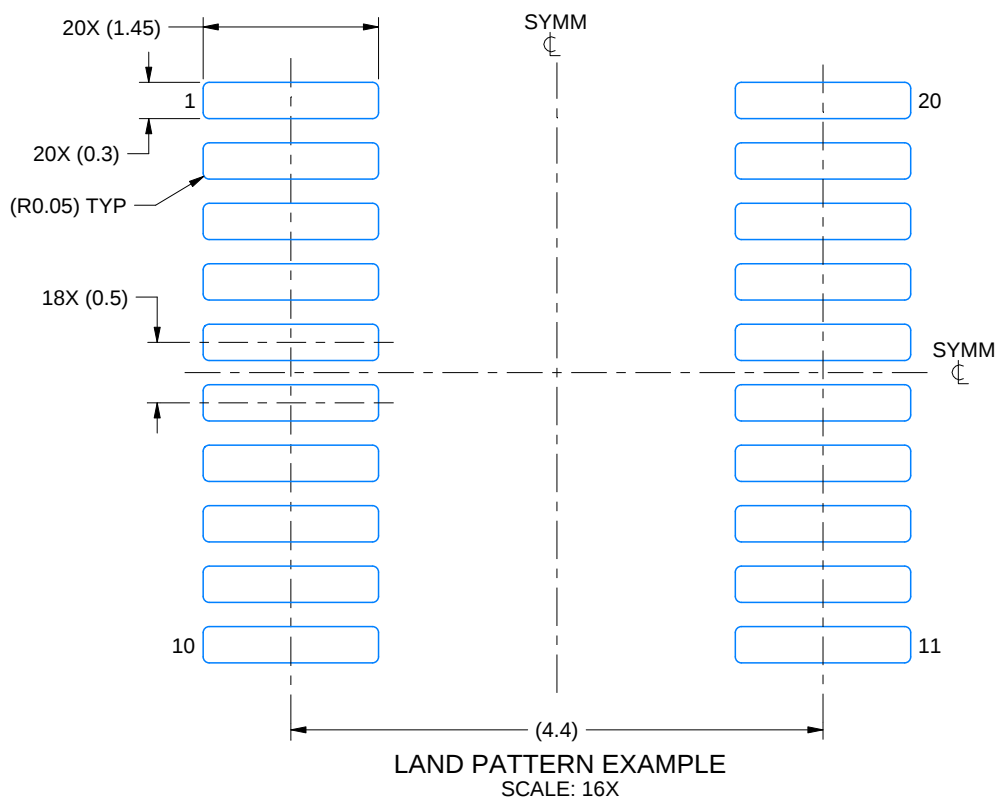
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

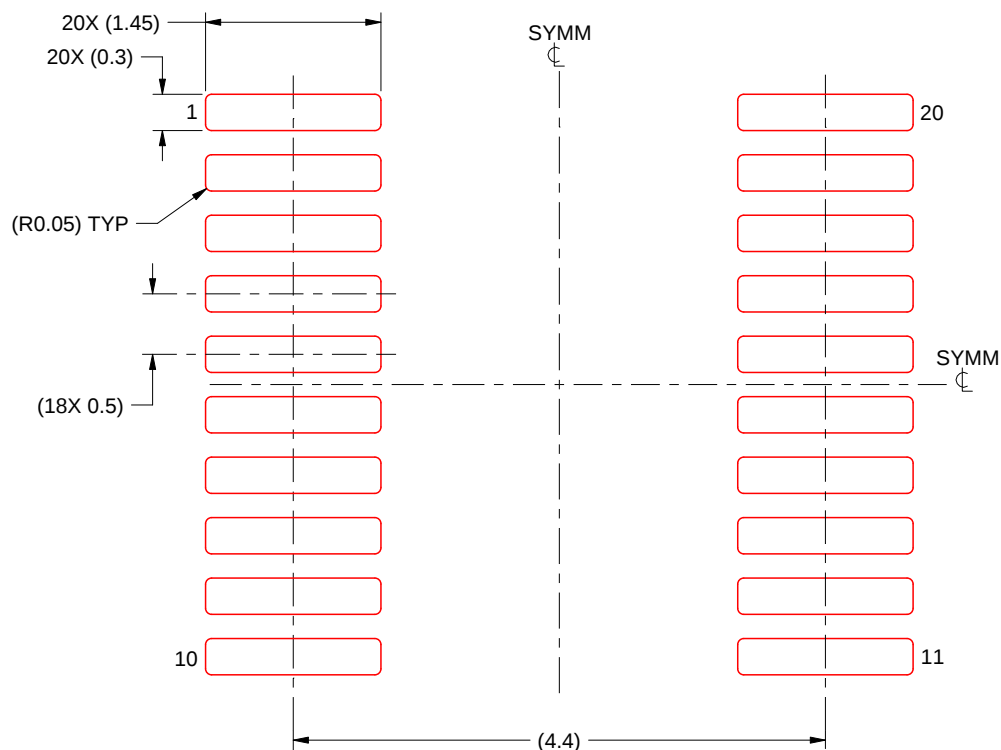
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

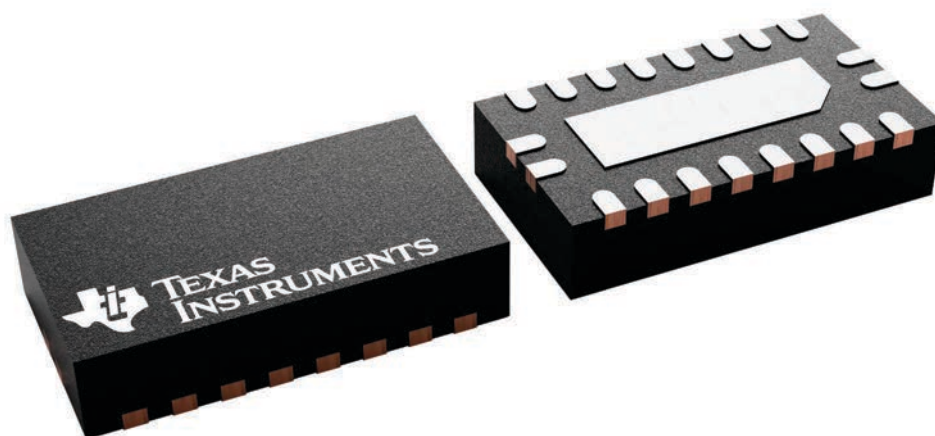
RKS 20

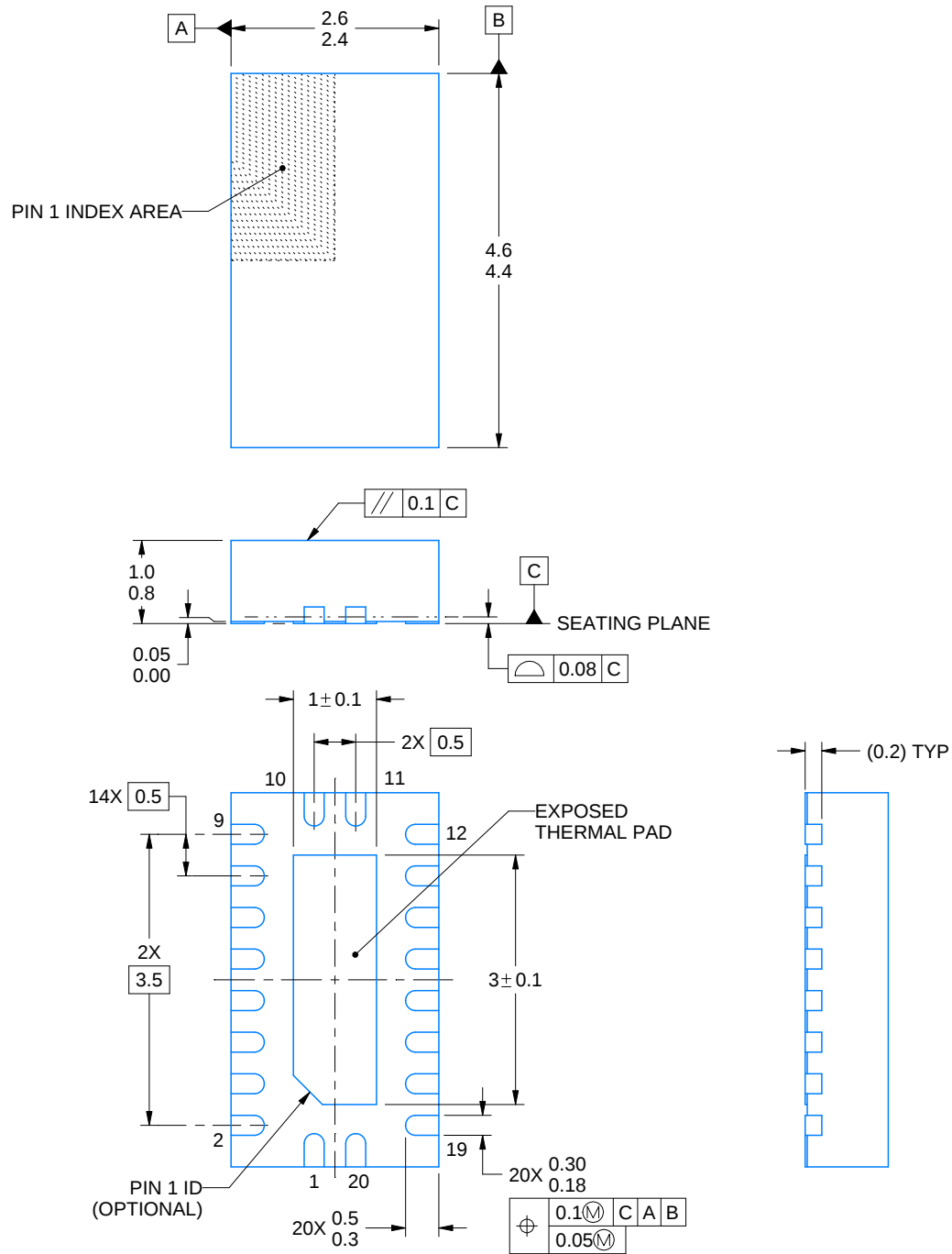
VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4222490/B 02/2021

NOTES:

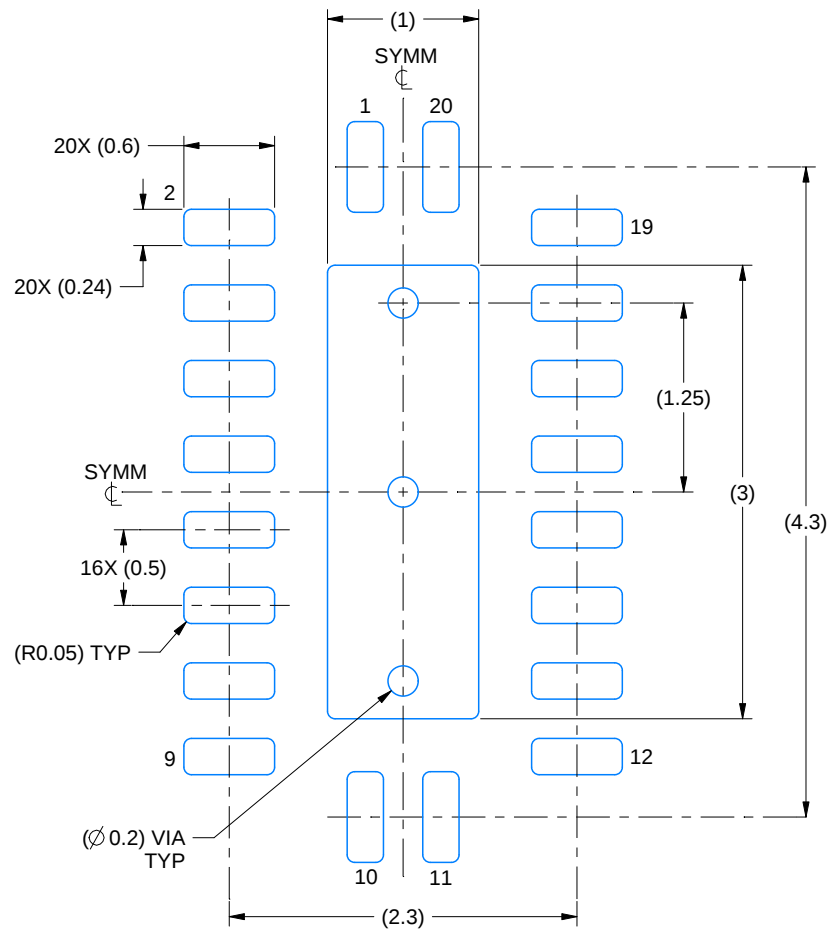
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

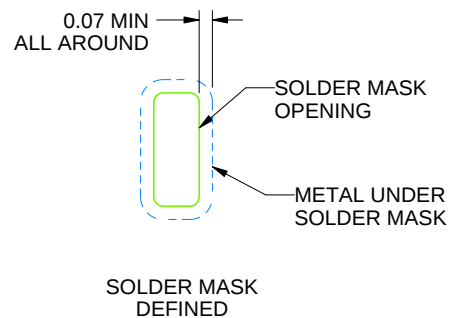
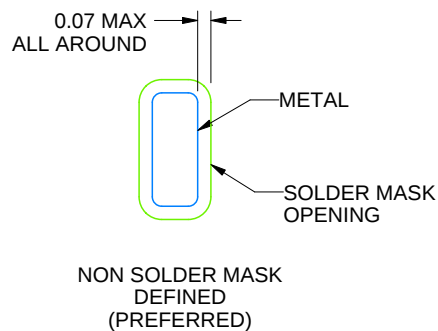
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

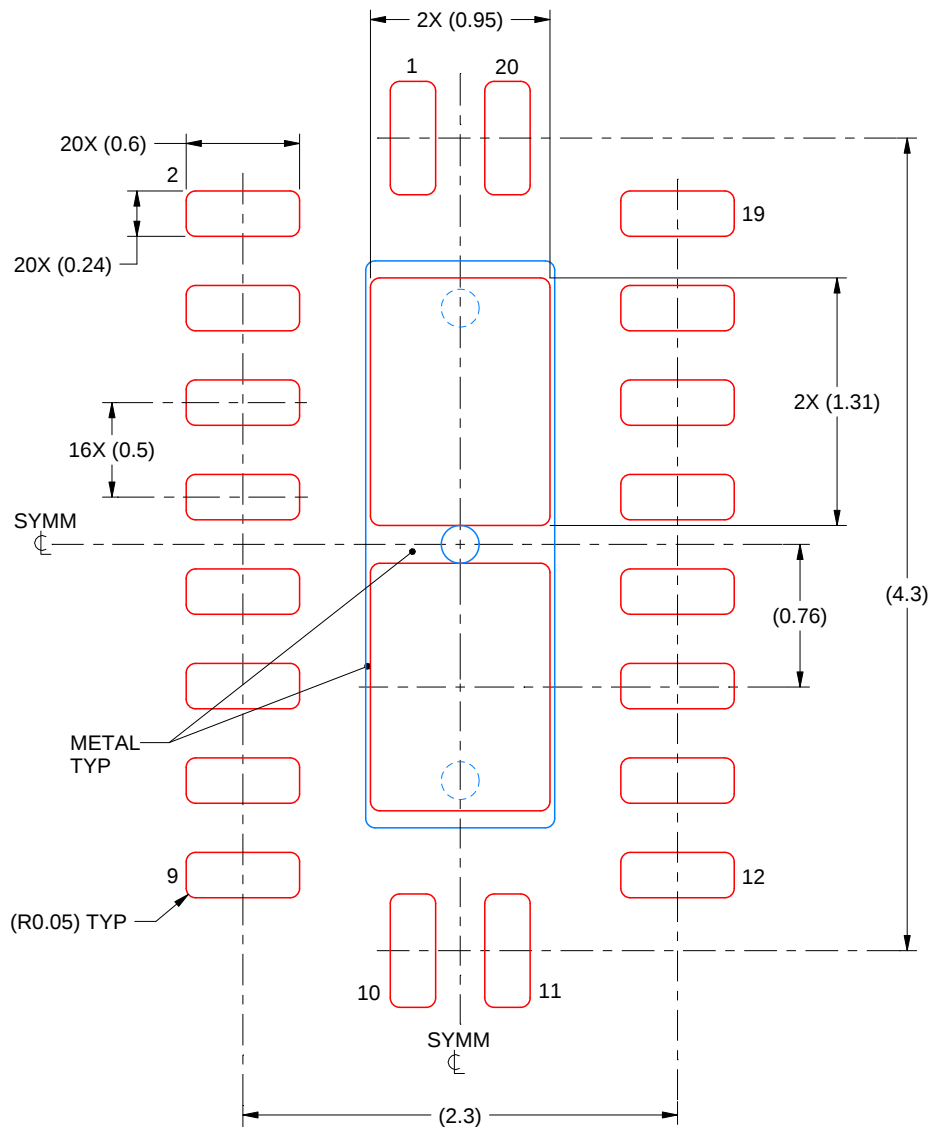
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 83% PRINTED SOLDER COVERAGE BY AREA
 SCALE:25X

4222490/B 02/2021

NOTES: (continued)

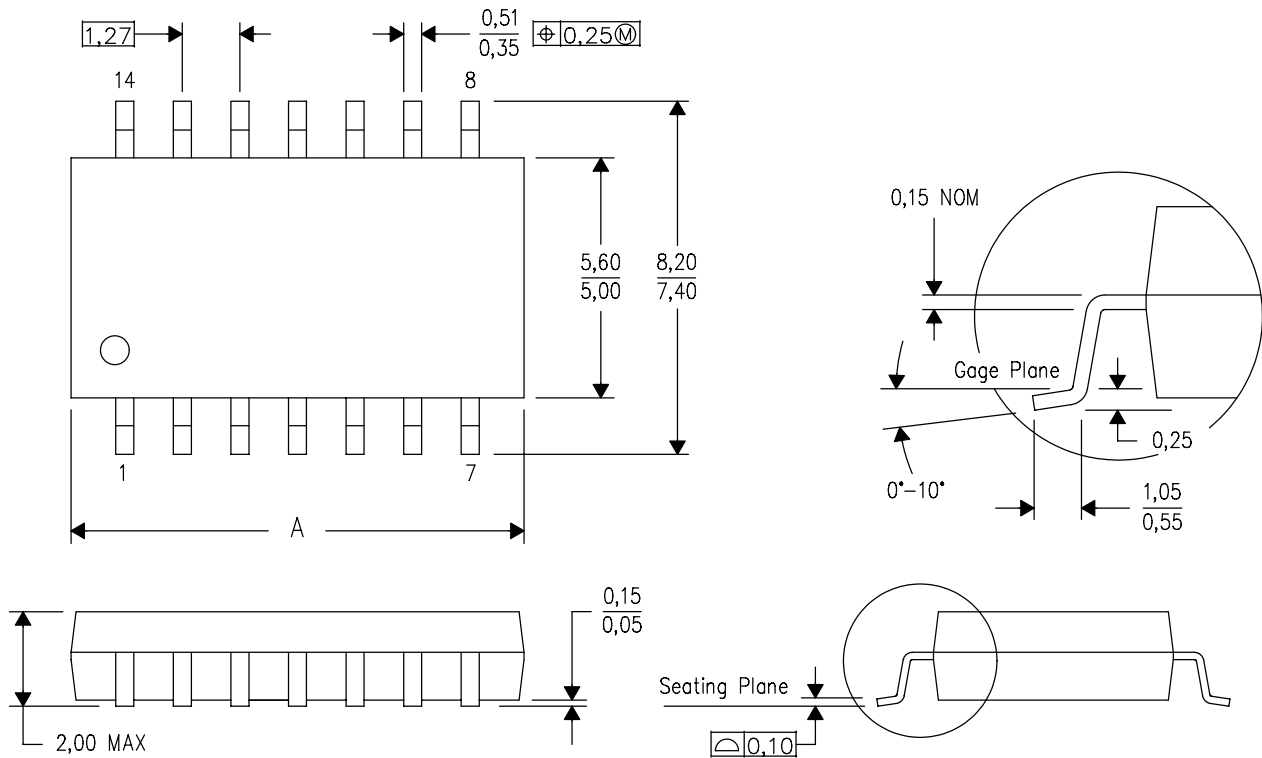
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

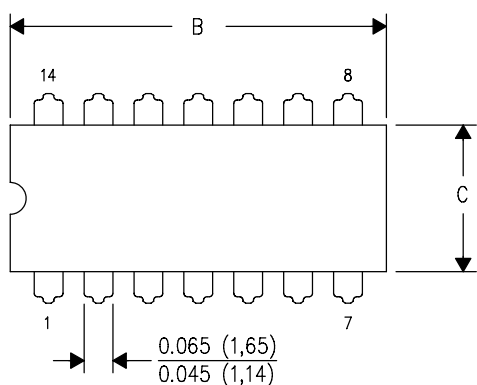
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

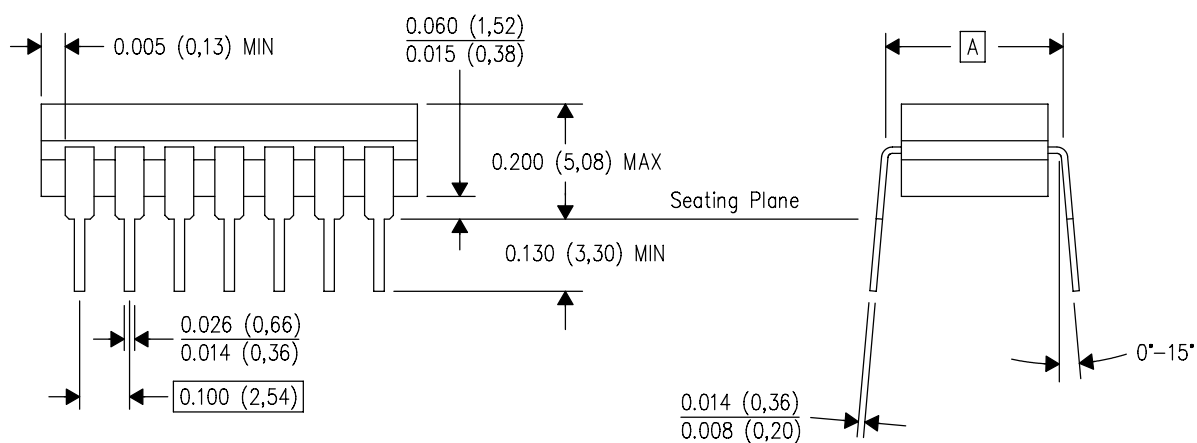
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

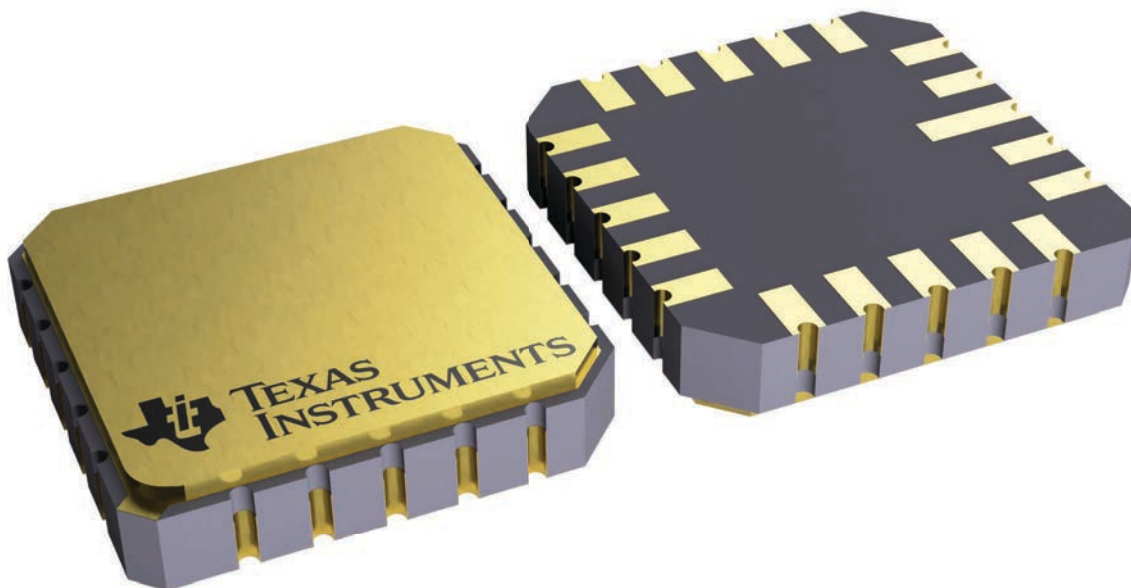
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

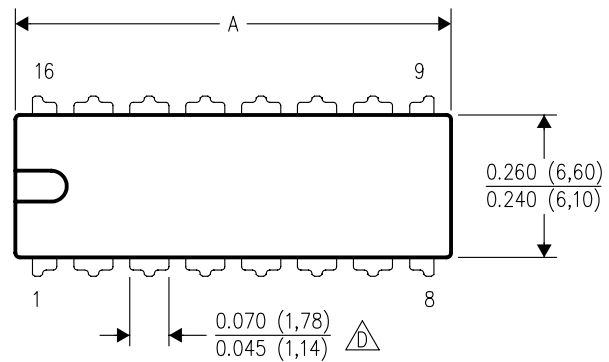


4229370VA\

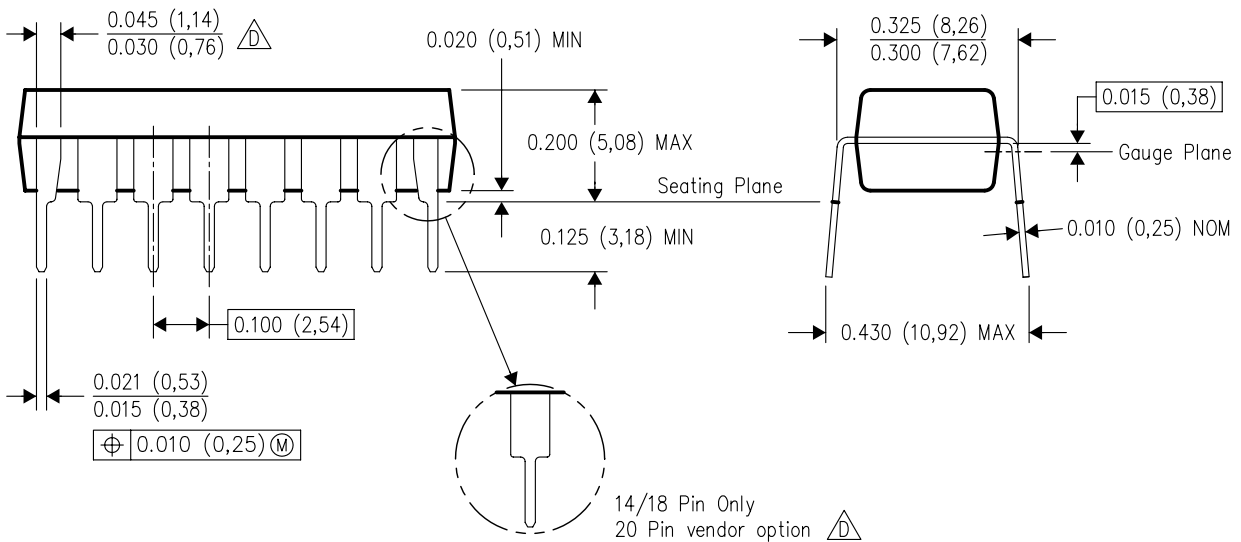
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

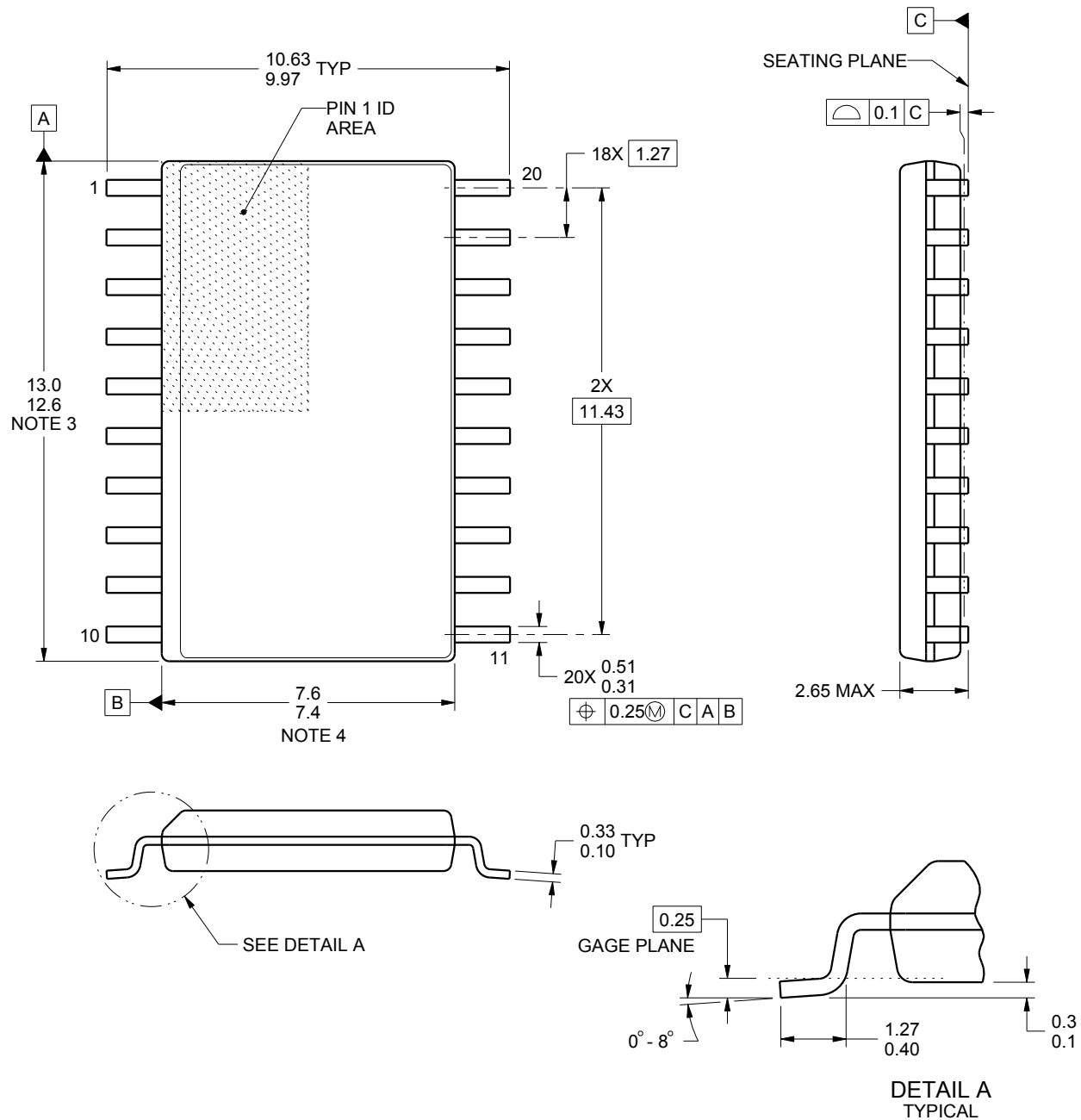
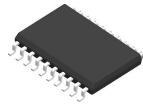


PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

NOTES:

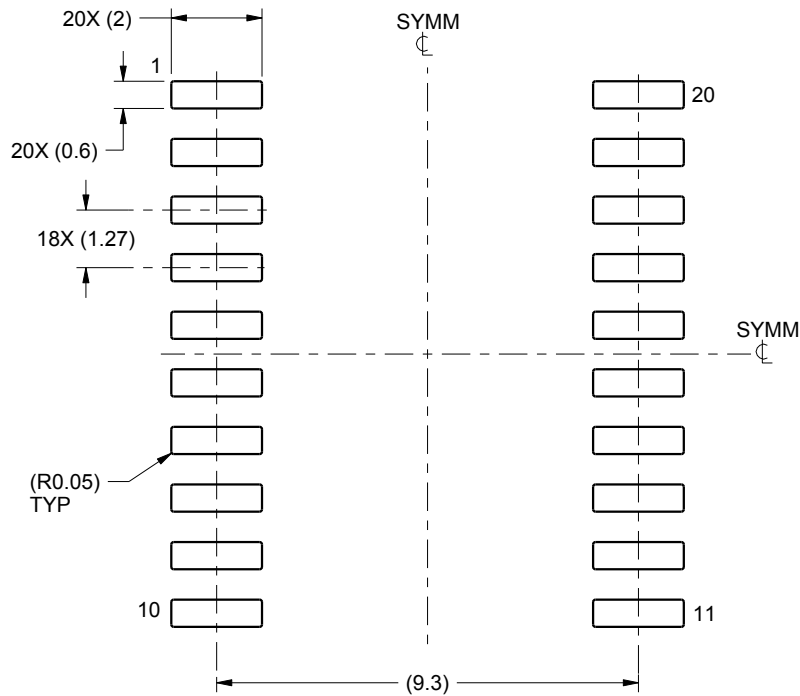
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

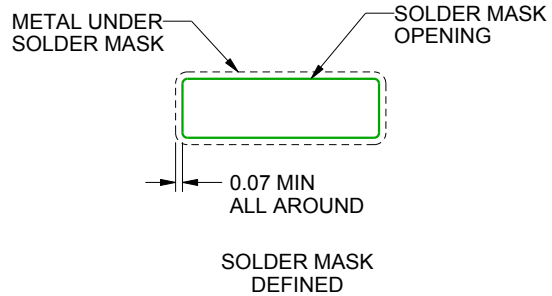
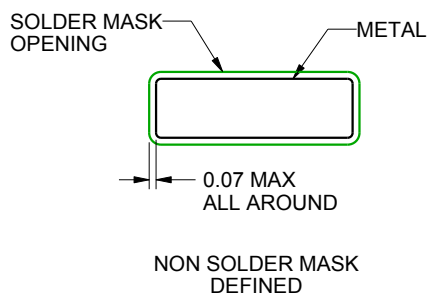
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

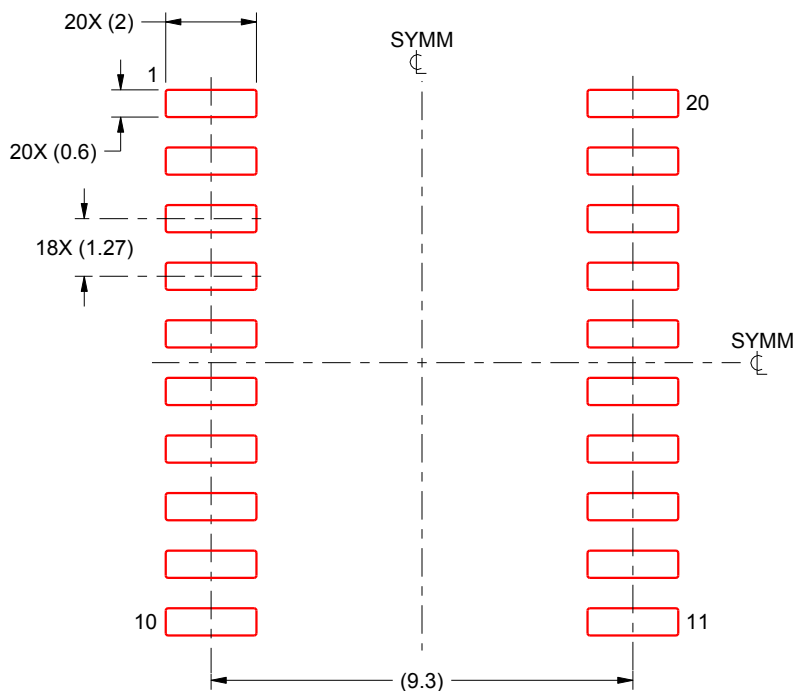
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月