# SN74AHC1G125 具有三态输出的单通道总线缓冲门

## 1 特性

- 工作电压范围为 2V 至 5.5V
- 电压为 5V 时，$t_{pd}$ 最大值为 6ns
- 低功耗，$I_{CC}$ 最大值为 10 µ A
- 5V 时，输出驱动为 ±8mA

## 2 应用

- 投影仪
- 电视
- 服务器
- 电机控制：交流感应
- 患者监护
- 电子销售终端

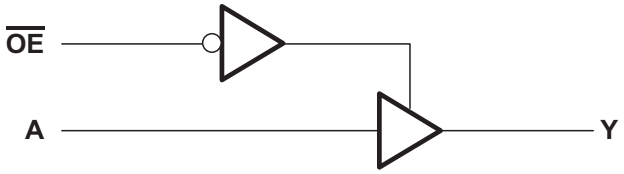
## 3 说明

SN74AHC1G125 器件是一款具有三态输出的单通道总线缓冲门/线路驱动器。当输出使能 ($\overline{OE}$) 输入为高电平时，输出被禁用。当 $\overline{OE}$ 为低电平时，真实数据从 A 输入传递到 Y 输出。

**封装信息**

| 器件型号 | 封装(1) | 封装尺寸(2) | 封装尺寸(3) |
|---|---|---|---|
| SN74AHC1G125 | DBV（SOT-23，5） | 2.8mm × 2.8mm | 2.9mm x 1.6mm |
| | DCK（SC-70，5） | 2.00mm × 2.1mm | 2mm × 1.25mm |
| | DRL（SOT-553，5） | 1.6mm x 1.6mm | 1.6mm × 1.2mm |

(1) 更多相关信息，请参阅第 11 节。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 封装尺寸（长 x 宽）为标称值，不包括引脚。




简化原理图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

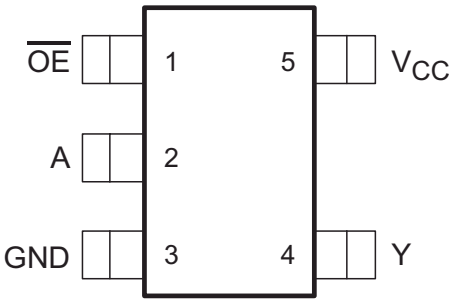
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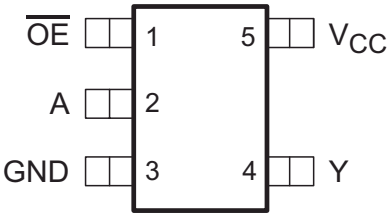

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## 4 Pin Configuration and Functions

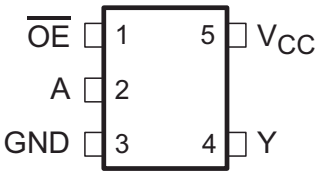
**DBV PACKAGE**
**(TOP VIEW)**




**DCK PACKAGE**
**(TOP VIEW)**




**DRL PACKAGE**
**(TOP VIEW)**




See mechanical drawings for dimensions.

**表 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | $\overline{OE}$ | I | Output Enable |
| 2 | A | I | Input A |
| 3 | GND | — | Ground Pin |
| 4 | Y | O | Output Y |
| 5 | $V_{CC}$ | — | Power Pin |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | – 0.5 | 7 | V |
| $V_I$ (2) | Input voltage range | | – 0.5 | 7 | V |
| $V_O$ (2) | Output voltage range | | – 0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | – 20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous channel current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature range | | – 65 | 150 | °C |
| $T_J$ | Junction Temperature | | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±1500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | – 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | – 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | – 8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |


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over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

| THERMAL METRIC(1) | | SN74AHC1G125 | | | UNIT |
|---|---|---|---|---|---|
| | | DBV (SOT-23, 5) | DCK (SC-70, 5) | DRL (SOT-553, 5) | |
| | | 5 PINS | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 278 | 289.2 | 328.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 180.5 | 205.8 | 105.1 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 184.4 | 176.2 | 150.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 115.4 | 117.6 | 6.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 183.4 | 175.1 | 148.4 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bot) thermal resistance | N/A | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –50 µA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 50 µA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.44 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | Input leakage current | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{OZ}$ | Off-State (High-Impedance State) Output Current (of a 3-State Output) | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | µA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 1 | | 10 | | 10 | µA |
| $C_i$ | Input capacitance | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | 10 | | 10 | pF |
| $C_o$ | Output capacitance | $V_O$ = $V_{CC}$ or GND | 5 V | | 10 | | | | | | pF |

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## 5.6 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | −40°C to 85°C | | −40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 5.6 | 8 | 1 | 9.5 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 8 | 1 | 9.5 | 1 | 10.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.4 | 8 | 1 | 9.5 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 5.4 | 8 | 1 | 9.5 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 7 | 9.7 | 1 | 11.5 | 1 | 12.5 | ns |
| $t_{PLZ}$ | | | | | 7 | 9.7 | 1 | 11.5 | 1 | 12.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 8.1 | 11.5 | 1 | 13 | 1 | 14 | ns |
| $t_{PHL}$ | | | | | 8.1 | 11.5 | 1 | 13 | 1 | 14 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 7.9 | 11.5 | 1 | 13 | 1 | 14 | ns |
| $t_{PZL}$ | | | | | 7.9 | 11.5 | 1 | 13 | 1 | 14 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | 1 | 16 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | 1 | 16 | |

## 5.7 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | −40°C to 85°C | | −40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | 1 | 7 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | 6.5 | 1 | 7 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 3.6 | 5.1 | 1 | 6 | 1 | 6.5 | ns |
| $t_{PZL}$ | | | | | 3.6 | 5.1 | 1 | 6 | 1 | 6.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4.6 | 6.8 | 1 | 8 | 1 | 8.5 | ns |
| $t_{PLZ}$ | | | | | 4.6 | 6.8 | 1 | 8 | 1 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | 8.5 | 1 | 9.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 5.1 | 7.1 | 1 | 8 | 1 | 9 | ns |
| $t_{PZL}$ | | | | | 5.1 | 7.1 | 1 | 8 | 1 | 9 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.1 | 8.8 | 1 | 10 | 1 | 11 | ns |
| $t_{PLZ}$ | | | | | 6.1 | 8.8 | 1 | 10 | 1 | 11 | |

## 5.8 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |


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## 5.9 Typical Characteristics

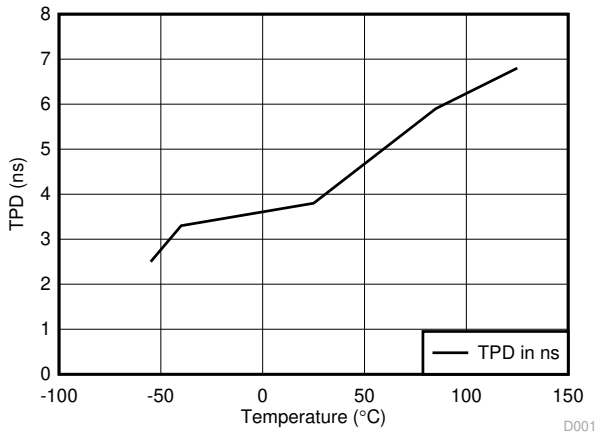



图 5-1. TPD vs Temperature

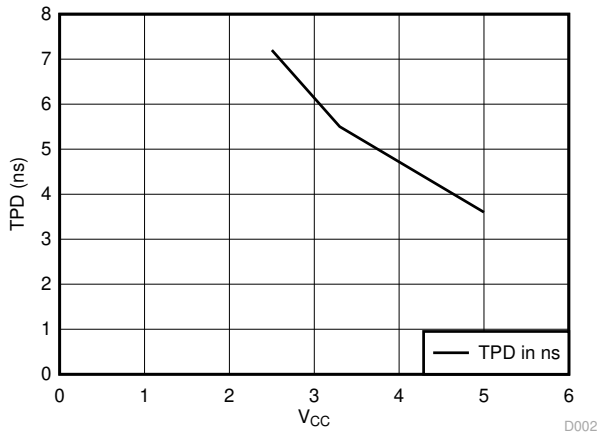
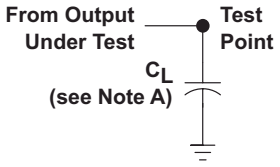
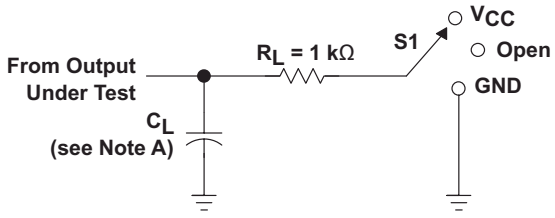



图 5-2. TPD vs $V_{CC}$ at 25°C

## 6 Parameter Measurement Information

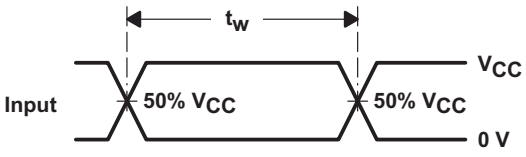



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

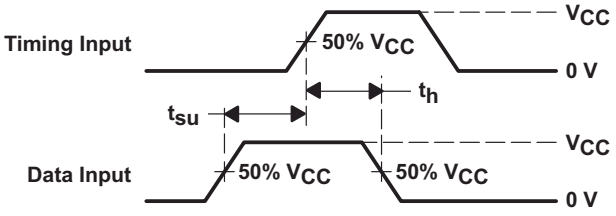



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |

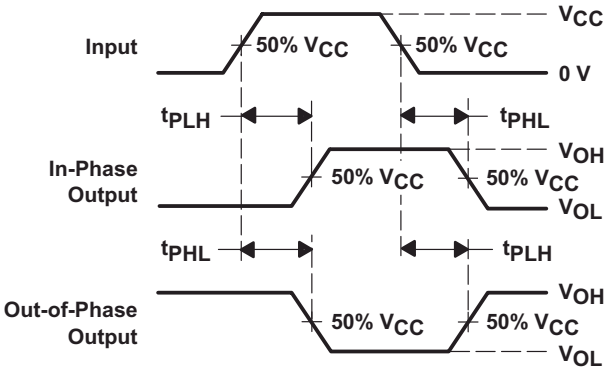
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



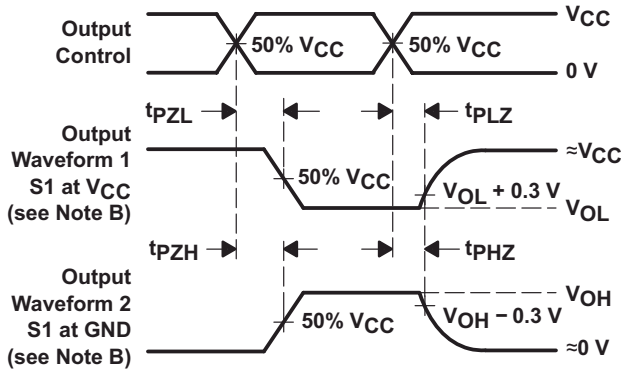

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**图 6-1. Load Circuit and Voltage Waveforms**


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# 7 Detailed Description

## 7.1 Overview

The SN74AHC1G125 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable ( $\overline{OE}$) input is high. When $\overline{OE}$ is low, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 7.2 Functional Block Diagram

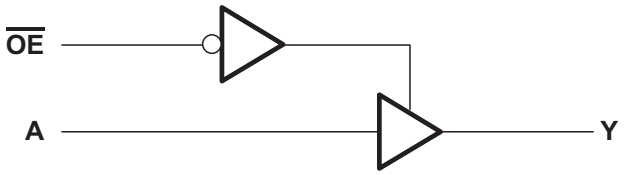



图 7-1. Logic Diagram (Positive Logic)

## 7.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V

## 7.4 Device Functional Modes

表 7-1. Function Table

| INPUTS(1) | | OUTPUT(2) |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don’t Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

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# 8 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 8.1 Application Information

SN74AHC1G125 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid $V_{CC}$ making it Ideal for down translation.

## 8.2 Typical Application

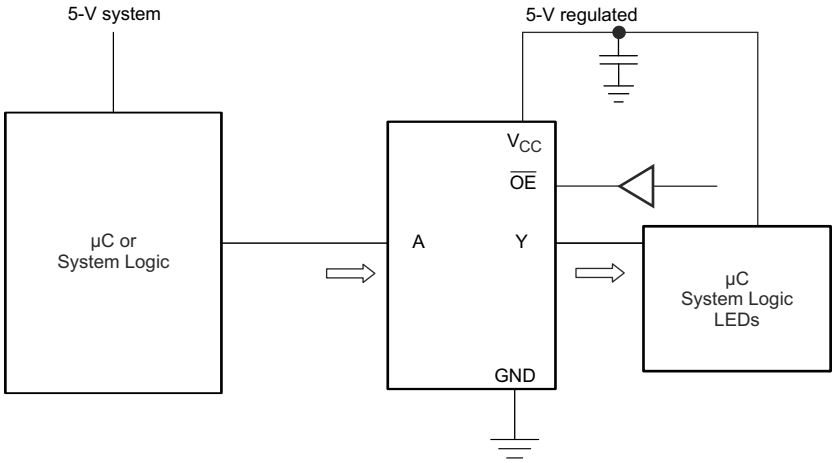



**图 8-1. Typical Application Schematic**

### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### 8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the *节 5.3* table.
   - For specified High and low levels, see $V_{IH}$ and $V_{IL}$ in the *节 5.3* table.
2. Recommend Output Conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.


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### 8.2.3 Application Curves

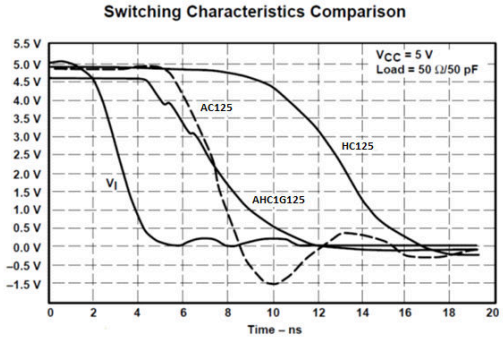



图 8-2.

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *节 5.3* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple $V_{CC}$ pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 图 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

#### *8.4.1.1 Layout Example*

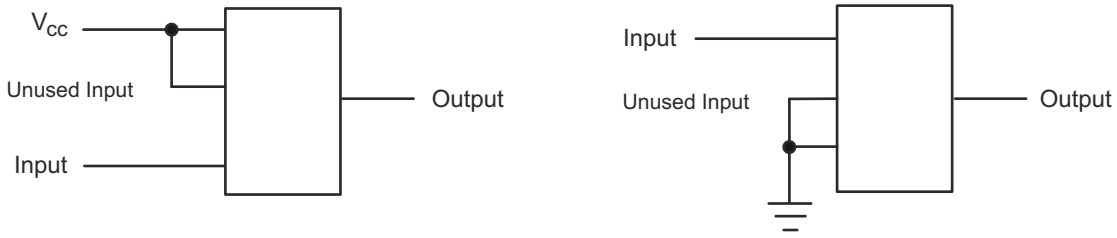



图 8-3. Layout Diagram

# 9 Device and Documentation Support

## 9.1 Documentation Support (Analog)

### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

## 9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 10 Revision History

| Changes from Revision L (October 2023) to Revision M (February 2024) | Page |
|---|---|
| • Updated thermal values for DBV package from R θ JA = 231.3 to 278, R θ JC(top) = 119.9 to 180.5, R θ JB = 60.6 to 184.4, Ψ JT = 17.8 to 115.4, Ψ JB = 60.1 to 183.4, R θ JC(bot) = N/A, all values in °C/W | 5 |

| Changes from Revision K (December 2014) to Revision L (October 2023) | Page |
|---|---|
| • 更新了整个文档中的表格、图和交叉参考的编号格式 | 1 |
| • Updated thermal values for DCK package from R θ JA = 287.6 to 289.2, R θ JC(top) = 97.7 to 205.8, R θ JB = 65 to 176.2, Ψ JT = 2 to 117.6, Ψ JB = 64.2 to 175.1, R θ JC(bot) = N/A, all values in °C/W | 5 |


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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 74AHC1G125DBVRE4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A25G |
| 74AHC1G125DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A25G |
| 74AHC1G125DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A25G |
| 74AHC1G125DBVTE4 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A25G |
| 74AHC1G125DBVTG4 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A25G |
| 74AHC1G125DBVTG4.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A25G |
| 74AHC1G125DCKRE4 | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AM3 |
| 74AHC1G125DCKRG4.A | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AM3 |
| 74AHC1G125DCKTG4 | Obsolete | Production | SC70 (DCK) \| 5 | - | - | Call TI | Call TI | -40 to 125 | AM3 |
| SN74AHC1G125DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (39HH, 3BXF, A253, A25G, A25J, A 25L, A25S) |
| SN74AHC1G125DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (39HH, 3BXF, A253, A25G, A25J, A 25L, A25S) |
| SN74AHC1G125DBVT | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 125 | (A253, A25G, A25J, A25S) |
| SN74AHC1G125DCK3 | Last Time Buy | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SNBI | Level-1-260C-UNLIM | -40 to 85 | AMY |
| SN74AHC1G125DCK3.A | Last Time Buy | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SNBI | Level-1-260C-UNLIM | -40 to 85 | AMY |
| SN74AHC1G125DCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (1RB, AM3, AMG, AM J, AML, AMS) |
| SN74AHC1G125DCKR.A | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (1RB, AM3, AMG, AM J, AML, AMS) |
| SN74AHC1G125DCKT | Obsolete | Production | SC70 (DCK) \| 5 | - | - | Call TI | Call TI | -40 to 125 | (AM3, AMG, AMJ, AM S) |
| SN74AHC1G125DRLR | Active | Production | SOT-5X3 (DRL) \| 5 | 4000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AMS |
| SN74AHC1G125DRLR.A | Active | Production | SOT-5X3 (DRL) \| 5 | 4000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AMS |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AHC1G125 :**

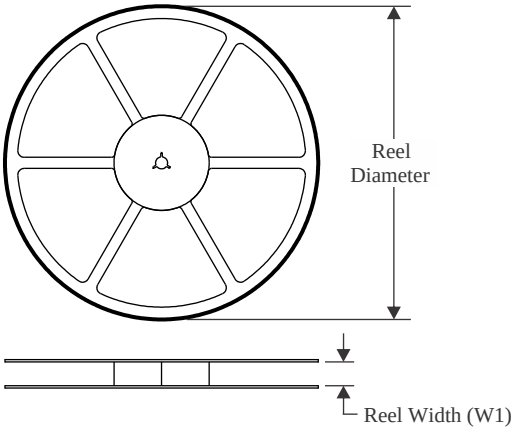
- Automotive : SN74AHC1G125-Q1

NOTE: Qualified Version Definitions:

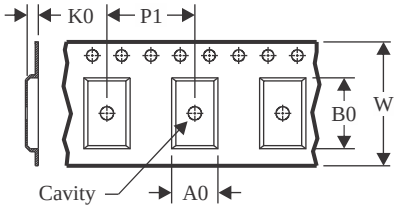
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

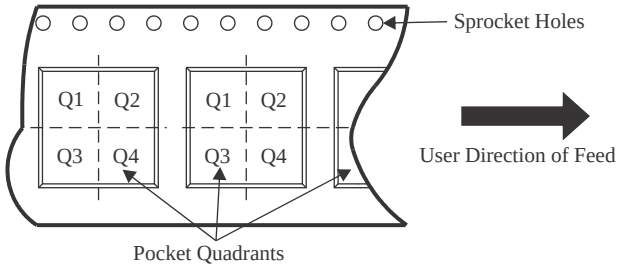



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

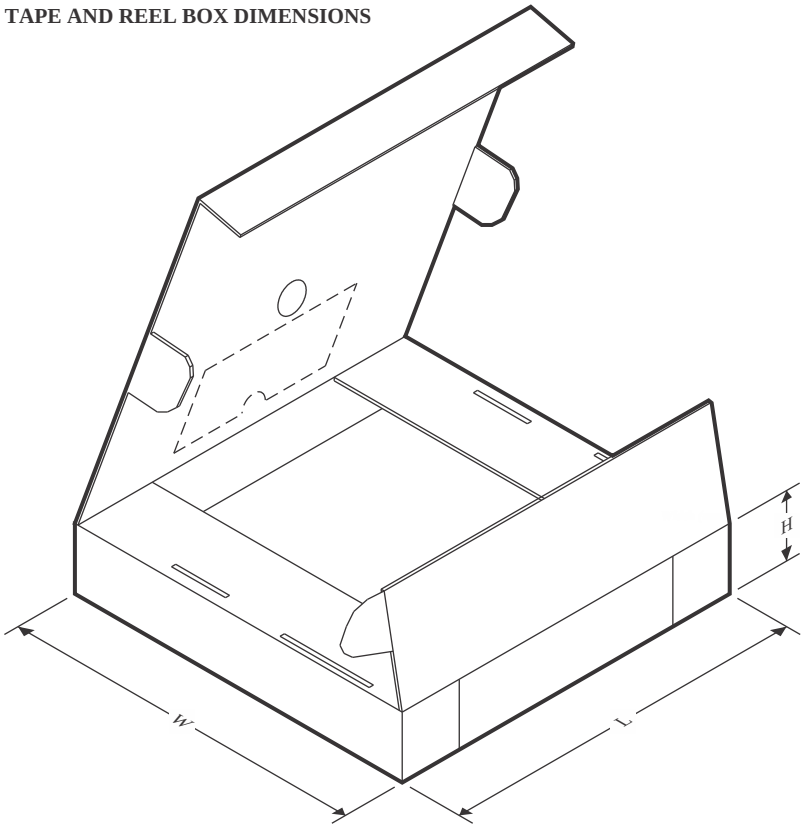
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74AHC1G125DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| 74AHC1G125DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G125DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AHC1G125DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AHC1G125DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AHC1G125DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AHC1G125DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

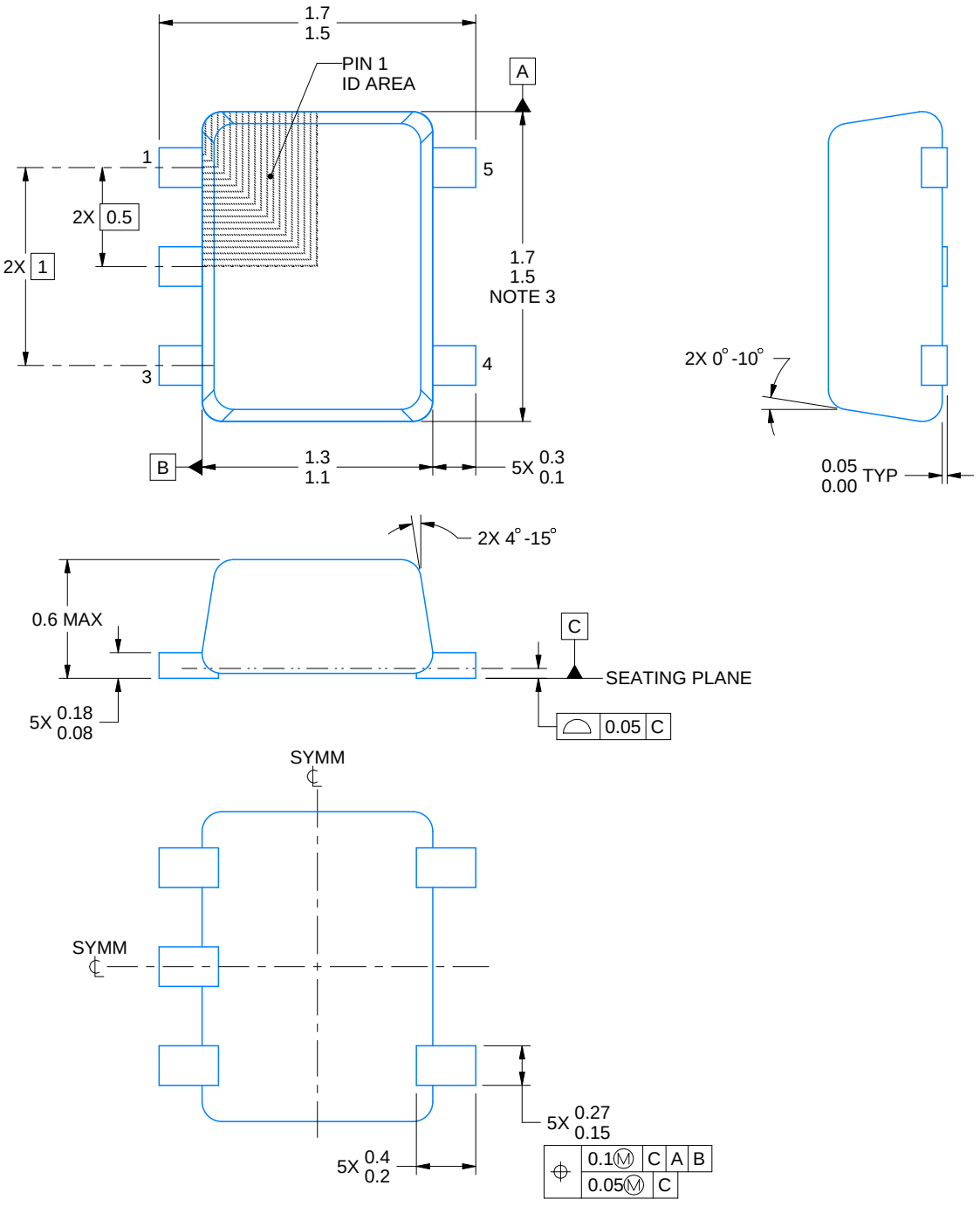
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74AHC1G125DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| 74AHC1G125DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G125DBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74AHC1G125DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHC1G125DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHC1G125DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHC1G125DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |

# PACKAGE OUTLINE

## DRL0005A

## SOT - 0.6 mm max height

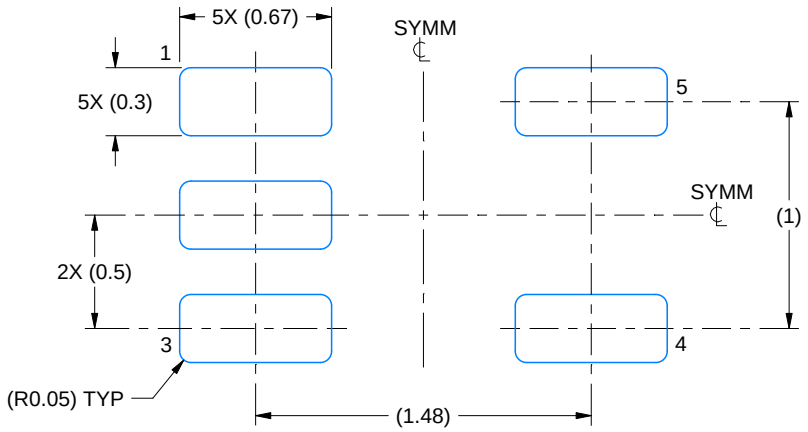
PLASTIC SMALL OUTLINE



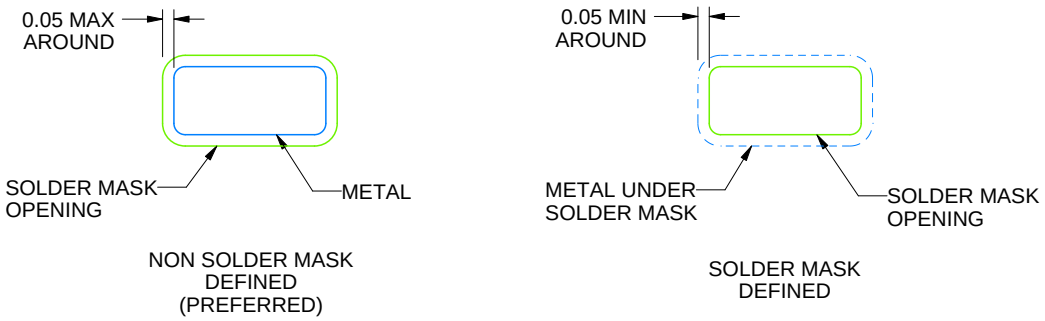

4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1




LAND PATTERN EXAMPLE
SCALE:30X

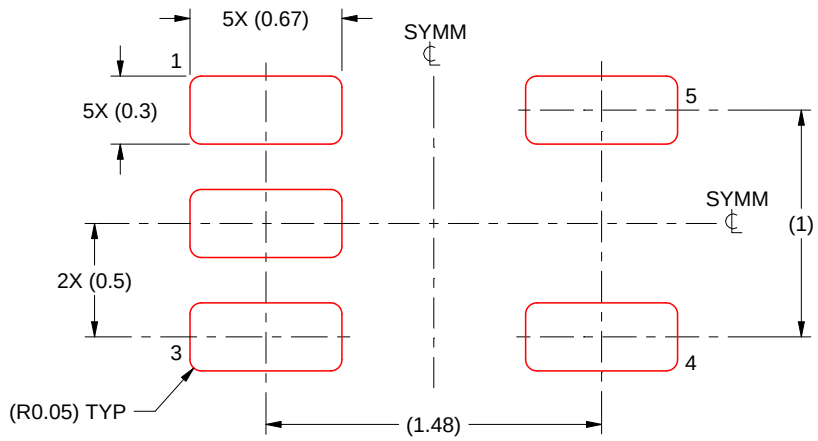



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

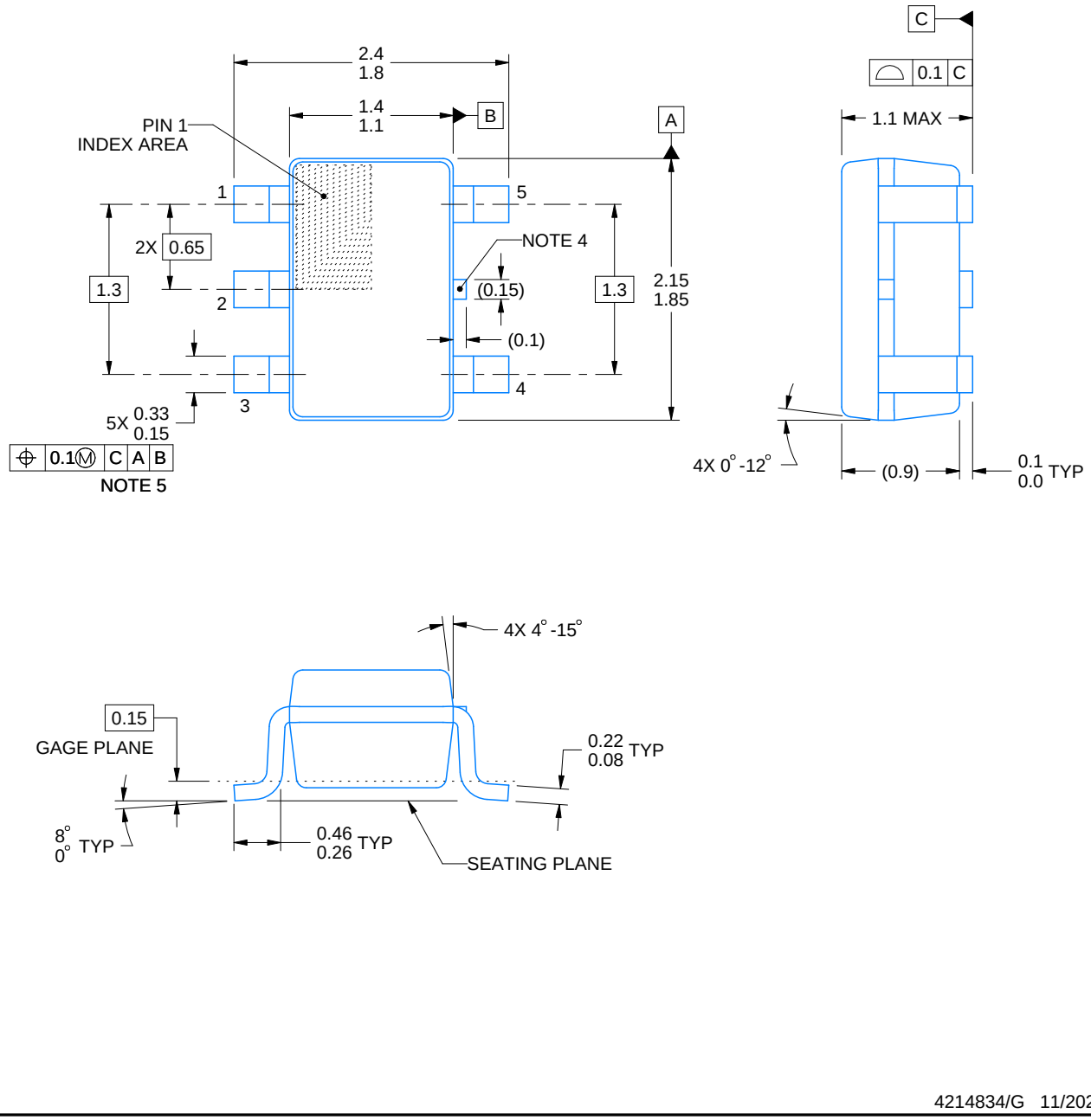
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

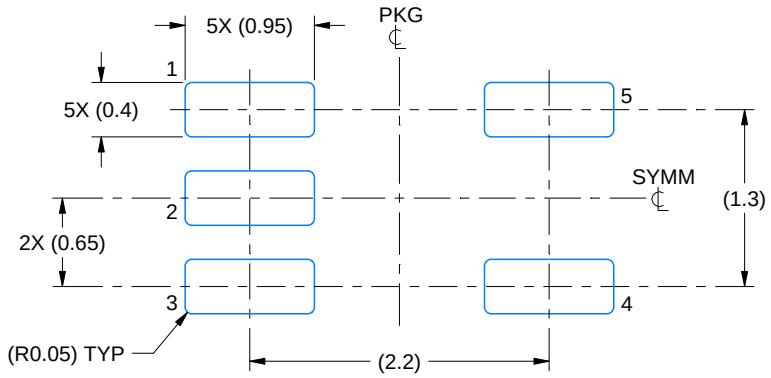
SMALL OUTLINE TRANSISTOR



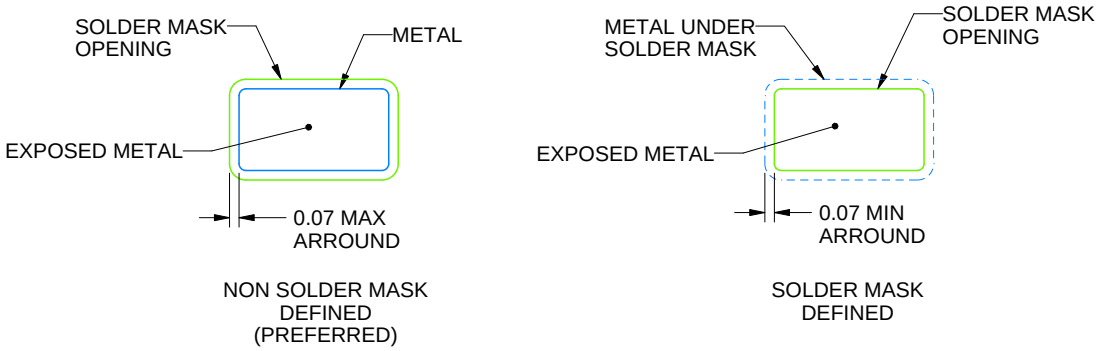

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

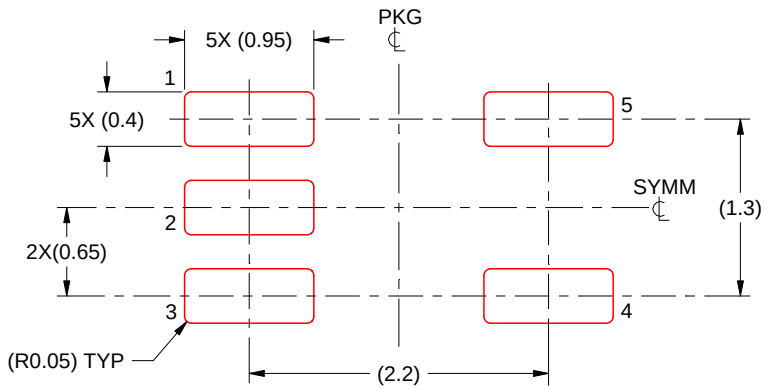



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

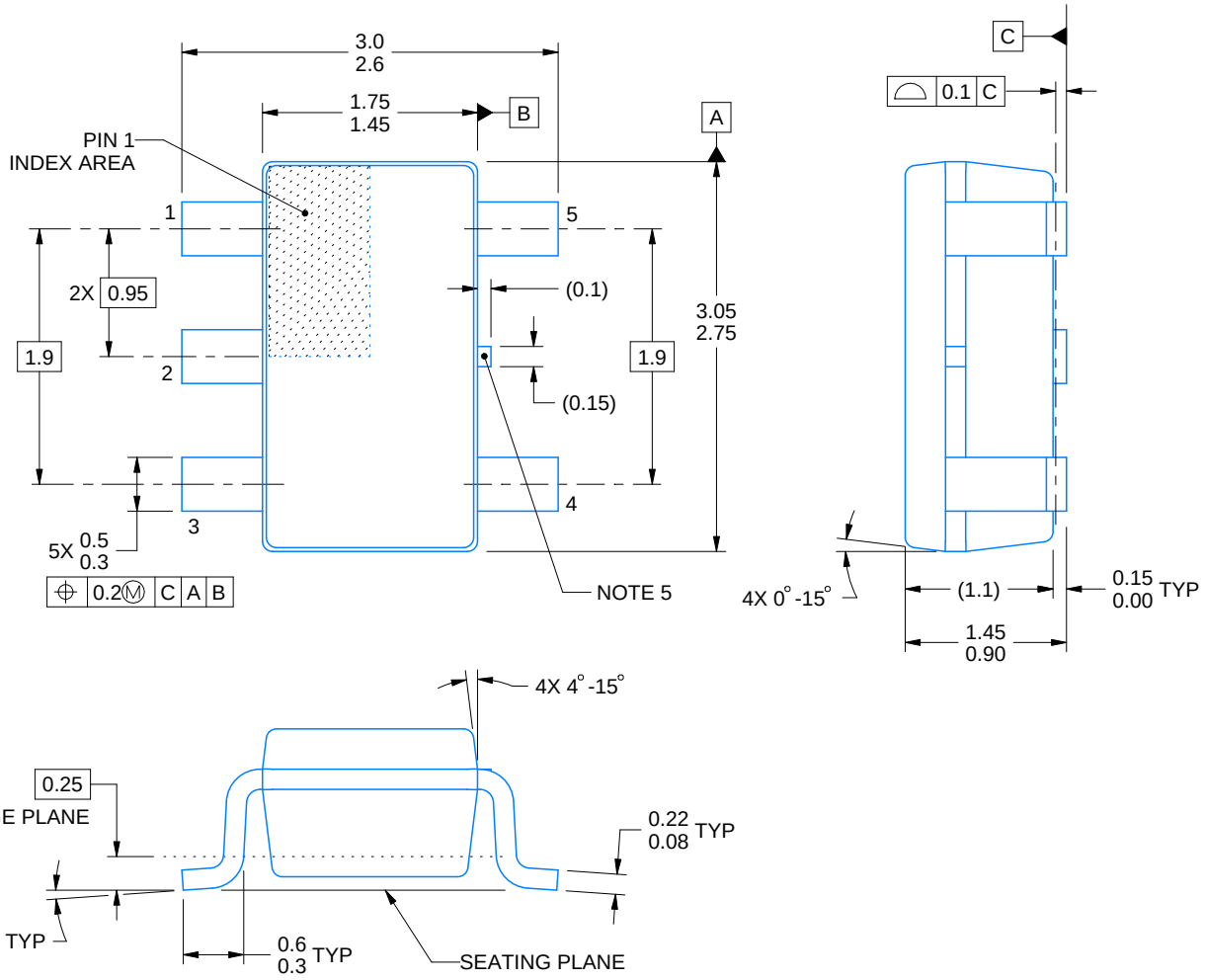
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

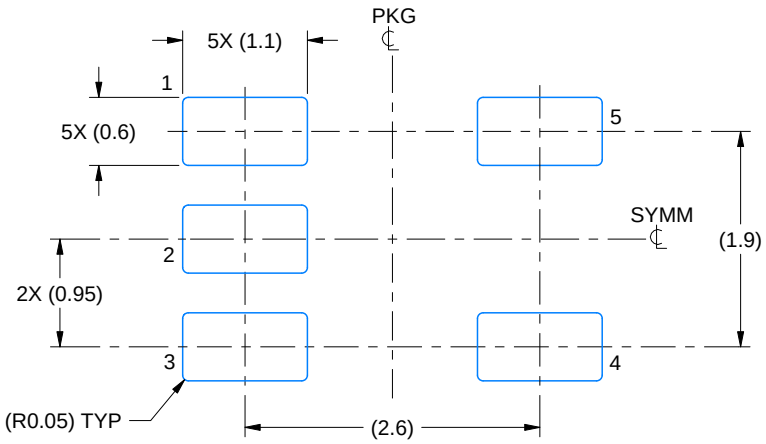
SMALL OUTLINE TRANSISTOR



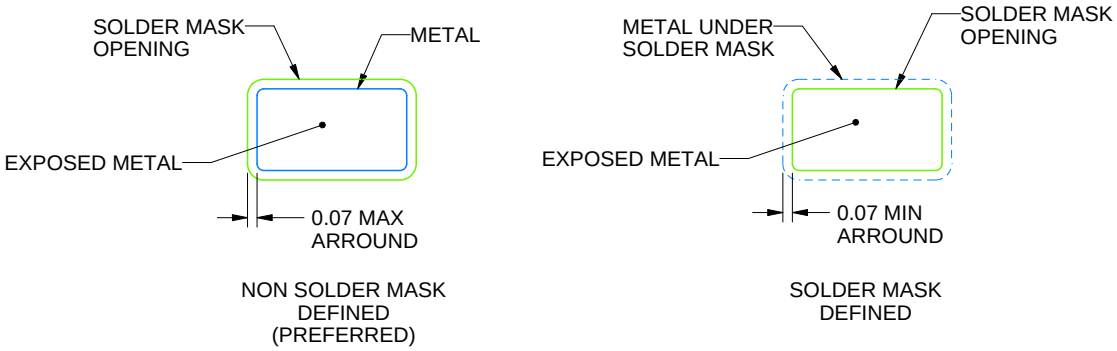

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

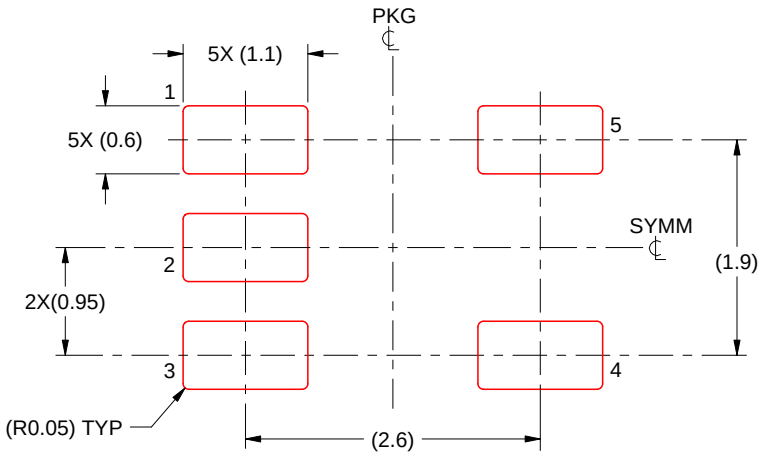



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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