SN74AHC1G00 单路 2 输入正与非门

1 特性

- 工作电压范围：2V 至 5.5V
- 5V 时 t_{pd} 最大值为 6.5ns
- 低功耗：最大 I_{CC} 为 10μA
- 5V 下的输出驱动为 ±8mA
- 所有输入端均采用施密特触发器，使得电路能够承受较慢的输入上升和下降时间
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 启用或禁用数字信号
- 控制指示灯 LED
- 通信模块和系统控制器之间的转换

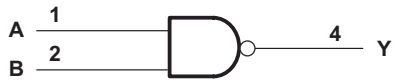
3 说明

SN74AHC1G00 以正逻辑执行布尔函数 $Y = \overline{A \cdot B}$ 或 $Y = \overline{A} + \overline{B}$。

封装信息

器件型号	封装(1)	封装尺寸(2)	封装尺寸(2)
SN74AHC1G00	DBV（SOT-23，5）	2.9mm x 2.8mm	2.9mm x 1.6mm
	DCK（SC-70，5）	2mm x 2.1mm	2mm x 1.25mm
	DRL (SOT, 5)	1.6mm x 1.6mm	1.6mm x 1.2mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

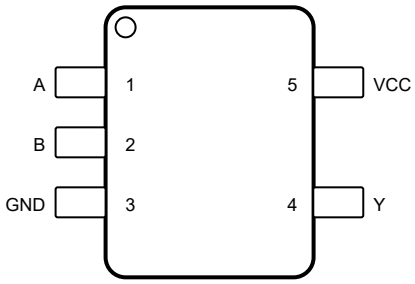


图 4-1. DBV Package 5-Pin SOT-23 Top View

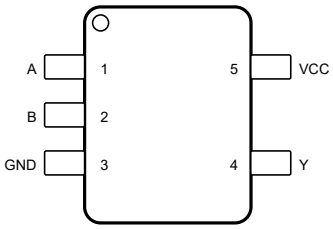


图 4-2. DCK Package 5-Pin SC70 Top View

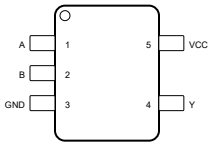


图 4-3. DRL Package 5-Pin SOT Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	A	I	A input
2	B	I	B input
3	GND	—	Ground
4	Y	O	Output
5	V_{CC}	—	Power

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I (2)	Input voltage		–0.5	7	V
V_O (2)	Output voltage		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0)		–20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	

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5.3 Recommended Operating Conditions（续）

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.4 Thermal Information

THERMAL METRIC(1)		SN74AHC1G00			UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	289.2	256	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.5	205.8	130	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	176.2	152	°C/W
ψ_{JT}	Junction-to-top characterization parameter	115.4	117.6	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	183.4	175.1	152	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –50 µA	T_A = 25°C	2 V	1.9	2		V
			T_A = –40°C to +85°C		1.9			
			T_A = –40°C to +125°C		1.9			
			T_A = 25°C	3 V	2.9	3		
			T_A = –40°C to +85°C		2.9			
			T_A = –40°C to +125°C		2.9			
			T_A = 25°C	4.5 V	4.4	4.5		
			T_A = –40°C to +85°C		4.4			
			T_A = –40°C to +125°C		4.4			
		I_{OH} = –4 mA	T_A = 25°C	3 V	2.58			
			T_A = –40°C to +85°C		2.48			
			T_A = –40°C to +125°C		2.48			
		I_{OH} = –8 mA	T_A = 25°C	4.5 V	3.94			
			T_A = –40°C to +85°C		3.8			
			T_A = –40°C to +125°C		3.8			

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5.5 Electrical Characteristics（续）

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	I_{OL} = 50 µA	T_A = 25°C	2 V			0.1	V
			T_A = –40°C to +85°C				0.1	
			T_A = –40°C to +125°C				0.1	
			T_A = 25°C	3 V			0.1	
			T_A = –40°C to +85°C				0.1	
			T_A = –40°C to +125°C				0.1	
			T_A = 25°C	4.5 V			0.1	
			T_A = –40°C to +85°C				0.1	
			T_A = –40°C to +125°C				0.1	
		I_{OL} = 4 mA	T_A = 25°C	3 V			0.36	
			T_A = –40°C to +85°C				0.44	
			T_A = –40°C to +125°C				0.44	
		I_{OL} = 8 mA	T_A = 25°C	4.5 V			0.36	
			T_A = –40°C to +85°C				0.44	
			T_A = –40°C to +125°C				0.44	
I_I	Input leakage current	V_I = 5.5 V or GND	T_A = 25°C	0 V to 5.5 V			±0.1	µA
			T_A = –40°C to +85°C				±1	
			T_A = –40°C to +125°C				±1	
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0	T_A = 25°C	5.5 V			1	µA
			T_A = –40°C to +85°C				10	
			T_A = –40°C to +125°C				10	
C_i	Input Capacitance	V_I = V_{CC} or GND	T_A = 25°C	5 V		2	10	pF
			T_A = –40°C to +85°C				10	
			T_A = –40°C to +125°C				10	

(1) Recommended T_A = –40°C to +125°C

5.6 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A [1]	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	C_L = 15 pF	25°C		5.5	7.9	ns
				–40°C to +85°C	1		9.5	
				–40°C to +125°C	1		10.5	
t_{PHL}				25°C		5.5	7.9	
				–40°C to +85°C	1		9.5	
				–40°C to +125°C	1		10.5	
t_{PLH}	A or B	Y	C_L = 50 pF	25°C		8	11.4	ns
				–40°C to +85°C	1		13	
				–40°C to +125°C	1		14	
t_{PHL}				25°C		8	11.4	
				–40°C to +85°C	1		13	
				–40°C to +125°C	1		14	

(1) Recommended T_A = –40°C to +125°C

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5.7 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A (1)	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	C_L = 15 pF	25°C		3.7	5.5	ns
				–40°C to +85°C	1		6.5	
				–40°C to +125°C	1		7	
t_{PHL}				25°C		3.7	5.5	
				–40°C to +85°C	1		6.5	
				–40°C to +125°C	1		7	
t_{PLH}	A or B	Y	C_L = 50 pF	25°C		5.2	7.5	ns
				–40°C to +85°C	1		6.5	
				–40°C to +125°C	1		9	
t_{PHL}				25°C		5.2	7.5	
				–40°C to +85°C	1		6.5	
				–40°C to +125°C	1		9	

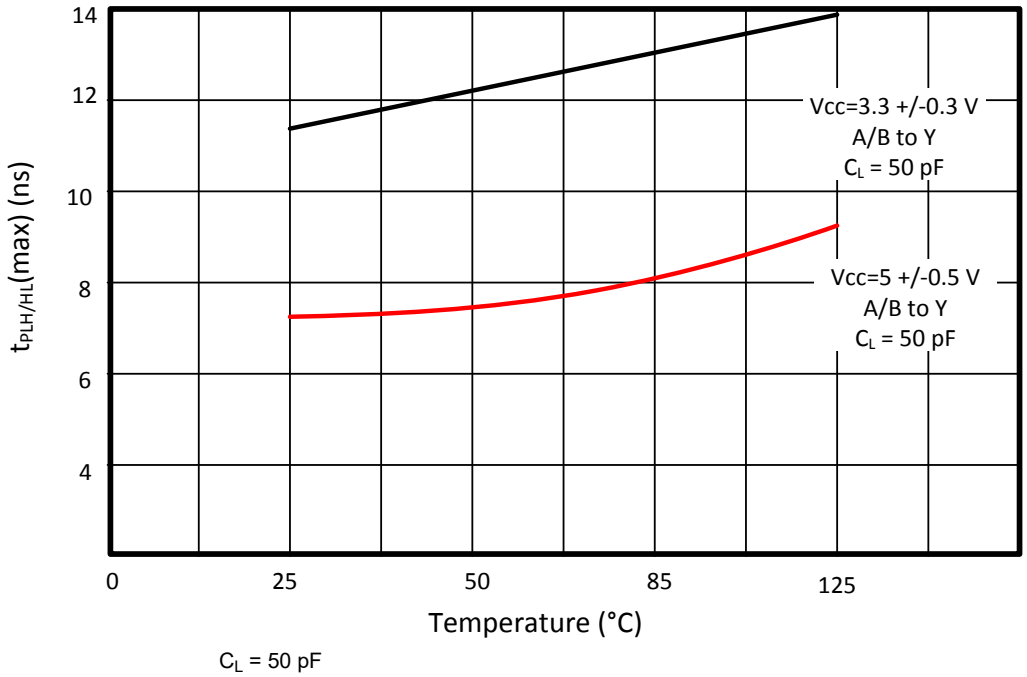
(1) Recommended T_A = –40°C to +125°C

5.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz		9.5		pF

5.9 Typical Characteristics

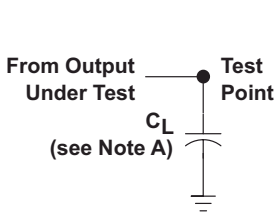


C_L = 50 pF

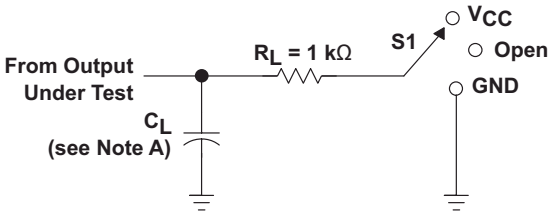
图 5-1. Propagation Delay vs Temperature

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6 Parameter Measurement information

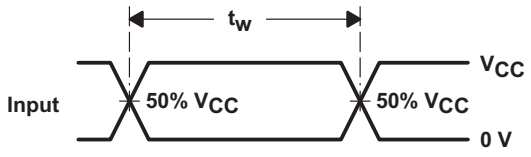


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

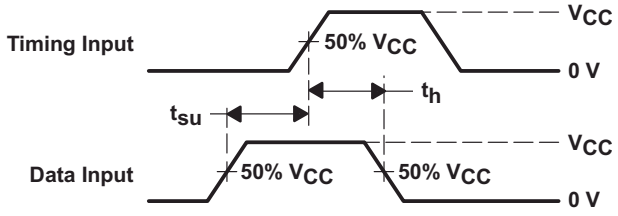


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

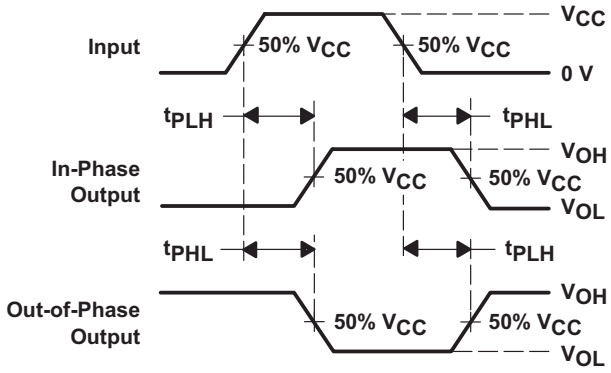
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



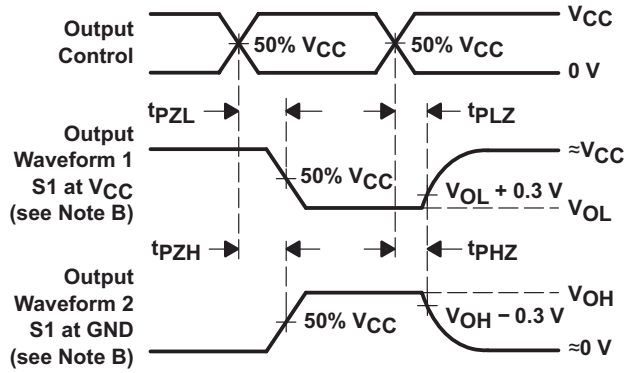
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

The SN74AHC1G00 device performs the NAND Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The device has a wide operating range of V_{CC} from 2 V to 5 V.

7.2 Functional Block Diagram



图 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

The SN74AHC1G00 device has wide operating voltage range for logic system from 2 V to 5 V. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low power consumption of 10-uA (maximum) makes this device a good choice for portable and battery power-sensitive applications. The Schmitt trigger action on all inputs have noise rejection capabilities.

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS(1)		OUTPUT(2)
A	B	Y
H	H	L
L	X	H
X	L	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

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8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Typical Application

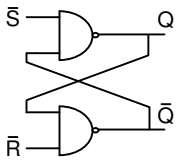


图 8-1. Typical Application

8.1.1 Design Requirements

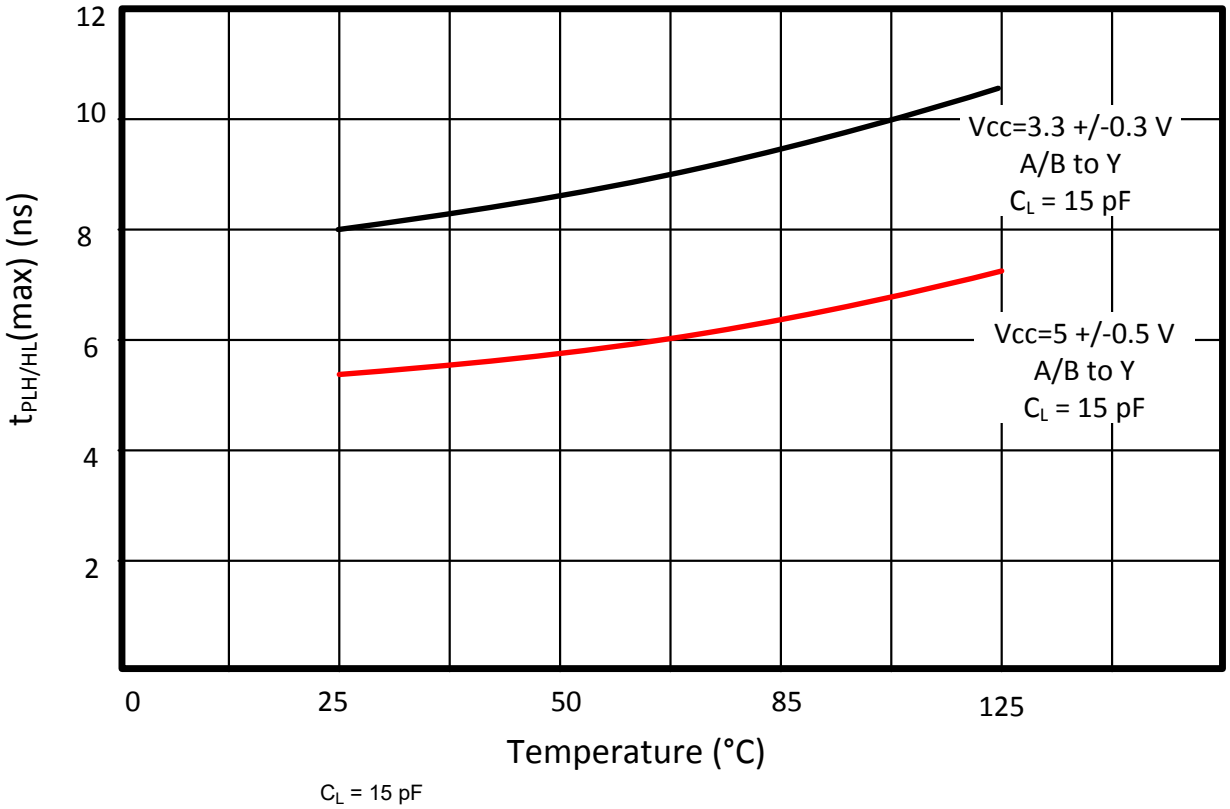
This SN74AHC1G00 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads. Routing and load conditions must be considered to prevent ringing.

8.1.2 Detailed Design Procedure

- Recommended input conditions:
  - Specified high and low levels. See V_{IH} and V_{IL} in *节 5.3*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- Recommended output conditions:
  - Load currents must not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

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8.1.3 Application Curve



C_L = 15 pF

图 8-2. Propagation Delay vs Temperature

8.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *节 5.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor; if there are multiple V_{CC} terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

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8.3 Layout

8.3.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float.

In many cases, functions or parts of functions of digital logic devices are unused. For example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The following are the rules must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the input and output, so they also cannot float when disabled.

8.3.2 Layout Example

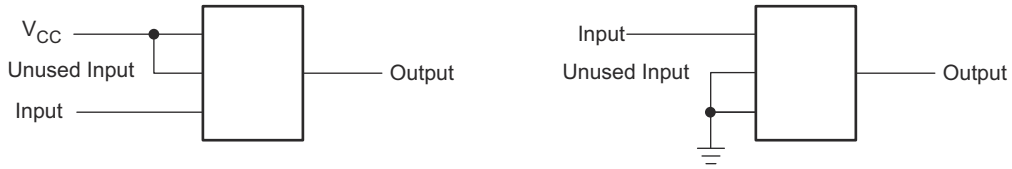


图 8-3. Layout Recommendation

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Introduction to Logic* application report
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*application note

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision P (October 2023) to Revision Q (January 2024)	Page
• Updated thermal values for DBV package from RθJA = 240 to 278, RθJC(top) = 174.5 to 180.5, RθJB = 73.7 to 184.4, ΨJT = 54.9 to 115.4, ΨJB = 60.1 to 183.4, RθJC(bot) = N/A, all values in °C/W	5

Changes from Revision O (April 2016) to Revision P (October 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated thermal values for DCK package from RθJA = 276.53 to 289.2, RθJC(top) = 118.5 to 205.8, RθJB = 62.8 to 176.2, ΨJT = 6.7 to 117.6, ΨJB = 62.1 to 175.1, RθJC(bot) = N/A, all values in °C/W	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC1G00DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(35XH, 3BSF, A003, A00G, A00J, A 00L, A00S)
SN74AHC1G00DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(35XH, 3BSF, A003, A00G, A00J, A 00L, A00S)
SN74AHC1G00DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A00G
SN74AHC1G00DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A00G
SN74AHC1G00DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	(A003, A00G, A00J, A00S)
SN74AHC1G00DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A00G
SN74AHC1G00DCK3	Obsolete	Production	SC70 (DCK) | 5	-	-	Call TI	Call TI	-40 to 125	AAY
SN74AHC1G00DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QP, AA3, AAG, AA J, AAL, AAS)
SN74AHC1G00DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1QP, AA3, AAG, AA J, AAL, AAS)
SN74AHC1G00DCKRE4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3
SN74AHC1G00DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3
SN74AHC1G00DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3
SN74AHC1G00DCKT	Obsolete	Production	SC70 (DCK) | 5	-	-	Call TI	Call TI	-40 to 125	(AA3, AAG, AAJ, AA S)
SN74AHC1G00DCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3
SN74AHC1G00DCKTG4.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3
SN74AHC1G00DRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(AAB, AAS)
SN74AHC1G00DRLR.A	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(AAB, AAS)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC1G00 :

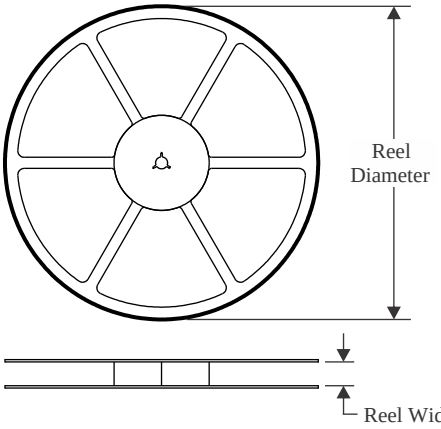
- Automotive : SN74AHC1G00-Q1

NOTE: Qualified Version Definitions:

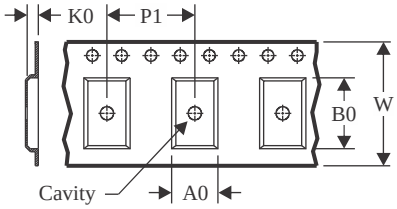
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

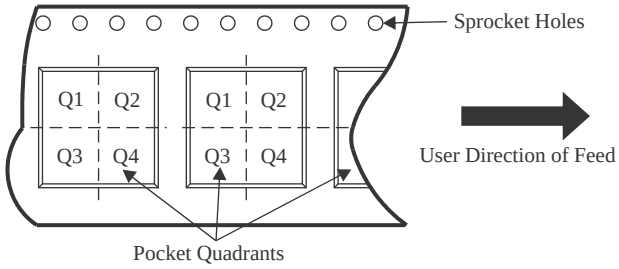


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

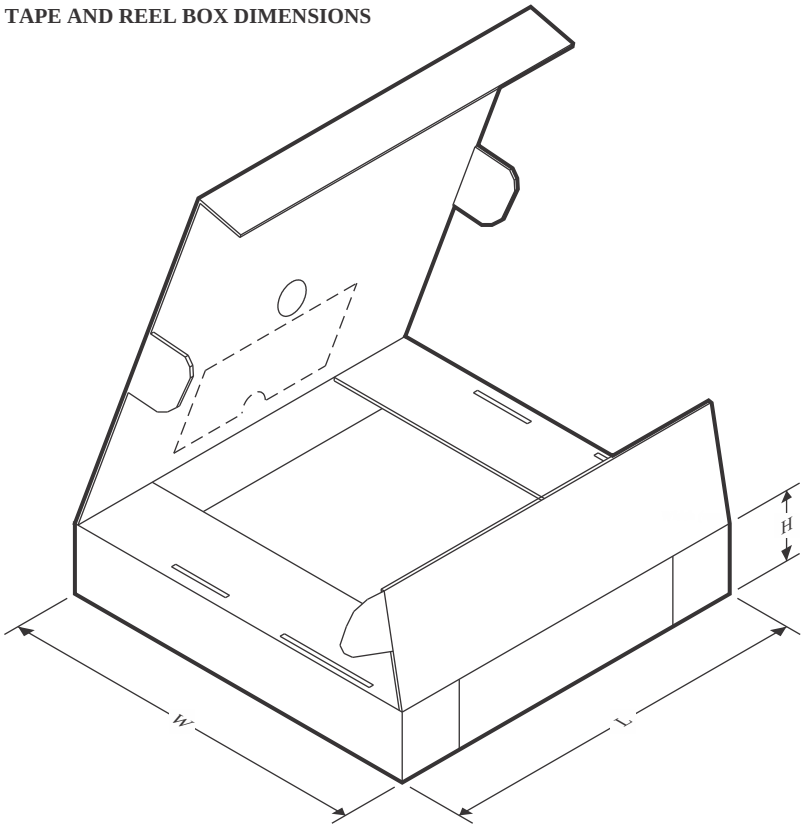
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G00DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHC1G00DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G00DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G00DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AHC1G00DRLR	SOT-5X3	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

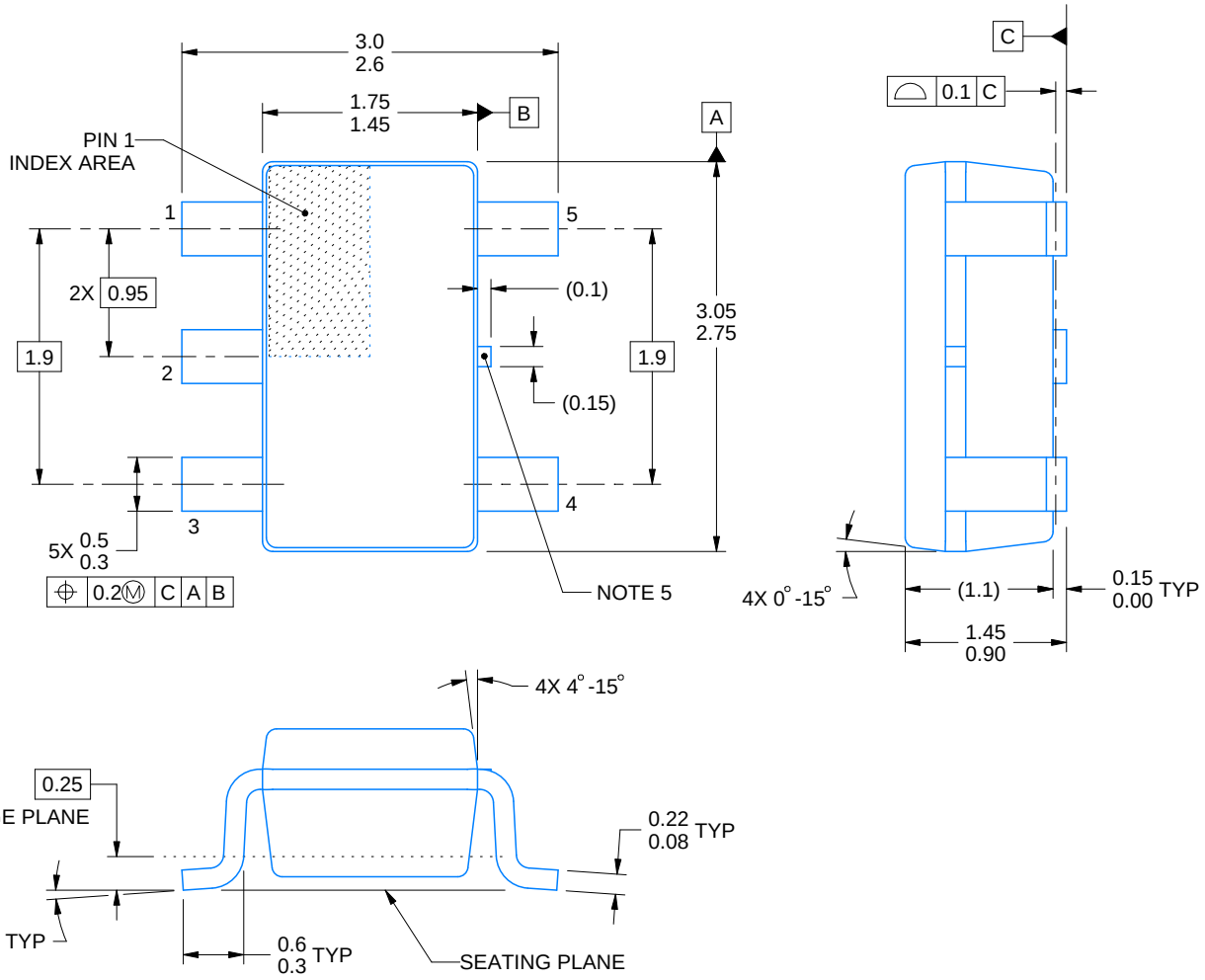
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHC1G00DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AHC1G00DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G00DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AHC1G00DRLR	SOT-5X3	DRL	5	4000	184.0	184.0	19.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

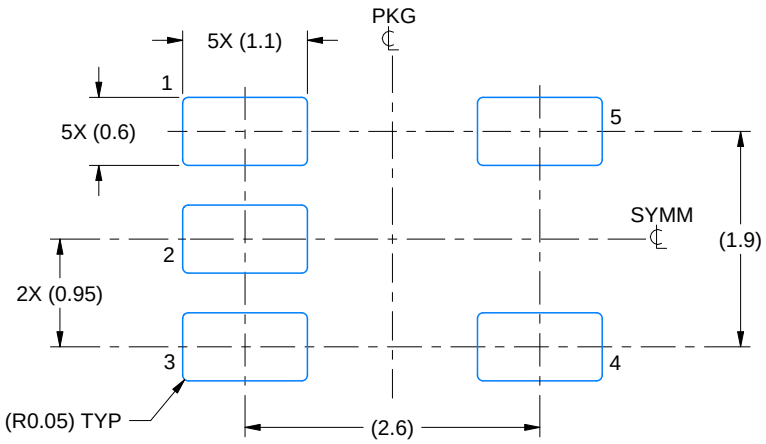
SMALL OUTLINE TRANSISTOR



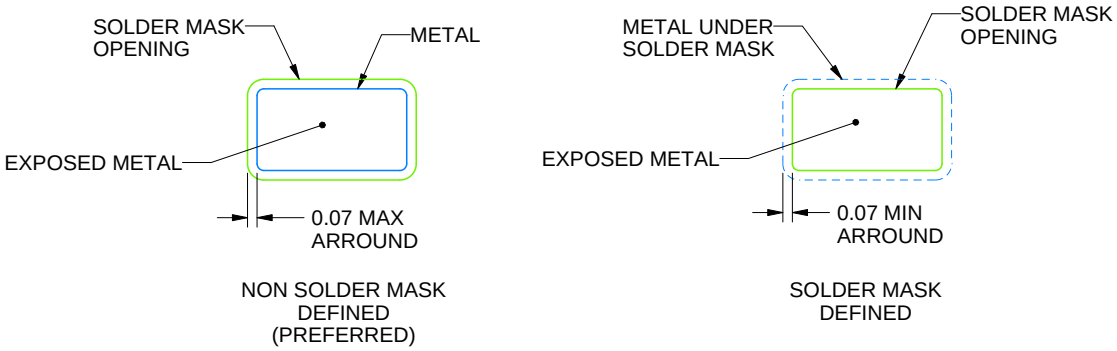
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

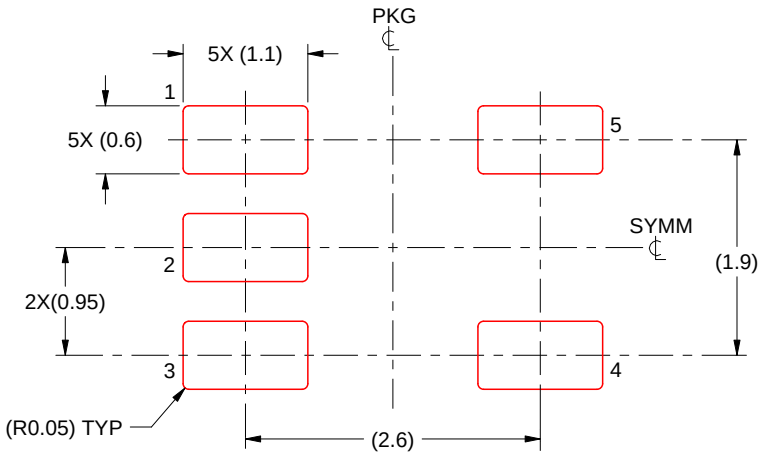


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

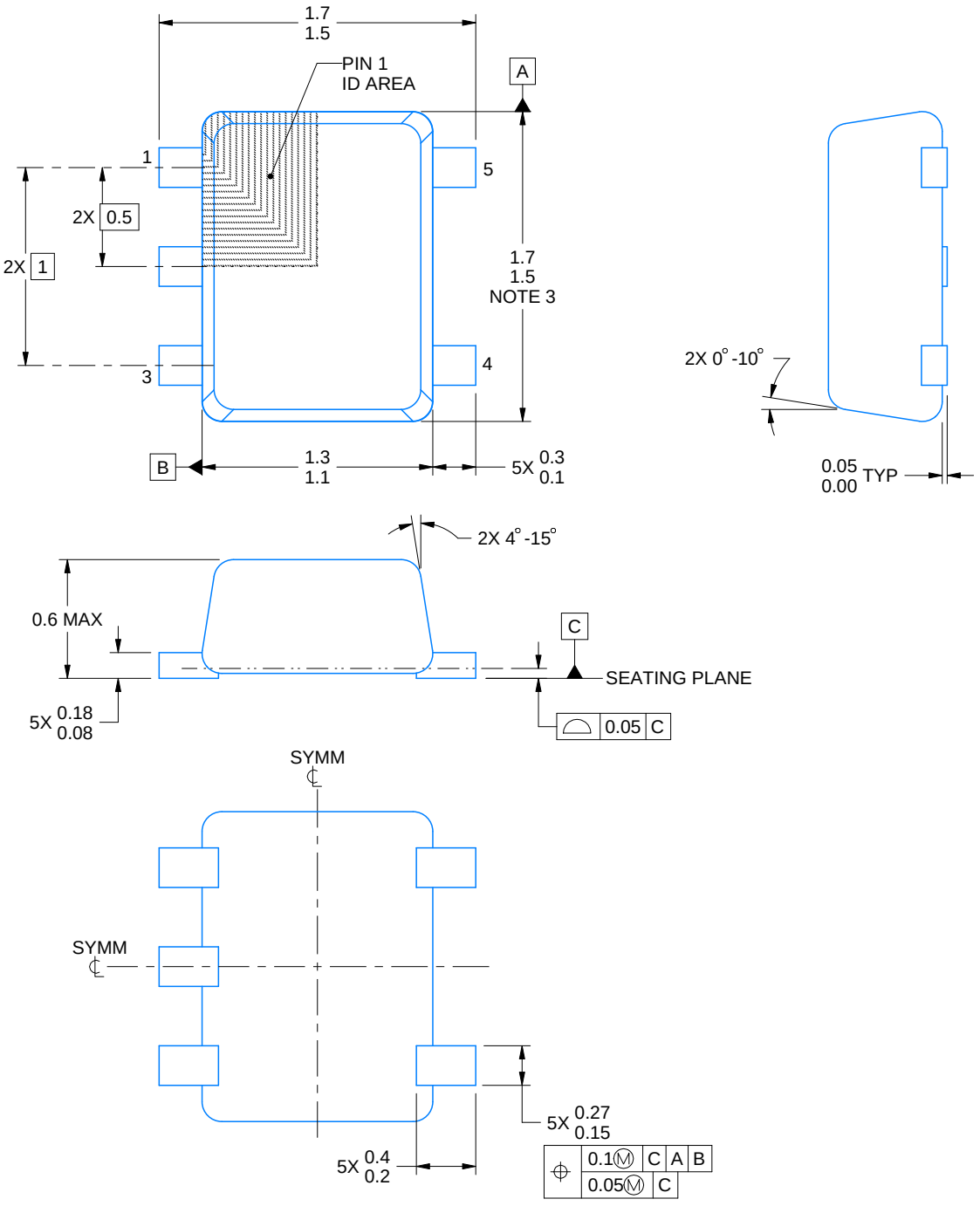
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

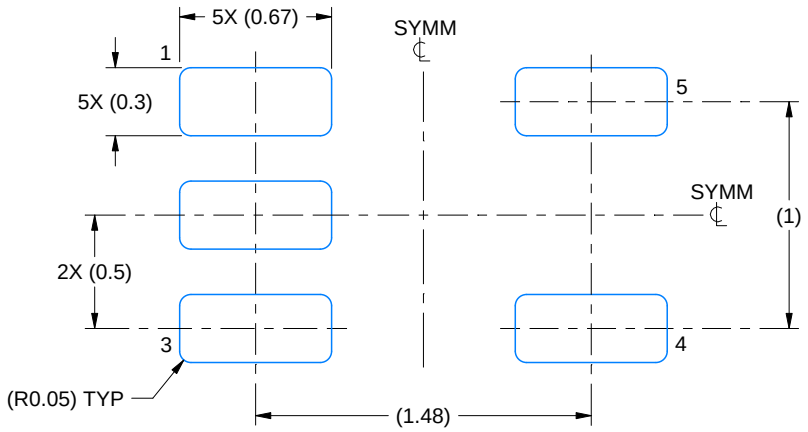
PLASTIC SMALL OUTLINE



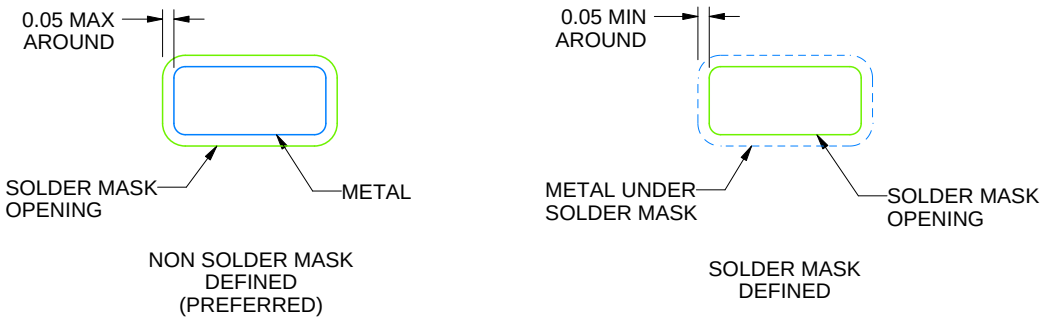
4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

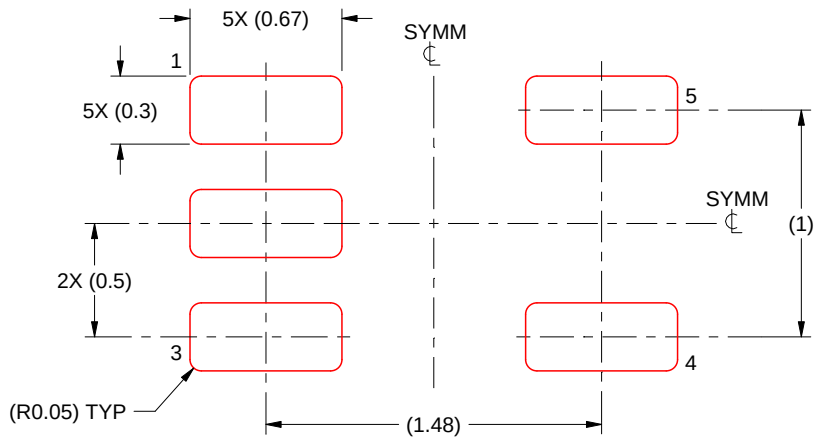


SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

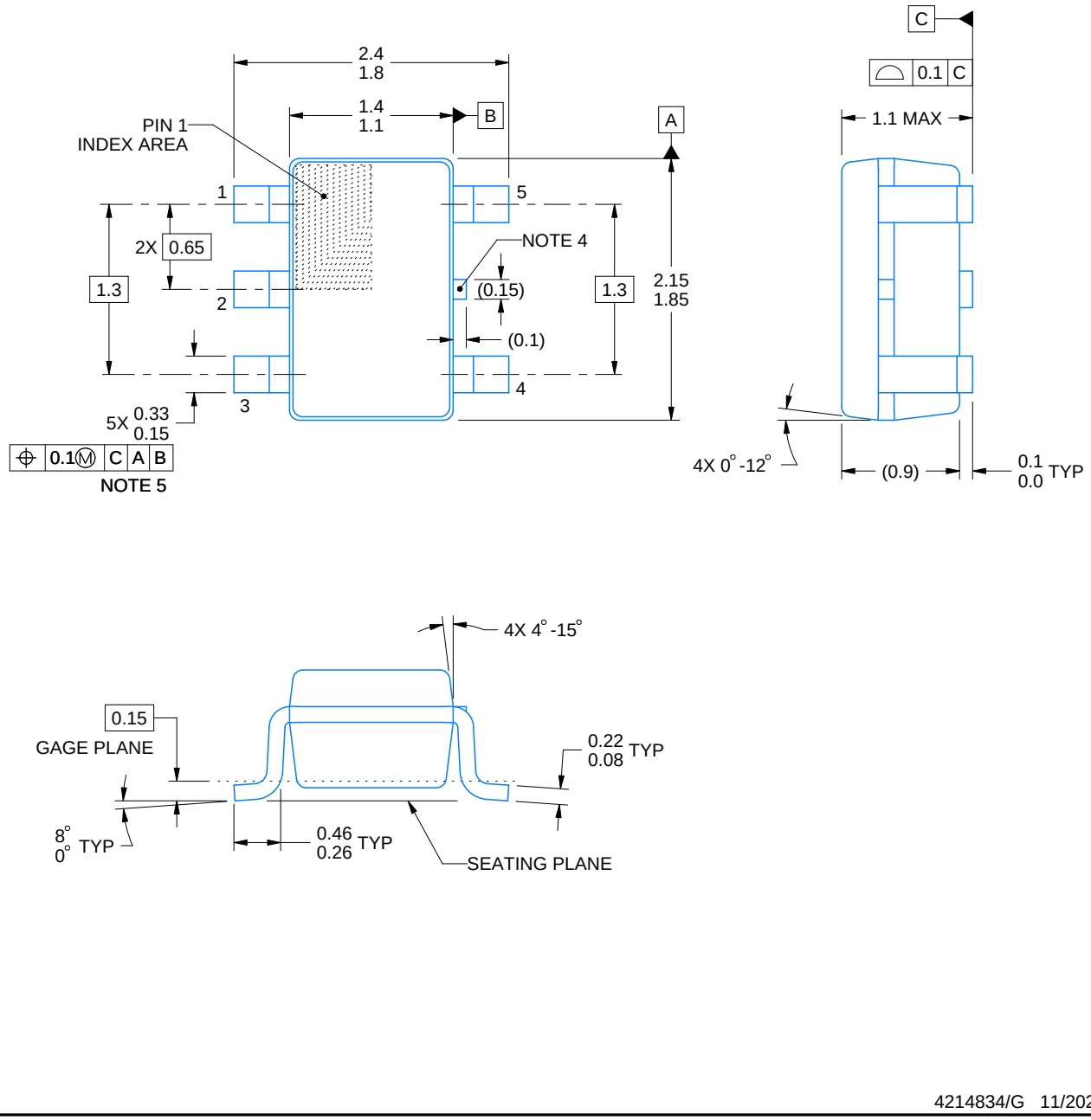
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

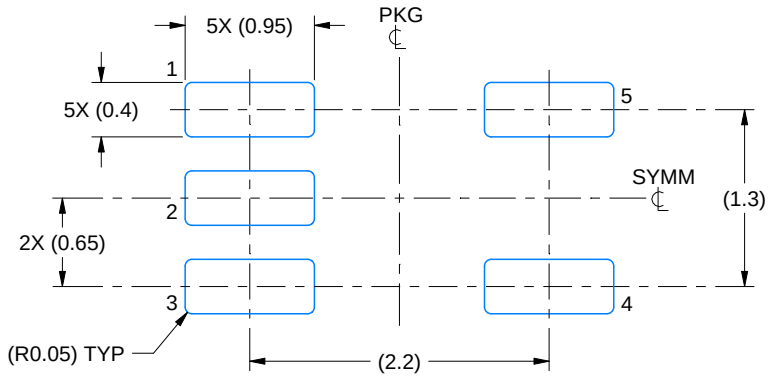
SMALL OUTLINE TRANSISTOR



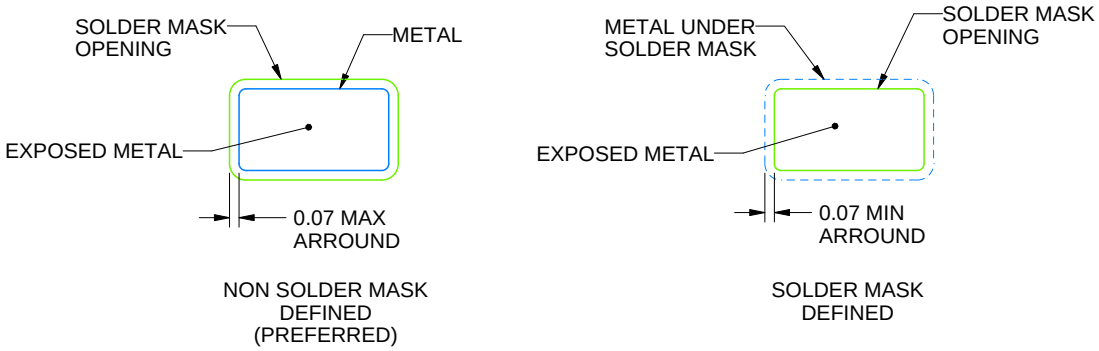
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

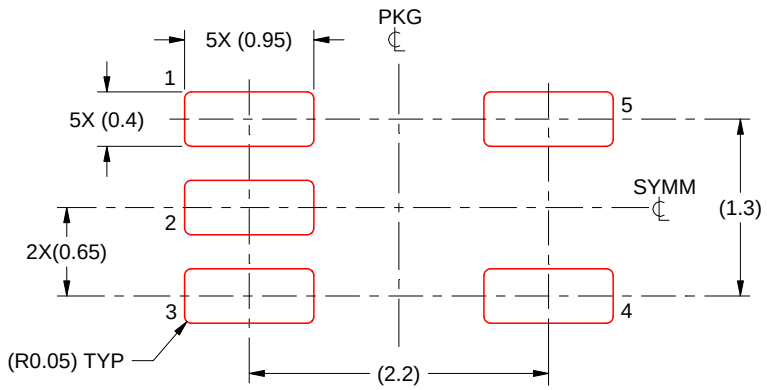


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月