

SN54ACT1284, SN74ACT1284 7-BIT BUS INTERFACES WITH 3-STATE OUTPUTS

SCAS459D – NOVEMBER 1994 – REVISED OCTOBER 2003

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 20 ns at 5 V
- 3-State Outputs Directly Drive Bus Lines
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
- Designed for the IEEE 1284-I (Level-1 Type) and IEEE 1284-II (Level-2 Type) Electrical Specifications

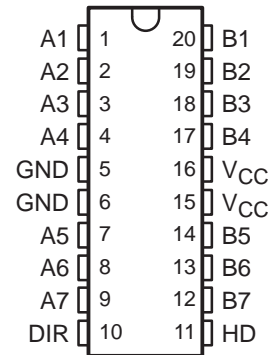
description/ordering information

The 'ACT1284 devices are designed for asynchronous two-way communication between data buses. The control function minimizes external timing requirements.

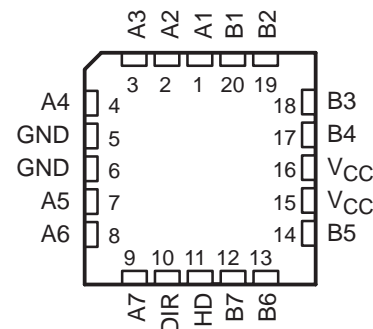
The devices allow data transmission in either the A-to-B or the B-to-A direction for bits 1, 2, 3, and 4, depending on the logic level at the direction-control (DIR) input. Bits 5, 6, and 7, however, always transmit in the A-to-B direction.

The output drive for each mode is determined by the high-drive (HD) control pin. When HD is high, the high drive is delivered by the totem-pole configuration, and when HD is low, the outputs are open drain. This meets the drive requirements as specified in the IEEE 1284-I (level-1 type) and the IEEE 1284-II (level-2 type) parallel peripheral-interface specification.

SN54ACT1284 . . . J OR W PACKAGE
SN74ACT1284 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT1284 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube	SN74ACT1284DW	ACT1284
		Tape and reel	SN74ACT1284DWR	
	SOP – NS	Tape and reel	SN74ACT1284NSR	ACT1284
	SSOP – DB	Tape and reel	SN74ACT1284DBR	AU284
–55°C to 125°C	TSSOP – PW	Tube	SN74ACT1284PW	AU284
		Tape and reel	SN74ACT1284PWR	
	CDIP – J	Tube	SNJ54ACT1284J	SNJ54ACT1284J
	CFP – W	Tube	SNJ54ACT1284W	SNJ54ACT1284W
	LCCC – FK	Tube	SNJ54ACT1284FK	SNJ54ACT1284FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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SN54ACT1284, SN74ACT1284

7-BIT BUS INTERFACES

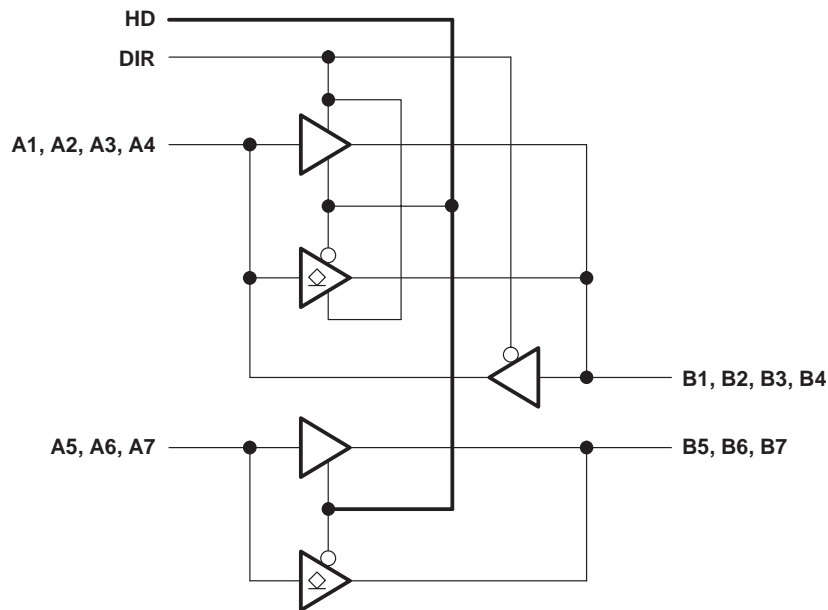
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A to B: Bits 5, 6, 7
		Totem pole	B to A: Bits 1, 2, 3, 4
L	H	Totem pole	B to A: Bits 1, 2, 3, 4 and A to B: Bits 5, 6, 7
H	L	Open drain	A to B: Bits 1, 2, 3, 4, 5, 6, 7
H	H	Totem pole	A to B: Bits 1, 2, 3, 4, 5, 6, 7

logic diagram (positive logic)



SN54ACT1284, SN74ACT1284 7-BIT BUS INTERFACES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
B-port input and output voltage range, V_I and V_O (see Notes 1 and 2)	–2 V to 7 V
A-port input and output voltage range, V_I and V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
DW package	58°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The ac input voltage pulse duration is limited to 20 ns if the input voltage goes more negative than –0.5 V.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		SN54ACT1284		SN74ACT1284		UNIT	
		MIN	MAX	MIN	MAX		
V_{CC}	Supply voltage	4.7	5.5	4.7	5.5	V	
V_{IH}	High-level input voltage	2		2		V	
V_{IL}	Low-level input voltage		0.8		0.8	V	
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V	
V_O	Open-drain output voltage	HD low	0	5.5	0	5.5	V
		B port, HD high		–14		–14	mA
I_{OH}	High-level output current	A port		–4		–4	
		B port		14		14	mA
I_{OL}	Low-level output current	A port		4		4	
		T_A	Operating free-air temperature	–55	125	0	70

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ACT1284, SN74ACT1284

7-BIT BUS INTERFACES

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} †	SN54ACT1284			SN74ACT1284			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{hys}	Input hysteresis	V _{IT+} – V _{IT-} for all inputs	5 V	0.4			0.4			V
			4.7 V	0.2			0.2			
V _{OH}	B port	I _{OH} = –14 mA	4.7 V	2.4			2.4			V
	A port	I _{OH} = –50 μA	MIN to MAX	V _{CC} –0.2			V _{CC} –0.2			
		I _{OH} = –4 mA	4.7 V	3.7			3.7			
V _{OL}	B port	I _{OL} = 14 mA	4.7 V				0.4			V
	A port	I _{OL} = 50 μA	4.7 V				0.2			
		I _{OL} = 4 mA					0.4			
I _I		V _I = V _{CC} or GND	5.5 V				±1			μA
I _{OZ}	A or B ports‡	V _O = V _{CC} or GND	5.5 V				±20			μA
I _{off}	B port	V _I or V _O ≤ 7 V	0 V				±100			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V				1.5			mA
C _i	Control inputs	V _I = V _{CC} or GND	5 V	4			4			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	5 V	12			12			pF
Z _O	B port	I _{OH} = –20 mA, I _{OH} = –50 mA	5 V	8	30		8	30		Ω

† For I/O ports, the parameter I_{OZ} includes the input leakage current I_I.

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

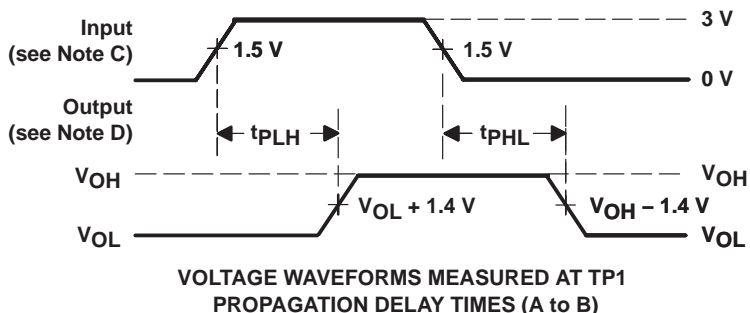
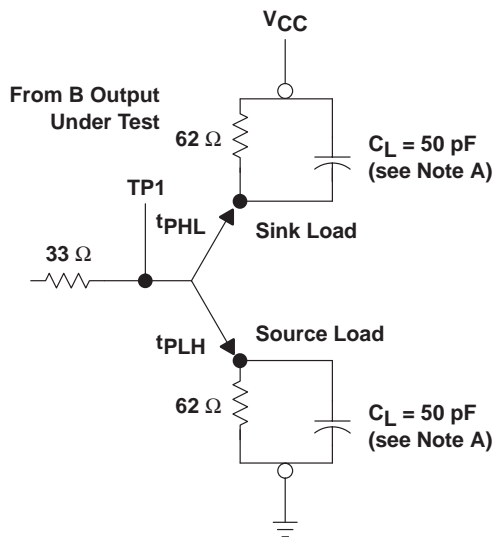
PARAMETER		FROM (INPUT)	TO (OUTPUT)	SN54ACT1284		SN74ACT1284		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	Totem pole	A or B	B or A	1	20	1	20	ns
t _{PHL}				1	20	1	20	
SR	Totem pole	B output		0.05	0.4	0.05	0.4	V/ns
t _{pd(EN)}	Totem pole	HD	B	1	20	1	20	ns
t _{pd(DIS)}				1	20	1	20	
t _r , t _f	Open drain	A	B	120		120		ns

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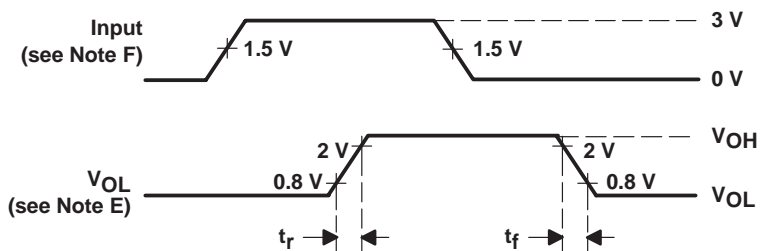
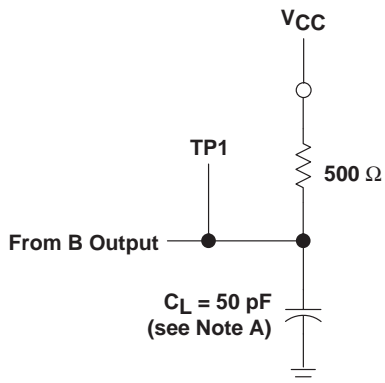


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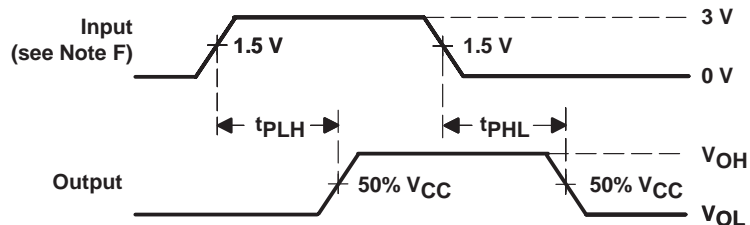
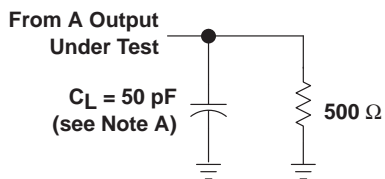
PARAMETER MEASUREMENT INFORMATION



A-TO-B LOAD (totem pole)



A-TO-B LOAD (open drain)



B-TO-A LOAD (totem pole)

- NOTES: A. C_L includes probe and jig capacitance.
 B. The outputs are measured one at a time with one transition per measurement.
 C. Input rise and fall times are 3 ns, $150 \text{ ns} < \text{pulse duration} < 10 \text{ } \mu\text{s}$ for both low-to-high and high-to-low transitions.
 D. Slew rate is defined as 10% and 90% of the transition times.
 E. Rise and fall times, open drain, are $< 120 \text{ ns}$.
 F. Input rise and fall times are 3 ns.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ACT1284DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AU284
SN74ACT1284DBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AU284
SN74ACT1284DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT1284
SN74ACT1284DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT1284
SN74ACT1284DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT1284
SN74ACT1284DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT1284
SN74ACT1284NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT1284
SN74ACT1284NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACT1284
SN74ACT1284PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AU284
SN74ACT1284PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AU284

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT1284DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ACT1284DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ACT1284NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ACT1284PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT1284DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ACT1284DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ACT1284NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ACT1284PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ACT1284DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ACT1284DW.A	DW	SOIC	20	25	507	12.83	5080	6.6

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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