

SN74AC573 具有三态输出的八路 D 型透明锁存器

1 特性

- V_{CC} 工作范围为 2V 至 6V
- 输入电压高达 6V
- 5V 时 t_{pd} 最大值为 9ns
- 三态输出直接驱动总线

2 应用

- 缓冲寄存器
- 双向总线驱动器
- 工作寄存器

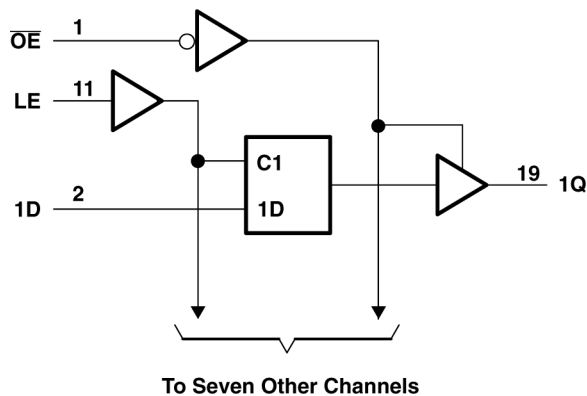
3 说明

这些 8 位锁存器具有专门设计用于驱动高电容或相对低阻抗负载的三态输出。这些器件特别适用于实现缓冲寄存器、I/O 端口、双向总线驱动器和工作寄存器。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SN74AC573	RKS (VQFN , 20)	4.5mm × 2.5mm	4.5mm × 2.5mm
	DB (SSOP , 20)	7.2mm × 7.8mm	7.2mm x 5.30mm
	DGV (TVSOP , 20)	5mm × 6.4mm	5mm × 4.4mm
	DW (SOIC , 20)	12.8mm × 10.3mm	12.80mm x 7.50mm
	NS (SOP , 20)	12.6mm × 7.8mm	12.6mm x 5.3mm
	N (PDIP , 20)	24.33mm × 9.4mm	24.33mm x 6.35mm
	PW (TSSOP , 20)	6.5mm × 6.4mm	6.50mm x 4.40mm

- (1) 如需更多信息, 请参阅节 11。
- (2) 封装尺寸 (长×宽) 为标称值, 并包括引脚 (如适用)。
- (3) 本体尺寸 (长×宽) 为标称值, 不包括引脚。



逻辑图 (正逻辑)

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4 引脚配置和功能

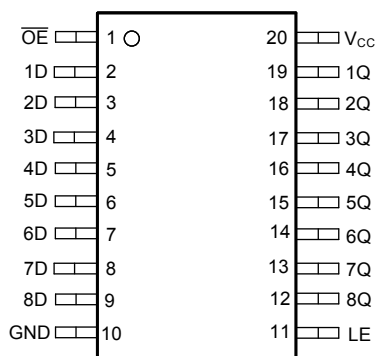


图 4-1. DB、DGV、DW、NS、N 或 PW 封装，20 引脚 SSOP、TVSOP、SOIC、SOP、PDIP 或 TSSOP (顶视图)

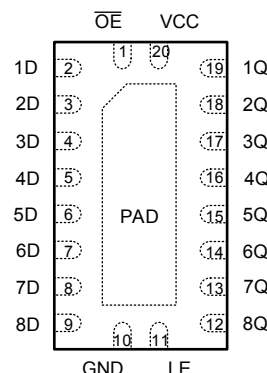


图 4-2. RKS 封装，20 引脚 VQFN (顶视图)

表 4-1. 引脚功能

引脚		类型 ⁽¹⁾	说明
名称	编号		
OE	1	I	输出使能测试点
1D	2	I	1D 输入
2D	3	I	2D 输入
3D	4	I	3D 输入
4D	5	I	4D 输入
5D	6	I	5D 输入
6D	7	I	6D 输入
7D	8	I	7D 输入
8D	9	I	8D 输入
GND	10	—	地
LE	11	I	锁存使能输入
8Q	12	O	8Q 输出
7Q	13	O	7Q 输出
6Q	14	O	6Q 输出
5Q	15	O	5Q 输出
4Q	16	O	4Q 输出
3Q	17	O	3Q 输出
2Q	18	O	2Q 输出
1Q	19	O	1Q 输出
V _{CC}	20	—	电源引脚
散热焊盘 ⁽²⁾		—	散热焊盘可连接到 GND 或悬空。请勿连接到任何其他信号或电源。

(1) I = 输入，O = 输出，I/O = 输入或输出，G = 接地，P = 电源。

(2) 仅限 RKS 封装。

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）⁽¹⁾

		最小值	最大值	单位
V_{CC}	电源电压范围	-0.5	+7	V
V_I ²	输入电压范围	-0.5	$V_{CC}+0.5$	V
V_O ²	输出电压范围	-0.5	$V_{CC}+0.5$	V
I_{IK}	输入钳位电流	($V_I < 0$ 或 $V_I > V_{CC}$)		±20 mA
I_{OK}	输出钳位电流	($V_O < 0$ 或 $V_O > V_{CC}$)		±20 mA
I_O	持续输出电流	($V_O = 0$ 至 V_{CC})		±50 mA
	通过 V_{CC} 或 GND 的持续电流			±200 mA
T_{stg}	贮存温度范围	-65	150	°C

- (1) 应力超出绝对最大额定值下列出的值可能会对器件造成损坏。这些仅为压力额定值，并不表示器件在这些条件下以及在建议的工作条件以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
- (2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

5.2 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）¹

		最小值	最大值	单位
V_{CC}	电源电压	2	6	V
V_{IH}	高电平输入电压	$V_{CC} = 3V$	2.1	V
		$V_{CC} = 4.5V$	3.15	
		$V_{CC} = 5.5V$	3.85	
V_{IL}	低电平输入电压	$V_{CC} = 3V$	0.9	V
		$V_{CC} = 4.5V$	1.35	
		$V_{CC} = 5.5V$	1.65	
V_I	输入电压	0	V_{CC}	V
V_O	输出电压	0	V_{CC}	V
I_{OH}	高电平输出电流	$V_{CC} = 3V$	-12	mA
		$V_{CC} = 4.5V$	-24	
		$V_{CC} = 5.5V$	-24	
I_{OL}	低电平输出电流	$V_{CC} = 3V$	12	mA
		$V_{CC} = 4.5V$	24	
		$V_{CC} = 5.5V$	24	
$\Delta t / \Delta v$	输入转换上升或下降速率		8	ns/V
T_A	自然通风工作温度	-40	85	°C

- (1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 **CMOS 输入缓慢变化或悬空的影响**，文献编号 SCBA004。

5.3 热性能信息

热指标	SN74AC573						单位
	DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RKS (VQFN)	
	20 引脚	20 引脚	20 引脚	20 引脚	20 引脚	20 引脚	
$R_{\theta JA}$ 结至环境热阻 ⁽¹⁾	101.2	70	69	60	126.2	68	°C/W

(1) 有关新旧热指标的更多信息，请参阅[半导体和 IC 封装热指标](#)应用报告。

5.4 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	$T_A = 25^{\circ}\text{C}$			SN74AC573		单位
			最小值	典型值	最大值	最小值	最大值	
V_{OH}	$I_{OH} = -50 \mu\text{A}$	3V	2.9			2.9		V
		4.5V	4.4			4.4		
		5.5V	5.4			5.4		
	$I_{OH} = -12 \text{ mA}$	3V	2.58			2.48		
		4.5V	3.94			3.8		
		5.5V	4.94			4.8		
	$I_{OH} = -75 \text{ mA}^{(1)}$	5.5V				3.85		
V_{OL}	$I_{OL} = 50 \mu\text{A}$	3V			0.1		0.1	V
		4.5V			0.1		0.1	
		5.5V			0.1		0.1	
	$I_{OL} = 12 \text{ mA}$	3V			0.36		0.44	
		4.5V			0.36		0.44	
		5.5V			0.36		0.44	
	$I_{OL} = 75 \text{ mA}$	5.5V					1.65	
I_I	$V_I = V_{CC}$ 或 GND	5.5V			± 0.1		± 1	μA
I_{OZ}	$V_O = V_{CC}$ 或 GND	5.5V			± 0.25		± 2.5	μA
I_{CC}	$V_I = V_{CC}$ 或 GND, $I_O = 0$	5.5V			4		40	μA
C_i	$V_I = V_{CC}$ 或 GND	5V		5				pF

(1) 一次不应测试超过一个输出，且测试持续时间不应超过 10ms。

5.5 时序要求， $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

在推荐的自然通风条件下的工作温度范围内测得， $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ （除非另有说明）（请参阅[负载电路和电压波形](#)）

		$T_A = 25^{\circ}\text{C}$		SN74AC573		单位
		最小值	最大值	最小值	最大值	
t_w	脉冲持续时间，LE 高电平	6		7		ns
t_{su}	设置时间，LE ↓ 前的数据	3.5		4		ns
t_h	保持时间，LE ↓ 后的数据	2		2		ns

5.6 时序要求, $V_{CC} = 5V \pm 0.5V$

在推荐的自然通风条件下的工作温度范围内测得, $V_{CC} = 5V \pm 0.5V$ (除非另有说明) (请参阅[负载电路和电压波形](#))

		$T_A = 25^\circ\text{C}$		SN74AC573		单位
		最小值	最大值	最小值	最大值	
t_w	脉冲持续时间, LE 高电平	4		5		ns
t_{su}	设置时间, LE ↓ 前的数据	3		3.5		ns
t_h	保持时间, LE ↓ 后的数据	2		2		ns

5.7 开关特性, $V_{CC} = 3V \pm 0.3V$

在推荐的自然通风条件下的工作温度范围内测得, $V_{CC} = 3V \pm 0.3V$ (除非另有说明) (请参阅[负载电路和电压波形](#))

参数	从 (输入)	至 (输出)	$T_A = 25^\circ\text{C}$		SN74AC573		单位
			最小值	最大值	最小值	最大值	
t_{PLH}	D	Q	2.5	13	2	15	ns
t_{PHL}			2.5	12	2	14	
t_{PLH}	LE	Q)	2.5	13	2	15	ns
t_{PHL}			2.5	12	2	14	
t_{PZH}	$\overline{OE}$	Q)	2.5	11	2	12	ns
t_{PZL}			2.5	11	2	12.5	
t_{PHZ}	$\overline{OE}$	Q)	2.5	12.5	2	13.5	ns
t_{PLZ}			2.5	9.5	2	10.5	

5.8 开关特性, $V_{CC} = 5V \pm 0.5V$

在推荐的自然通风条件下的工作温度范围内测得, $V_{CC} = 5V \pm 0.5V$ (除非另有说明) (请参阅[负载电路和电压波形](#))

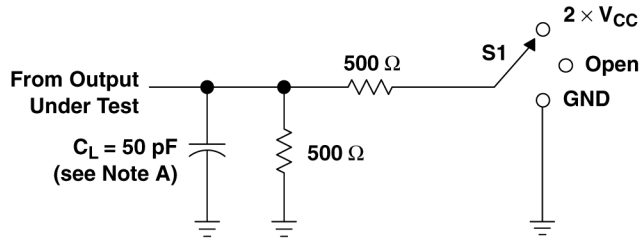
参数	从 (输入)	至 (输出)	$T_A = 25^\circ\text{C}$		SN74AC573		单位
			最小值	最大值	最小值	最大值	
t_{PLH}	D	Q	2.5	10	2	11.5	ns
t_{PHL}			2.5	9.5	2	11	
t_{PLH}	LE	Q)	2.5	9.5	2	11	ns
t_{PHL}			2.5	8.5	2	10	
t_{PZH}	$\overline{OE}$	Q)	2.5	9	2	10	ns
t_{PZL}			2.5	8.5	2	9.5	
t_{PHZ}	$\overline{OE}$	Q)	2.5	11	2	12	ns
t_{PLZ}			2.5	8	2	9	

5.9 工作特性

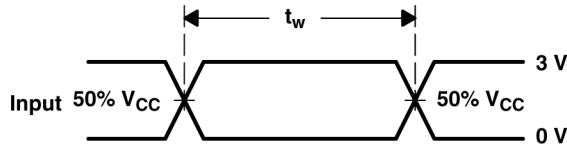
$V_{CC} = 5V$, $T_A = 25^\circ\text{C}$

参数	测试条件	典型值	单位
C_{pd} 功率耗散电容	$C_L = 50\text{pF}$, $f = 1\text{MHz}$	25	pF

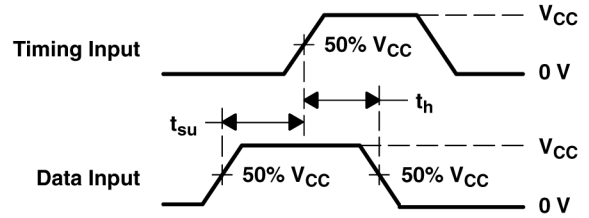
6 参数测量信息



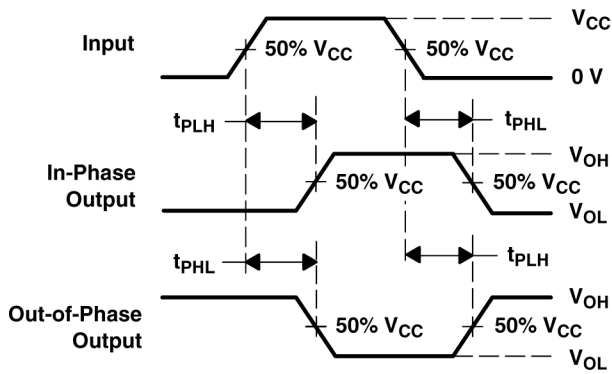
LOAD CIRCUIT



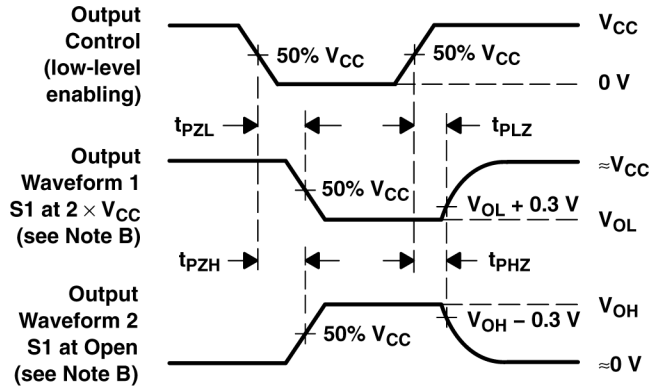
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- A. C_L 包括探头和夹具电容。
- B. 波形 1 用于具有内部条件的输出，使得输出为低电平，除非被输出控制禁用。波形 2 用于具有内部条件的输出，使得输出为高电平，除非被输出控制禁用。
- C. 所有输入脉冲由具有以下特性的发生器提供： $PRR \leq 1\text{MHz}$ ， $Z_O = 50\ \Omega$ ， $t_r \leq 2.5\text{ns}$ ， $t_f \leq 2.5\text{ns}$ 。
- D. 一次测量一个输出，每次测量一个输入转换。

图 6-1. 负载电路和电压波形

表 6-1.

测试	S1
t_{PLH}/t_{PHL}	开路
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	开路

7 详细说明

7.1 概述

这 8 个锁存器均是 D 型透明锁存器。在锁存器使能 (LE) 输入为高电平时，Q 输出将跟随数据 (D) 输入。当 LE 为低电平时，Q 输出锁存在 D 输入端设置的逻辑电平。

缓冲输出使能 ($\overline{OE}$) 输入可用于将八个输出置于正常逻辑状态 (高或低逻辑电平) 或高阻抗状态。在高阻抗状态下，输出既不对总线施加大量负载，也不显著驱动总线。高阻抗状态和增加的驱动在无需接口或上拉元件的情况下提供了驱动总线组织式系统中总线的能力。

$\overline{OE}$ 不影响锁存器的内部运行。当输出处于高阻抗状态时，可以保留旧数据或输入新数据。

7.2 功能方框图

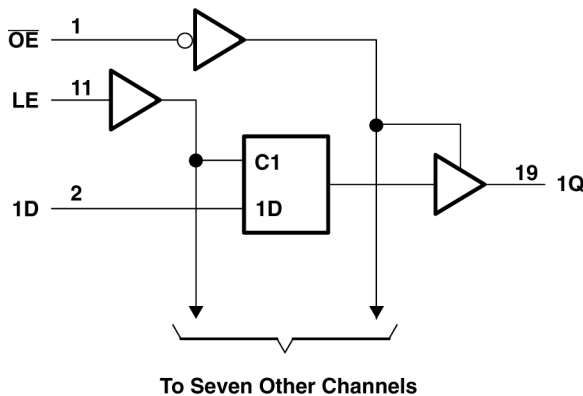


图 7-1. 逻辑图 (正逻辑)

7.3 器件功能模式

表 7-1. 功能表 (每个锁存器)

输入 ⁽¹⁾			输出 ⁽²⁾ Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

- (1) H = 高电压电平, L = 低电压电平, X = 高或低电压电平
 (2) H = 驱动高电平, L = 驱动低电平, Q₀ = 驱动先前的高电平或低电平状态, Z = 高阻抗

8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 电源相关建议

电源可以是 5.2 表中最小和最大电源电压额定值之间的任何电压。根据 5.1 表，通过地或 V_{CC} 的总电流不得超过 $\pm 70\text{mA}$ 。

每个 V_{CC} 引脚必须具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，TI 建议使用 $0.1\mu\text{F}$ 电容器；如果有多个 V_{CC} 引脚，则 TI 建议为每个电源引脚使用 $0.01\mu\text{F}$ 或 $0.022\mu\text{F}$ 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。 $0.1\mu\text{F}$ 和 $1\mu\text{F}$ 电容器通常并联使用。为了获得更佳效果，旁路电容器必须尽可能靠近电源引脚安装。

8.2 布局

8.2.1 布局指南

当使用多位逻辑器件时，输入决不能悬空。

在许多情况下，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时，未使用数字逻辑器件的功能或部分功能。此类输入引脚不得悬空，因为外部连接处的未定义电压会导致未定义的运行状态。布局图指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。必须应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，它们会连接到 GND 或 V_{CC} ，具体取决于哪种更合理或更方便。除非器件是收发器，否则允许输出悬空。如果收发器有一个输出使能引脚，它会在置为有效时禁用该器件的输出部分。这不会禁用 I/O 的输入部分，因此它们在禁用后不能悬空。

8.2.2 布局示例

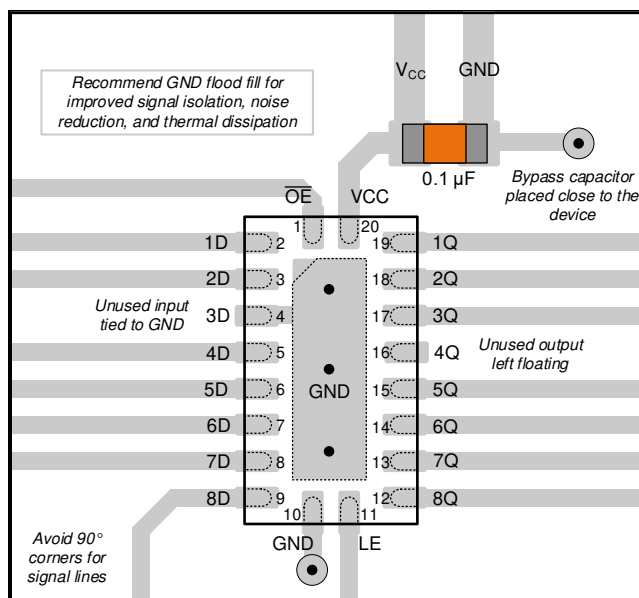


图 8-1. SN74AC573 的布局示例

9 器件和文档支持

TI 提供大量的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

9.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.3 商标

TI E2E™ is a trademark of Texas Instruments.

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9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (November 2023) to Revision H (February 2024)	Page
• 向 封装信息 表中添加了本体尺寸.....	1
• 更新了 $R_{\theta JA}$ 值：DW = 58 至 101.2，PW = 83 至 126.2，所有值均以 °C/W 为单位.....	5
• 添加了 应用和实施 部分.....	9

Changes from Revision F (June 2023) to Revision G (November 2023)	Page
• 更新了 封装信息 表以包含封装引线尺寸.....	1
• 添加了 RKS 封装信息.....	1

11 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AC573DBR	NRND	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573DBR.A	NRND	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573DBRG4	NRND	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	AC573
SN74AC573DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573
SN74AC573DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573
SN74AC573DWRG4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC573N
SN74AC573N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC573N
SN74AC573NSR	NRND	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573NSR.A	NRND	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	AC573
SN74AC573PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573
SN74AC573PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573
SN74AC573PWRE4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573RKSR	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC573
SN74AC573RKSR.A	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC573

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AC573 :

- Automotive : [SN74AC573-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC573DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC573DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AC573DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC573NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AC573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AC573RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC573DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AC573DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AC573DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AC573NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AC573PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AC573RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



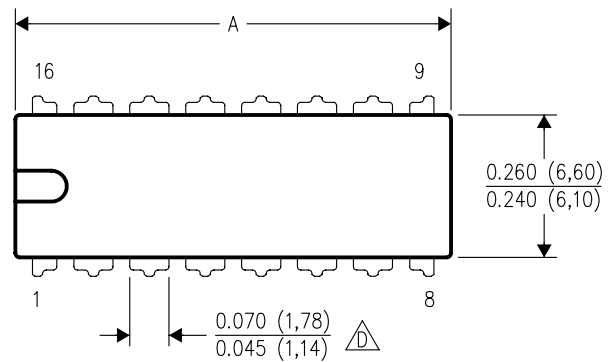
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AC573N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AC573N.A	N	PDIP	20	20	506	13.97	11230	4.32

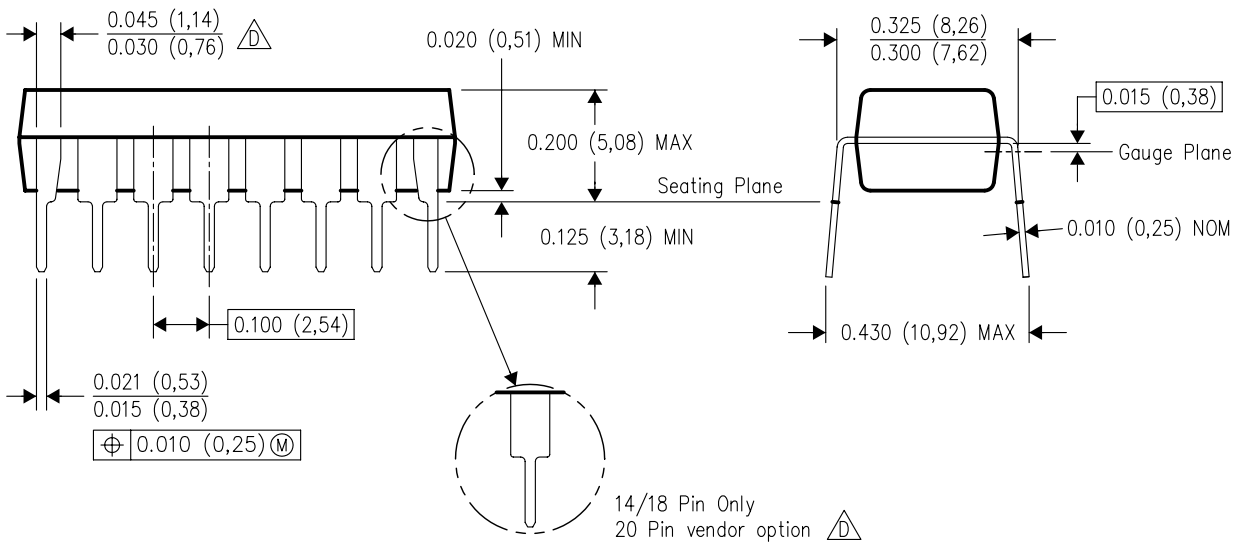
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



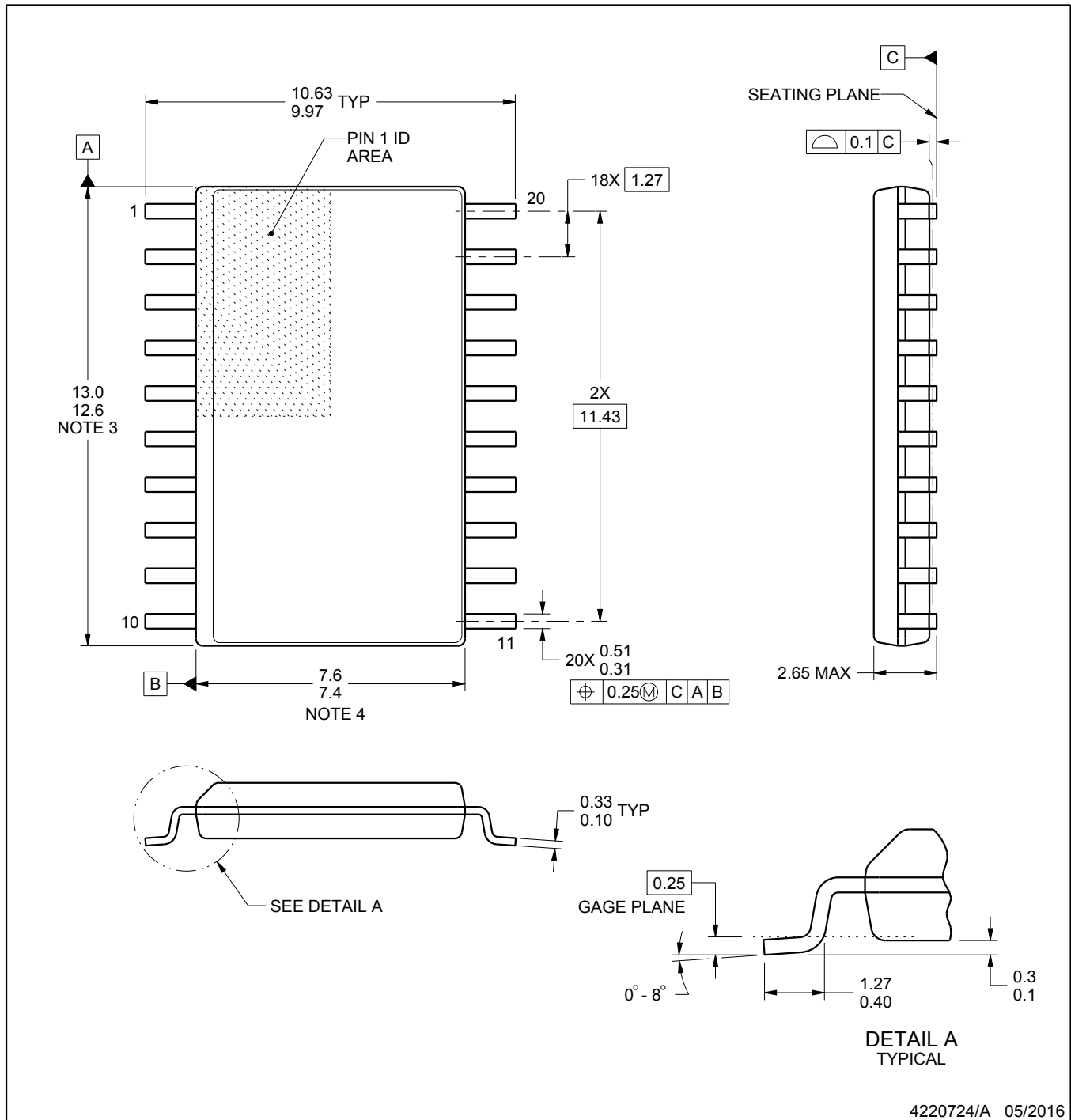
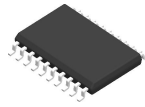
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

NOTES:

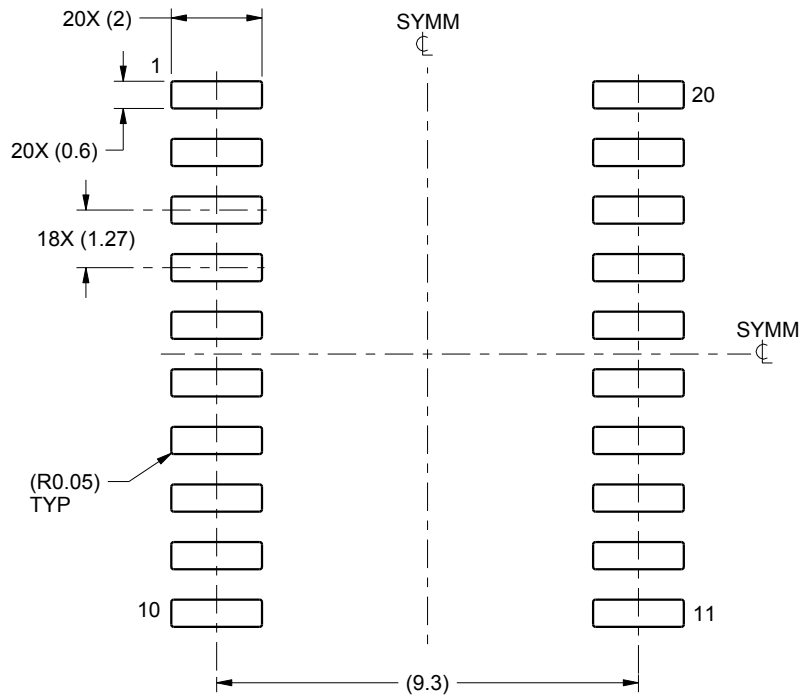
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

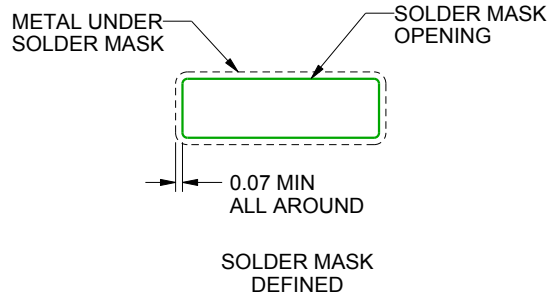
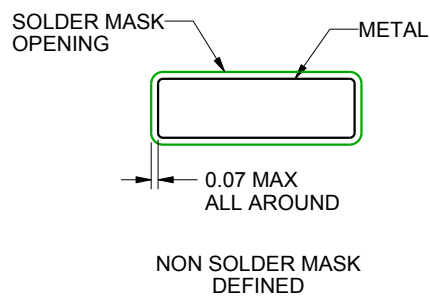
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

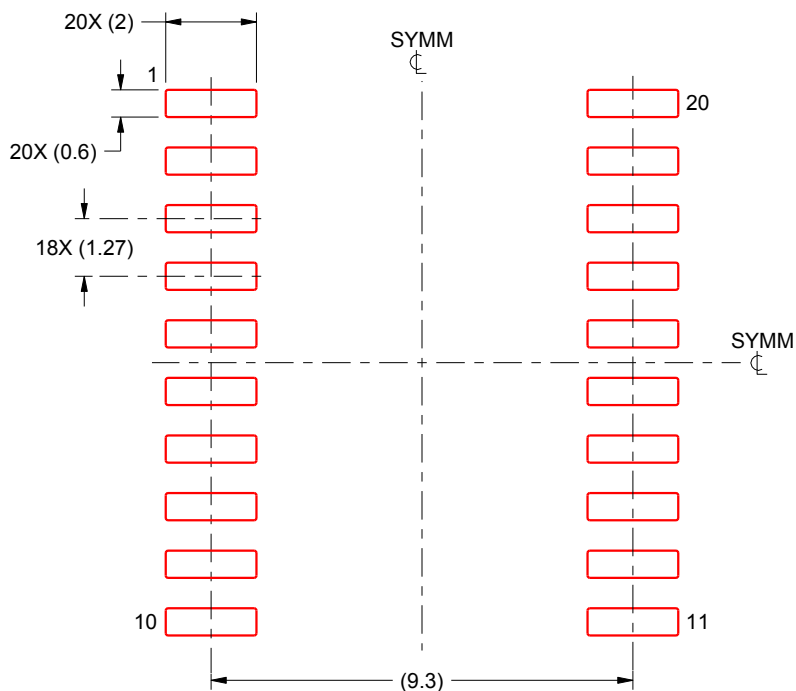
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

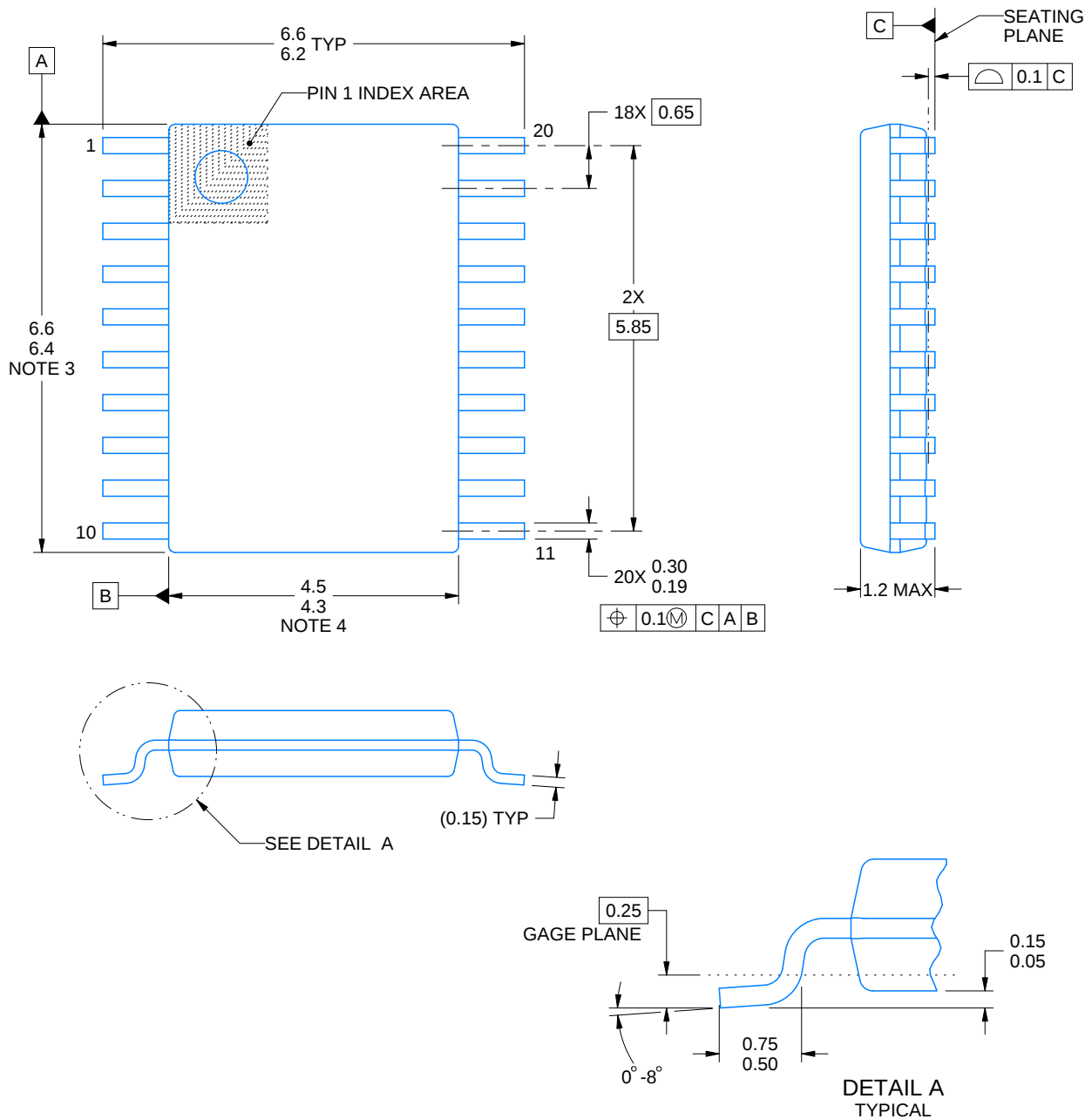
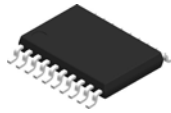


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

NOTES:

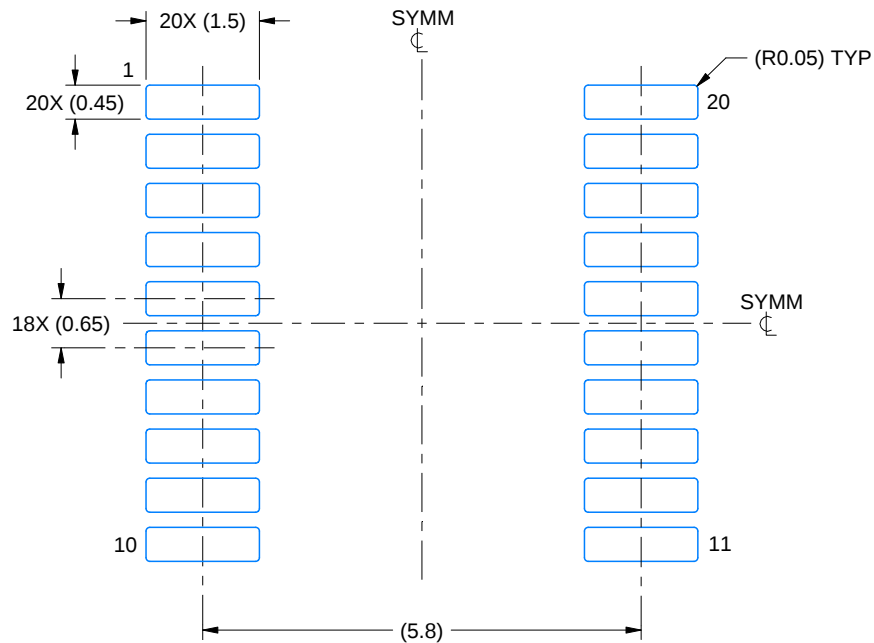
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

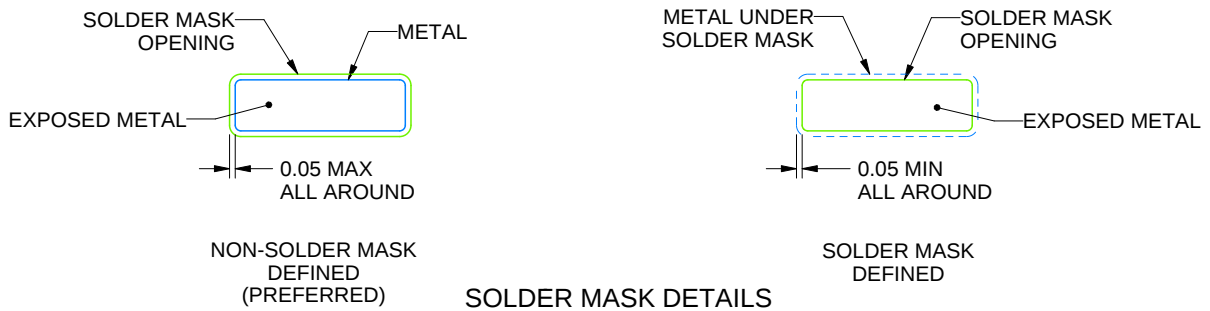
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

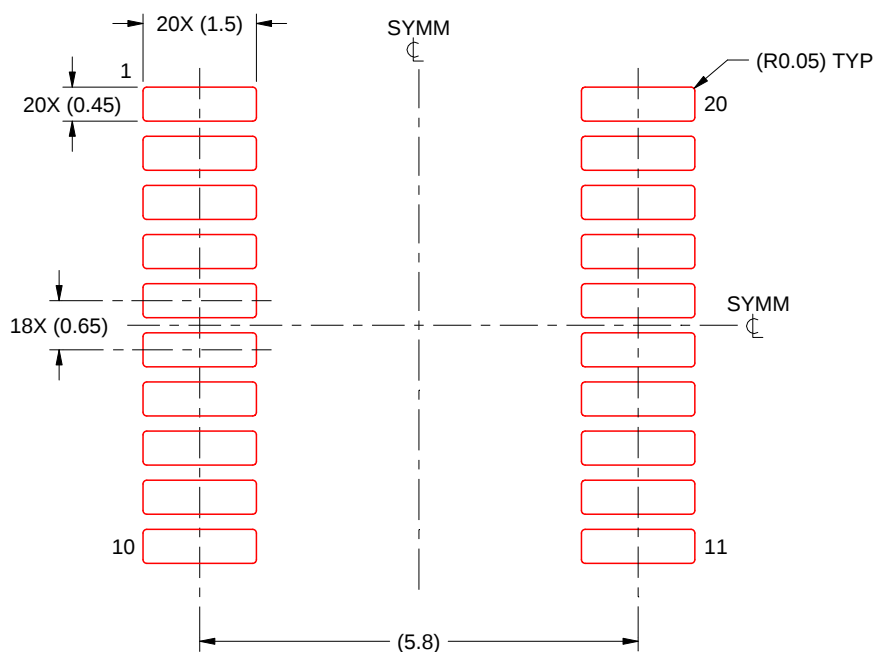
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

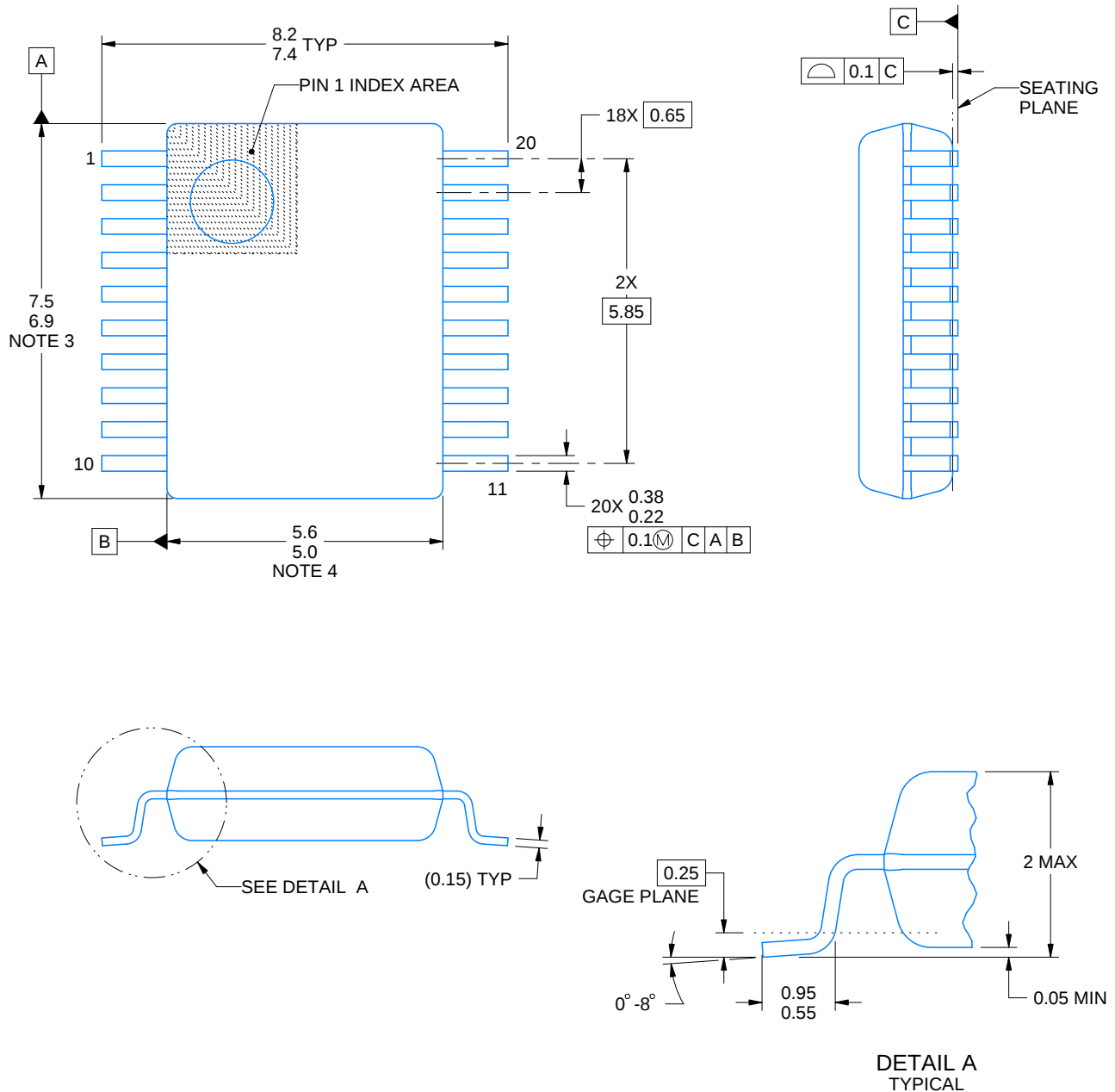
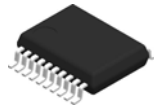


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

NOTES:

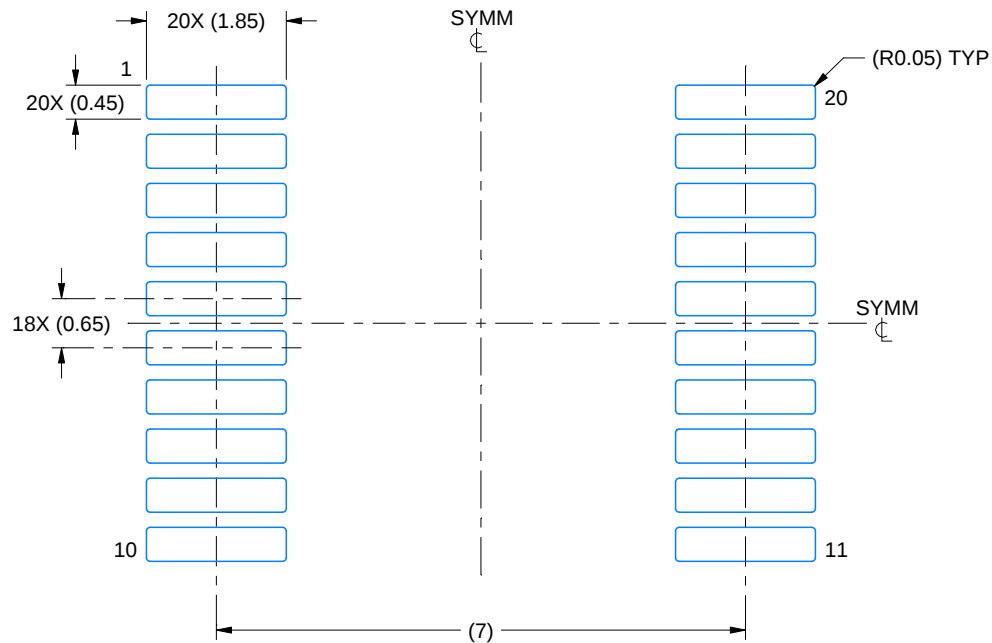
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

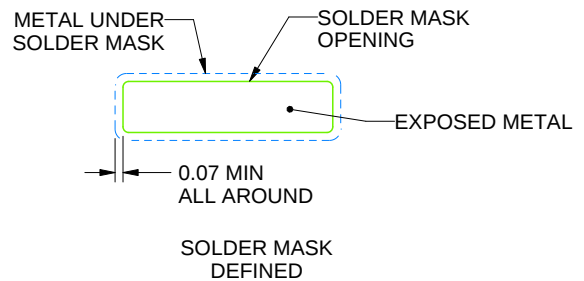
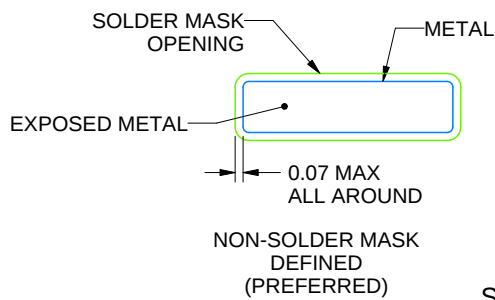
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

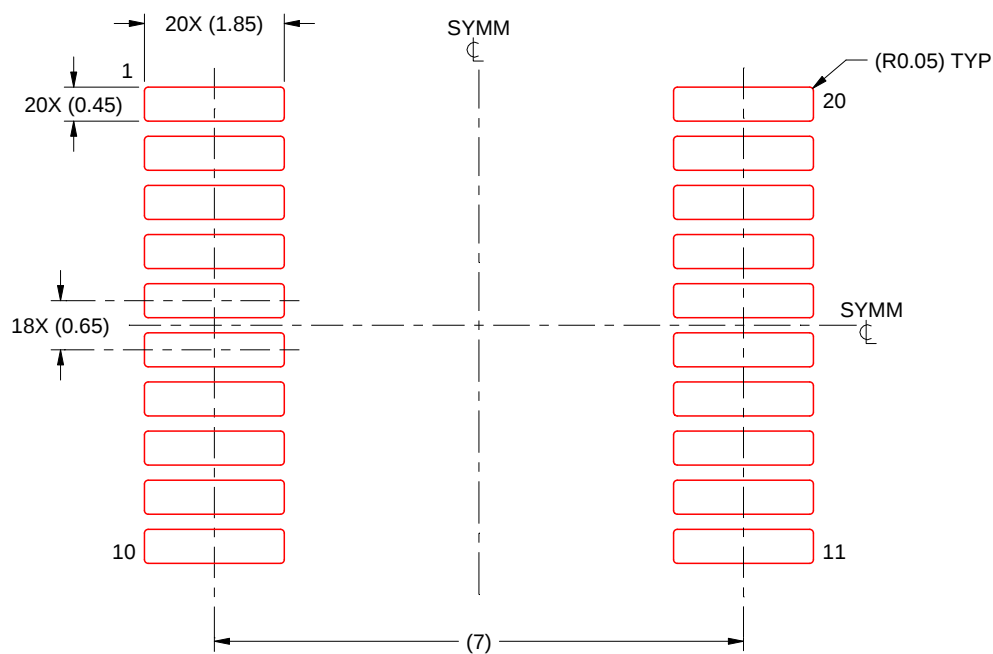
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

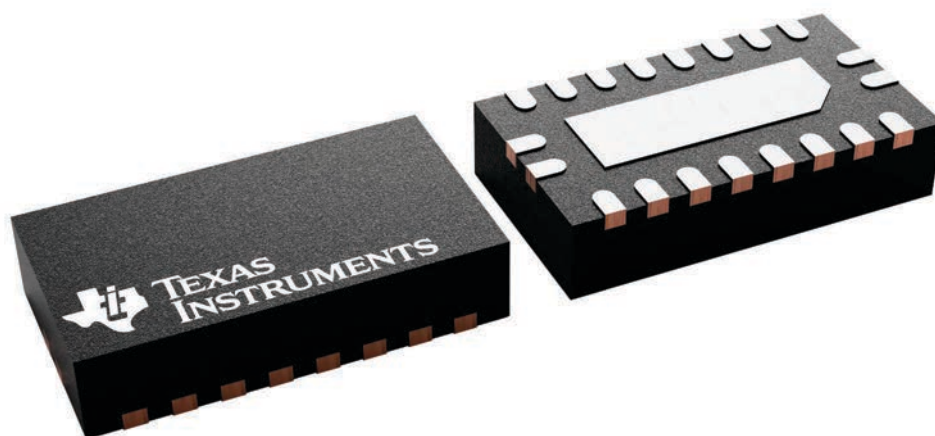
RKS 20

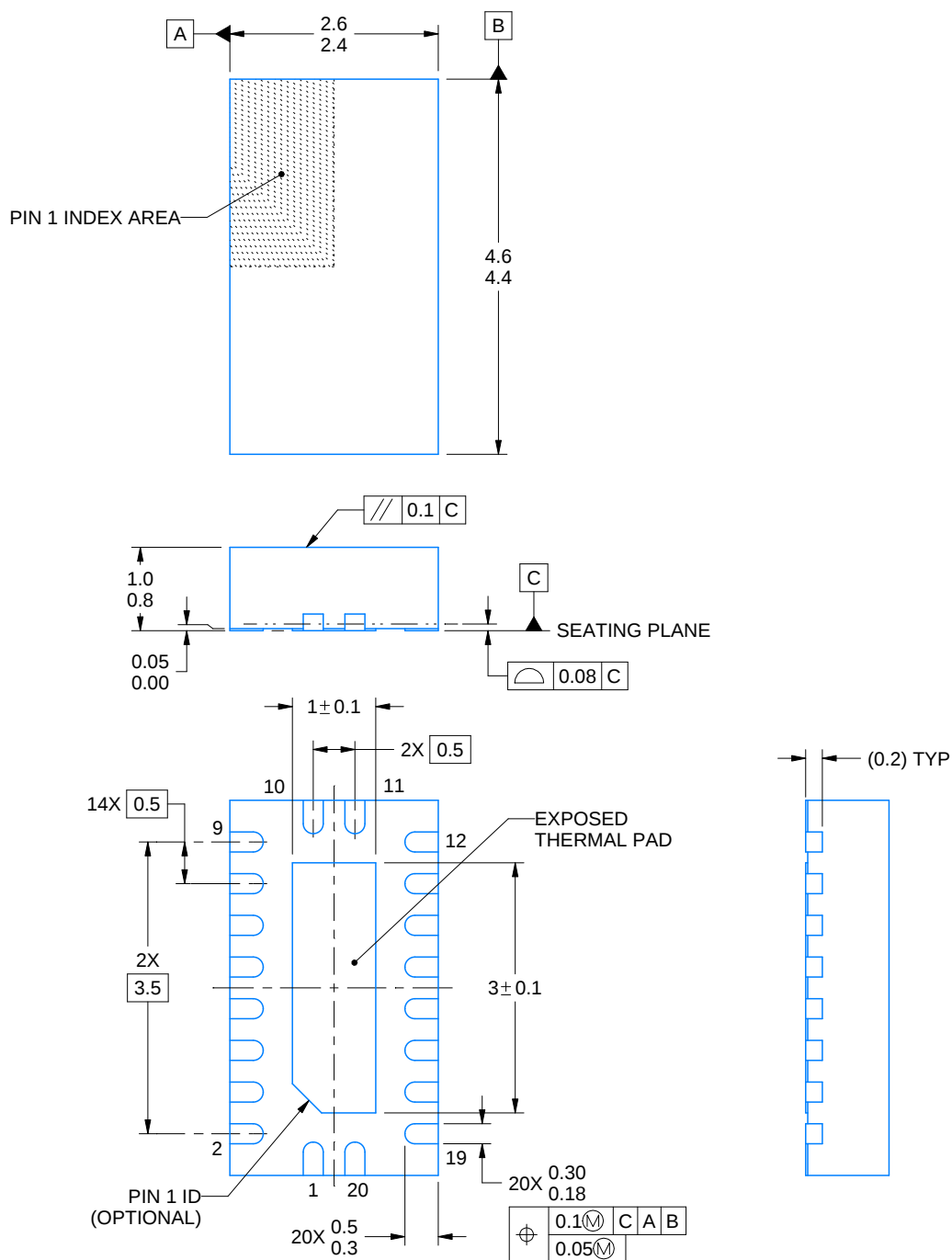
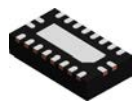
VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4222490/B 02/2021

NOTES:

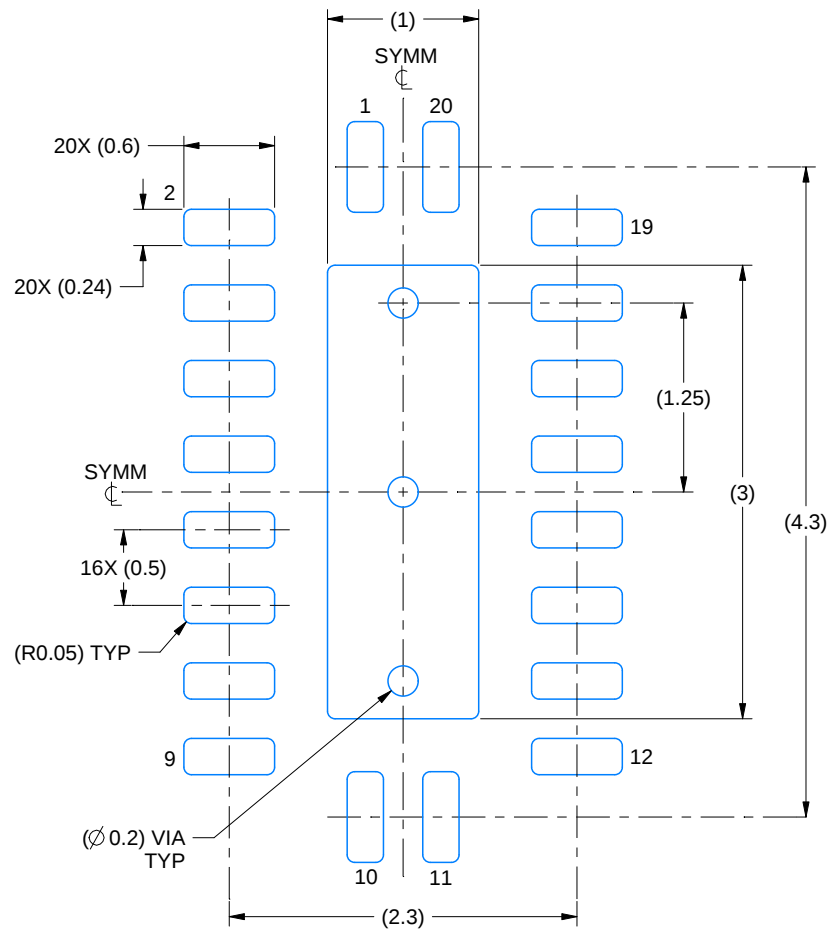
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

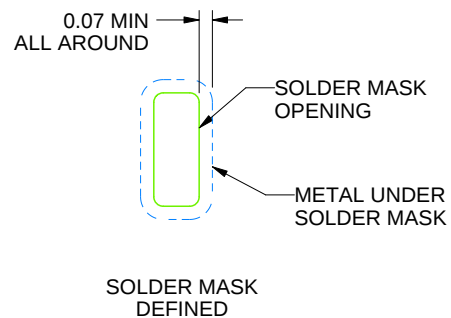
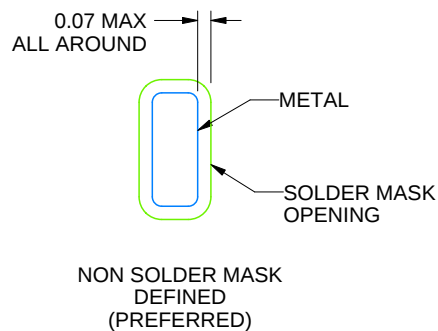
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

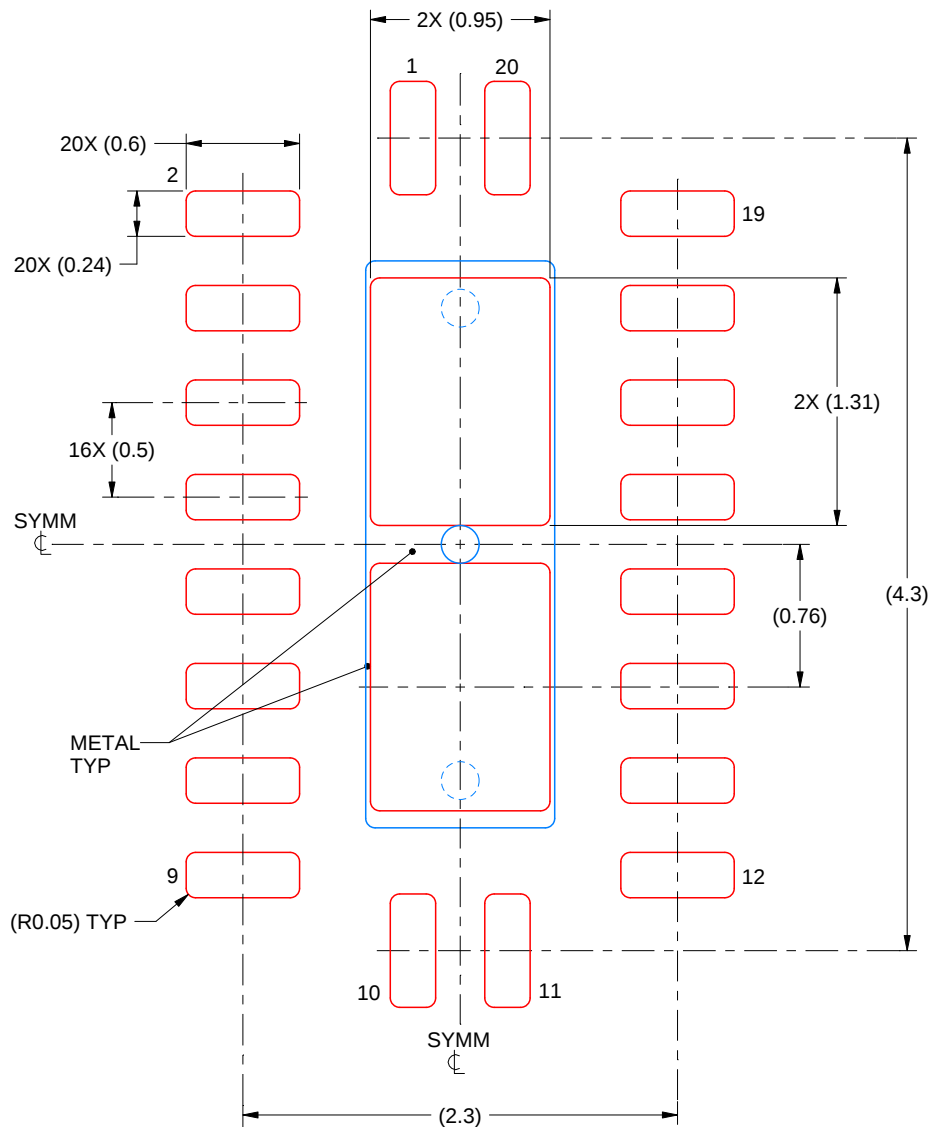
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 83% PRINTED SOLDER COVERAGE BY AREA
 SCALE:25X

4222490/B 02/2021

NOTES: (continued)

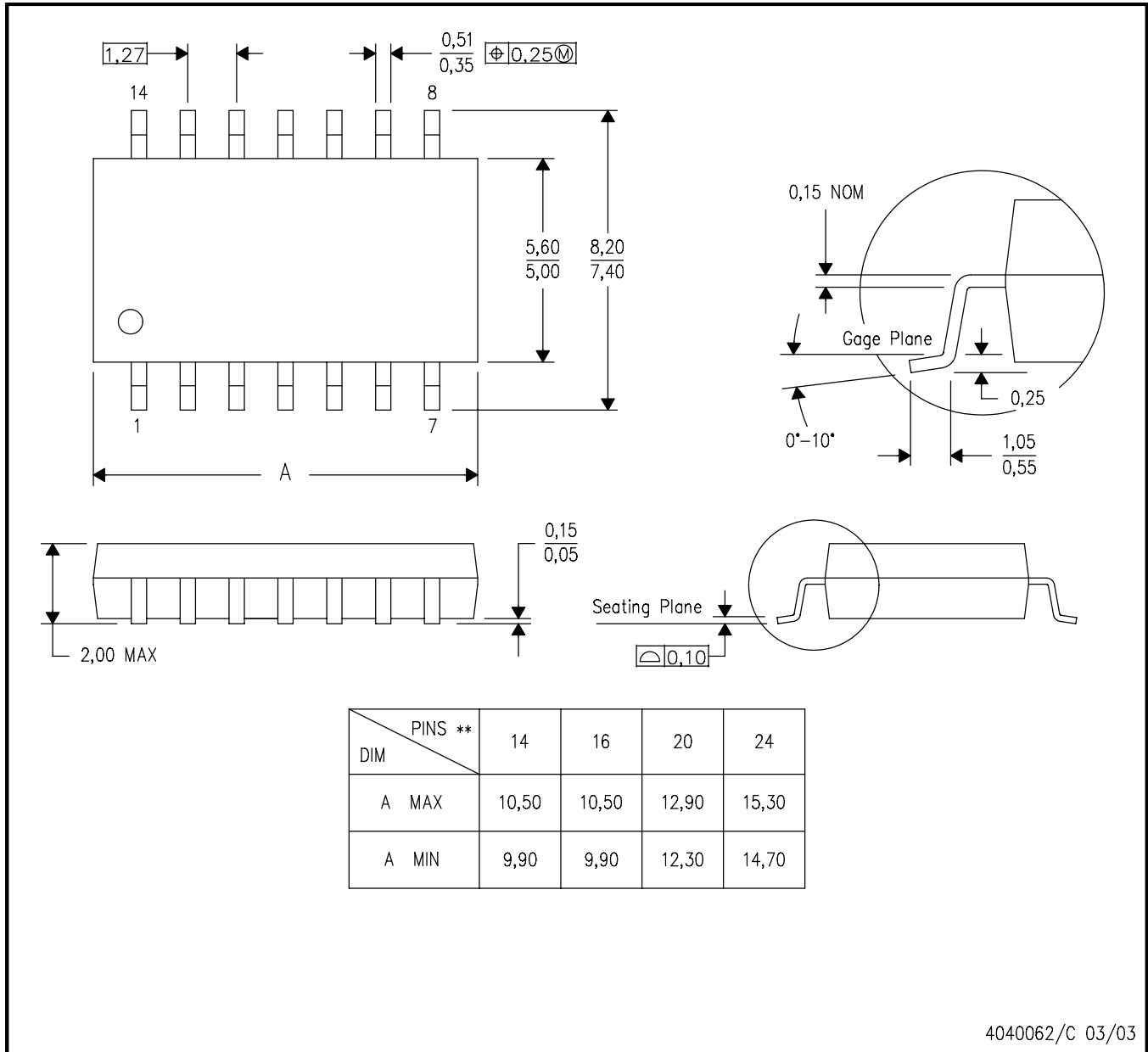
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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最后更新日期：2025 年 10 月