SN65DSIx6-Q1 MIPI® DSI 转 eDP™ 桥接器

1 特性

- 符合嵌入式 DisplayPort™(eDP™) 1.4 标准，支持 1 条、2 条或 4 条信道在 1.62Gbps (RBR)、2.16Gbps、2.43Gbps、2.7Gbps (HBR)、3.24Gbps、4.32Gbps 或 5.4Gbps (HBR2) 速率下运行。
- 实现 MIPI®D-PHY 版本 1.1 物理层前端和显示串行接口 (DSI) 版本 1.02.00
- 双通道 DSI 接收器在每个通道上可针对 1 条，2 条，3 条或 4 条 D-PHY 数据信道进行配置，每信道的运行速率高达 1.5Gbps
- 支持 RGB666 和 RGB888 格式的 18bpp 与 24bpp DSI 视频流
- 适合 60fps 4K 4096 × 2304 分辨率（18bpp 颜色），以及 60fps WUXGA 1920 × 1200 分辨率 和 3D 图形显示（120fps 等效）
- MIPI 前端可配置为单通道或双通道 DSI 配置
- 支持双通道 DSI 奇校验、偶校验、左移位和右移位操作模式
- 1.2V VCC 主电源，1.8V 电源用于数字 I/O
- 低功耗 特性 包括面板刷新和 MIPI 超低功耗状态 (ULPS) 支持
- DisplayPort 信道极性和分配均可配置。
- 通过外部基准时钟 (REFCLK) 支持 12MHz、19.2MHz、26MHz、27MHz 和 38.4MHz 等频率
- ESD 额定值 ±2 kV (HBM)
- 采用 64 引脚 HTQFP (PAP) 封装
- 温度范围：-40°C 至 +85°C

2 应用

- 平板电脑、笔记本、上网本
- 移动互联网设备/汽车信息娱乐系统

3 说明

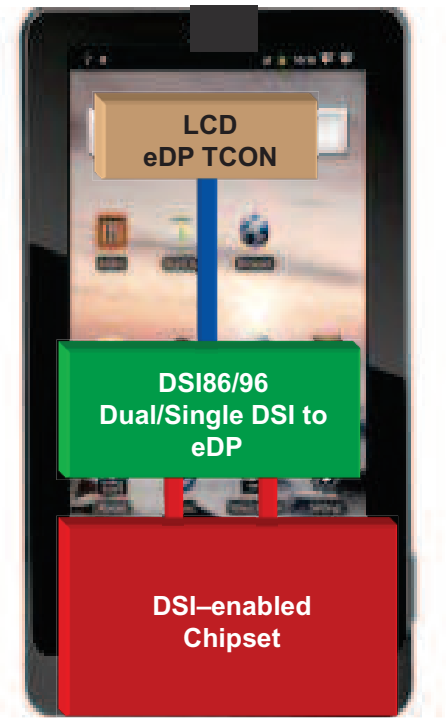
SN65DSI86-Q1 DSI 转嵌入式显示端口 (eDP) 桥接器特有 一个双通道 MIPI D-PHY 接收器前端配置，此配置中在每个通道上具有 4 条信道，每条信道的运行速率为 1.5Gbps，最大输入带宽为 12Gbps。该桥接器可解码 MIPI DSI 18bpp RGB666 和 24bpp RGB888 视频流，并将格式化视频数据流转换到具有多达四条信道的 DisplayPort，每条信道的运行速率为 1.62Gbps、2.16 Gbps、2.43 Gbps、2.7Gbps、3.24Gbps、4.32Gbps 或 5.4Gbps。

SN65DSI86-Q1 非常适用于每秒 60 帧的 WQXGA，以及等效 120fps（高达 24bpp）的 4K 3D 图形和全高清 (HD) (1920x1080) 分辨率。执行了部分线路缓冲以适应 DSI 与 DisplayPort 接口间的数据流不匹配。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN65DSI86-Q1	HTQFP (64)	10mm x 10mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (July 2014) to Revision A **Page**

- Changed Description for ADDRESS 0x5A BIT(S) 1:0 from 'Reserved' to 'ASSR_CONTROL' with Bit assignments of 00, 01, 10, and 11 in Table 23. 47
- Added Table 33 in Standard CFR Registers 64

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5 说明 （续）

采用符合工业标准的接口技术设计，能够与多种微处理器兼容，并具有多种功耗管理 特性，包括面板刷新支持和 MIPI 定义的超低功耗状态 (ULPS) 支持。

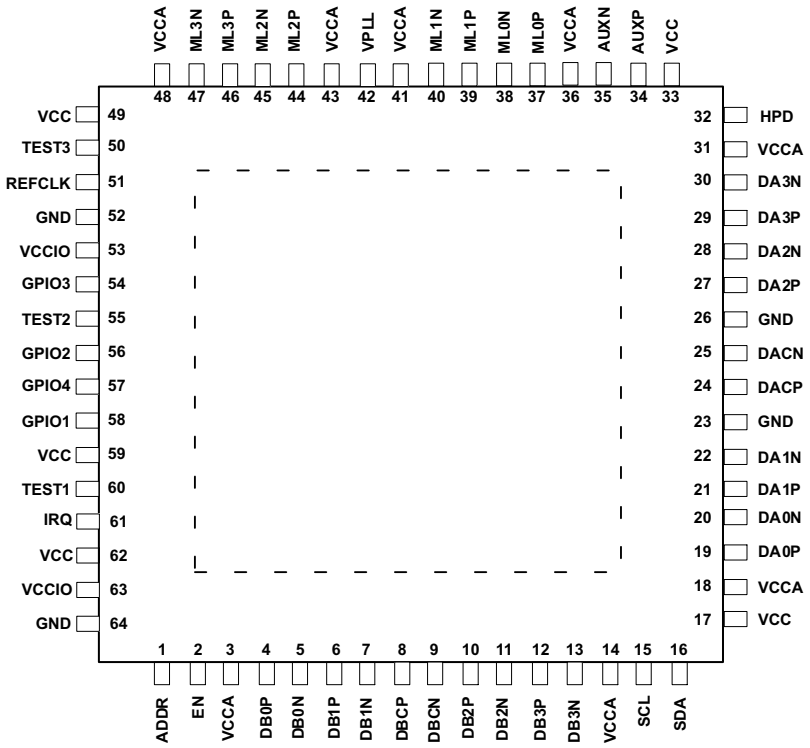
SN65DSI86 Q1 采用小外形10mm × 10mm HTQFP（间距 0.5mm）封装，工作温度范围为 –40°C 到 +85°C。

本文档后续部分的 SN65DSI86-Q1 是指 SN65DSIx6 或 DSIx6。

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6 Pin Configuration and Functions

PAP Package
64-Pin HTQFP
Top View



See Layout Guidelines for additional information.

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
DA0P	19	I	MIPI D-PHY Channel A Data Lane 0; data rate up to 1.5 Gbps.
DA0N	20		
DA1P	21	I	MIPI D-PHY Channel A Data Lane 1; data rate up to 1.5 Gbps.
DA1N	22		
DACP	24	I	MIPI D-PHY Channel A Clock Lane; operates up to 750MHz. Under proper conditions, this clock can be used instead of REFCLK to feed DP_PLL
DACN	25		
DA2P	27	I	MIPI D-PHY Channel A Data Lane 2; data rate up to 1.5 Gbps.
DA2N	28		
DA3P	29	I	MIPI D-PHY Channel A Data Lane 3; data rate up to 1.5 Gbps.
DA3N	30		
DB0P	4	I	MIPI D-PHY Channel B Data Lane 0; data rate up to 1.5 Gbps.
DB0N	5		
DB1P	6	I	MIPI D-PHY Channel B Data Lane 1; data rate up to 1.5 Gbps.
DB1N	7		
DBCP	8	I	MIPI D-PHY Channel B Clock Lane; operates up to 750 MHz.
DBCN	9		
DB2P	10	I	MIPI D-PHY Channel B Data Lane 2; data rate up to 1.5 Gbps.
DB2N	11		

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
DB3P	12	I	MIPI D-PHY Channel B Data Lane 3; data rate up to 1.5 Gbps.
DB3N	13		
ML0P	37	O	DisplayPort Lane 0 transmit differential pair. Supports 1.62Gbps, 2.16Gbps, 2.43Gbps, 2.7Gbps, 3.24Gbps, 4.32Gbps, and 5.4Gbps. All DisplayPort lanes transmit at the same data rate.
ML0N	38		
ML1P	39	O	DisplayPort Lane 1 transmit differential pair. Supports 1.62Gbps, 2.16Gbps, 2.43Gbps, 2.7Gbps, 3.24Gbps, 4.32Gbps, and 5.4Gbps. All DisplayPort lanes transmit at the same data rate.
ML1N	40		
ML2P	44	O	DisplayPort Lane 2 transmit differential pair. Supports 1.62Gbps, 2.16Gbps, 2.43Gbps, 2.7Gbps, 3.24Gbps, 4.32Gbps, and 5.4Gbps. All DisplayPort lanes transmit at the same data rate.
ML2N	45		
ML3P	46	O	DisplayPort Lane 3 transmit differential pair. Supports 1.62Gbps, 2.16Gbps, 2.43Gbps, 2.7Gbps, 3.24Gbps, 4.32Gbps, and 5.4Gbps. All DisplayPort lanes transmit at the same data rate.
ML3N	47		
AUXP	34	I/O	Aux Channel Differential Pair.
AUXN	35		
TEST1	60	I PD	Test Mode. When high, the SN65DSIx6 enters Test Mode. This pin should be left unconnected or tied to ground for normal operation.
TEST2	55	I/O PD	Used for internal test, HBR2 Compliance Eye, and Symbol Error Rate Measurement pattern. For normal operation, this pin should be pull-down to ground or left unconnected. Refer to DP Training and Compliance patterns for information on HBR2 Compliance Eye and Symbol Error Rate Measurement patterns.
TEST3	50	I	Used for Texas Instruments internal use only. This pin must be left unconnected or tied to ground through a 0.1µF capacitor.
GPIO1	58	I/O	General Purpose I/O. Refer to General Purpose Input and Outputs for details on GPIO functionality. When these pins are set high, they should be tied to the same 1.8V power rail where SN65DSIx6 VCCIO 1.8V power rail is connected.
GPIO2	56		
GPIO3	54		
GPIO4	57		
HPD	32	I PD	HPD Input. This input requires an 51K 1% series resistor.
ADDR	1	I	Local I2C Interface Target Address Select. In normal operation, this pin is an input. When the ADDR pin is programmed high, it should be tied to the same 1.8V power rails where the SN65DSIx6 VCCIO 1.8V power rail is connected.
EN	2	I PU	Chip Enable and Reset. Device is reset (shutdown) when EN is low.
REFCLK	51	I	REFCLK. Frequency determined by value programmed in I2C register or value of GPIO[3:1] latched at rising edge of EN. Supported frequencies are: 12MHz, 19.2MHz, 26MHz, 27MHz, and 38.4MHz. This pin must be tied to or pulled down to ground when DACP/N feeds the DisplayPort PLL.
SCL	15	I	Local I2C Interface Clock
SDA	16	I/O	Local I2C Interface Data
IRQ	61	O	Interrupt Signal
GND	23, 26, 52, 64, Thermal pad	G	Reference Ground
VCCA	3, 14, 18, 31, 36, 41, 43, 48	P	1.2V Power Supply for Analog Circuits. VCCA and VCC must be applied simultaneously.
VCC	17, 33, 49, 59, 62	P	1.2V Power Supply for digital core
VPLL	42	P	1.8V Power Supply for DisplayPort PLL
VCCIO	53, 63	P	1.8V Power Supply for Digital I/O.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CCA}, V_{CC}	–0.3	1.3	V
	V_{CCIO}, V_{PLL}	–0.3	2.175	
Input voltage	All input terminals	–0.5	2.175	V
Operating temperature		–40	85	°C
Storage temperature, T_{stg}		–65	105	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 Classification Level H2, all pins(1)		–2000	2000	V
		Charged device model (CDM), per AEC Q100-011 Classification Level C4B	Corner pins	–750	750	
			Other pins	–500	500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CCA}	VCCA Power supply; analog circuits	1.14	1.2	1.26	V
V_{CC}	VCC Power supply; digital circuits	1.14	1.2	1.26	V
V_{CCIO}	VCCIO Power Supply; digital IOs.	1.65	1.8	1.98	V
V_{PLL}	VPLL Power Supply, DisplayPort PLL	1.65	1.8	1.98	V
V_{PSN}	Supply noise on any VCC terminal	$f_{(noise)}$ > 1 MHz		0.05	V
V_{DSI_PIN}	DSI input pin voltage range	–50		1350	mV
$f_{(I2C)}$	Local I^2C input frequency			400	kHz
f_{HS_CLK}	DSI HS clock input frequency	40		750	MHz
Z_L	DP output differential load impedance	90		110	Ω
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		105	°C

7.4 Thermal Information

THERMAL METRIC(1)		SN65DSI86-Q1 PAP 64 TERMINALS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.5	°C/W
ψ_{JT}	Junction-to-top thermal resistance metric (High-K board(1))	0.7	°C/W
ψ_{JB}	Junction-to-board thermal resistance metric (High-K board(1))	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
STANDARD IO (TEST1, TEST2, ADDR, SCL, SDA, IRQ, REFCLK, EN, GPIO[4:1])						
V_{IL}	Low-level control signal input voltage				0.3 × V_{CCIO}	V
V_{IH}	High-level control signal input voltage		0.7 × V_{CCIO}			V
V_{OH}	High-level output voltage	I_{OH} = –2 mA	1.3			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_{IH}	High-level input current	Any input terminal			±5	µA
I_{IL}	Low-level input current					
I_{OZ}	High-impedance output current	Any output terminal			±10	µA
I_{OS}	Short-circuit output current	Any output driving GND short			±2	mA
I_{CCA}	V_{CCA} device active current	V_{CCA} = 1.2 V (2)		70	126	mA
I_{CC}	V_{CC} device active current	V_{CCA} = 1.2 V (2)		43	52	mA
I_{CCIO}	V_{CCIO} and V_{PLL} device active current	V_{CCIO} = 1.8 V, V_{PLL} = 1.8 V (2)		32	32	mA
$I_{SUSPEND_CCA}$	V_{CCA} device suspend current	All data and clock lanes are in ultra-low power state (ULPS) and SUSPEND = 1		9.8		mA
$I_{SUSPEND_CC}$	V_{CC} device suspend current	All data and clock lanes are in ultra-low power state (ULPS) and SUSPEND = 1		9		mA
$I_{SUSPEND_CCIO}$	V_{CCIO} and V_{PLL} device suspend current	All data and clock lanes are in ultra-low power state (ULPS) and SUSPEND = 1		1.16		mA
I_{EN_CCA}	V_{CCA} shutdown current	EN = 0		0.95		mA
I_{EN_CC}	V_{CC} shutdown current	EN = 0		2		mA
I_{EN_CCIO}	V_{CCIO} and V_{PLL} shutdown current	EN = 0		0.038		mA
R_{EN}	EN control input resistor			150		kΩ
ADDR, EN, SCL, SDA, DBP/N[3:0], DAP/N[3:1], DBCP/N, DACP/N						
I_{LEAK}	Input failsafe leakage current	V_{CC} = 0; V_{CCIO} = 0 V. Input pulled up to V_{CCIO} max. DSI inputs pulled up to 1.3 V	–40		40	µA
MIPI DSI INTERFACE						
V_{IH-LP}	LP receiver input high threshold	See Figure 5	880			mV
V_{IL-LP}	LP receiver input low threshold				550	mV
V_{OH-LP}	LP transmitter high-level output voltage		1100		1300	mV
V_{OL-LP}	LP transmitter low-level output voltage		–50		50	mV
V_{IHCD}	LP Logic 1 contention threshold		450			mV
V_{ILCD}	LP Logic 0 contention threshold				200	mV
$\|V_{ID}\|$	HS differential input voltage		70		270	mV
$\|V_{IDT}\|$	HS differential input voltage threshold				50	mV
$V_{IL-ULPS}$	LP receiver input low threshold; ultra-low power state (ULPS)				300	mV
V_{CM-HS}	HS common mode voltage; steady-state		70		330	mV
ΔV_{CM-HS}	HS common mode peak-to-peak variation including symbol delta and interference				100	mV
V_{IH-HS}	HS single-ended input high voltage	See Figure 5			460	mV
V_{IL-HS}	HS single-ended input low voltage		–40			mV

(1) All typical values are at V_{CC} = 1.2 V, V_{CCA} = 1.2 V, V_{CCIO} = 1.8 V, and V_{PLL} = 1.8 V, and T_A = 25°C
(2) Maximum condition: WQXGA 60 fps Dual-Link 2xDP at HBR2, PLL enabled; typical condition: WUXGA 60 fps 1xDP at HBR2, PLL enabled

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$V_{TERM-EN}$	HS termination enable; single-ended input voltage (both Dp AND Dn apply to enable)	Termination is switched simultaneous for Dn and Dp			450	mV
$R_{DIFF-HS}$	HS mode differential input impedance		80		125	Ω
DisplayPort MAIN LINK						
$V_{TX_DC_CM}$	Output common mode voltage		0		2	V
$V_{TX_AC_CM_HBR_RBR}$	TX AC common mode voltage for HBR and RBR.				20	mVRMS
$V_{TX_AC_CM_HBR2}$	TX AC common mode voltage for HBR2				30	mVRMS
$V_{TX_DIFFPP_LVL0}$	Differential peak-to-peak output voltage level 0	Based on default state of V0_P0_VOD register	300	400	460	mV
$V_{TX_DIFFPP_LVL1}$	Differential peak-to-peak output voltage level 1	Based on default state of V1_P0_VOD register	450	600	690	mV
$V_{TX_DIFFPP_LVL2}$	Differential peak-to-peak output voltage level 2	Based on default state of V2_P0_VOD register	600	800	920	mV
$V_{TX_DIFFPP_LVL3}$	Differential peak-to-peak output voltage level 3	Based on default state of V3_P0_VOD register. Level 3 is not enabled by default	600	800	920	mV
$V_{TX_PRE_RATIO_0}$	Pre-emphasis level 0		0	0	0	dB
$V_{TX_PRE_RATIO_1}$	Pre-emphasis level 1		2.8	3.5	4.2	dB
$V_{TX_PRE_RATIO_2}$	Pre-emphasis level 2		4.8	6.0	7.2	dB
$V_{TX_PRE_RATIO_3}$	Pre-emphasis level 3	Level 3 is not enabled by default	4.8	6.0	7.2	dB
$V_{TX_PRE_POST2_RATIO_0}$	Post-cursor2 level 0		0	0	0	dB
$V_{TX_PRE_POST2_RATIO_1}$	Post-cursor2 level 1		–1.1	–0.9	–0.7	dB
$V_{TX_PRE_POST2_RATIO_2}$	Post-cursor2 level 2		–2.3	–1.9	–1.5	dB
$V_{TX_PRE_POST2_RATIO_3}$	Post-cursor2 level 3	Level 3 is not enabled by default	–3.7	–3.1	–2.5	dB
I_{TX_SHORT}	TX short circuit current limit				50	mA
R_{TX_DIFF}	Differential impedance		80	100	120	Ω
$C_{AC_COUPLING}$	AC coupling capacitor		75		200	nF
DisplayPort HPD						
V_{HPD_PLUG}	Hot plug detection threshold	Measured at 51-kΩ series resistor.	2.2			V
V_{HPD_UNPLUG}	Hot unplug detection threshold	Measured at 51-kΩ series resistor.			0.8	V
RHPDPD	HPD internal pulldown resistor		51	60	69	kΩ
DisplayPort AUX INTERFACE						
$V_{AUX_DIFF_PP_TX}$	Peak-to-peak differential voltage at transmit pins	$V_{AUX_DIFF_PP} = 2 \times \lvert V_{AUXP} - V_{AUXN} \rvert$	0.18		1.38	V
$V_{AUX_DIFF_PP_RX}$	Peak-to-peak differential voltage at receive pins	$V_{AUX_DIFF_PP} = 2 \times \lvert V_{AUXP} - V_{AUXN} \rvert$	0.18		1.36	V
R_{AUX_TERM}	AUX channel termination DC resistance			100		Ω
$V_{AUX_DC_CM}$	AUX channel DC common mode voltage		0		1.2	V
$V_{AUX_TURN_CM}$	AUX channel turnaround common-mode voltage				0.3	V
I_{AUX_SHORT}	AUX Channel short circuit current limit				90	mA
C_{AUX}	AUX AC-coupling capacitor		75		200	nF

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7.6 Timing Requirements

		MIN	MAX	UNIT
Power-up For DPPLL_CLK_SRC = REFCLK, See Figure 1				
td1	$V_{CC/A}$ stable before V_{CCIO}/V_{PLL} stable	0		µs
td2	$V_{CC/A}$ and V_{CCIO}/V_{PLL} stable before EN assertion	100		µs
td3	REFCLK active and stable before EN assertion	0		µs
td4	GPIO[3:1] stable before EN assertion	0		ns
td5	GPIO[3:1] stable after EN assertion	5		µs
td6	LP11 state on DSI channels A and B before EN assertion	0		ns
td7	LP11 state on DSI channels A and B after EN assertion(1)	100		µs
t_{VCC_RAMP}	V_{CC} supply ramp requirements	0.2	100	ms
t_{VCCA_RAMP}	V_{CCA} supply ramp requirements	0.2	100	ms
t_{VCCIO_RAMP}	V_{CCIO} supply ramp requirements	0.2	100	ms
t_{VPLL_RAMP}	V_{PLL} supply ramp requirements	0.2	100	ms
Power-up For DPPLL_CLK_SRC = DACP/N, See Figure 2				
td1	$V_{CC/A}$ stable before V_{CCIO}/V_{PLL}stable	0		µs
td2	$V_{CC/A}$ and V_{CCIO}/V_{PLL} stable before EN assertion	100		µs
td3	REFCLK low before EN assertion	10		µs
td4	GPIO[3:1] stable before EN assertion	0		ns
td5	GPIO[3:1] stable after EN assertion	5		µs
td6	LP11 state on DSI channels A and B before EN assertion	0		ns
td7	LP11 state on DSI channels A and B after EN assertion(1)	100		µs
td8	DACP/N active and stable before DP_PLL_EN bit is set.	100		µs
t_{VCC_RAMP}	V_{CC} supply ramp requirements	0.2	100	ms
t_{VCCA_RAMP}	V_{CCA} supply ramp requirements	0.2	100	ms
t_{VCCIO_RAMP}	V_{CCIO} supply ramp requirements	0.2	100	ms
t_{VPLL_RAMP}	V_{PLL} supply ramp requirements	0.2	100	ms
SUSPEND Timing Requirements, See Figure 3				
td1	LP11 or ULPS on DSI channel A and B before assertion of SUSPEND.	200		ns
td2	Delay from SUSPEND asserted to DisplayPort Main Link powered off.	2 × t_{REFCLK}		
td3	REFCLK active hold time after assertion of SUSPEND	4 × t_{REFCLK}		
td4	REFCLK active setup time before deassertion of SUSPEND.	100		ns
td5	Delay from SUSPEND deasserted to DisplayPort Main Link active and transmitting IDLE pattern. Semi-Auto Link Training is NOT used.		20 + (1155 × t_{REFCLK})	µs
td6	LP11 state or ULPS on DSI channels A and B after SUSPEND deassertion	20 + (1155 × t_{REFCLK})		µs

(1) Access to DSIx6 CFR from I^2C or DSI allowed after td7.

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7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
MIPI DSI INTERFACE						
t_{GS}	DSI LP glitch suppression pulse width				300	ps
$t_{HS\text{-}SETUP}$	DSI HS data to clock setup time		0.2			UI
$t_{HS\text{-}HOLD}$	DSI HS clock to data hold time		0.2			UI
DisplayPort MAIN LINK						
F_{BR7}	Bit rate 7		5.37138	5.4	5.40162	Gbps
F_{BR6}	Bit rate 6		4.297104	4.32	4.321296	Gbps
F_{BR5}	Bit rate 5		3.222828	3.24	3.240972	Gbps
F_{BR4}	Bit rate 4		2.68569	2.7	2.70081	Gbps
F_{BR3}	Bit rate 3		2.417121	2.43	2.430729	Gbps
F_{BR2}	Bit rate 2		2.148552	2.16	2.160648	Gbps
F_{BR1}	Bit rate 1		1.611414	1.62	1.620486	Gbps
UI_{BR7}	Unit interval for BR7	High limit = +300 ppm. Low limit = –5300 ppm		185		ps
UI_{BR6}	Unit interval for BR6	High limit = +300 ppm. Low limit = –5300 ppm		231.5		ps
UI_{BR5}	Unit interval for BR5	High limit = +300 ppm. Low limit = –5300 ppm		308.6		ps
UI_{BR4}	Unit interval for BR4	High limit = +300 ppm. Low limit = –5300 ppm		370.4		ps
UI_{BR3}	Unit interval for BR3	High limit = +300 ppm. Low limit = –5300 ppm		411.5		ps
UI_{BR2}	Unit interval for BR2	High limit = +300 ppm. Low limit = –5300 ppm		463		ps
UI_{BR1}	Unit interval for BR1	High limit = +300 ppm. Low limit = –5300 ppm		617.3		ps
t_{ERC_L0}	Differential output rise or fall time with DP_ERC set to 0		50	61	80	ps
t_{ERC_L1}	Differential output rise or fall time with DP_ERC set to 1		74	95	115	ps
t_{ERC_L2}	Differential output rise or fall time with DP_ERC set to 2		108	123	146	ps
t_{ERC_L3}	Differential output rise or fall time with DP_ERC set to 3		136	153	168	ps
$t_{TX_RISE_FALL_MISMATCH}$	Lane intra-pair output skew at TX pins				5%	
t_{INTRA_SKEW}	Intra-pair differential skew				20	ps
t_{INTER_SKEW}	Inter-pair differential skew				100	ps
$t_{TX_EYE_HBR2}$	Minimum TX eye width at TX package pins for HBR2(2)		0.73			UI_{HBR2}
$t_{TX_EYE_MED_TO_MAX_JIT_HBR2}$	Maximum time between the jitter median and maximum deviation from the median at TX package pins for HBR2(2)				0.135	UI_{HBR2}
$t_{TX_EYE_HBR}$	Minimum TX eye width at TX package pins for HBR(2)		0.72			UI_{HBR}
$t_{TX_EYE_MED_TO_MAX_JIT_HBR}$	Maximum time between the jitter median and maximum deviation from the median at TX package pins for HBR(2)				0.147	UI_{HBR}
$t_{TX_EYE_RBR}$	Minimum TX eye width at TX package pins for RBR(2)		0.82			UI_{RBR}

(1) All typical values are at V_{CC} = 1.2 V and T_A = 25 °C
(2) BR refers to BR1; HBR refers to BR; HBR2 refers to BR7.

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Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{TX_EYE_MED_TO_MAX_JIT_RBR}$	Maximum time between the jitter median and maximum deviation from the median at TX package pins for RBR(2)				0.09	UI_{RBR}
t_{XSSC_AMP}	Link clock down-spreading		0%		0.5%	
t_{SSC_FREQ}	Link clock down-spreading frequency		30		33	kHz
DisplayPort AUX INTERFACE						
UI_{MAN}	Manchester transaction unit interval		0.4		0.6	µs
$t_{auxjitter_tx}$	Cycle-to-cycle jitter time at transmit pins				0.08	UI_{MAN}
$t_{auxjitter_rx}$	Cycle-to-cycle jitter time at receive pins				0.04	UI_{MAN}
REFCLK						
f_{REFCLK}	REFCLK frequency. supported frequencies: 12 MHz, 19.2 MHz, 26 MHz, 27 MHz, 38.4 MHz		12		38.4	MHz
$t_{RISEFALL}$	REFCLK rise or fall time	10% to 90%	100 ps		23	ns
t_{REFCLK}	REFCLK period		26.0417		83.333	ns
t_{pj}	REFCLK peak-to-peak phase jitter				50	ps
Duty	REFCLK duty cycle		40%	50%	60%	

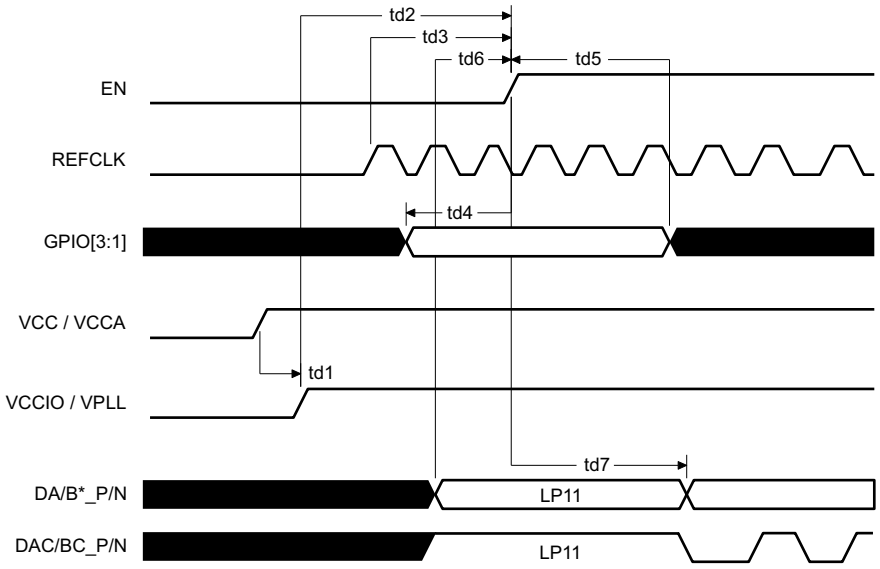


Figure 1. Power-Up Timing Definitions for DPPLL_CLK_SRC = REFCLK

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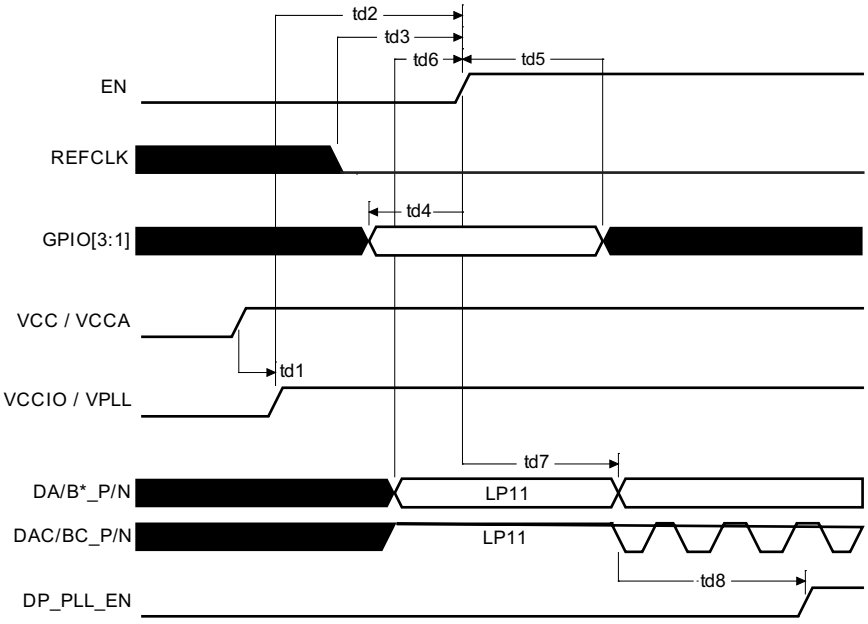


Figure 2. Power-Up Timing Definitions for DPPLL_CLK_SRC = DACP/N

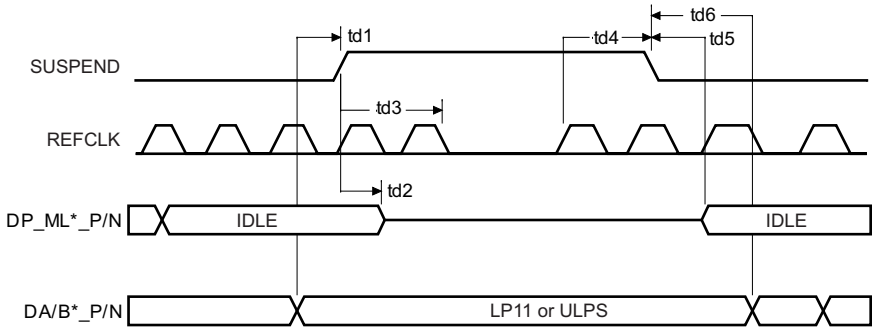


Figure 3. SUSPEND Timing Definitions

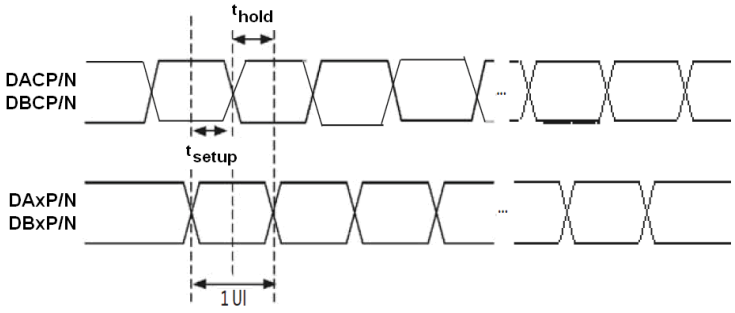


Figure 4. DSI HS Mode Receiver Timing Definitions

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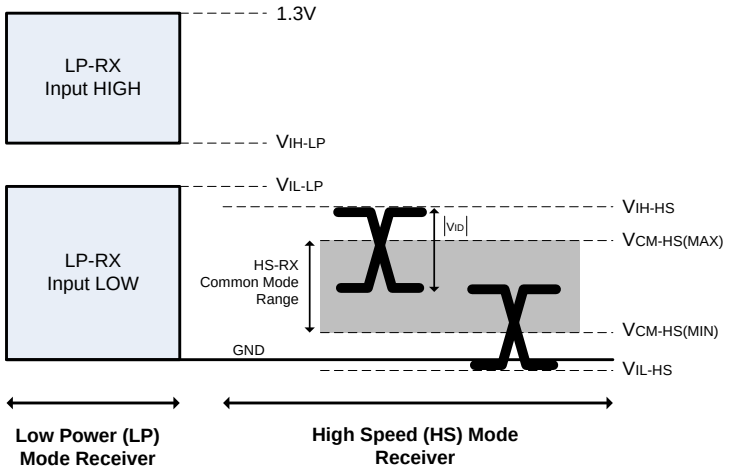


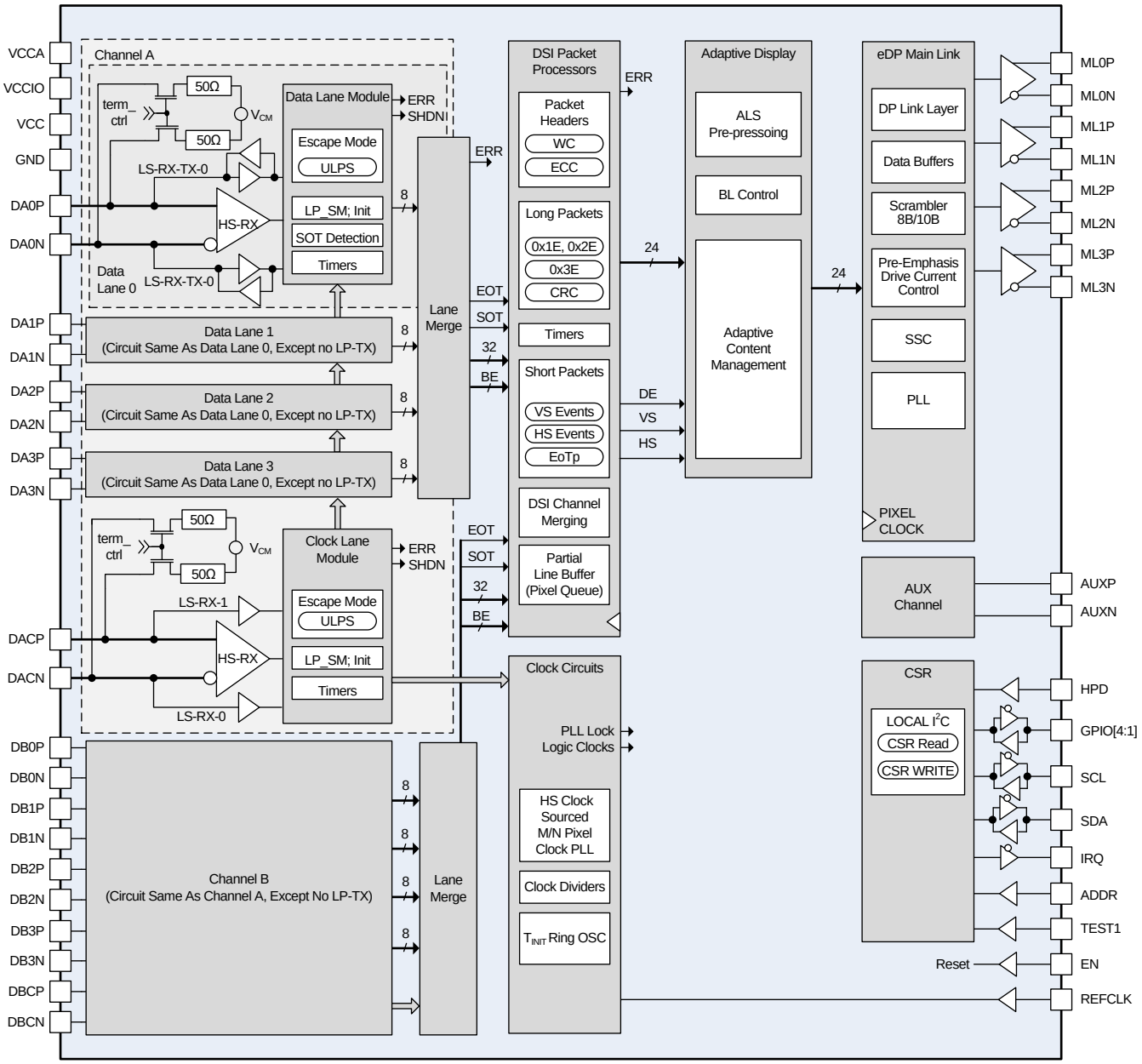
Figure 5. DSI Receiver Voltage Definitions

8 Detailed Description

8.1 Overview

The SN65DSIx6 is a MIPI DSI to eDP bridge, and supports MIPI DSI RGB 18 bpp (loosely packed or tightly packed) and 24 bpp formats. The SN65DSIx6 packetizes the 18-bpp or 24-bpp RGB data received on the DSI inputs and transmits over the eDP interface in SST format at data rates up to 5.4 Gbps. With support of up to eight DSI lanes at 1.5 Gbps per DSI lane, and four lanes of eDP at speeds up to 5.4 Gbps, the SN65DSIx6 is perfectly suited for both standard high definition (HD) displays as well has ultra HD displays like 4K2K.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 MIPI Dual DSI Interface

The SN65DSIx6 supports two 4-lane MIPI DSI inputs called DSIA and DSIB. Each lane supports a data rate up to 1.5 Gbps and can accept 18 bpp or 24 bpp RGB data. When only using the DSIA channel, the SN65DSIx6 can support an maximum video stream rate of 6 Gbps that easily supports HD resolutions. If larger resolutions like 4K2K are required, the maximum stream rate can be increased to 12 Gbps by using both DSIA and DSIB channels. When using both DSIA and DSIB channels, the SN65DSIx6 requires the pixels on each active line to be broken up into either odd pixels on DSIA and even pixels on DSIB, or left half of line on DSIA and right half of line on DSIB.

The SN65DSIx6 also supports DSI generic read and write operation. Using DSI generic reads and writes, the external GPU can configure the SN65DSIx6 internal registers and communicate with eDP panels. The DSI generic read and writes is also used for panel self refresh (PSR). In order to use the PSR feature, the eDP panel must support PSR and the GPU must support generating generic reads and writes without stopping the video stream. Generic reads and writes must be performed during video blanking time in order for PSR to work properly.

8.3.2 Embedded DisplayPort Interface

The SN65DSIx6 supports Single-Stream Transport (SST) mode over one, two, or 4 lanes at data rates of 1.62 Gbps (RBR), 2.16 Gbps, 2.43 Gbps, 2.7 Gbps (HBR), 3.24 Gbps, 4.32 Gbps, and 5.4 Gbps (HBR2). All lanes operate at the same rate (SN65DSIx6 does not support each lane being at a different data rate). The SN65DSIx6 allows for software control of the eDP interfaces voltage swing level, pre-emphasis level, and SSC. Because the SN65DSIx6 is a DSI to eDP bridge, the SN65DSIx6 only supports eDP panels which support ASSR (Alternate Scrambler Seed Reset). Software must either through the DSI interface or I^2C interface enable ASSR in the eDP panel before attempting to link train. See the *Example Script* section on how to enable ASSR in the eDP panel.

8.3.3 General-Purpose Input and Outputs

The SN65DSIx6 provides four GPIO pins that can be configured as an input or output. The GPIOs default to input but can be changed to output by changing the appropriate GPIO register.

GPIO Functions:

1. Input
2. Output
3. SUSPEND Input (powers down entire chip except for I^2C interface)
4. PWM
5. DSIA VSYNC
6. DSIA HSYNC

8.3.3.1 GPIO REFCLK and DSIA Clock Selection

The clock source for the SN65DSIx6 is derived from one of two sources: REFCLK pin or DACP/N pins. On the rising edge of EN, the sampled state of GPIO[3:1] as well as the detection of a clock on REFCLK pin is used to determine the clock source and the frequency of that clock. After the EN, software through the I^2C interface can change the configuration of REFCLK_FREQ, and CHA_DSI_CLK_RANGE registers for the case where GPIO[3:1] sampled state does not represent the intended functionality. Because the clock source is determined at the assertion of EN, software can not change the clock source. See Table 1 for GPIO to REFCLK or DACP/N frequency combinations.

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Feature Description (continued)

Table 1. GPIO REFCLK or DACP/N Frequency Selection(1)(2)(3)

GPIO[3:1]	REFCLK FREQUENCY (DPPLL_CLK_SRC = 0)	DACP/N CLOCK FREQUENCY (DPPLL_CLK_SRC = 1)	REFCLK_FREQ
3'b000	12 MHz	468 MHz (DSIACLK / 39 = 12 MHz)	0x0
3'b001	19.2 MHz	384 MHz (DSIACLK / 20 = 19.2 MHz)	0x1
3'b010	26 MHz	416 MHz (DSIACLK / 16 = 26 MHz)	0x2
3'b011	27 MHz	486 MHz (DSIACLK / 18 = 27 MHz)	0x3
3'b100	38.4 MHz	460.8 MHz (DSIACLK / 12 = 38.4 MHz)	0x4
3'b101 through 3'b111	19.2 MHz	384 MHz (DSIACLK / 20 = 19.2 MHz)	0x5 through 0x7

(1) For case when DPPLL_CLK_SRC = 1, the SN65DSIx6 will update the CHA_DSI_CLK_RANGE and CHB_DSI_CLK_RANGE with a value that represents the selected DSI clock frequency. Software can change this value.
(2) REFCLK pin must be tied or pull-down to GND when the DACP/N is used as the clock source for the DPPLL.
(3) If GPIO selection of REFCLK or DACP/N frequency is not used, then software must program the REFCLK_FREQ, CHA_DSI_CLK_RANGE and CHB_DSI_CLK_RANGE through the I^2C interface prior to issuing any DSI commands or packets to the SN65DSIx6.

8.3.3.2 Suspend Mode

Suspend mode is intended to be used with the *Panel Self Refresh (PSR)* feature of the eDP sink. The PSR feature saves system power but this power savings must not produce any noticeable display artifacts to the end user. The deassertion of EN produces the greatest DSIx6 power savings, but the reconfiguration of the DSIx6 may be too slow, and therefore produce a bad end-user experience. In this case, Suspend mode is the next best option for reducing DSIx6 power consumption while in an active PSR state. Suspend mode allows for quick exit from an active PSR state.

When GPIO1 is configured for suspended operation (GPIO1 pin is asserted), then the DSIx6 is placed in low-power mode. The suspend (GPIO1) pin is sampled by the rising edge of REFCLK. If the suspend pin is sampled asserted, then all CSR registers do not reset to the default values, and the DP PLL, DP interface, and DSI interfaces are powered off, as shown in Figure 3. REFCLK can be turned off when DSIx6 is in Suspend mode. *Timing Requirements* summarizes the timing requirements to take the DSIx6 into Suspend mode.

The DSIx6 supports assertion of IRQ for HPD events. When an IRQ_HPD event is detected and both IRQ_EN and IRQ_HPD_EN bits are set, then the DSIx6 will assert the IRQ.

In order to take the DSIx6 out of Suspend mode, the REFCLK must be running before and after the suspend (GPIO1) pin is deasserted. After the DP PLL is locked, the DSIx6 transitions the ML_TX_MODE from Main Link Off to either Normal or Semi-Auto Link depending on the state of PSR_TRAIN register. If the PSR_EXIT_VIDEO bit is set, then active video begins transmitting over the DisplayPort interface after the first vertical sync start (VSS) is detected on the DSI interface. If the PSR_EXIT_VIDEO bit is not set, software must enable the VSTREAM_ENABLE bit. Then active video begins transmitting over the DisplayPort interface after the first vertical sync start The *Timing Requirements* table summarizes the timing requirements to take the DSIx6 into SUSPEND mode. (VSS) is detected on the DSI interface.

NOTE

If the GPIO4_CTRL is configured for PWM, the PWM will be active during SUSPEND. If the system designer does not wish the PWM active during SUSPEND, then software can change the GPIO4_CTRL to Input before entering SUSPEND and then re-enable PWM after exiting SUSPEND by changing the GPIO4_CTRL to PWM.

NOTE

For the case when DPPLL_CLK_SRC = 1, REFCLK mentioned in this section is replaced with a divided down version of the DSIA_CLK (DCAP/N). The means that DSIA_CLK must be active before the assertion of SUSPEND and before the deassertion of SUSPEND as specified in *Timing Requirements* . The DSIA_CLK can be stopped while in SUSPEND as long as above requirements are meet.

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8.3.3.3 Pulse Width Modulation (PWM)

The SN65DSIx6 supports controlling the brightness of eDP display via pulse width modulation. The PWM signal is output over GPIO4 when GPIO4 control register is configured for PWM. For the SN65DSI86, the brightness is controlled by the BACKLIGHT register.

The granularity of brightness is controlled directly by the 16-bit BACKLIGHT_SCALE register. This register allows a granularity of up to 65535 increments. This register, in combination with either the BACKLIGHT register, will determine the duty cycle of the PWM. For example, if the BACKLIGHT_SCALE register is programmed to 0xFF and the BACKLIGHT is programmed to 0x40, then the duty cycle will be 25% (25% of the PWM period will be high and 75% of the PWM period will be low). The duty cycle would be 100% (PWM always HIGH) if the BACKLIGHT register was programmed to 0xFF and would be 0% (PWM always low) if BACKLIGHT register was programmed to 0x00. The BACKLIGHT_SCALE should be set equal to the digital value corresponding to the maximum possible backlight brightness that the display can produce. For example, if the backlight level is 16-bit, then BACKLIGHT_SCALE should be 0xFFFF, if it is an 8-bit range, then BACKLIGHT_SCALE should be set to 0x00FF.

Duty Cycle (high pulse) = (BACKLIGHT) / (BACKLIGHT_SCALE +1)

The frequency of the PWM is determined by the REFCLK_FREQ register and the value programmed into both the PWM_PRE_DIV and BACKLIGHT_SCALE registers. The equation below determines the PWM frequency:

PWM FREQ = REFCLK_FREQ / (PWM_PRE_DIV × BACKLIGHT_SCALE + 1)

Regardless of the state of the DPPLL_CLK_SRC register, the REFCLK_FREQ value in above equation will be based on the frequencies of DPPLL_CLK_SRC equal 0 (12 MHz, 19.2 MHz, 26 MHz, 27 MHz, 38.4 MHz). The REFCLK_FREQ will not be the DSIA CLK frequency in the case where DPPLL_CLK_SRC equals one.

NOTE

REFCLK or DACP/N must be running if GPIO4 is configured for PWM.

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8.4 Device Functional Modes

8.4.1 Reset Implementation

When EN is deasserted, CMOS inputs are ignored, the MIPI D-PHY inputs are disabled, and outputs are high impedance. It is critical to transition the EN input from a low to a high level after the V_{CC} supply has reached the minimum recommended operating voltage. This is achieved by a control signal to the EN input, or by an external capacitor connected between EN and GND. To insure that the SN65DSIx6 is properly reset, the EN pin must be deasserted for at least 100 µs before being asserted.

When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V_{CC} supply, where a slower ramp-up results in a larger value external capacitor. See the latest reference schematic for the SN65DSIx6 device and/or consider approximately 200-nF capacitor as a reasonable first estimate for the size of the external capacitor.

Both EN implementations are shown in Figure 6 and Figure 7.

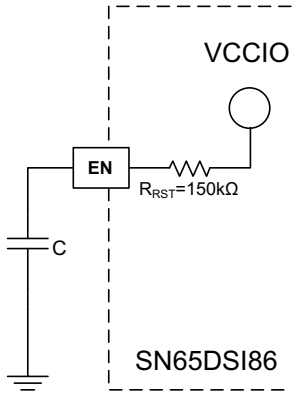


Figure 6. External Capacitor Controlled EN

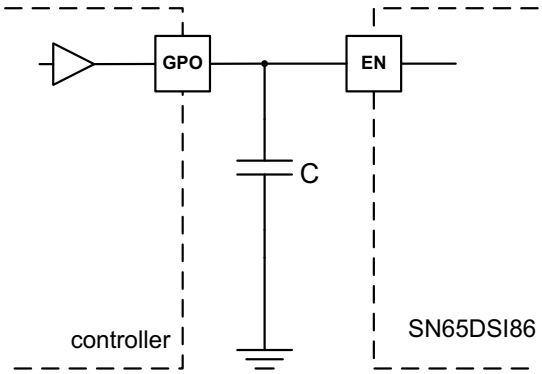


Figure 7. EN Input from Active Controller

8.4.2 Power-Up Sequence

STEP NUMBER	DESCRIPTION
1	EN deasserted (LOW) and all Power Supplies active and stable. Depending on whether DPPLL_CLK_SRC is REFCLK pin or the DACP/N pins, GPIO[3:1] set to value that matches the REFCLK or DACP/N frequency. See the Table 1 for GPIO to REFCLK/DACP/N frequency combinations. If GPIO are not going to be used to select the REFCLK/DACP/N frequency, then software must program the REFCLK_FREQ register via I^2C after the EN is asserted. This knowledge of the REFCLK_FREQ is also used by the DSIx6 to determine the DSI Clock frequency when DPPLL_CLK_SRC is REFCLK pin.
2	EN is asserted (HIGH).
3	Configure number of DSI channels and lanes per channel. The DSIx6 defaults to 1 lane of DSI Channel A. DSI Channel B is disabled by default. When using DSI to configure the DSIx6, software needs to keep in mind the default configuration of the DSI channels only allows access to internal CSR through either 1 lane of HSDT or LPDT. Once CFR defaults are changed, all future CFR accesses should use the new DSI configuration. DSI Channel B can never be used to access internal DSIx6 CSR space. I^2C access to internal DSIx6 CSR is always available.
4	Configure REFCLK or DACP/N Frequency. If GPIO[3:1] is used to set the REFCLK or DACP/N frequency, then this step can be skipped. This step must be completed before any DisplayPort AUX channel communication can occur. SW needs to program REFCLK_FREQ to match the frequency of the clock provided to REFCLK pin or DACP/N pins. The knowledge of the REFCLK_FREQ is also used by the DSIx6 to determine the DSI Clock frequency when DPPLL_CLK_SRC is REFCLK pin.
5	The DSIx6 supports polarity inversion of each of the MLP[3:0] and MLN[3:0] pins. This feature helps prevent any DisplayPort Main Link differential pair crossing on the PCB. If the system implementer uses this feature, then the MLx_POLR registers need to be updated to match the system implementation.
6	The DSIx6 supports the ability to assign physical MLP/N[3:0] pins to a specific logical lane in order to help in the routing on the PCB. By default, physical pins MLP/N0 is logical lane 0, physical pins MLP/N1 is logical lane 1, physical pins MLP/N2 is logical lane 2, and physical pins MLP/N3 is logical lane 3. If the actual system implementation does not match the DSIx6 default values, then the LNx_ASSIGN fields need to be updated to match the system implementation.

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Device Functional Modes (continued)

STEP NUMBER	DESCRIPTION
7	By default, all interrupt sources are disabled (IRQ will not get asserted). SW needs to enable interrupt sources it cares about.
8	In an eDP application, HPD is not required. If HPD is not used, software needs to disable HPD by writing to the HPD_DISABLE register and then go to the next step. If HPD is used, then software must remain in this step until an HPD_INSERTION occurs. Once a HPD_INSERTION occurs, software can go to the next step.
9	Resolution capability of eDP Panel through reading EDID. In a eDP application, the Panel resolution capability may be known in advance. If this is the case, then this step can be skipped. Two methods are available for reading the EDID: direct method and indirect method.
	1. Using the direct method, SW needs to program I2C_ADDR_CLAIMx registers and enable them. Once this is done, any I^2C transaction that targets the I2C_ADDR_CLAIMx address will be translated into a I2C-Over-AUX transaction. In order to use the direct method, the I^2C master must support clock stretching.
	2. Using the indirect method, SW needs to use Native and I2C-Over-Aux registers. When using the indirect method, the maximum read size allowed is 16 bytes. This means reading the EDID must be broken into 16-byte chunks.
10	eDP Panel DisplayPort Configuration Data (DPCD). In eDP applications, the eDP panel DPCD information maybe known in advance. If this is the case, then this step can be skipped. SW can obtain the DPCD information by using the Native Aux Registers. The eDP panel capability is located at DisplayPort Address 0x00000 through 0x0008F. When reading the DPCD capability, SW needs to be aware that Native Aux transactions, like I2C-Over-Aux, is limited to a read size of 16 bytes. This means SW must read the DPCD in 16-byte chunks.
11	Based on resolution and capabilities of eDP sink obtained from EDID and DPCD, GPU should program the appropriate number of data lanes (DP_NUM_LANES) and data rate (DP_DATARATE) to match source capabilities and sink requirements. SSC_ENABLE can also be set if the eDP sink supports SSC.
12	Enable the DisplayPort PLL by writing a 1 to the DP_PLL_EN register. Before proceeding to next step, software should verify the PLL is locked by reading the DP_PLL_LOCK bit.
13	The SN65DSIx6 only supports ASSR Display Authentication method and this method is enabled by default. An eDP panel must support this Authentication method. Software will need to enable this method in the eDP panel at DisplayPort address 0x0010A.
14	Train the DisplayPort Link. Based on the resolution requirements of the application and the capabilities of the eDP panel, software needs to choose the optimum lane count and datarate for DisplayPort Main Links. The DSIx6 provides three methods for Link Training: Manual, Fast, and Semi-Auto.
	1. Manual Method is completely under SW control. SW can follow training steps outlined in the DisplayPort Standard or SW can perform a subset of what the DisplayPort standard requires.
	2. Fast Link Train. Prior knowledge of the calibrated settings is required in order to use Fast Link Train. SW needs to program both the DSIx6 and the eDP panel with the calibrated settings. Once this is done, software can change the ML_TX_MODE from Main Link Off to Fast Link Training. The DSIx6 will transmit the enabled TPS1 and/or TPS2 pattern and then transition the ML_TX_MODE to Normal Mode.
	3. Semi-Auto Link Training. This method is intended if there is a preferred datarate and lane count but the other parameters like TX_SWING and Pre-Emphasis are not known or eDP sink does not support Fast Training. SW can transition the ML_TX_MODE to Semi-Auto Link Training. If training is successful, the LT_PASS flag will get set and the ML_TX_MODE will be transitioned to Normal Mode. If training is unsuccessful, the LT_FAIL flag will get set and the ML_TX_MODE will transition to Main Link Off. SW then will have to specify a different data rate and/or lane count combination and attempt Auto-Link training again. This is repeated until successful link training occurs. Please keep in mind that changes in data rate will cause the DP PLL to lose lock. SW should always wait until DP_PLL_LOCK bit is set before attempting another Semi-Auto Link training.
15	Video Registers need to be programmed. Video Registers are used by the DSIx6 to recreate the video timing provided from the DSI interface to the DisplayPort interface.
16	Configure GPIO control registers if default state if not used. The GPIO default to Inputs.
17	Video stream can be enabled in the GPU and sent via the DSI interface to the DSIx6.
18	SW can now enable the DSIx6 to pass the video stream provided on the DSI interface to the DisplayPort interface by writing a 1 to the VSTREAM_ENABLE register.

8.4.3 Power Down Sequence

STEP NUMBER	DESCRIPTION
1	Clear VSTREAM_ENABLE bit.
2	Stop DSI stream from GPU. DSI lanes must be placed in LP11 state.
3	Program the ML_TX_MODE to 0x0 (OFF).
4	Program the DP_NUM_LANES register to 0x0.

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STEP NUMBER	DESCRIPTION
5	Clear the DP_PLL_EN bit.
6	Deassert the EN pin.
7	Remove power from supply pins (V_{CC}, V_{CCA}, V_{CCIO}, V_{PLL})

8.4.4 Display Serial Interface (DSI)

The DSI interface can be used for two purposes: (1) Configuring DSIx6 CSR, and (2) Streaming RGB video to an external DisplayPort sink. When used to configure the DSIx6, all communication from the DSIx6 to the GPU (read responses) will use DSI channel A lane 0 in LP signaling mode. The DSIx6 supports communication from GPU to DSIx6 in both HS mode and LP mode.

8.4.4.1 DSI Lane Merging

The SN65DSIx6 supports one DSI data lane per input channel by default, and may be configured to support two, three, or four DSI data lanes per channel. The bytes received from the data lanes are merged in HS mode to form packets that carry the video stream or target DSIx6 CFR space. DSI data lanes are bit and byte aligned. Figure 8 illustrates the lane merging function for each channel; 4-Lane, 3-Lane, and 2-Lane modes are illustrated.

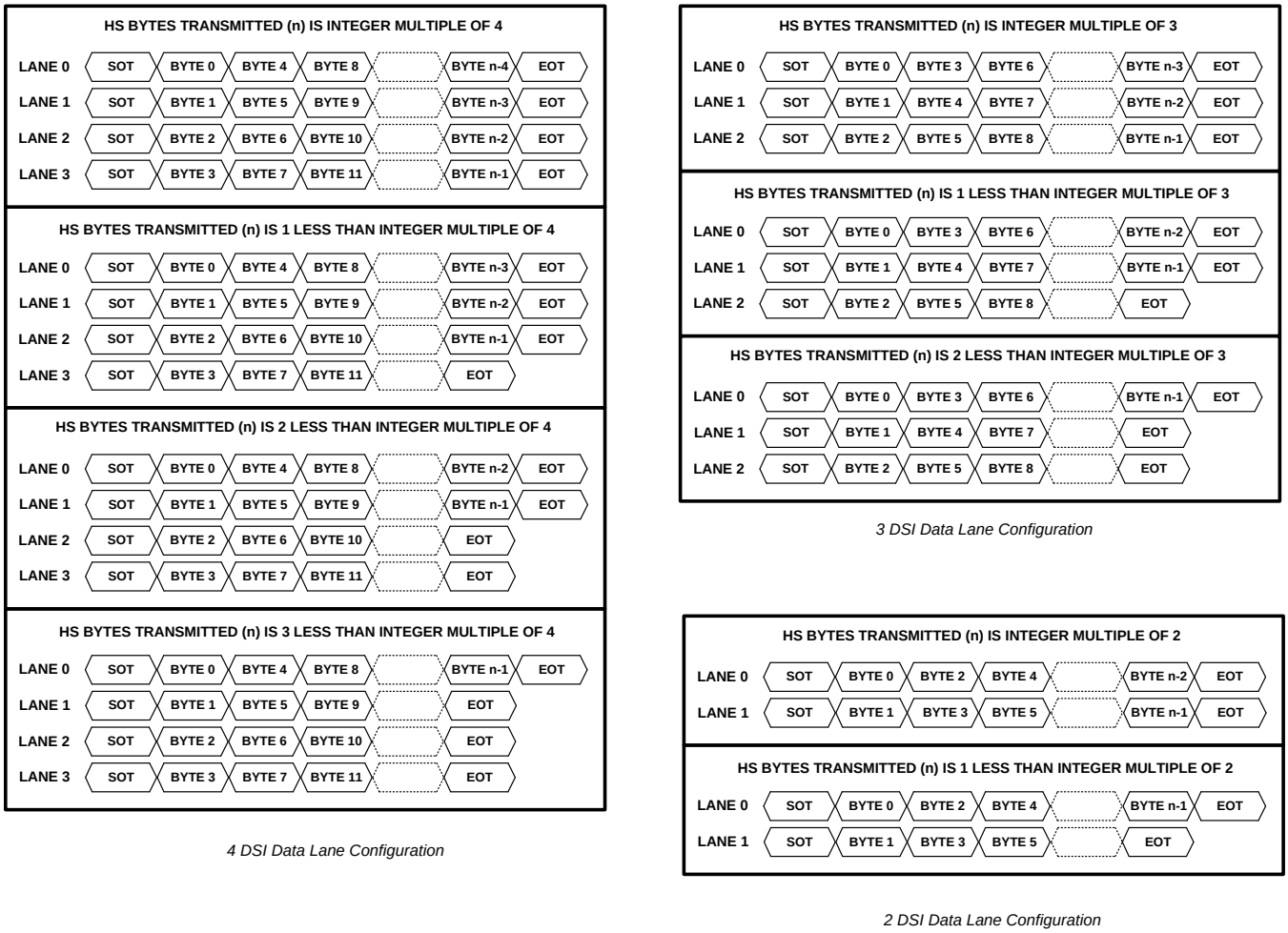


Figure 8. SN65DSIx6 DSI Lane Merging Illustration

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8.4.4.2 DSI Supported Data Types

Table 2 summarizes the DSI data types supported by the DSIx6. Any Data Type received by the DSIx6 that is not listed below will be ignored.

Table 2. Supported HS DSI Data Types from GPU

DATA TYPE	DESCRIPTION	DSI CHANNEL	PURPOSE
0x01	Vsync Start	A and B	Events for Video Timing
0x11	Vsync End	A and B	
0x21	Hsync Start	A and B	
0x31	HSync End	A and B	
0x08	End of Transmission packet (EoTp)	A and B	Marks the end of a HS transmission.
0x09	Null Packet	A and B	
0x19	Blanking Packet	A and B	
0x24	Generic Read Request 2 parameters	A only	Read CFR Request
0x37	Set Maximum Return Packet Size	A only	Specifics the maximum amount data returned from a Generic Read Request supported by GPU.
0x23	Generic Short Write 2 parameters	A only	Configure CFR
0x29	Generic Long Write	A only	Configure CFR and Secondary Data Packets
0x1E	Pixel Stream 18-bit RGB-666 Packed format	A and B	Active Pixel Data
0x2E	Pixel Stream 18-bit RGB-666 Loosely Packed Format	A and B	
0x3E	Pixel Stream 24-bit RGB-888 format	A and B	

Table 3. SN65DSIx6 LPDT DSI Data Type from GPU

DATA TYPE	DESCRIPTION	DSI CHANNEL	PURPOSE
0x24	Generic Read Request 2 parameters	CHA Lane 0	Read CFR requests
0x23	Generic Short Write 2 parameters	CHA Lane 0	Configure CFR.
0x08	EoTp	CHA Lane 0	Indicates end of HS transmission.

Table 4. SN65DSIx6 DSI Data Type Responses

DATA TYPE	DESCRIPTION	DSI CHANNEL	PURPOSE
0x11	Generic Short Read Response 1 Byte	CHA Lane 0	LPDT Response from Read Request
0x02	Acknowledge and Error Report	CHA Lane 0	LPDT Response following a Generic Read/Write with errors. Or an unsolicited BTA.
N/A	Acknowledge Trigger Message	CHA Lane 0	Trigger Message used to indicate no errors detected in Generic Request.

8.4.4.3 Generic Request Datatypes

The Generic Request datatypes are used for reading and writing to DSIx6 CFR space as well as for providing DisplayPort secondary data packets. The DSIx6 supports these request types in the form of high-speed data transmissions or low power data transmissions (LPDT).

To properly sample high-speed data received on the DSI interface, the DSIx6 implements a hardware mechanism, known as DSI_CLK_RANGE Estimator, to determine the DSI clock frequency. This hardware mechanism uses the REFCLK as a reference for calculating the DSI clock frequency. When the REFCLK_FREQ register correctly matching the REFCLK frequency, the DSI_CLK_RANGE Estimator will be able determine the DSIA and DSIB clock frequency. The DSI_CLK_RANGE Estimator requires a throw-away read (that is, read from address 0x00) before hardware will update CHA_DSI_CLK_RANGE and CHB_DSI_CLK_RANGE registers. Note

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that this first access may set some DSI error bits. In the cases where the system designer does not wish to use the DSI_CLK_RANGE Estimator, software can write the desired DSI Clock frequency to the CHA_DSI_CLK_RANGE and CHB_DSI_CLK_RANGE. Once these registers are written, the DSI_CLK_RANGE Estimator will be disabled and it becomes system software responsibility to make sure the CHA_DSI_CLK_RANGE and CHB_DSI_CLK_RANGE registers always reflect the actual DSI clock frequency.

8.4.4.3.1 Generic Read Request 2-Parameters Request

The Generic Read Request with 2 parameters will be used for reading DSIx6 CFR registers. The current address space requirement for the DSIx6 is just 256 bytes. This means the MS Byte of ADDR (bits 15 to 8) will always be zero. The MS Byte of the ADDR is intended for future expansion. The SN65DSIx6 response size defaults to one byte as defined by [DSI]. Software can use the Set Maximum Return Packet Size to inform the DSI86 that the GPU can support more than one byte, but the DSIx6 will always provide a response of one byte. If a single-bit ECC error was detected and corrected in the request, the DSIx6 will provide the requested data along with an Acknowledge and Error Report packet. If multi-bit ECC errors are detected and not corrected, the DSIx6 will only respond with an Acknowledge and Error Report packet.

SOT	ID = 0x24	ADDR (LS Byte)	ADDR (MS Byte)	ECC	EOT

Figure 9. Generic Read Request 2 Parameters Format

8.4.4.3.2 Generic Short Write 2-Parameters Request

The Generic Short Write with 2 parameters can be used for writing to DSIx6 CFR registers. The first parameter is the CFR Address and the second parameter is the data to be written to the address pointed to by the first parameter.

SOT	ID = 0x23	ADDR (Byte)	DATA	ECC	EOT

Figure 10. Generic Short Write Request 2 Parameters Format

NOTE

If GPU completes transmission with a BTA, the DSIx6 will respond with either an Acknowledge, if no errors were detected in current or previous packets, or an Acknowledge and Error Report packet, if errors were detected in current or previous packets.

8.4.4.3.3 Generic Long Write Packet Request

The Generic Long Write packet is used to write to CFRS within the DSIx6 as well as send secondary data packet to the eDP panel. The MS Byte of ADDR (bits 15 to 8) must be used to select whether the packet is SDP or whether it targets DSIx6 CFR registers. If the MS Byte of ADDR is equal to 0x80, then the DSIx6 will interpret the Generic Long Write to be a secondary data packet. If the MS Byte of ADDR is equal to 0x00, then the DSIx6 will interpret the Generic Long Write to target CFR space. For all other values of MS Byte of the ADDR, the DSIx6 will ignore the request and set the appropriate error flag.

SOT	ID = 0x29	WC (LS Byte)	WC (MS Byte)	ECC	ADDR (LS Byte)	ADDR (MS Byte)	DATA0	DATA1	DATA [WC-3]	CHKSUM (LS Byte)	CHKSUM (MS Byte)	EOT

Figure 11. Generic Long Write Format

NOTE

The WC field value must include the two ADDR bytes and the amount of data to be written. For example, if the amount of data to be written is 1 byte, then the WC(LS Byte) must be 0x03 and the WC(MS Byte) must be 0x00. Also, the maximum WC field value supported by the SN65DSIx6 is 258 bytes or (0x0102). When writing to DSIx6 CFR space, the maximum WC field value supported is three bytes. If GPU completes transmission with a BTA, the DSIx6 must respond with either an Acknowledge, if no errors were detected in current or previous packets, or an Acknowledge and Error Report packet, if errors were detected in current or previous packets.

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8.4.4.4 DSI Pixel Stream Packets

The SN65DSIx6 processes 18 bpp (RGB666) and 24 bpp (RGB888) DSI packets on each channel as illustrated below:

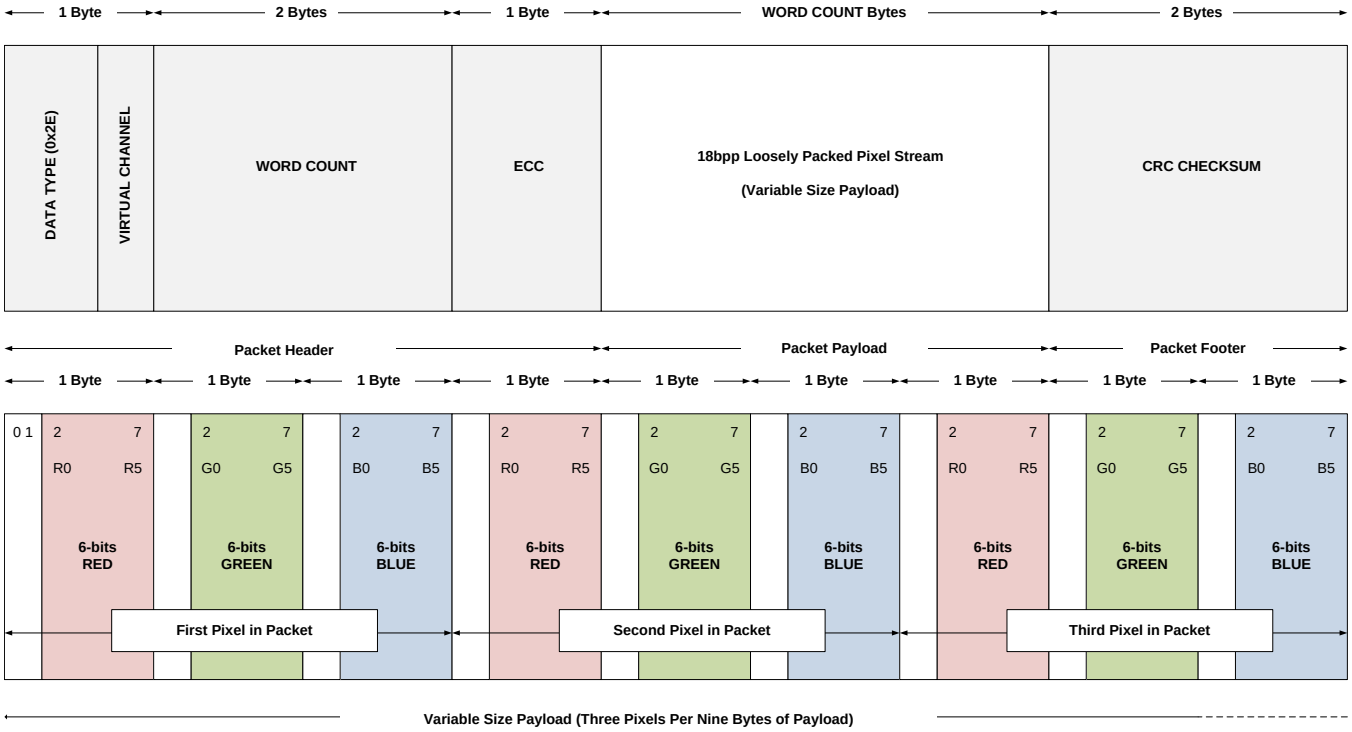


Figure 12. 18 bpp (Loosely Packed) DSI Packet Structure

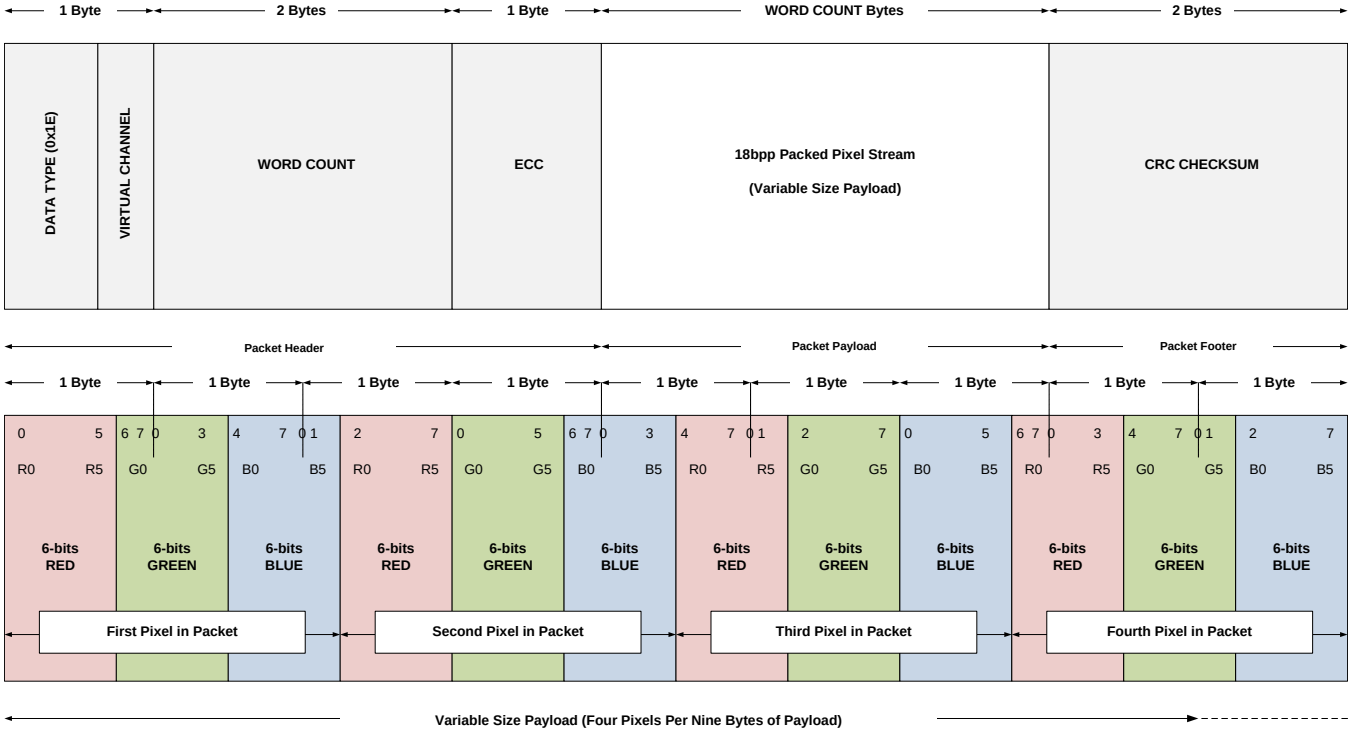


Figure 13. 18 bpp (Tightly Packed) DSI Packet Structure

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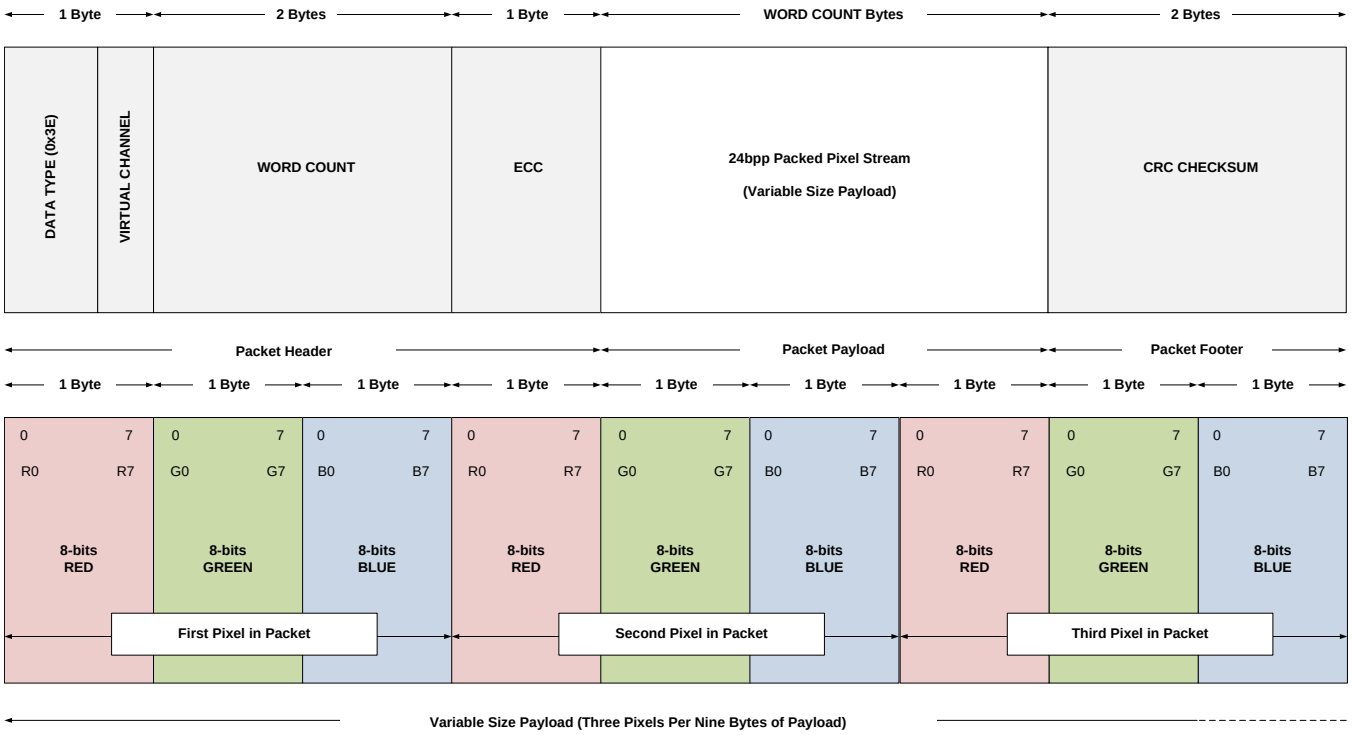


Figure 14. 24bpp DSI Packet Structure

Table 5. Example of 4-Lane DSI Packet Data for 24 bpp RGB

Lane 0	Lane 1	Lane 2	Lane 3
SOT	SOT	SOT	SOT
0x3E	WC (LS Byte)	WC(MS Byte)	ECC
R0-7:0	G0-7:0	B0-7:0	R1-7:0
G1-7:0	B1-7:0	R2-7:0	G2-7:0
B2-7:0	R3-7:0	G3-7:0	B3-7:0
R4-7:0	G4-7:0	B4-7:0	R5-7:0
G5-7:0	B5-7:0	CRC (LS Byte)	CRC (MS Byte)
EOT	EOT	EOT	EOT

8.4.4.5 DSI Video Transmission Specifications

The SN65DSIx6 expects the GPU to provide video timing events and active pixel data in the proper order in the form of a real-time pixel stream. According to the DSI specification [DSI], active pixel data is transmitted in one of two modes: Non-Burst and Burst. The SN65DSIx6 supports both non-burst and burst mode packet transmission. The burst mode supports time-compressed pixel stream packets that leave added time per scan line for power savings LP mode. For a robust and low-power implementation, the transition to LP mode is recommended on every video line, although once per frame is considered acceptable.

According to the DSI specification [DSI], timing events can be provided in one of two types: Sync Pulses, and Sync Events. The SN65DSIx6 supports both types. For the Sync Pulse type of timing event, the GPU will send VSYNC START (VSS), VSYNC END (VSE), HSYNC START (HSS), and HSYNC END (HSE) packets. For Sync Event type, the GPU will only send the sync start packets (VSS and HSS). For both types of timing events, the DSIx6 will use the values programmed into the Video Registers to determine the sync end events (VSE and HSE). Please note when configured for dual DSI channels, the SN65DSIx6 will use VSS, VSE, and HSS packets from channel A. The DSIx6 will use channel A events to recreate the same timings on the DisplayPort interface. The VSS, VSE, and HSS packets from channel B are used to internally align data on channel B to channel A.

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The first line of a video frame must start with a VSS packet, and all other lines start with VSE or HSS. The position of the synchronization packets in time is of utmost importance because this has a direct impact on the visual performance of the display panel.

As required in the DSI specification, the SN65DSIx6 requires that pixel stream packets contain an integer number of pixels (that is, end on a pixel boundary); TI recommends to transmit an entire scan line on one pixel stream packet. When a scan line is broken in to multiple packets, inter-packet latency must be considered such that the video pipeline (that is, pixel queue or partial line buffer) does not run empty (that is, under-run); during scan line processing. If the pixel queue runs empty, the SN65DSIx6 transmits zero data (18'b0 or 24'b0) on the DisplayPort interface.

When configured for dual DSI channels, the SN65DSIx6 supports ODD/EVEN configurations and LEFT/RIGHT configurations. In the ODD/EVEN configuration, the odd pixels for each scan line are received on channel A, and the even pixels are received on channel B. In LEFT/RIGHT mode, the left portion of the line is received on channel A, and the right portion of the line is received on channel B. The pixels received on channel B in LEFT/RIGHT mode are buffered during the left-side transmission to DisplayPort, and begin transmission to DisplayPort when the left-side input buffer runs empty. The only requirement for LEFT/RIGHT mode is CHB_ACTIVE_LINE_LENGTH must be at least 1 pixel.

NOTE

The DSIx6 does not support the DSI Virtual Channel capability.

Table 6. Summary of DSI Video Input Requirements

NUMBER	REQUIREMENT
1	DSI datatypes VSS and HSS are required, but datatypes HSE and VSE are optional.
2	The exact time interval between each HSS must be maintained.
3	The time between the HSS and HACT (known as HBP) does not have to be maintained. The DSIx6 will recreate HBP on DisplayPort.
4	The time from the end of HACT to HSS (known as HFP) does not have to be maintained. The DSIx6 will recreate HFP on DisplayPort.
5	The time from VSS to first line of active video must be maintained.
6	The time from end of last line of active video to the beginning of the first line of active video must be maintained. This time is defined as the Vertical Blanking period.

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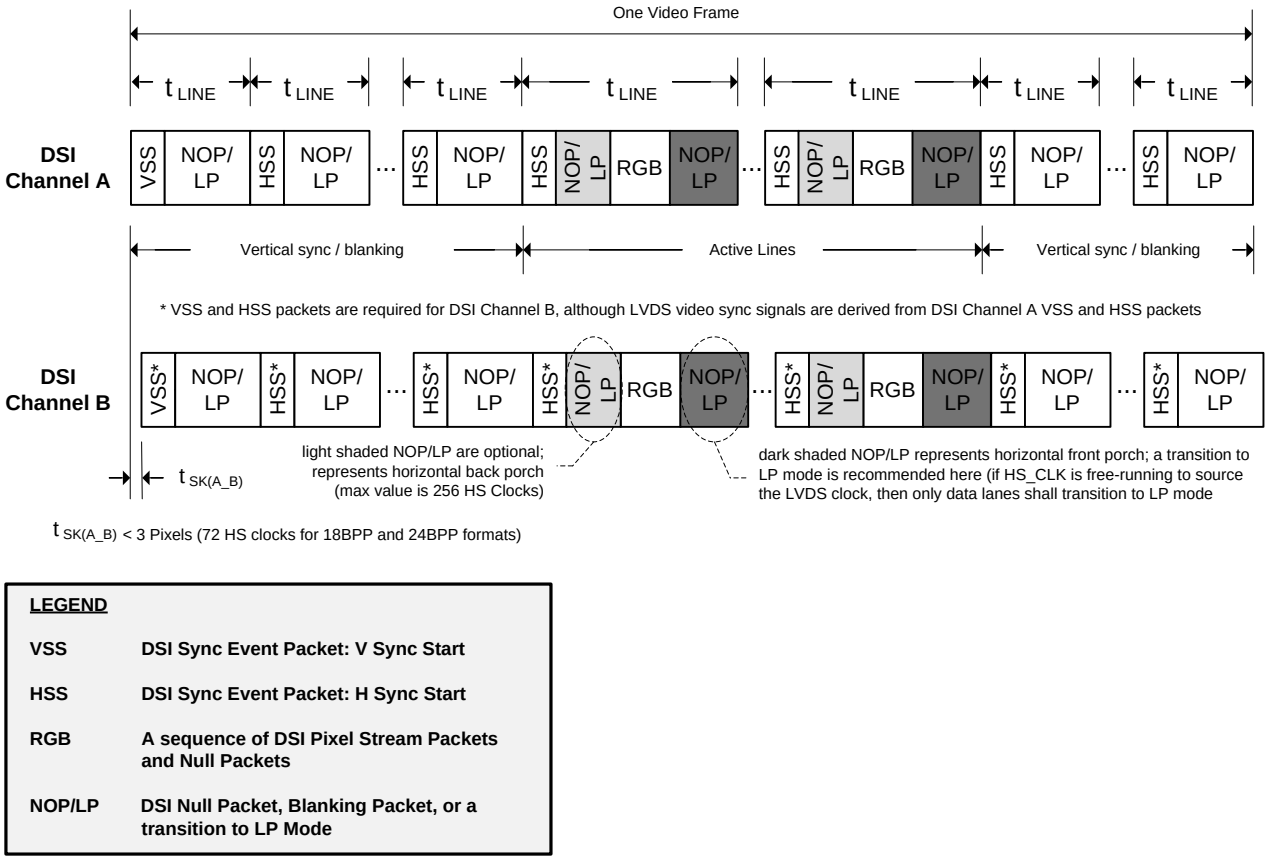


Figure 15. DSI Channel Transmission and Transfer Function

8.4.4.6 Video Format Parameters

It is the responsibility of the GPU software to program the DSIx6 *Video Registers* with the Video format that is expected to be displayed on the eDP panel. The DSIx6 expects the parameters in Table 7 to be programmed. The DSIx6 will use these parameters to determine the DisplayPort MSA parameters that are transmitted over DisplayPort every vertical blanking period. These MSA parameters are used by the eDP panel to recreate the video format provided on the DSI interface.

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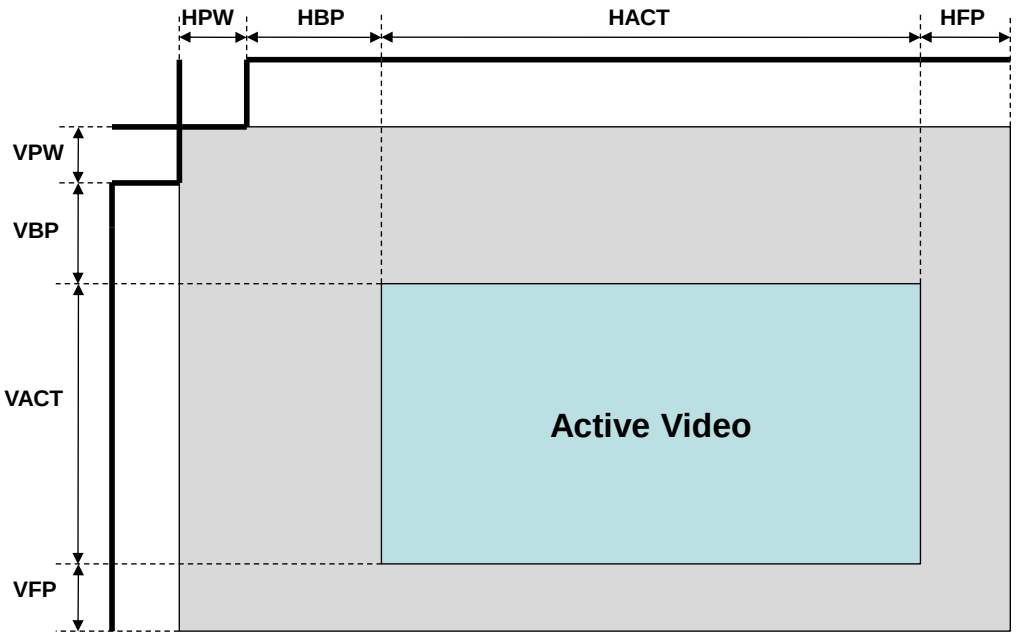


Figure 16. Video Format

Table 7. Video Format Parameters

PARAMETER	DESCRIPTION	DSIx6 REGISTER
HPOL	Used to specify if the HPW is high or low.	CHA_HSYNC_POLARITY
HPW	The width of the Horizontal Sync Pulse in pixels	{CHA_HSYNC_PULSE_WIDTH_HIGH, CHA_HSYNC_PULSE_WIDTH_LOW}
HBP	The size of the Horizontal Back Porch in pixels	CHA_HORIZONTAL_BACK_PORCH
HACT	The length, in pixels, of the active horizontal line.	{CHA_ACTIVE_LINE_LENGTH_HIGH, CHA_ACTIVE_LINE_LENGTH_LOW} + {CHB_ACTIVE_LINE_LENGTH_HIGH, CHB_ACTIVE LINE_LENGTH_LOW}
HFP	The size of the Horizontal Front Porch in pixels.	CHA_HORIZONTAL_FRONT_PORCH
HTOTAL	Total length, in pixels, of a horizontal line.	HPW + HBP + HACT + HFP
VPOL	Used to specify if the VPW is high or low	CHA_VSYNC_POLARITY
VPW	The width of the Vertical Sync Pulse in lines. The width must be at least 1 line.	{CHA_VSYNC_PULSE_WIDTH_HIGH, CHA_VSYNC_PULSE_WIDTH_LOW}
VBP	The size of the Vertical Back Porch in lines. The size must be at least 1 line.	CHA_VERTICAL_BACK_PORCH
VACT	The number of vertical active lines.	{CHA_VERTICAL_DISPLAY_SIZE_HIGH, CHA_VERTICAL_DISPLAY_SIZE_LOW}
VFP	The size of the Vertical Front Porch in lines. The size must be at least 1 line.	CHA_VERTICAL_FRONT_PORCH
VTOTAL	The total number of vertical lines in a frame.	VPW + VBP + VACT + VFP

8.4.4.7 GPU LP-TX Clock Requirements

The GPU is responsible for controlling its own LP clock frequency to match the DSIx6. The GPU LP TX clock frequency must be in the range of 67% to 150% of the DSIx6 LP TX clock frequency. The DSIx6 LP TX clock frequency is detailed in Table 8.

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Table 8. DSIx6 LP TX Clock Frequency

REFCLK_FREQ	LP TX Clock Frequency
0x0	12 MHz
0x1	19.2 MHz
0x2	13 MHz
0x3	13.5 MHz
0x4	19.2 MHz

8.4.5 DisplayPort

The SN65DSIx6 supports Single-Stream Transport (SST) mode over 1, 2, or 4 lanes at a datarate of 1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.7 Gbps, 3.24 Gbps, 4.32 Gbps, or 5.4 Gbps. The SN65DSIx6 does not support Multi-Stream Transport (MST) mode.

8.4.5.1 HPD (Hot Plug/Unplug Detection)

The HPD signal is used by a DisplayPort source (DSIx6) for detecting when a downstream port (DisplayPort Panel) is attached or removed as well as for link status information. The [EDP] specification states that the HPD signal is required for an eDP Panel but is optional for a eDP source (DSIx6). The DSIx6 supports the HPD signal. It is up to the system implementer to determine if HPD signal is needed for the DSIx6. If not used, the system implementer should pull-up HPD to 3.3 V or set the HPD_DISABLE bit. If HPD_DISABLE is set, then all HPD events (IRQ_HPD, HPD_REMOVAL, HPD_INSERTION, HPD_REPLUG) are disabled.

When IRQ_EN and IRQ_HPD_EN is enabled, the DSIx6 will assert the IRQ whenever the eDP generates a IRQ_HPD event. An IRQ_HPD event is defined as a change from INSERTION state to the IRQ_HPD state.

The DSIx6 will also interpret a DisplayPort device removal or insertion as an HPD_REMOVAL or HPD_INSERTION event. A HPD_REMOVAL event is defined as a change that causes the HPD state to transition from INSERTION state to the REMOVAL state. A HPD_INSERT event is defined as a change that causes the HPD state to transition from the REMOVAL state to the INSERTION state. The REPLUG event is caused by the sink deasserting HPD for more than 2 ms but less than 100 ms. If software needs to determine the state of the HPD pin, it should read the HPD Input register. The HPD state machine operates off an internal ring oscillator. The ring oscillator frequency will vary based on PVT (process voltage temperature). The min/max range in the HPD State Diagram refers to the possible times based off variation in the ring oscillator frequency.

NOTE

HPD has a minimum of 60-kΩ ±15% internal pulldown resistor.

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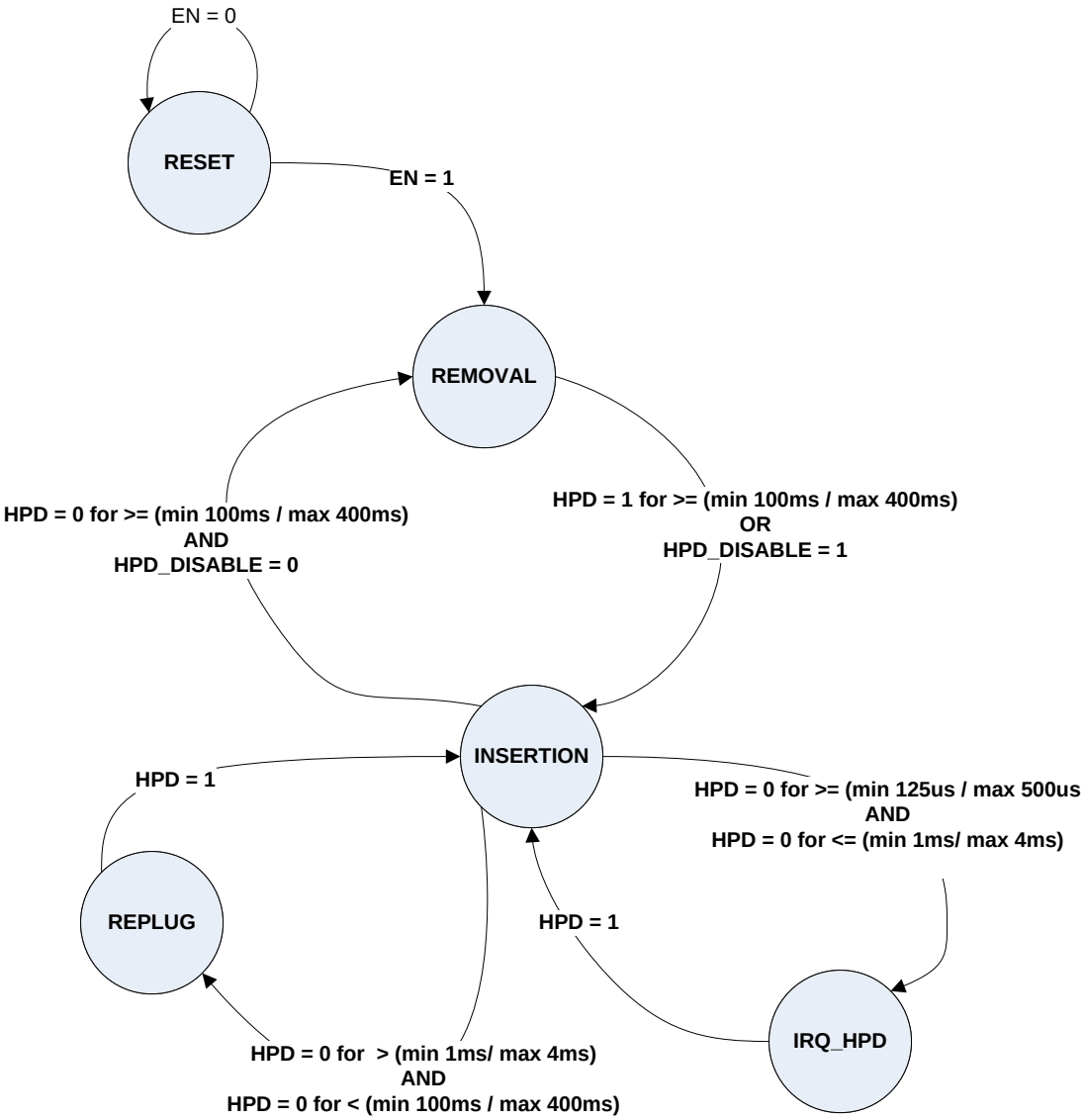


Figure 17. HPD State Diagram

8.4.5.2 AUX_CH

The AUX_CH supported by the DSIx6 is a half-duplex, bidirectional, ac-coupled, doubly-terminated differential pair. Manchester-II coding is used as the channel coding for the AUX_CH and supports a datarate of 1 Mbps. Fast AUX (also known as FAUX) is not supported by the DSIx6. Over the AUX_CH, the DSIx6 will always transmit the most significant bit (MSB) first and the least significant bit (LSB) last. Bit 7 is the MSB and Bit 0 is the LSB.

The AUX_CH provides a side-band channel between the DSIx6 and the downstream eDP device. Through the AUX_CH, the following is some of the information which can be obtained from or provided to the downstream eDP device:

1. eDP Downstream DPCD capabilities (number of lanes, datarate, display authenticate method, and so on)
2. EDID information of display like native resolution (obtained by I^2C over AUX transactions)
3. Link training and status
4. MCCS control

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8.4.5.2.1 Native Aux Transactions

Native Aux transaction is broken into two pieces: Request and Reply. The DSIx6 will always be the originator of the Request (sometimes under GPU control and other times under DSIx6 HW control) and the recipient of the Reply from the downstream device.

Request Syntax: <4-bit AUX_CMD> <20-bit AUX_ADDR> <7-bit AUX_LENGTH> <DATA0 … DATA15>

Reply Syntax: <4-bit AUX_CMD> <4'b0000> <DATA0 … DATA15>

Table 9. Definition of the AUX_CMD Field for Request Transactions

AUX_CMD[3:0]	DESCRIPTION
0x0	I2C-Over-Aux Write MOT = 0.
0x1	I2C-Over-Aux Read MOT = 0
0x2	I2C-Over-Aux Write Status Update MOT = 0.
0x3	Reserved. DSIx6 will ignore.
0x4	I2C-Over-Aux Write MOT = 1
0x5	I2C-Over-Aux Read MOT = 1
0x6	I2C-Over-Aux Write Status Update MOT=1.
0x7	Reserved. DSIx6 will ignore.
0x8	Native Aux Write
0x9	Native Aux Read
0xA through 0xF	Reserved. DSIx6 will ignore.

For Native Aux Reply transactions, the DSIx6 will update the status field in the CFR with command provided by the eDP device. For example, if the eDP receiver replies with a AUX_DEFER, the DSIx6 will attempt the request seven times (100 µs between each attempt) before updating the AUX_DEFR status field with 1'b1. If the eDP receiver does NOT reply before the 400-µs reply timer times out, then the DSIx6 will wait 100 µs before trying the request again. The DSIx6 will retry the request 7 times before giving up and then update the AUX_RPLY_TOUT field with 1'b1.

Example: Native Aux read of the eDP receiver capability field at DCPD address 0x00000h through 0x00008

1. Software programs the AUX_CMD field with 0x9.
2. Software programs the AUX_ADDR[19:16] field with 0x0.
3. Software programs the AUX_ADDR[15:8] field with 0x0.
4. Software programs the AUX_ADDR[7:0] field with 0x0.
5. Software programs the AUX_LENGTH field with 0x8.
6. Software sets the SEND bit.
7. DSIx6 will transmit the following packet: <SYNC> <0x90> <0x00> <0x00> <0x07> <STOP>
8. Within 300 µs, the eDP receiver will reply with the following: <SYNC> <0x00> <DATA0> <DATA1> <DATA2> <DATA3> <DATA4> <DATA5> <DATA6> <DATA7> <STOP>
9. DSIx6 will update AUX_RDATA0 through AUX_RDATA7 with the data received from the eDP receiver.
10. DSIx6 will update the AUX_LENGTH field with 0x8 indicating eight bytes we received.
11. DSIx6 will then clear the SEND bit.
12. If enabled, the IRQ will be asserted to indicate to GPU that the Native Aux Read completed.
13. GPU should read from the Interrupt Status register to see if the Native Aux Read completed successfully.

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8.4.5.3 I2C-Over-AUX

There are two methods available for I2C-Over-Aux: Direct Method (also known as Clock stretching) and Indirect Method (CFR Read/Write).

8.4.5.3.1 Direct Method (Clock Stretching)

The Direct Method (Clock Stretching) involves delaying the acknowledge or data to the I^2C Master by the DSIx6 driving the SCL pin low. Once the DSIx6 is ready to acknowledge an I^2C write transaction or return read data for a I^2C read transaction, the DSIx6 will tri-state the SCL pin therefore allowing the acknowledge cycle to complete.

In order to enable the Direct Method (Clock Stretching) software must do the following:

1. Program the 7-bit I^2C slave address(s) into the I2C_ADDR_CLAIMx register(s).
2. Enable Direct Method by setting the I2C_CLAIMx_EN bit(s)

8.4.5.3.2 Indirect Method (CFR Read/Write)

The Indirect Method is intended to be used by a GPU which does NOT support the Direct Method (Clock Stretching). The Indirect Method involves programming the appropriate CFR registers. The Indirect Method is very similar to the Native Aux method described above.

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Example of Indirect I^2C Read of the EDID.

1. Program the AUX_CMD = 0x4, AUX_ADDR[7:0] = 0x50, and AUX_LENGTH = 0x00.
2. Set the SEND bit.
3. The DSIx6 will clear the SEND bit once the Request has been ACKed.
4. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 5.
5. Program the AUX_CMD = 0x4, AUX_ADD[7:0] = 0x50, AUX_LENGTH = 0x01, and AUX_WDATA0 = 0x00.
6. Set the SEND bit.
7. The DSIx6 will clear the SEND bit once the Request has been ACKed.
8. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 9.
9. Program the AUX_CMD = 0x5, AUX_ADDR[7:0] = 0x50, and AUX_LENGTH = 0x00.
10. Set the SEND bit.
11. The DSIx6 will clear the SEND bit once the Request has been ACKed.
12. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 13.
13. Program the AUX_CMD = 0x5, AUX_ADDR[7:0] = 0x50, and AUX_LENGTH = 0x10.
14. Set the SEND bit.
15. The DSIx6 will clear the SEND bit once the Request has been ACKed.
16. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag, read data from AUX_RDATA0 through AUX_DATA15, and go to step 13.
17. If read of EDID is complete, the go to step 18. If read of EDID is not complete, then go to Step 13.
18. Program the AUX_CMD = 0x1, AUX_ADDR[7:0] = 0x50, and AUX_LENGTH = 0x00.
19. Set the SEND bit.
20. The DSIx6 will clear the SEND bit once the Request has been ACKed.
21. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 22.
22. Read of EDID finished.

Example of an indirect I^2C Write (Changing EDID Segment Pointer):

1. Program the AUX_CMD = 0x4, AUX_ADDR[7:0] = 0x30, and AUX_LENGTH = 0x00.
2. Set the SEND bit.
3. The DSIx6 will clear the SEND bit once the Request has been ACKed.
4. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 5.
5. Program the AUX_CMD = 0x4, AUX_ADDR[7:0] = 0x30, AUX_LENGTH = 0x01, and AUX_WDATA0 = 0x01.
6. Set the SEND bit.
7. The DSIx6 will clear the SEND bit once the Request has been ACKed.
8. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 9.
9. Program the AUX_CMD = 0x0, AUX_ADDR[7:0] = 0x30, and AUX_LENGTH = 0x00.
10. Set the SEND bit.
11. The DSIx6 will clear the SEND bit once the Request has been ACKed.
12. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 13.
13. Finished.

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The DSIx6 will handle all aspects of completing a request I2C-Over-Aux Read or Write. Once the requested Read or Write completes, the DSIx6 will clear the SEND bit and if an error occurred, the DSIx6 will set the NAT_I2C_FAILED flag. The NAT_I2C_FAILED flag will get set if for some reason the slave NACK the I^2C Address. If the Slave NACK without completing the entire request AUX_LENGTH, the DSIx6 will set the AUX_SHORT flag and update the AUX_LENGTH register with the amount of data completed and then clear the SEND bit. Upon clearing the SEND bit and if IRQ assertion is enabled, the DSIx6 will assert IRQ.

8.4.5.4 DisplayPort PLL

By default, the DisplayPort PLL is disabled (DP_PLL_EN = 0). To perform any operations over the DisplayPort Main link interface, the DP_PLL_EN must be enabled. Before enabling the DisplayPort PLL, software must program the DP_DATARATE register with the desired datarate. Also if SSC is going to be used, the SSC_ENABLE and SSC_SPREAD should also be programmed. Once the DP_PLL_EN is programmed to 1, software should wait until the DP_PLL_LOCK bit is set before performing any DisplayPort Main Link operations.

Depending on DSIx6 configuration, the amount of time for the DP PLL to lock will vary. Table 10 describes the lock times for various configurations.

Table 10. DP_PLL Lock Times

REFCLK_FREQ	SSC_ENABLE	MAXIMUM LOCK TIME
0	X	20 µs + (1152 × T_{REFCLK})
1	X	
2	X	
4	X	
3	1	
3	0	20 µs + (128 × T_{REFCLK})

8.4.5.5 DP Output VOD and Pre-emphasis Settings

The DSIx6 has user configurable VOD, pre-emphasis, and post-cursor2 levels. The post cursor 2 level is defined by the DP_POST_CURSOR2 level. The VOD and pre-emphasis levels are defined by the *DP Link Training Lookup Table*. The defaults settings from this lookup table are described in Table 11.

Table 11. Pre-Emphasis Default Settings

	PRE-EMPHASIS			
VOD LEVEL	LEVEL 0	LEVEL 1	LEVEI 2	LEVEL 3
Level 0 (400 mV)	Enabled (0 dB)	Enabled (3.74 dB)	Enabled (6.02 dB)	Disabled
Level 1 (600 mV)	Enabled (0 dB)	Enabled (3.10 dB)	Enabled (5.19 dB)	Disabled
Level 2 (800 mV)	Enabled (0 dB)	Enabled (2.50 dB)	Disabled	Disabled
Level 3	Disabled	Disabled	Disabled	Disabled

All of these default values can be changed by modifying the values in the DP Link Training Lookup Table

8.4.5.6 DP Main Link Configurability

The SN65DSIx6 has four physical DisplayPort lanes and each physical lane can be assigned to one specific logical lane. By default, physical lanes 0 through 3 are mapped to logical lanes 0 through 3. When routing between the SN65DSIx6 and a non-standard eDP receptacle, the physical to logical lane mapping can be changed so that PCB routing complexity is minimized. Table 12 depicts the supported logical to physical combinations based on the number of lanes programmed into the DP_NUM_LANES registers.

Table 12. Logical to Physical Supported Combinations

DP_NUM_LANES	LN0_ASSIGN	LN1_ASSIGN	LN2_ASSIGN	LN3_ASSIGN
1	0 or 1. 0 is recommended.			
2	0 or 1	0 or 1		
4	0, 1, 2, or 3	0, 1, 2, or 3	0, 1, 2, or 3	0, 1, 2, or 3

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Note the DSIx6 DisplayPort logic uses clocks from physical lane 0, and therefore these clocks from physical lane 0 will be active whenever the DP PLL is enabled. When using less than four DP lanes, the optimal power consumption is achieved by always using physical lane 0.

8.4.5.7 DP Main Link Training

The DSIx6 supports four methods to train the DisplayPort link:

1. Manual Training
2. Fast Training
3. Semi-Auto Training
4. Redriver Semi-Auto Training

NOTE

It is software responsibility to enable the Display Authentication Method in the eDP Display before any link training can be performed. The DSIx6 is enabled for ASSR authentication method by default. The DSIx6 supports Enhanced Framing. If the eDP panel supports DPCD Revision 1.2 or higher, software must enable the Enhanced Framing Mode.

8.4.5.7.1 Manual Link Training

This method is completely under software control. Software is required to handle the entire link training process.

8.4.5.7.2 Fast Link Training

In order the use the Fast Training method, there must be prior knowledge of the eDP receiver capabilities. Software must program both the DSIx6 and the eDP receiver with pre-calibrated parameters (DP_TX_SWING, DP_PRE_EMPHASIS, DP_NUM_LANES, and DP_DATARATE). Upon completing the programming of the pre-calibrated settings, software must transition the ML_TX_MODE to Fast Link Training. If TPS1 during Fast Link Training is enabled, DSIx6 will then transmit the clock recovery pattern (TPS1) for at least 500 µs and then transition ML_TX_MODE to normal. If TPS2 during Fast Link training is enabled, then after the TPS1, the DSIx6 will transmit TPS2 for 500 µs before transitioning ML_TX_MODE to normal. If neither TPS1 nor TPS2 during Fast Link Training is enabled, then the DSIx6 will transition straight to normal mode.

NOTE

GPU should determine if the eDP Display supports Fast Link training by reading the NO_AUX_HANDSHAKE_LINK_TRAINING bit at DCPD address 0x00003 bit 6. If this bit is set, then the eDP Display supports Fast Link Training.

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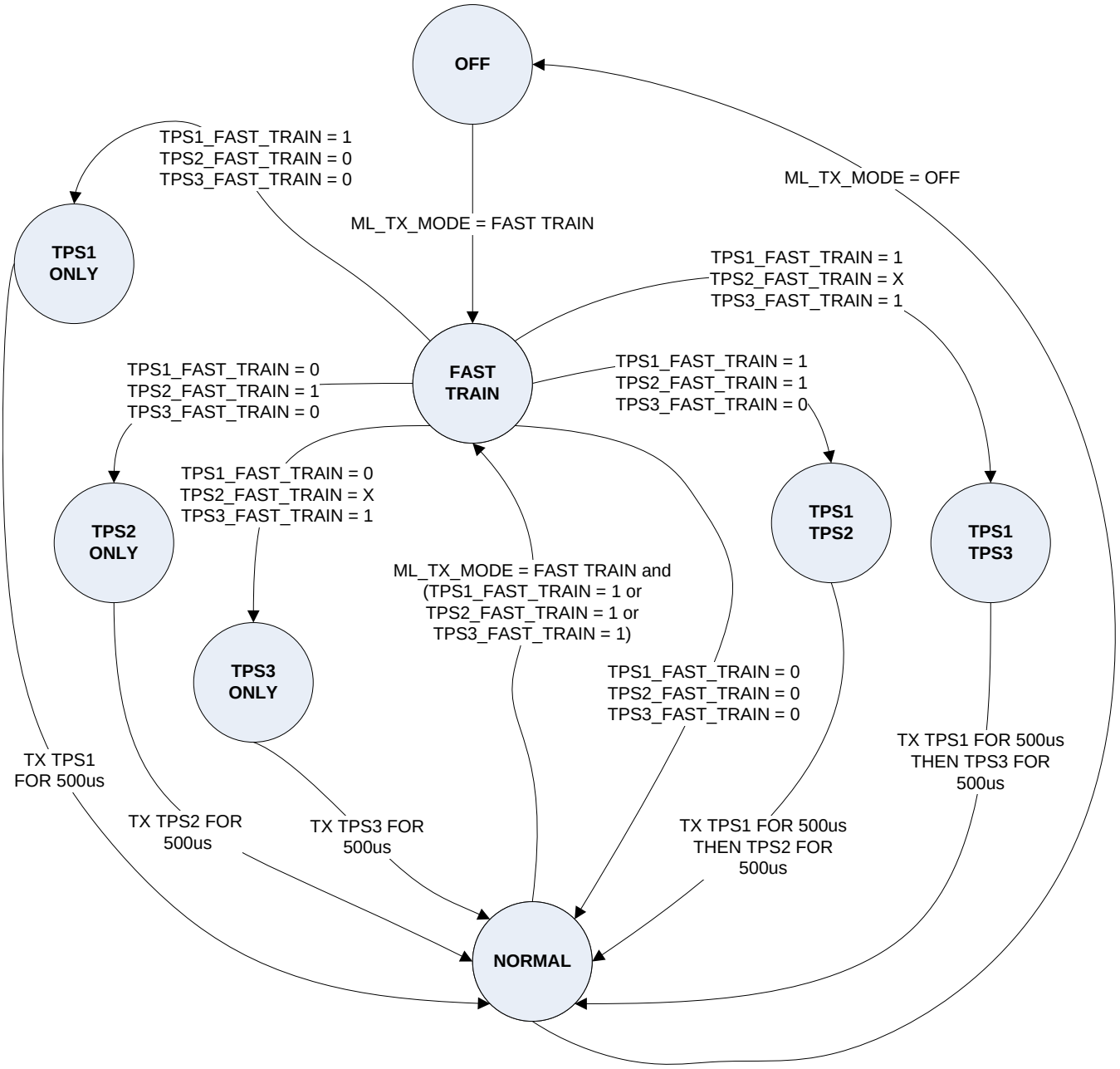


Figure 18. Fast-Link Training State Diagram

8.4.5.7.3 Semi-Auto Link Training

In order to use the semi-auto link training mode, software must first program the target DP_NUM_LANES and DP_DATARATE. Once these fields have been programmed, software can then transition the ML_TX_MODE to Semi-Auto Link Training. The DSIx6 will then attempt to train the DisplayPort link at the specified datarate and number of lanes. The DSIx6 will try all possible combinations of DP_PRE_EMPHASIS and DP_TX_SWING. Training will end as soon as a passing combination is found or all combinations have been tried and failed. The possible combinations are determined by the setting in the *DP Link Training LUT registers*. If training is successful, the DSIx6 will update the DP_POST_CURSOR2, DP_PRE_EMPHASIS, and DP_TX_SWING with

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the passing combination and then transition the ML_TX_MODE to normal. If training is unsuccessful, the DSIx6 will transition the ML_TX_MODE to Main Link Off. If enabled, the DSI will assert the IRQ pin whether or not training was successful. Software will then need to specify a different target DP_NUM_LANES and DP_DATARATE and then transition the ML_TX_MODE to Semi-Auto Link Training. This process is repeated until successful link training occurs.

NOTE

After software has enabled Semi-Auto Linking training, software must wait for the training to complete before performing any AUX transactions (Native Aux or I2C-Over-Aux).

8.4.5.7.4 Redriver Semi-Auto Link Training

In some systems a DisplayPort redriver (like the DP130) would sit between the SN65DSIx6 and the eDP panel. In these applications, it is important to train the DisplayPort link between the DSIx6 and the redriver to one setting and training the link between the redriver and the eDP panel to a different setting. For this application, Redriver Semi-Auto Link training can be used.

Redriver Semi-Auto Link training is essentially the same as Semi-Auto Link training with one major difference. That difference is Redriver Semi-Auto Link Training will never change the DP_TX_SWING, DP_PRE_EMPHASIS, and DP_POST_CURSOR2 levels being driven by the SN65DSIx6. These settings will always stay fixed to their programmed values. The SN65DSIx6 will still send all aux requests to the eDP panel DPCD registers. The redriver will snoop these aux transactions and train the link between it and the eDP panel.

8.4.5.8 Panel Size vs DP Configuration

Table 13 is provided as a guideline of the best DP configuration (datarate and number of lanes) for a specific video resolution and color depth. The preferred (P) setting assumes the eDP panel supports the 5.4 Gbps datarate.

Table 13. Recommended DP Configuration

COMMON VIDEO MODE NAME	VESA® TIMING NAME (HORIZONTAL × VERTICAL AT FRAME RATE)	PIXEL CLOCK RATE (MHz)	RGB666				RGB888			
			STREAM BIT RATE (Gbps)	REQUIRED NUMBER OF DP LANES AT			STREAM BIT RATE (Gbps)	REQUIRED NUMBER OF DP LANES AT		
				1.62 Gbps	2.7 Gbps	5.4 Gbps		1.62 Gbps	2.7 Gbps	5.4 Gbps
XGA	1024 × 768 at 60 Hz CVT (reduced blanking)	56	1.01	1 (P)	1	1	1.34	2	1 (P)	1
WXGA	1280 × 768 at 60 Hz CVT (reduced blanking)	68	1.23	1 (P)	1	1	1.64	2	1 (P)	1
WXGA	1280 × 800 at 60 Hz CVT (reduced blanking)	71	1.28	1 (P)	1	1	1.7	2	1 (P)	1
HD	1366 × 768 at 60 Hz	86	1.54	2	1 (P)	1	2.05	2	1 (P)	1
WXGA+	1440 × 900 at 60 Hz CVT (reduced blanking)	89	1.6	2	1 (P)	1	2.13	2	1 (P)	1
SXGA+	1400 × 1050 at 60 Hz CVT (reduced blanking)	101	1.82	2	1 (P)	1	2.42	2	2	1 (P)
HD+	1600 × 900 at 60 Hz (reduced blanking)	108	1.94	2	1 (P)	1	2.59	4	2	1 (P)
WSXGA+	1680 × 1050 at 60 Hz CVT (reduced blanking)	119	2.12	2	1 (P)	1	2.86	4	2	1 (P)
UXGA	1600 × 1200 at 60 Hz CVT (reduced blanking)	130	2.34	2	2	1 (P)	3.13	4	2	1 (P)
FHD	1920 × 1080 at 60 Hz	149	2.67	4	2	1 (P)	3.56	4	2	1 (P)
WUXGA	1920 × 1200 at 60 Hz CVT (reduced blanking)	154	2.77	4	2	1 (P)	3.7	4	2	1 (P)
WQXGA	2560 × 1600 at 60 Hz CVT (reduced blanking)	269	4.83	4	4	2 (P)	6.44	NA	4	2 (P)

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8.4.5.9 Panel Self Refresh (PSR)

The panel self refresh (PSR) feature enables system-level power savings when the displayed image remains static for multiple display frames. The eDP display (sink) stores a static image locally in a remote frame buffer (RFB) within the sink and displays this image from the RFB while the eDP Main link may be turned off (SUSPEND asserted). The DSIx6 may turn off other features in addition to the main link for further power savings. The system software makes the determination on what power savings must be implemented (like shutdown of DP link (SUSPEND asserted), shutdown of entire SN65DSIx6 (EN deasserted), and so on). When implementing PSR, any power savings must not impact system responsiveness to user input that affects the display, such as cursor movement.

In the list below are the requirements the GPU and system designer must meet when implementing PSR:

1. Updates to the remote frame buffer located in sink must include two of the same static frame. The reason for this requirement is the DSIx6 will never pass the first frame received on the DSI interface to the DisplayPort interface. All subsequent frames will be passed to the DisplayPort interface.
2. If PWM signal is controlled directly by the DSIx6 and SUSPEND asserted, the REFCLK must remain active.

8.4.5.10 Secondary Data Packet (SDP)

All secondary data packets (SDP) are provided to the DSIx6 through the DSI interface during vertical blanking periods. (SDP are not supported using the I^2C interface.) The DSIx6 will wrap the SDP provided to the DSI interface with the SS and SE control symbols and then transmit over the DP interface during the vertical blanking period. Secondary data packets are used to pass non-active video data to the eDP sink. Information like stereo video attributes and/or PSR-state data is sent using SDP. When SDP is used for stereo video attributes, software must program the MSA_MISC1_2_1 register with a zero.

The DSIx6 requires that the SDP be provided to the DSI interface in the following order:

1. 4 Bytes of Header (HB0 through HB3)
2. 4 Bytes of Header parity (PB0 through PB3)
3. 8 Bytes of Data (DB0 through DB7)
4. 2 Bytes of Data parity (PB4 and PB5)
5. 8 Bytes of Data (DB8 through DB15)
6. 2 Bytes of Data parity (PB6 and PB7)

For data payloads greater than 16 bytes, data must be provided in multiples of 8 bytes with of 2 bytes of parity. If the final multiple is less than 8, zero padding must be used to fill the remaining data positions.

8.4.5.11 Color Bar Generator

The DSIx6 implements a SMPTE color bar. The color bar generator does not require the DSI interface. All color bars will be transmitted at a 60-Hz frame rate. The active video size of the Color bar is determined by the values programmed into the Video Registers.

The color bar generator supports the following color bars for both horizontal and vertical direction:

1. 8 color {White, Yellow, Cyan, Green, Magenta, Red, Blue, Black}
2. 8 gray scale {White, Light Gray, Gray, Light Slate Gray, Slate Gray, Dim Gray, Dark Slate Gray, Black}
3. 3 color {Red, Green, Blue}
4. Stripes {White, Black}. Every other pixel (pixel1 = white, pixel2 = black, pixel3 = white, and so on).

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Table 14. 24-bit RGB Color Codes

COLOR	RED	GREEN	BLUE
Black	0x00	0x00	0x00
Red	0xFF	0x00	0x00
Green	0x00	0xFF	0x00
Blue	0x00	0x00	0xFF
Yellow	0xFF	0xFF	0x00
White	0xFF	0xFF	0xFF
Magenta	0xFF	0x00	0xFF
Cyan	0x00	0xFF	0xFF
Gray	0xBE	0xBE	0xBE
Light Gray	0xD3	0xD3	0xD3
Light Slate Gray	0x77	0x88	0x99
Slate Gray	0x70	0x80	0x90
Dim Gray	0x69	0x69	0x69
Dark Slate Gray	0x2F	0x4F	0x4F

NOTE

Both VSTREAM_ENABLE and Color_Bar_En must be set in order to transmit Color Bar over DisplayPort interface. Also, ML_TX_MODE must be programmed to Normal Mode.

8.4.5.12 DP Pattern

DSIx6 supports the training and compliance patterns mentioned in Table 15. The value of ML_TX_MODE register controls what pattern will be transmitted.

Table 15. DP Training and Compliance Patterns

PATTERN	[DP] SECTION
IDLE	5.1.3.1
TPS1	Table 3-16 and 2.9.3.6.1
TPS2	Table 3-16
TPS3	Table 3-16
PRBS7	Table 2-75 address 0x00102.
HBR2 Compliance Eye(1)	2.9.3.6.5
Symbol Error Rate Measurement(1)	2.9.3.6.2 and 2.10.4
80 bit Customer Pattern	2.9.3.6.4

(1) HBR2 Compliance Eye and Symbol Error Rate Measurement require TEST2 pin to be pulled up before the assertion of EN and software program a 1 to bit 0 of offset 0x16 at Page 7 followed by a write of 0 to bit 0 of offset 0x5A at Page 0 before writing either a 0x6 or 0x7 to ML_TX_MODE register.

8.4.5.12.1 HBR2 Compliance Eye

When the ML_TX_MODE is set to HBR2 Compliance Eye, the SN65DSIx6 will use the value programmed into the HBR2_COMPEYEPAT_LENGTH register to determine the number of scrambled 0 before transmitting an Enhanced Frame Scrambler Reset sequence. The Enhanced Framing Scrambler Reset sequence used is determined by ENCH_FRAME_PATT register.

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Table 16. Common 80-bit Custom Patterns

Byte#	PLTPAT	PCTPAT
0	0x1F	0x1F
1	0x7C	0x7C
2	0xF0	0xF0
3	0xC1	0xC1
4	0x07	0xCC
5	0x1F	0xCC
6	0x7C	0xCC
7	0xF0	0x4C
8	0xC1	0x55
9	0x07	0x55

8.4.5.12.2 80-Bit Custom Pattern

The 80-bit Custom pattern is used for generating the Post Cursor2 Test Pattern (PCTPAT) and the Pre-Emphasis Level Test Pattern (PLTPAT). The SN65DSIx6 will continuously transmit the value programmed into the *80BIT_CUSTOM_PATTERN* registers when the ML_TX_MODE is programmed to 80-bit Custom Pattern. The SN65DSIx6 will always transmit over the enabled DisplayPort Lanes the LSB of the byte first and the MSB of the byte last. The byte at the lowest address is transmitted first.

8.4.5.13 BPP Conversion

The SN65DSIx6 transmits either 18bpp or 24bpp over the DisplayPort interface based on the DP_18BPP_EN bit. When this bit is cleared and 18 bpp is being received on DSI interface, the SN65DSIx6 performs the following translation of the 18 bpp into 24 bpp: new[7:0] = {original[5:0], original[5:4]}. When the DP_18BPP_EN bit is set and 24 bpp is being received on DSI interface, the SN65DSIx6 performs the following translation of 24 bpp to 18 bpp: new[5:0] = original[7:2].

8.5 Programming

8.5.1 Local I^2C Interface Overview

The SN65DSIx6 local I^2C interface is enabled when EN is input high, access to the CSR registers is supported during ultra-low power state (ULPS). The SCL and SDA terminals are used for I^2C clock and I^2C data, respectively. The SN65DSIx6 I^2C interface conforms to the two-wire serial interface defined by the I^2C Bus Specification, Version 2.1 (January 2000), and supports fast mode transfers up to 400 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7-bit device address for SN65DSIx6 is factory preset to 010110X with the least significant bit being determined by the ADDR control input. Table 17 clarifies the SN65DSIx6 target address.

Table 17. SN65DSIx6 I^2C Target Address Description

SN65DSIx6 I^2C TARGET ADDRESS							
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	1	0	1	1	0	ADDR	0/1
When ADDR = 1, Address Cycle is 0x5A (Write) and 0x5B (Read) When ADDR = 0, Address Cycle is 0x58 (Write) and 0x59 (Read)							

The following procedure is followed to write to the SN65DSIx6 I^2C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSIx6 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The master presents the subaddress (I^2C register within SN65DSIx6) to be written, consisting of one byte of data, MSB-first.
3. The master presents the subaddress (I^2C register within SN65DSIx6) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSIx6 acknowledges the subaddress cycle.

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5. The master presents the first byte of data to be written to the I^{2}C register.
6. The SN65DSIx6 acknowledges the byte transfer.
7. The master terminates the write operation by generating a stop condition (P).
8. The master terminates the write operation by generating a stop condition (P).

The following procedure is followed to read the SN65DSIx6 I^{2}C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SN65DSIx6 7-bit address and a one-value W/R bit to indicate a read cycle.
2. The SN65DSIx6 acknowledges the address cycle.
3. The SN65DSIx6 transmit the contents of the memory registers MSB-first starting at register 00h or last read subaddress+1. If a write to the SN65DSIx6 I^{2}C register occurred prior to the read, then the SN65DSIx6 will start at the subaddress specified in the write.
4. The SN65DSIx6 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I^{2}C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the SN65DSIx6 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure is followed for setting a starting subaddress for I^{2}C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSIx6 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The SN65DSIx6 acknowledges the address cycle.
3. The master presents the subaddress (I^{2}C register within SN65DSIx6) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSIx6 acknowledges the subaddress cycle.
5. The master terminates the write operation by generating a stop condition (P).

NOTE

If no subaddressing is included for the read procedure, then reads start at register offset 00h and continue byte by byte through the registers until the I^{2}C master terminates the read operation. If a I^{2}C write occurred prior to the read, then the reads start at the subaddress specified by the write.

8.6 Register Map

Many of the SN65DSIx6 functions are controlled by the Control and Status Registers (CSR). All CSR registers are accessible through the local I^{2}C interface or through DSI interface.

Reads from reserved fields not described return zeros, and writes to read-only reserved registers are ignored. Writes to reserved register which are marked with W will produce unexpected behavior.

Table 18. Bit Field Access Tag Descriptions

ACCESS TAG	NAME	MEANING
R	Read	The field may be read by software
W	Write	The field may be written by software
S	Set	The field may be set by a write of one. Writes of zeros to the field have no effect.
C	Clear	The field may be cleared by a write of one. Writes of zero to the field have no effect.
U	Update	Hardware may autonomously update this field.
NA	No Access	Not accessible or not applicable

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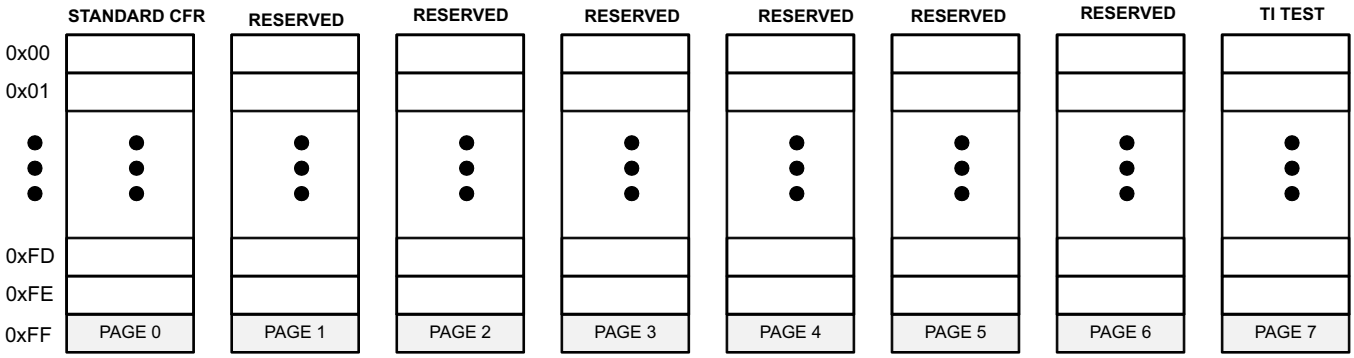


Figure 19. Register Map

8.6.1 Standard CFR Registers (PAGE 0)

Table 19. CSR Bit Field Definitions—ID Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x00 through 0x07	7:0	DEVICE_ID For the SN65DSIx6 these fields return a string of ASCII characters returning DSI86 preceded by three space characters. Addresses 0x07 through 0x00 = {0x20, 0x20, 0x20, 0x44, 0x53, 0x49, 0x38, 0x36}	
0x08	7:0	DEVICE_REV Device revision; returns 0x02.	

Table 20. CSR Bit Field Definitions—Reset and Clock Registers

ADDRESS	BIT(S)	DESCRIPTION		ACCESS
0x09	0	SOFT_RESET This bit automatically clears when set to 1 and returns zeros when read. This bit must be set after the CSRs are updated. This bit must also be set after making any changes to the DIS clock rate or after changing between DSI burst and non-burst modes. 0 = No action (default) 1 = Reset device to default condition excluding the CSR bits.		W
0x0A	7	DP_PLL_LOCK 0 = DP_PLL not locked (default) 1 = DP_PLL locked		R
	6:4	Reserved		R
	3:1	REFCLK_FREQ. This field is used to control the clock source and frequency select inputs to the DP PLL. Any change in this field will cause the DP PLL to reacquire lock. On the rising edge of EN the DSIx6 will sample the state of GPIO[3:1] as well as detect the presence or absence of a clock on REFCLK pin. The outcome will determine whether the clock source for the DP PLL is from the REFCLK pin or the DSIA CLK. The outcome will also determine the frequency of the clock source.		RWU
		DPPLL_CLK_SRC = 0	DPPLL_CLK_SRC = 1	
		000 = 12 MHz 001 = 19.2 MHz (Default) 010 = 26 MHz 011 = 27 MHz 100 = 38.4 MHz All other combinations are 19.2 MHz	000 = Continuous DSIA CLK at 468 MHz 001 = Continuous DSIA CLK at 384 MHz 010 = Continuous DSIA CLK at 416 MHz 011 = Continuous DSIA CLK at 486 MHz 100 = Continuous DSIA CLK at 460.8 MHz All other combinations are DSIA CLK at 384 MHz.	
	0	DPPLL_CLK_SRC. This status field indicates the outcome of the clock detection on the REFCLK pin. 0 = Clock detected on REFCLK pin. DP_PLL clock derived from input REFCLK (default). 1 = No clock detected on REFCLK pin. DP_PLL clock derived from MIPI D-PHY channel A HS continuous clock		RU
0x0B	7:0	Reserved		R
0x0C	7:0	Reserved		R

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Table 20. CSR Bit Field Definitions—Reset and Clock Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x0D	0	DP_PLL_EN When this bit is set, the DP PLL is enabled 0 = PLL disabled (default) 1 = PLL enabled	RW

Table 21. CSR Bit Field Definitions—DSI Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x10	7	LEFT_RIGHT_PIXELS This bit selects the pixel arrangement in dual-channel DSI implementations. 0 = DSI channel A receives ODD pixels and channel B receives EVEN (default) 1 = DSI channel A receives LEFT image pixels and channel B receives RIGHT image pixels	RW
	6:5	DSI_CHANNEL_MODE 00 = Dual-channel DSI receiver 01 = Single channel DSI receiver A (default) 10 = Reserved. 11 = Reserved	RW
	4:3	CHA_DSI_LANES This field controls the number of lanes that are enabled for DSI Channel A. 00 = Four lanes are enabled 01 = Three lanes are enabled 10 = Two lanes are enabled 11 = One lane is enabled (default) Note: Unused DSI inputs pins on the SN65DSIx6 should be left unconnected.	RW
	2:1	CHB_DSI_LANES This field controls the number of lanes that are enabled for DSI Channel B. 00 = Four lanes are enabled 01 = Three lanes are enabled 10 = Two lanes are enabled 11 = One lane is enabled (default) Note: Unused DSI inputs pins on the SN65DSIx6 should be left unconnected.	RW
	0	SOT_ERR_TOL_DIS 0 = Single bit errors are tolerated for the start of transaction SoT leader sequence (default) 1 = No SoT bit errors are tolerated	RW
0x11	7:6	CHA_DSI_DATA_EQ This field controls the equalization for the DSI Channel A Data Lanes 00 = No equalization (default) 01 = Reserved 10 = 1 dB equalization 11 = 2 dB equalization	RW
	5:4	CHB_DSI_DATA_EQ This field controls the equalization for the DSI Channel B Data Lanes 00 = No equalization (default) 01 = Reserved 10 = 1 dB equalization 11 = 2 dB equalization	RW
	3:2	CHA_DSI_CLK_EQ This field controls the equalization for the DSI Channel A Clock 00 = No equalization (default) 01 = Reserved 10 = 1 dB equalization 11 = 2 dB equalization	RW
	1:0	CHB_DSI_CLK_EQ This field controls the equalization for the DSI Channel A Clock 00 = No equalization (default) 01 = Reserved. 10 = 1 dB equalization 11 = 2dB equalization	RW

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Table 21. CSR Bit Field Definitions—DSI Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x12	7:0	CHA_DSI_CLK_RANGE This field specifies the DSI clock frequency range in 5-MHz increments for DSI Channel A clock. The SN65DSIx6 estimates the DSI clock frequency using the REFCLK frequency determined at the rising edge of EN and updates this field accordingly. Software can override this value. If the CHA_DSI_CLK_RANGE is not loaded before receiving the first DSI packet, the SN65DSIx6 uses the first packet to estimate the DSI_CLK frequency and loads this field with this estimate. This first packet may not be received; thus, the host should send a first dummy packet (such as DSI read or write to register 0x00). This field may be written by the host at any time. Any non-zero value written by the host is used instead of the automatically-estimated value. 0x00 through 0x07: Reserved 0x08 = 40 ≤ frequency < 45 MHz 0x09 = 45 ≤ frequency < 50 MHz . . . 0x96 = 750 ≤ frequency < 755 MHz 0x97 through 0xFF: Reserved	RWU
0x13	7:0	CHB_DSI_CLK_RANGE This field specifies the DSI clock frequency range in 5-MHz increments for DSI Channel B clock. The SN65DSIx6 estimates the DSI clock frequency using the REFCLK frequency determined at the rising edge of EN and updates this field accordingly. Software can override this value. If the CHB_DSI_CLK_RANGE is not loaded before receiving the first DSI packet, the SN65DSIx6 uses the first packet to estimate the DSI_CLK frequency and loads this field with this estimate. This first packet may not be received; thus, the host should send a first dummy packet (such as DSI read or write to register 0x00). This field may be written by the host at any time. Any non-zero value written by the host is used instead of the automatically-estimated value. 0x00 through 0x07: Reserved 0x08 = 40 ≤ frequency < 45 MHz 0x09 = 45 ≤ frequency < 50 MHz . . . 0x96 = 750 ≤ frequency < 755 MHz 0x97 through 0xFF: Reserved	RWU

Table 22. CSR Bit Field Definitions—Video Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x20	7:0	CHA_ACTIVE_LINE_LENGTH_LOW When the SN65DSIx6 is configured for a single DSI input, this field controls the length in pixels of the active horizontal line for Channel A. When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of odd pixels in the active horizontal line that are received on DSI channel A. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of left pixels in the active horizontal line that are received on DSI channel A. The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00. **Note**: When the SN65DSIx6 is configured for dual DSI inputs in Left/Right mode and LEFT_CROP field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied.	RW
0x21	3:0	CHA_ACTIVE_LINE_LENGTH_HIGH When the SN65DSIx6 is configured for a single DSI input, this field controls the length in pixels of the active horizontal line for Channel A. When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of odd pixels in the active horizontal line that are received on DSI channel A. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of left pixels in the active horizontal line that are received on DSI channel A. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00. **Note**: When the SN65DSIx6 is configured for dual DSI inputs in Left/Right mode and LEFT_CROP field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied.	RW

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Table 22. CSR Bit Field Definitions—Video Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x22	7:0	CHB_ACTIVE_LINE_LENGTH_LOW When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of even pixels in the active horizontal line that are received on DSI channel B. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of right pixels in the active horizontal line that are received on DSI channel B. The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00. **Note**: When the SN65DSIx6 is configured for dual DSI inputs in Left/Right mode and RIGHT_CROP field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied.	RW
0x23	3:0	CHB_ACTIVE_LINE_LENGTH_HIGH When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of even pixels in the active horizontal line that are received on DSI channel B. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of right pixels in the active horizontal line that are received on DSI channel B. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00. **Note**: When the SN65DSIx6 is configured for dual DSI inputs in Left/Right mode and RIGHT_CROP field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied.	RW
0x24	7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW This field controls the vertical display size in lines for Channel A. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size. This field defaults to 0x00.	RW
0x25	3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH This field controls the vertical display size in lines for Channel A. The value in this field is the upper 4 bits of the 12-bit value for the vertical display size. This field defaults to 0x00.	RW
0x26 through 0x2B	7:0	Reserved	R
0x2C	7:0	CHA_HSYNC_PULSE_WIDTH_LOW This field controls the width in pixel clocks of the HSync Pulse Width for Channel A. The value in this field is the lower 8 bits of the 15-bit value for HSync Pulse width. This field defaults to 0x00.	RW
0x2D	7	CHA_HSYNC_POLARITY. 0 = Active High Pulse. Synchronization signal is high for the sync pulse width. (default) 1 = Active Low Pulse. Synchronization signal is low for the sync pulse width.	RW
	6:0	CHA_HSYNC_PULSE_WIDTH_HIGH This field controls the width in pixel clocks of the HSync Pulse Width for Channel A. The value in this field is the upper 7 bits of the 15-bit value for HSync Pulse width. This field defaults to 0x00.	RW
0x2E through 0x2F	7:0	Reserved.	R
0x30	7:0	CHA_VSYNC_PULSE_WIDTH_LOW This field controls the length in lines of the VSync Pulse Width for Channel A. The value in this field is the lower 8 bits of the 15-bit value for VSync Pulse width. This field defaults to 0x00. The total size of the VSYNC pulse width must be at least 1 line.	RW
0x31	7	CHA_VSYNC_POLARITY. 0 = Active High Pulse. Synchronization signal is high for the sync pulse width. (Default) 1 = Active Low Pulse. Synchronization signal is low for the sync pulse width.	RW
	6:0	CHA_VSYNC_PULSE_WIDTH_HIGH This field controls the width in lines of the VSync Pulse Width for Channel A. The value in this field is the upper 7 bits of the 15-bit value for VSync Pulse width. This field defaults to 0x00. The total size of the VSYNC pulse width must be at least 1 line.	RW
0x32 through 0x33	7:0	Reserved.	R

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Table 22. CSR Bit Field Definitions—Video Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x34	7:0	CHA_HORIZONTAL_BACK_PORCH This field controls the time in pixel clocks between the end of the HSync Pulse and the start of the active video data for Channel A. This field defaults to 0x00.	RW
0x35	7:0	Reserved.	R
0x36	7:0	CHA_VERTICAL_BACK_PORCH This field controls the number of lines between the end of the VSync Pulse and the start of the active video data for Channel A. This field defaults to 0x00. The total size of the Vertical Back Porch must be at least 1 line.	RW
0x37	7:0	Reserved	R
0x38	7:0	CHA_HORIZONTAL_FRONT_PORCH This field controls the time in pixel clocks between the end of the active video data and the start of the HSync Pulse for Channel A. This field defaults to 0x00.	RW
0x39	7:0	Reserved.	R
0x3A	7:0	CHA_VERTICAL_FRONT_PORCH This field controls the number of lines between the end of the active video data and the start of the VSync Pulse for Channel A. This field defaults to 0x00. The total size of the Vertical Front Porch must be at least 1 line.	RW
0x3B	7:0	Reserved	R
0x3C	4	COLOR_BAR_EN. When this bit is set, the SN65DSIx6 generates a video test pattern on DisplayPort based on the values programmed into the Video Registers for Channel A. 0 = Transmit of SMPTE color bar disabled. (default) 1 = Transmit of SMPTE color bar enabled.	RW
	3	Reserved.	R
	2:0	COLOR_BAR_PATTERN. 000 = Vertical Colors: 8 Color (Default) 001 = Vertical Colors: 8 Gray Scale 010 = Vertical Colors: 3 Color 011 = Vertical Colors: Stripes 100 = Horizontal Colors: 8 Color 101 = Horizontal Colors: 8 Gray Scale 110 = Horizontal Colors: 3 Color 111 = Horizontal Colors: Stripes	RW
0x3D	7:0	RIGHT_CROP. This field controls the number of pixels removed from the beginning of the active video line for DSI Channel B. This field only has meaning if the LEFT_RIGHT_PIXELS = 1. This field defaults to 0x00. **Note**: When the SN65DSIx6 is configured for dual DSI inputs in Left/Right mode and this field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied.	RW
0x3E	7:0	LEFT_CROP. This field controls the number of pixels removed from the end of the active video line for DSI Channel A. This field only has meaning if the LEFT_RIGHT_PIXELS = 1. This field defaults to 0x00. **Note**: When the SN65DSIx6 is configured for dual DSI inputs in Left/Right mode and this field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied.	RW

Table 23. CSR Bit Field Definitions—DisplayPort Specific Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x40	7:0	MVID[7:0]	RU
0x41	7:0	MVID[15:8]	RU
0x42	7:0	MVID[23:16]	RU
0x43	7:0	NVID[7:0]	RU
0x44	7:0	NVID[15:8]	RU
0x45	7:0	NVID[23:16]	RU

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Table 23. CSR Bit Field Definitions—DisplayPort Specific Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x46	7:0	Htotal[7:0]. Defaults to 0x00.	RU
0x47	7:0	Htotal[15:8]. Defaults to 0x00.	RU
0x48	7:0	Vtotal[7:0]. Defaults to 0x00.	RU
0x49	7:0	Vtotal[15:8]. Defaults to 0x00.	RU
0x4A	7:0	Hstart[7:0]. Defaults to 0x00.	RU
0x4B	7:0	Hstart[15:8]. Defaults to 0x00.	RU
0x4C	7:0	Vstart[7:0]. Defaults to 0x00.	RU
0x4D	7:0	Vstart[15:8]. Defaults to 0x00.	RU
0x4E	7:0	HSW[7:0]. Defaults to 0x00.	RU
0x4F	7:0	HSP_HSW[15:8]. Defaults to 0x00.	RU
0x50	7:0	VSW[7:0]. Defaults to 0x00.	RU
0x51	7:0	VSP_VSW[15:8]. Defaults to 0x00.	RU
0x52	7:0	Hwidth[7:0]. Defaults to 0x00.	RU
0x53	7:0	Hwidth[15:8]. Defaults to 0x00.	RU
0x54	7:0	Vheight[7:0]. Defaults to 0x00.	RU
0x55	7:0	Vheight[15:8]. Defaults to 0x00.	RU
0x56	7:5	MSA_MISC0_7_5. This field represents the bits per color. 000 = 6 bits per color. 001 = 8 bits per color (Default) Others are not supported.	RU
	4	MSA_MISC0_4. Defaults to zero.	RW
	3	MSA_MISC0_3. Defaults to zero.	RW
	2:1	MSA_MISC0_2_1. This field indicates the format of the data is either RGB, YCbCr(422 or 444). The DSIx6 only supports RGB so this field will always be 0x0. 00 = RGB (default)	RU
	0	MSA_MISC0_0. 0 = Link clock and stream clock are async. (default) 1 = Link clock and stream clock are sync.	RU
0x57	7	MSA_MISC1_7. Y-only video. The DSIx6 does not support this feature so this field defaults to zero.	R
	6:3	MSA_MISC1_6_3. Reserved. Default to 0x0.	R
	2:1	MSA_MISC1_2_1. This field is the stereo video attribute data. 00 = No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done using SDP called Video Stream Configuration (VSC) packet. (Default) 01 = Next frame is Right Eye. 10 = Reserved. 11 = Next Frame is Left Eye.	RW
	0	MSA_MISC1_0. Default to zero.	R
0x58	7	TU_SIZE_OVERRIDE. This field is used to control whether DSIx6 determines Transfer Unit Size or the size is determine by the TU_SIZE field. 0 = DSIx6 determines TU size. (default) 1 = TU size is determined by TU_SIZE field.	RW
	6:0	TU_SIZE. This field is used to program the DisplayPort transfer Unit size. Valid values are between 32 (0x20) and 64 (0x40). Default is 64. When DSIx6 determines the TU size, the DSIx6 will update this register with the value determined by hardware. SN65DSIx6 will interpret all invalid values to be a transfer unit size of 64 (0x40).	RWU

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Table 23. CSR Bit Field Definitions—DisplayPort Specific Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x59	7:6	LN3_ASSIGN. See the *DP Main Link Configurability* section in this document for supported logical to physical combinations based on DP_NUM_LANES. 00 = Logical Lane3 is routed to physical ML0P/N pins 01 = Logical Lane3 is routed to physical ML1P/N pins 10 = Logical Lane3 is routed to physical ML2P/N pins 11 = Logical Lane3 is routed to physical ML3P/N pins (default)	RW
	5:4	LN2_ASSIGN. See the *DP Main Link Configurability* section in this document for supported logical to physical combinations based on DP_NUM_LANES 00 = Logical Lane2 is routed to physical ML0P/N pins 01 = Logical Lane2 is routed to physical ML1P/N pins 10 = Logical Lane2 is routed to physical ML2P/N pins (default) 11 = Logical Lane2 is routed to physical ML3P/N pins.	RW
	3:2	LN1_ASSIGN. See the *DP Main Link Configurability* section in this document for supported logical to physical combinations based on DP_NUM_LANES 00 = Logical Lane1 is routed to physical ML0P/N pins 01 = Logical Lane1 is routed to physical ML1P/N pins (default) 10 = Logical Lane1 is routed to physical ML2P/N pins 11 = Logical Lane1 is routed to physical ML3P/N pins.	RW
	1:0	LN0_ASSIGN. See the *DP Main Link Configurability* section in this document for supported logical to physical combinations based on DP_NUM_LANES. 00 = Logical Lane0 is routed to physical ML0P/N pins (default) 01 = Logical Lane0 is routed to physical ML1P/N pins 10 = Logical Lane0 is routed to physical ML2P/N pins 11 = Logical Lane0 is routed to physical ML3P/N pins	RW
0x5A	7	ML3_POLR. When this field is set, the polarity of ML3, specified by LN3_ASSIGN, is inverted. 0 = ML3 polarity is normal (default) 1 = ML3 polarity is inverted.	RW
	6	ML2_POLR. When this field is set, the polarity of ML2, specified by LN2_ASSIGN, is inverted. 0 = ML2 polarity is normal (default) 1 = ML2 polarity is inverted.	RW
	5	ML1_POLR. When this field is set, the polarity of ML1, specified by LN1_ASSIGN, is inverted. 0 = ML1 polarity is normal (default) 1 = ML1 polarity is inverted.	RW
	4	ML0_POLR. When this field is set, the polarity of ML0, specified by LN0_ASSIGN, is inverted. 0 = ML0 polarity is normal (default) 1 = ML0 polarity is inverted.	RW
	3	VSTREAM_ENABLE. The DSIx6 will clear this field if the following conditions are true: Exiting SUSPEND and the PSR_EXIT_VIDEO bit is cleared. 0 = Video data from DSI is not passed to DisplayPort (default). IDLE pattern will be sent instead. 1 = Video data from DSI is passed to DisplayPort	RWU
	2	ENH_FRAME_ENABLE. 0 = Disable Enhanced Framing. 1 = Enable Enhanced Framing (default)	RWU
	1:0	ASSR_CONTROL.This field controls the scrambler seed used. Standard DP scrambler seed value is 0xFFFF. The ASSR seed value is 0xFFFF. This field is R/W if TEST2 pin is sampled high on rising edge of EN and bit 0 of offset 0x16 in Page 7 is set. Otherwise this field is read-only. 00 = Standard DP Scrambler Seed. 01 = Alternative Scrambler Seed Reset (Default). 10 = Reserved. 11 = Reserved.	R/RW
0x5B	1	ENCH_FRAME_PATT 0 = SR BF BF SR or BS BF BF BS (Default) 1 = SR CP CP SR or BS CP CP BS	RW
	0	DP_18BPP_EN. If this field is set, then 18BPP format will be transmitted over eDP interface regardless of the DSI pixel stream data type format. 0 = 24BPP RGB. (default) 1 = 18BPP RGB	RW

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Table 23. CSR Bit Field Definitions—DisplayPort Specific Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x5C	4	HPD. Returns the state of the HPD pin after 100-ms de-bounce	RU
	0	HPD_DISABLE 0 = HPD input is enabled. (default) 1 = HPD input is disabled	RW

Table 24. CSR Bit Field Definitions—GPIO Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x5E	7	GPIO4_INPUT. Returns the state of the GPIO4 pin.	RU
	6	GPIO3_INPUT. Returns the state of the GPIO3 pin.	RU
	5	GPIO2_INPUT. Returns the state of the GPIO2 pin.	RU
	4	GPIO1_INPUT. Returns the state of the GPIO1 pin.	RU
	3	GPIO4_OUTPUT. When GPIO4 Control is programmed to an Output, this field will control the output level of GPIO4. 0 = GPIO4 is driven to 0 (GND). (default) 1 = GPIO4 is driven to 1.	RW
	2	GPIO3_OUTPUT. When GPIO3 Control is programmed to an Output, this field will control the output level of GPIO3. 0 = GPIO3 is driven to 0 (GND). (default) 1 = GPIO3 is driven to 1.	RW
	1	GPIO2_OUTPUT. When GPIO2 Control is programmed to an Output, this field will control the output level of GPIO3. 0 = GPIO2 is driven to 0 (GND). (default) 1 = GPIO2 is driven to 1.	RW
	0	GPIO1_OUTPUT. When GPIO1 Control is programmed to an Output, this field will control the output level of GPIO1. 0 = GPIO1 is driven to 0 (GND). (default) 1 = GPIO1 is driven to 1.	RW
0x5F	7:6	GPIO4_CTRL 00 = Input (Default) 01 = Output 10 = PWM 11 = Reserved.	RW
	5:4	GPIO3_CTRL 00 = Input (Default) 01 = Output 10 = DSIA HSYNC or VSYNC 11 = Reserved	RW
	3:2	GPI02_CTRL 00 = Input (Default) 01 = Output 10 = DSIA VSYNC 11 = Reserved	RW
	1:0	GPIO1_CTRL 00 = Input (Default) 01 = Output 10 = SUSPEND Input 11 = Reserved	RW

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Table 25. CSR Bit Field Definitions—Native and I2C-Over-Aux Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x60	7:1	I2C_ADDR_CLAIM1. When I2C_CLAIM1_EN is enabled, the DSIx6 will claim I^2C slave address programmed into this field. This register defaults to 0x50 which is the typical address for the EDID.	RW
	0	I2C_CLAIM1_EN 0 = Disable (default) 1 = Enable	RW
0x61	7:1	I2C_ADDR_CLAIM2. When I2C_CLAIM2_EN is enabled, the DSIx6 will claim I^2C slave address programmed into this field. This register defaults to 0x30 which is the default segment pointer register.	RW
	0	I2C_CLAIM2_EN 0 = Disable (Default) 1 = Enable	RW
0x62	7:1	I2C_ADDR_CLAIM3. When I2C_CLAIM3_EN is enabled, the DSIx6 will claim I^2C slave address programmed into this field. This register defaults to 0x52 which is the typical address for the EDID.	RW
	0	I2C_CLAIM3_EN 0 = Disable (Default) 1 = Enable	RW
0x63	7:1	I2C_ADDR_CLAIM4. When I2C_CLAIM4_EN is enabled, the DSIx6 will claim I^2C slave address programmed into this field. This register defaults to 0x00.	RW
	0	I2C_CLAIM4_EN 0 = Disable (Default) 1 = Enable	RW
0x64 through 0x73	7:0	AUX_WDATA0 through AUX_WDATA15. Data to transmit. All of these registers default to 0x00.	RW
0x74	7:4	Reserved	R
	3:0	AUX_ADDR[19:16]. This field is address bits 19 through 16 of the Native Aux 20-bit address. This field must be filled with zeros for I2C-Over-Aux transitions. This field defaults to 0x0.	RW
0x75	7:0	AUX_ADDR[15:8]. This field is bits 15 through 8 of the Native Aux 20-bit address. This field must be filled with zeros for I2C-Over-Aux request transactions. This field defaults to 0x00.	RW
0x76	7:0	AUX_ADDR[7:0]. This field is address bits 7 through 0 of the Native Aux 20-bit address. For I2C-Over-Aux request transactions this field must be the 7-bit I^2C address. This field defaults to 0x00.	RW
0x77	4:0	AUX_LENGTH. Amount of Data to transmit or amount of data received. Limited to up to 16 bytes. For example, if LENGTH is 0x10, then DSIx6 will interpret this to mean 16 (0x10). For replies, DSIx6 will update this field with the number of bytes returned. This field defaults to 0x00.	RWU
0x78	7:4	AUX_CMD. This field is used to indicate the type of request. This field defaults to 0x00. See Table 9 for request transactions codes.	RW
	0	SEND. When set to a 1, the DSIx6 will send the Native Aux request or initiate the I2C-Over_Aux transaction. DSIx6 will clear this bit when the request completed successfully or failed due to an error. This field defaults to 0.	RSU
0x79 through 0x88	7:0	AUX_RDATA0 through AUX_RDATA15. Data received. All of these registers default to 0x00.	RU

Table 26. CSR Bit Field Definitions—Link Training Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x89 through 0x92	7:0	80BIT_CUSTOM_PATTERN. These 10 bytes represent the 80-bit Custom pattern. The default pattern is 0x1F, 0x7C, 0xF0, 0xC1, 0x07, 0x1F, 0x7C, 0xF0, 0xC1, and 0x07. In the DisplayPort PHY CTS specification this pattern is known as PLTPAT. The SN65DSIx6 will continuously transmit over all enabled DisplayPort lanes starting at the LSB of data at address 0x89 through the MSB of data at address 0x92 last.	RW

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Table 26. CSR Bit Field Definitions—Link Training Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x93	7:6	DP_PRE_EMPHASIS This field selects the pre-emphasis setting for all DP Main Links. The actual pre-emphasis level is determined by the DP Link Training LUT registers. 00 = Pre-Emphasis Level 0 (Default) 01 = Pre-Emphasis Level 1 10 = Pre-Emphasis Level 2 11 = Pre-Emphasis Level 3	RWU
	5:4	DP_NUM_LANES. 00 = Not Configured. (Default) 01 = 1 DP lane. 10 = 2 DP lanes. 11 = 4 DP lanes.	RW
	3:1	SSC_SPREAD 000 = Down-spread 5000 ppm 001 = Down-spread 4375 ppm 010 = Down-spread 3750 ppm (default) 011 = Down-spread 3150 ppm 100 = Down-spread 2500 ppm 101 = Center-spread 3750 ppm 110 = Center-spread 4375 ppm 111 = Center-spread 5000 ppm	RW
	0	SSC_ENABLE 0 = Clock spread is disabled (default) 1 = Clock spread is enabled.	RW
0x94	7:5	DP_DATARATE 000 = Not Configured (Default) 001 = 1.62 Gbps per lane (RBR) 010 = 2.16 Gbps per lane 011 = 2.43 Gbps per lane 100 = 2.70 Gbps per lane (HBR) 101 = 3.24 Gbps per lane 110 = 4.32 Gbps per lane. 111 = 5.4 Gbps per lane (HBR2)	RW
	3:2	DP_ERC. This field controls the edge rate for Main Link DisplayPort interface. 00 = 61 ps (default) 01 = 95 ps 10 = 122 ps 11 = 153 ps	RW
	1:0	DP_TX_SWING This field selects the differential output voltage level for all DP Main Links. The actual pk-pk differential tx voltage is determined by the *DP Link Training LUT registers*. Note that Voltage Swing level 3 is disabled by default. 00 = Voltage Swing Level 0 (Default) 01 = Voltage Swing Level 1 10 = Voltage Swing Level 2 11 = Voltage Swing Level 3	RWU

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Table 26. CSR Bit Field Definitions—Link Training Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x95	7	TPS1_FAST_TRAIN. 0 = TPS1 will not be transmitted in Fast Link Training Mode (Default) 1 = TPS1 will be transmitted in Fast Link Training Mode	RW
	6	TPS2_FAST_TRAIN 0 = TPS2 will NOT be transmitted in Fast Link Training mode (default) 1 = TPS2 will be transmitted in Fast Link Training Mode	RW
	5	TPS3_FAST_TRAIN 0 = TPS3 will not be used for TPS2 in Fast Link Training Mode (default) 1 = TPS3 will be used instead of TPS2 in Fast Link Training Mode.	RW
	4	SCRAMBLE_DISABLE 0 = Scrambling Enabled (default) 1 = Scrambling Disabled.	RW
	3:1	DP_POST_CURSOR2. This field contains the post cursor2 value, where PST2 = 20 × LOG(1 – 0.05 × DP_POST_CURSOR2) (in dB) This field controls the Post Cursor2 is setting for all DP Main Links 000 = Post-Cursor2 Level 0 (0 dB) (Default) 010 = Post-Cursor2 Level 1 (0.92 dB) 100 = Post-Cursor2 Level 2 (1.94 dB) 110 = Post-Cursor2 Level 3 (3.10 dB).	RWU
	0	ADJUST_REQUEST_DISABLE. This field is used during Semi-Auto Link training. 0 = DSIx6 will read from DPCD address to determine next training level (pre-emphasis, tx swing level, and post-cursor2). (Default) 1 = DSIx6 will not read from DPCD address to determine next training level. It will instead go to next available Pre-emphasis level. After maximum pre-emphasis level has been reached, the DSIx6 will attempt next DP_TX_SWING and reset pre-emphasis level back to level 0. Post-Cursor2 is not used in this mode.	RW
0x96	3:0	ML_TX_MODE 0000 = Main Link Off (default) 0001 = Normal mode (Idle pattern or active video) 0010 = TPS1 0011 = TPS2 0100 = TPS3 0101 = PRBS7 0110 = HBR2 Compliance Eye Pattern 0111 = Symbol Error Rate Measurement Pattern 1000 = 80-bit Custom Pattern 1001 = Fast Link Training 1010 = Semi-Auto Link Training. 1011 = Redriver Semi-Auto Link Training All others are Reserved.	RWU
0x97	7:0	HBR2_COMPEYEPAT_LENGTH_LOW. This field is the count of number of scrambled 0 symbols to be output for every Enhanced Framing Scrambler Reset sequence. This count includes the reset sequence. A value less than four causes scrambled 0 symbols to be output with no scrambler reset sequence. This field represents the lower 8 bits of the 16-bit HBR2_COMPEYEPAT_LENGTH register. This field defaults to 0x04.	RW
0x98	7:0	HBR2_COMPEYEPAT_LENGTH_HIGH. This field is the count of number of scrambled 0 symbols to be output for every Enhanced Framing Scrambler Reset sequence. This count includes the reset sequence. A value less than four causes scrambled 0 symbols to be output with no scrambler reset sequence. This field represents the upper 8 bits of the 16-bit HBR2_COMPEYEPAT_LENGTH register. This field defaults to 0x01.	RW
0x99	7	LINK_RATE_SET_EN. When this field is cleared, the Semi-Auto Link training will write the appropriate value (0x06 for 1.62 Gbps, 0x0A for 2.7 Gbps, or 0x14 for 5.4 Gbps) to the sink LINK_BW_SET register at DPCD address 0x00110. When this field is set, the Semi-Auto Link Training will write the value in the LINK_RATE_SET field to the sink LINK_RATE_SET register at DPCD address 0x00115. Defaults to 0.	RW
	2:0	LINK_RATE_SET. When LINK_RATE_SET_EN bit is set, the value in this field will be written to the sink LINK_RATE_SET register at DPCD address 0x00115 during Semi-Auto Link training process. Defaults to 0x0.	RW

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Table 27. CSR Bit Field Definitions—PWM Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xA0	7:0	PWM_PRE_DIV The value programmed into this field along with the value in BACKLIGHT_SCALE is used to set the PWM frequency. The PWM frequency = REFCLK / (PWM_PRE_DIV × BACKLIGHT_SCALE + 1). This field defaults to 0x01.	RW
0xA1	7:0	BACKLIGHT_SCALE_LOW. The digital value corresponding to the maximum possible backlight input value. Default to 0xFF. The value in this field is the lower 8 bits of the 16-bit BACKLIGHT_SCALE register.	RW
0xA2	7:0	BACKLIGHT_SCALE_HIGH.The digital value corresponding to the maximum possible backlight input value. Default to 0xFF. The value in this field is the upper 8 bits of the 16-bit BACKLIGHT scale register.	RW
0xA3	7:0	BACKLIGHT_LOW Screen brightness on a scale of 0 to BACKLIGHT_SCALE. This register is used for SN65DSI86. The value in this field is the lower 8 bits of the 16-bit BACKLIGHT register. Defaults to 0x00	RW
0xA4	7:0	BACKLIGHT_HIGH Screen brightness on a scale of 0 to BACKLIGHT_SCALE. This register is used for SN65DSI86. The value in this field is the upper 8 bits of the 16-bit BACKLIGHT register. Default to 0x00. The DSIx6 will latch the 16-bit BACKLIGHT value on a write to this field.	RW
0xA5	1	PWM_EN. 0 = PWM is disabled. (Default). 1 = PWM enabled.	RW
	0	PWM_INV. When this bit is set, the PWM output will be inverted. 0 = Normal (default) 1 = Inverted.	RW

Table 28. CSR Bit Field Definitions—DP Link Training LUT

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xB0	7:4	V0_P0_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V0_P0_PRE) (in dB), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 0 are select by the training algorithm. The default value for this field is 0 (0 dB).	RW
	3:0	V0_P0_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V0_P0_VOD (in mV), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 0 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 4 (400 mV).	RW
0xB1	7:4	V0_P1_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V0_P1_PRE) (in dB), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 1 are select by the training algorithm. The default value for this field is 7 (3.74 dB).	RW
	3:0	V0_P1_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V0_P1_VOD (in mV), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 1 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 8 (600 mV).	RW
0xB2	7:4	V0_P2_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V0_P2_PRE) (in dB), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 2 are select by the training algorithm. The default value for this field is 10 (6.02 dB).	RW
	3:0	V0_P2_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V0_P2_VOD (in mV), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 2 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW

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Table 28. CSR Bit Field Definitions—DP Link Training LUT (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xB3	7:4	V0_P3_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V0_P3_PRE) (in dB), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 3 are select by the training algorithm. The default value for this field is 10 (6.02 dB).	RW
	3:0	V0_P3_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V0_P3_VOD (in mV), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 3 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW
0xB4	7:4	V1_P0_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V1_P0_PRE) (in dB), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 0 are select by the training algorithm. The default value for this field is 0 (0 dB).	RW
	3:0	V1_P0_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V1_P0_VOD (in mV), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 0 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 8 (600 mV).	RW
0xB5	7:4	V1_P1_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V1_P1_PRE) (in dB), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 1 are select by the training algorithm. The default value for this field is 6 (3.10 dB).	RW
	3:0	V1_P1_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V1_P1_VOD (in mV), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 1 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW
0xB6	7:4	V1_P2_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V1_P2_PRE) (in dB), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 2 are select by the training algorithm. The default value for this field is 9 (5.19 dB).	RW
	3:0	V1_P2_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V1_P2_VOD (in mV), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 2 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW
0xB7	7:4	V1_P3_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V1_P3_PRE) (in dB), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 3 are select by the training algorithm. The default value for this field is 9 (5.19 dB).	RW
	3:0	V1_P3_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V1_P3_VOD (in mV), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 3 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW
0xB8	7:4	V2_P0_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V2_P0_PRE) (in dB), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 0 are select by the training algorithm. The default value for this field is 0 (0 dB).	RW
	3:0	V2_P0_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V2_P0_VOD (in mV), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 0 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW
0xB9	7:4	V2_P1_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V2_P1_PRE) (in dB), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 1 are select by the training algorithm. The default value for this field is 5 (2.50 dB).	RW
	3:0	V2_P1_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V2_P1_VOD (in mV), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 1 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW

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Table 28. CSR Bit Field Definitions—DP Link Training LUT (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xBA	7:4	V2_P2_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V2_P2_PRE) (in dB), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 2 are select by the training algorithm. The default value for this field is 5 (2.50 dB).	RW
	3:0	V2_P2_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V2_P2_VOD (in mV), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 2 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW
0xBB	7:4	V2_P3_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V2_P3_PRE) (in dB), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 3 are select by the training algorithm. The default value for this field is 5 (2.50 dB).	RW
	3:0	V2_P3_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V2_P3_VOD (in mV), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 3 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW
0xBC	7:4	V3_P0_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V3_P0_PRE) (in dB), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 0 are select by the training algorithm. The default value for this field is 0 (0 dB).	RW
	3:0	V3_P0_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V3_P0_VOD (in mV), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 0 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW
0xBD	7:4	V3_P1_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V3_P1_PRE) (in dB), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 1 are select by the training algorithm. The default value for this field is 0 (0 dB).	RW
	3:0	V3_P1_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V3_P1_VOD (in mV), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 1 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW
0xBE	7:4	V3_P2_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V3_P2_PRE) (in dB), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 2 are select by the training algorithm. The default value for this field is 0 (0 dB).	RW
	3:0	V3_P2_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V3_P2_VOD (in mV), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 2 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW
0xBF	7:4	V3_P3_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = –20 × LOG(1 – 0.05 × V3_P3_PRE) (in dB), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 3 are select by the training algorithm. The default value for this field is 0 (0 dB).	RW
	3:0	V3_P3_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 × V3_P3_VOD (in mV), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 3 are selected by the training algorithm. The maximum supported value is 12 (800 mV). Any value greater than 12 is reserved for SN65DSIx6. The default value for this field is 12 (800 mV).	RW

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Table 28. CSR Bit Field Definitions—DP Link Training LUT (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xC0	7	V0_P3_PRE_EN. When this field is set V0_P3_PRE is used in training algorithm. When this field is cleared, V0_P3_PRE is not used in training algorithm. The default for this field is 0 (disabled).	RW
	6	V0_P3_VOD_EN. When this field is set V0_P3_VOD is used in training algorithm. When this field is cleared, V0_P3_VOD is not used in training algorithm. The default for this field is 0 (disabled).	RW
	5	V0_P2_PRE_EN. When this field is set V0_P2_PRE is used in training algorithm. When this field is cleared, V0_P2_PRE is not used in training algorithm. The default for this field is 1 (enabled).	RW
	4	V0_P2_VOD_EN. When this field is set V0_P2_VOD is used in training algorithm. When this field is cleared, V0_P2_VOD is not used in training algorithm. The default for this field is 1 (enabled).	RW
	3	V0_P1_PRE_EN. When this field is set V0_P1_PRE is used in training algorithm. When this field is cleared, V0_P1_PRE is not used in training algorithm. The default for this field is 1 (enabled).	RW
	2	V0_P1_VOD_EN. When this field is set V0_P1_VOD is used in training algorithm. When this field is cleared, V0_P1_VOD is not used in training algorithm. The default for this field is 1 (enabled).	RW
	1	V0_P0_PRE_EN. When this field is set V0_P0_PRE is used in training algorithm. When this field is cleared, V0_P0_PRE is not used in training algorithm. The default for this field is 1 (enabled).	RW
	0	V0_P0_VOD_EN. When this field is set V0_P0_VOD is used in training algorithm. When this field is cleared, V0_P0_VOD is not used in training algorithm. The default for this field is 1 (enabled).	RW
0xC1	7	V1_P3_PRE_EN. When this field is set V1_P3_PRE is used in training algorithm. When this field is cleared, V1_P3_PRE is not used in training algorithm. The default for this field is 0 (disabled).	RW
	6	V1_P3_VOD_EN. When this field is set V1_P3_VOD is used in training algorithm. When this field is cleared, V1_P3_VOD is not used in training algorithm. The default for this field is 0 (disabled).	RW
	5	V1_P2_PRE_EN. When this field is set V1_P2_PRE is used in training algorithm. When this field is cleared, V1_P2_PRE is not used in training algorithm. The default for this field is 1 (enabled).	RW
	4	V1_P2_VOD_EN. When this field is set V1_P2_VOD is used in training algorithm. When this field is cleared, V1_P2_VOD is not used in training algorithm. The default for this field is 1 (enabled).	RW
	3	V1_P1_PRE_EN. When this field is set V1_P1_PRE is used in training algorithm. When this field is cleared, V1_P1_PRE is not used in training algorithm. The default for this field is 1 (enabled).	RW
	2	V1_P1_VOD_EN. When this field is set V1_P1_VOD is used in training algorithm. When this field is cleared, V1_P1_VOD is not used in training algorithm. The default for this field is 1 (enabled).	RW
	1	V1_P0_PRE_EN. When this field is set V1_P0_PRE is used in training algorithm. When this field is cleared, V1_P0_PRE is not used in training algorithm. The default for this field is 1 (enabled).	RW
	0	V1_P0_VOD_EN. When this field is set V1_P0_VOD is used in training algorithm. When this field is cleared, V1_P0_VOD is not used in training algorithm. The default for this field is 1 (enabled).	RW
0xC2	7	V2_P3_PRE_EN. When this field is set V2_P3_PRE is used in training algorithm. When this field is cleared, V2_P3_PRE is not used in training algorithm. The default for this field is 0 (disabled).	RW
	6	V2_P3_VOD_EN. When this field is set V2_P3_VOD is used in training algorithm. When this field is cleared, V2_P3_VOD is not used in training algorithm. The default for this field is 0 (disabled).	RW
	5	V2_P2_PRE_EN. When this field is set V2_P2_PRE is used in training algorithm. When this field is cleared, V2_P2_PRE is not used in training algorithm. The default for this field is 0 (disabled).	RW
	4	V2_P2_VOD_EN. When this field is set V2_P2_VOD is used in training algorithm. When this field is cleared, V2_P2_VOD is not used in training algorithm. The default for this field is 0 (disabled).	RW
	3	V2_P1_PRE_EN. When this field is set V2_P1_PRE is used in training algorithm. When this field is cleared, V2_P1_PRE is not used in training algorithm. The default for this field is 1 (enabled).	RW
	2	V2_P1_VOD_EN. When this field is set V2_P1_VOD is used in training algorithm. When this field is cleared, V2_P1_VOD is not used in training algorithm. The default for this field is 1 (enabled).	RW
	1	V2_P0_PRE_EN. When this field is set V2_P0_PRE is used in training algorithm. When this field is cleared, V2_P0_PRE is not used in training algorithm. The default for this field is 1 (enabled).	RW
	0	V2_P0_VOD_EN. When this field is set V2_P0_VOD is used in training algorithm. When this field is cleared, V2_P0_VOD is not used in training algorithm. The default for this field is 1 (enabled).	RW

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Table 28. CSR Bit Field Definitions—DP Link Training LUT (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xC3	7	V3_P3_PRE_EN. When this field is set V3_P3_PRE is used in training algorithm. When this field is cleared, V3_P3_PRE is not used in training algorithm. The default for this field is 0 (disabled).	RW
	6	V3_P3_VOD_EN. When this field is set V3_P3_VOD is used in training algorithm. When this field is cleared, V3_P3_VOD is not used in training algorithm. The default for this field is 0 (disabled).	RW
	5	V3_P2_PRE_EN. When this field is set V3_P2_PRE is used in training algorithm. When this field is cleared, V3_P2_PRE is not used in training algorithm. The default for this field is 0 (disabled).	RW
	4	V3_P2_VOD_EN. When this field is set V3_P2_VOD is used in training algorithm. When this field is cleared, V3_P2_VOD is not used in training algorithm. The default for this field is 0 (disabled).	RW
	3	V3_P1_PRE_EN. When this field is set V3_P1_PRE is used in training algorithm. When this field is cleared, V3_P1_PRE is not used in training algorithm. The default for this field is 0 (disabled).	RW
	2	V3_P1_VOD_EN. When this field is set V3_P1_VOD is used in training algorithm. When this field is cleared, V3_P1_VOD is not used in training algorithm. The default for this field is 0 (disabled).	RW
	1	V3_P0_PRE_EN. When this field is set V3_P0_PRE is used in training algorithm. When this field is cleared, V3_P0_PRE is not used in training algorithm. The default for this field is 0 (disabled).	RW
	0	V3_P0_VOD_EN. When this field is set V3_P0_VOD is used in training algorithm. When this field is cleared, V3_P0_VOD is not used in training algorithm. The default for this field is 0 (disabled).	RW

Table 29. CSR Bit Field Definitions—PSR Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xC8	1	PSR_EXIT_VIDEO. 0 = Upon exiting SUSPEND mode, the DSIx6 will transmit IDLE patterns and the VSTREAM_ENABLE bit will be cleared. GPU software is responsible for setting the VSTREAM_ENABLE bit. (default) 1 = Upon exiting SUSPEND mode, the DSIx6 will transmit IDLE patterns and the VSTREAM_ENABLE bit will be set.	RW
	0	PSR_TRAIN. This field controls whether or not the SN65DSIx6 will perform a Semi-Auto Link Training when exiting the SUSPEND mode. 0 = PSR train will be Normal Mode (idle pattern) (default) 1 = PSR train will be Semi-Auto Link Training.	RW

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Table 30. CSR Bit Field Definitions—IRQ Enable Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xE0	0	IRQ_EN When enabled by this field, the IRQ output is driven high to communicate IRQ events. 0 = IRQ output is high-impedance (default) 1 = IRQ output is driven high when a bit is set in registers 0xF0, 0xF1, 0xF2, 0xF3, 0xF4, or 0xF5 that also has the corresponding IRQ_EN bit set to enable the interrupt condition	RW
0xE1	7	CHA_CONTENTION_DET_EN 0 = CHA_CONTENTION_DET_ERR is masked (default) 1 = CHA_CONTENTION_DET_ERR is enabled to generate IRQ events	RW
	6	CHA_FALSE_CTRL_EN 0 = CHA_FALSE_CTRL_ERR is masked (default) 1 = CHA_FALSE_CTRL_ERR is enabled to generate IRQ events	RW
	5	CHA_TIMEOUT_EN 0 = CHA_TIMEOUT_ERR is masked (default) 1 = CHA_TIMEOUT_ERR is enabled to generate IRQ events	RW
	4	CHA_LP_TX_SYNC_EN 0 = CHA_LP_TX_SYNC_ERR is masked (default) 1 = CHA_LP_TX_SYNC_ERR is enabled to generate IRQ events	RW
	3	CHA_ESC_ENTRY_EN 0 = CHA_ESC_ENTRY_ERR is masked (default) 1 = CHA_ESC_ENTRY_ERR is enabled to generate IRQ events	RW
	2	CHA_EOT_SYNC_EN 0 = CHA_EOT_SYNC_ERR is masked (default) 1 = CHA_EOT_SYNC_ERR is enabled to generate IRQ events	RW
	1	CHA_SOT_SYNC_EN 0 = CHA_SOT_SYNC_ERR is masked (default) 1 = CHA_SOT_SYNC_ERR is enabled to generate IRQ events	RW
	0	CHA_SOT_BIT_EN 0 = CHA_SOT_BIT_ERR is masked (default) 1 = CHA_SOT_BIT_ERR is enabled to generate IRQ events	RW
0xE2	7	CHA_DSI_PROTOCOL_EN 0 = CHA_DSI_PROTOCOL_ERR is masked (default) 1 = CHA_DSI_PROTOCOL_ERR is enabled to generate IRQ events	RW
	6	Reserved	R
	5	CHA_INVALID_LENGTH_EN 0 = CHA_INVALID_LENGTH_ERR is masked (default) 1 = CHA_INVALID_LENGTH_ERR is enabled to generate IRQ events	RW
	4	Reserved.	R
	3	CHA_DATATYPE_EN 0 = CHA_DATATYPE_ERR is masked (default) 1 = CHA_ DATATYPE_ERR is enabled to generate IRQ events	RW
	2	CHA_CHECKSUM_EN 0 = CHA_CHECKSUM_ERR is masked (default) 1 = CHA_CHECKSUM_ERR is enabled to generate IRQ events	RW
	1	CHA_UNC_ECC_EN 0 = CHA_UNC_ECC_ERR is masked (default) 1 = CHA_UNC_ECC_ERR is enabled to generate IRQ events	RW
	0	CHA_COR_ECC_EN 0 = CHA_COR_ECC_ERR is masked (default) 1 = CHA_COR_ECC_ERR is enabled to generate IRQ events	RW

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Table 30. CSR Bit Field Definitions—IRQ Enable Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xE3	7	Reserved	R
	6	CHB_FALSE_CTRL_EN 0 = CHB_FALSE_CTRL_ERR is masked (default) 1 = CHB_FALSE_CTRL_ERR is enabled to generate IRQ events	RW
	5	Reserved.	R
	4	CHB_LP_TX_SYNC_EN 0 = CHB_LP_TX_SYNC_ERR is masked (default) 1 = CHB_LP_TX_SYNC_ERR is enabled to generate IRQ events	RW
	3	Reserved	R
	2	CHB_EOT_SYNC_EN 0 = CHB_EOT_SYNC_ERR is masked (default) 1 = CHB_EOT_SYNC_ERR is enabled to generate IRQ events	RW
	1	CHB_SOT_SYNC_EN 0 = CHB_SOT_SYNC_ERR is masked (default) 1 = CHB_SOT_SYNC_ERR is enabled to generate IRQ events	RW
	0	CHB_SOT_BIT_EN 0 = CHB_SOT_BIT_ERR is masked (default) 1 = CHB_SOT_BIT_ERR is enabled to generate IRQ events	RW
0xE4	7	CHB_DSI_PROTOCOL_EN 0 = CHB_DSI_PROTOCOL_ERR is masked (default) 1 = CHB_DSI_PROTOCOL_ERR is enabled to generate IRQ events	RW
	6	Reserved	R
	5	CHB_INVALID_LENGTH_EN 0 = CHB_INVALID_LENGTH_ERR is masked (default) 1 = CHB_INVALID_LENGTH_ERR is enabled to generate IRQ events	RW
	4	Reserved	R
	3	CHB_DATATYPE_EN 0 = CHB_DATATYPE_ERR is masked (default) 1 = CHB_ DATATYPE_ERR is enabled to generate IRQ events	RW
	2	CHB_CHECKSUM_EN 0 = CHB_CHECKSUM_ERR is masked (default) 1 = CHB_CHECKSUM_ERR is enabled to generate IRQ events	RW
	1	CHB_UNC_ECC_EN 0 = CHB_UNC_ECC_ERR is masked (default) 1 = CHB_UNC_ECC_ERR is enabled to generate IRQ events	RW
	0	CHB_COR_ECC_EN 0 = CHB_COR_ECC_ERR is masked (default) 1 = CHB_COR_ECC_ERR is enabled to generate IRQ events	RW

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Table 30. CSR Bit Field Definitions—IRQ Enable Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xE5	7	I2C_DEFR_EN 0 = I2C_DEFR is masked (default) 1 = I2C_DEFR is enabled to generate IRQ events.	RW
	6	NAT_I2C_FAIL_EN. 0 = NAT_I2C_FAIL is masked. (default) 1 = NAT_I2C_FAIL is enabled to generate IRQ events.	RW
	5	AUX_SHORT_EN 0 = AUX_SHORT is masked. (default) 1 = AUX_SHORT is enabled to generate IRQ events.	RW
	4	AUX_DEFR_EN. 0 = AUX_DEFR is masked. (default) 1 = AUX_DEFR is enabled to generate IRQ events.	RW
	3	AUX_RPLY_TOUT_EN. 0 = AUX_RPLY_TOUT is masked (default). 1 = AUX_RPLY_TOUT is enabled to generate IRQ events.	RW
	2	Reserved.	R
	1	Reserved.	R
	0	SEND_INT_EN. 0 = SEND_INT is masked (default) 1 = SEND_INT is enabled to generate IRQ events.	RW
0xE6	7	Reserved	R
	6	Reserved	R
	5	PLL_UNLOCK_EN 0 = PLL_UNLOCK is masked (default) 1 = PLL_UNLOCK is enabled to generate IRQ events	RW
	4	Reserved	R
	3	HPD_REPLUG_EN. 0 = HPD_REPLUG is masked (default) 1 = HPD_REPLUG is enabled to generate IRQ events	RW
	2	HPD_REMOVAL _EN 0 = HPD_REMOVAL is masked. (default) 1 = HPD_REMOVAL is enabled to generate IRQ events.	RW
	1	HPD_INSERTION_EN 0 = HPD_INSERTION is masked. (default) 1 = HPD_INSERTION is enabled to generate IRQ events.	RW
	0	IRQ_HPD_EN 0 = IRQ_HPD is masked. (default) 1 = IRQ_HPD is enabled to generate IRQ events.	RW

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Table 30. CSR Bit Field Definitions—IRQ Enable Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xE7	7	DPTL_VIDEO_WIDTH_PROG_ERR_EN 0 = DPTL_VIDEO_WIDTH_PROG_ERR is masked. (default) 1 = DPTL_VIDEO_WIDTH_PROG_ERR is enabled to generate IRQ events.	RW
	6	DPTL_LOSS_OF_DP_SYNC_LOCK_EN 0 = DPTL_LOSS_OF_DP_SYNC_LOCK_ERR is masked. (default) 1 = DPTL_LOSS_OF_DP_SYNC_LOCK_ERR is enabled to generate IRQ events.	RW
	5	DPTL_UNEXPECTED_DATA_EN 0 = DPTL_UNEXPECTED_DATA_ERR is masked. (default) 1 = DPTL_UNEXPECTED_DATA_ERR is enabled to generate IRQ events.	RW
	4	DPTL_UNEXPECTED_SECDATA_EN 0 = DPTL_UNEXPECTED_SECDATA_ERR is masked. (default) 1 = DPTL_UNEXPECTED_SECDATA_ERR is enabled to generate IRQ events.	RW
	3	DPTL_UNEXPECTED_DATA_END_EN 0 = DPTL_UNEXPECTED_DATA_END_ERR is masked. (default) 1 = DPTL_UNEXPECTED_DATA_END_ERR is enabled to generate IRQ events.	RW
	2	DPTL_UNEXPECTED_PIXEL_DATA_EN 0 = DPTL_UNEXPECTED_PIXEL_DATA_ERR is masked. (default) 1 = DPTL_UNEXPECTED_PIXEL_DATA_ERR is enabled to generate IRQ events.	RW
	1	DPTL_UNEXPECTED_HSYNC_EN 0 = DPTL_UNEXPECTED_HSYNC_ERR is masked. (default) 1 = DPTL_UNEXPECTED_HSYNC_ERR is enabled to generate IRQ events.	RW
	0	DPTL_UNEXPECTED_VSYNC_EN 0 = DPTL_UNEXPECTED_VSYNC_ERR is masked. (default) 1 = DPTL_UNEXPECTED_VSYNC_ERR is enabled to generate IRQ events.	RW
0xE8	7:2	Reserved	R
	1	DPTL_SECONDARY_DATA_PACKET_PROG_ERR_EN. 0 = DPTL_SECONDARY_DATA_PACKET_PROG_ERR is masked. (default) 1 = DPTL_SECONDARY_DATA_PACKET_PROG_ERR is enabled to generate IRQ events.	RW
	0	DPTL_DATA_UNDERRUN_EN 0 = DPTL_DATA_UNDERRUN_ERR is masked. (default) 1 = DPTL_DATA_UNDERRUN_ERR is enabled to generate IRQ events.	RW
0xE9	7:6	Reserved.	
	5	LT_EQ_CR_ERR_EN. 0 = LT_EQ_CR_ERR is masked (default) 1 = LT_EQ_CR_ERR is enabled to generate IRQ events.	RW
	4	LT_EQ_LPCNT_ERR_EN. 0 = LT_EQ_LPCNT_ERR is masked (default) 1 = LT_EQ_LPCNT_ERR is enabled to generate IRQ events.	RW
	3	LT_CR_MAXVOD_ERR_EN. 0 = LT_CR_MAXVOD_ERR is masked (default) 1 = LT_CR_MAXVOD_ERR is enabled to generate IRQ events.	RW
	2	LT_CR_LPCNT_ERR_EN. 0 = LT_CR_LPCNT_ERR is masked (default) 1 = LT_CR_LPCNT_ERR is enabled to generate IRQ events.	RW
	1	LT_FAIL_EN. 0 = LT_FAIL is masked (default) 1 = LT_FAIL is enabled to generate IRQ events.	RW
	0	LT_PASS_EN. 0 = LT_PASS is masked (default) 1 = LT_PASS is enabled to generate IRQ events.	RW

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Table 31. CSR Bit Field Definitions—IRQ Status Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xF0	7	CHA_CONTENTION_DET_ERR. When LP high or LP low fault is detected on the DSI channel A interface, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	6	CHA_FALSE_CTRL_ERR. When the DSI channel A packet processor detects a LP Request not followed by the remainder of a valid escape or turnaround sequence or if it detects a HS request not followed by a bridge state (LP-00), this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	5	CHA_TIMEOUT_ERR. When the HS Rx Timer or the LP TX timer expires, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	4	CHA_LP_TX_SYNC_ERR. When the DSI channel A packet processor detects data not synchronized to a byte boundary at the end of Low-Power transmission, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	3	CHA_ESC_ENTRY_ERR. When the DSI Channel A packet processor detects an unrecognized Escape Mode Entry Command, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	2	CHA_EOT_SYNC_ERR. When the DSI channel A packet processor detects that the last byte of a HS transmission does not match a byte boundary, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	1	CHA_SOT_SYNC_ERR. When the DSI channel A packet processor detects a corrupted SOT in a way that proper synchronization cannot be expected, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	0	CHA_SOT_BIT_ERR When the DSI channel A packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
0xF1	7	CHA_DSI_PROTOCOL_ERR. When the DSI channel A packet processor detects a DSI protocol error, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	6	Reserved.	R
	5	CHA_INVALID_LENGTH_ERR. When the DSI channel A packet processor detects an invalid transmission length, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	4	Reserved.	R
	3	CHA_DATATYPE_ERR. When the DSI channel A packet processor detects a unrecognized DSI data type, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	2	CHA_CHECKSUM_ERR When the DSI channel A packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	1	CHA_UNC_ECC_ERR When the DSI channel A packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU
	0	CHA_COR_ECC_ERR When the DSI channel A packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a 1 or when the DSIx6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report.	RCU

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Table 31. CSR Bit Field Definitions—IRQ Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xF2	7	Reserved	R
	6	CHB_FALSE_CTRL_ERR. When the DSI channel B packet processor detects a LP Request not followed by the remainder of a valid escape or turnaround sequence or if it detects a HS request not followed by a bridge state (LP-00), this bit is set; this bit is cleared by writing a 1.	RCU
	5	Reserved	R
	4	CHB_LP_TX_SYNC_ERR. When the DSI channel B packet processor detects data not synchronized to a byte boundary at the end of Low-Power transmission, this bit is set; this bit is cleared by writing a 1.	RCU
	3	Reserved	R
	2	CHB_EOT_SYNC_ERR. When the DSI channel B packet processor detects that the last byte of a HS transmission does not match a byte boundary, this bit is set; this bit is cleared by writing a 1.	RCU
	1	CHB_SOT_SYNC_ERR. When the DSI channel B packet processor detects a corrupted SOT in a way that proper synchronization cannot be expected, this bit is set; this bit is cleared by writing a 1.	RCU
	0	CHB_SOT_BIT_ERR When the DSI channel B packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a 1.	RCU
0xF3	7	CHB_DSI_PROTOCOL_ERR. When the DSI channel B packet processor detects a DSI protocol error, this bit is set; this bit is cleared by writing a 1.	RCU
	6	Reserved.	R
	5	CHB_INVALID_LENGTH_ERR. When the DSI channel B packet processor detects an invalid transmission length, this bit is set; this bit is cleared by writing a 1.	RCU
	4	Reserved.	R
	3	CHB_DATATYPE_ERR. When the DSI channel B packet processor detects a unrecognized DSI data type, this bit is set; this bit is cleared by writing a 1.	RCU
	2	CHB_CHECKSUM_ERR When the DSI channel B packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a 1.	RCU
	1	CHB_UNC_ECC_ERR When the DSI channel B packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a 1.	RCU
	0	CHB_COR_ECC_ERR When the DSI channel B packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a 1.	RCU
0xF4	7	I2C_DEFR. This field is set if an I2C-Over-Aux request has received a specific number X of I2C_DEFER from Sink. For direct method (clock stretching), the number X is 44. For indirect method, the number X is: 44 for AUX_LENGTH = 1 66 for AUX_LENGTH = 2 110 for 2 < AUX_LENGTH ≤ 4 154 for 4 < AUX_LENGTH ≤ 6 198 for 6< AUX_LENGTH ≤ 8 287 for 8< AUX_LENGTH ≤ 12 375 for 12 < AUX_LENGTH ≤ 16	RCU
	6	NAT_I2C_FAIL. This bit is set if the I2C-Over-Aux or Native AUX failed.	RCU
	5	AUX_SHORT. If set, then the bytes written or received did not match requested Length. SW should read AUX_LENGTH field to determine the amount of data written or read.	RCU
	4	AUX_DEFR. The DSIx6 will attempt to complete an AUX request by retrying the request seven times. This field is set if the response to the last retry is an AUX_DEFER.	RCU
	3	AUX_RPLY_TOUT. The DSIx6 will attempt to complete an AUX request by retrying the request seven times. This field is set if the response to the last retry is a 400-µs timeout.	RCU
	2	Reserved.	R
	1	Reserved.	R
	0	SEND_INT. This field is set whenever the SEND bit transitions from 1 to 0.	RCU

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Table 31. CSR Bit Field Definitions—IRQ Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0xF5	7	Reserved	R
	6	Reserved	R
	5	PLL_UNLOCK This bit is set whenever the PLL Lock status transitions from LOCK to UNLOCK.	RCU
	4	Reserved	R
	3	HPD_REPLUG. This field is set whenever the SN65DSIx6 detects a replug event on the HPD pin.	RCU
	2	HPD_REMOVAL. This field is set whenever the SN65DSIx6 detects a DisplayPort device removal.	RCU
	1	HPD_INSERTION. This field is set whenever the SN65DSIx6 detects a DisplayPort device insertion.	RCU
	0	IRQ_HPD. This field is set whenever the SN65DSIx6 detects a IRQ_HPD event.	RCU
0xF6	7	VIDEO_WIDTH_PROG_ERR. This field is set whenever the video parameters define more bytes of pixel data than can be transferred in the allotted video portion of the line time.	RCU
	6	LOSS_OF_DP_SYNC_LOCK_ERR. This field is set whenever the DP sync generator has lost lock with the DSI sync stream.	RCU
	5	DPTL_UNEXPECTED_DATA_ERR. This field is set whenever a data token at in the video stream from DSI was found at an invalid time syntactically.	RCU
	4	DPTL_UNEXPECTED_SECDATA_ERR. This field is set whenever a secondary data start token at in the video stream was found at an invalid time syntactically.	RCU
	3	DPTL_UNEXPECTED_DATA_END_ERR. This field is set whenever a data end token at in the video stream from DSI was found at an invalid time syntactically.	RCU
	2	DPTL_UNEXPECTED_PIXEL_DATA_ERR. This field is set whenever a video data start token at in the video stream from DSI was found at an invalid time syntactically.	RCU
	1	DPTL_UNEXPECTED_HSYNC_ERR. This field is set whenever a horizontal sync token at in the video stream from DSI was found at an invalid time syntactically.	RCU
	0	DPTL_UNEXPECTED_VSYNC_ERR. This field is set whenever a vertical sync token at in the video stream from DSI was found at an invalid time syntactically.	RCU
0xF7	7	Reserved	R
	1	DPTL_SECONDARY_DATA_PACKET_PROG_ERR. This field is set whenever a secondary data packet has an invalid length.	RCU
	0	DPTL_DATA_UNDERRUN_ERR. This field is set whenever no data was received when data should have been ready.	RCU
0xF8	7:6	Reserved.	R
	5	LT_EQ_CR_ERR. This field is set whenever link training fails in the channel equalization phase due to LANEx_CR_DONE not set.	RCU
	4	LT_EQ_LPCNT_ERR. This field is set whenever link training fails in the channel equalization phase due to the loop count being greater than five.	RCU
	3	LT_CR_MAXVOD_ERR. This field is set whenever link training fails in clock recovery phase due to maximum VOD reached without LANEx_CR_DONE bit(s) getting set.	RCU
	2	LT_CR_LPCNT_ERR. This field is set whenever link training fails in the clock recovery phase due to same VOD being used five times.	RCU
	1	LT_FAIL. This field is set whenever the Semi-Auto link training fails to train the DisplayPort Link.	RCU
	0	LT_PASS. This field is set whenever the Semi-Auto link training successfully trains the DisplayPort Link.	RCU

Table 32. Page Select Register

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
		PAGE_SELECT. This field is used to select a different page of 254 bytes. This register will reside in the same location for each Page. This register is independently controlled by either DSI or I^2C. This means the value written or read by I^2C does not affect the value written or read by DSI, or vice-versa. The SN65DSI86 can only access Page 0 and Page 7. 000 = Standard CFR registers. (Default) 111 = TI Test Registers.	

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ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0x16	0	ASSR_OVERRIDE. 0 = ASSR_CONTROL is read-only. (Default) 1 = ASSR_CONTROL is read/write.	RW

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality

9.1 Application Information

The SN65DSIx6 is a bridge which interfaces DSI to embedded DisplayPort (eDP). Because it does not support HDCP, it is only intended for internal applications like notebooks and tablets. Four lanes of HBR2 (17.28 Gbps before 8b10b encoding) and dual DSI input (up to 8 lanes at 1.5 Gbps for a total of 12 Gbps) allows the SN65DSIx6 to support large high resolution eDP panels.

9.2 Typical Application

9.2.1 1080p (1920x1080 60 Hz) Panel

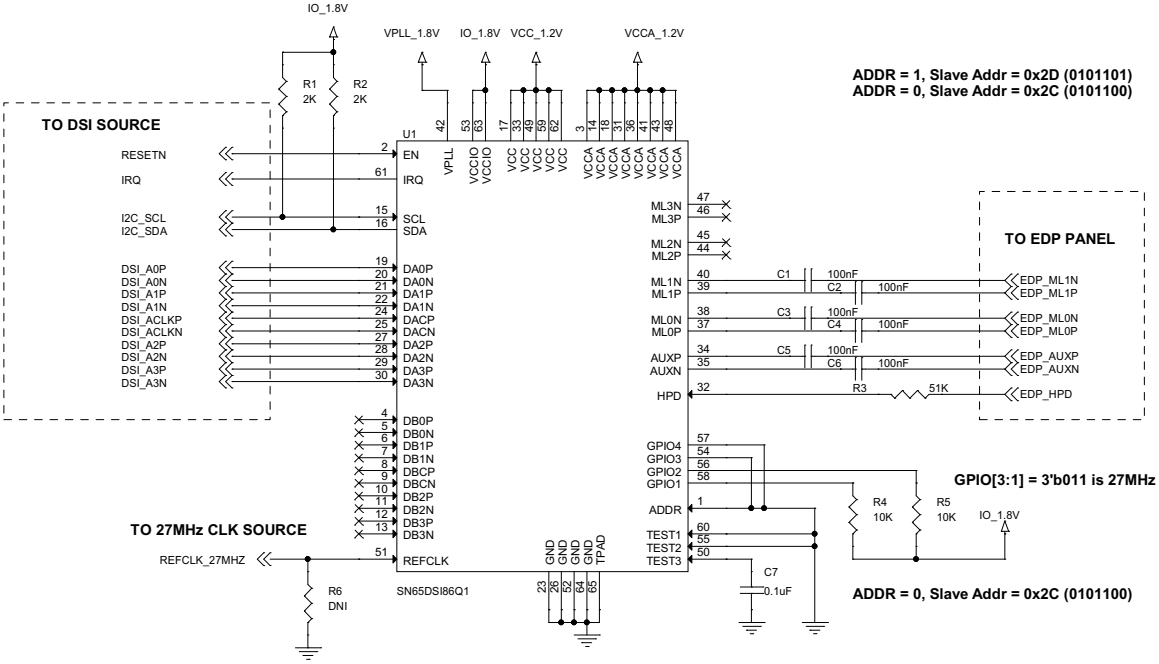


Figure 20. 1080p (1920 × 1080 60 Hz) Panel

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 34.

Table 34. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC} and V_{CCA} Supply	1.2 V (± 5%)
V_{CCIO} Supply	1.8 V (± 10%)
V_{PLL} Supply	1.8 V (± 10%)
Clock Source (REFCLK or DSIA_CLK)	REFCLK
REFCLK Frequency (12 MHz, 19.2 MHz, 26 MHz, 27 MHz, or 38.4 MHz)	27 MHz
DSIA Clock Frequency	N/A
eDP PANEL EDID RESOLUTION INFORMATION	

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Typical Application (continued)

Table 34. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Pixel Clock (MHz)	148.5
Horizontal Active (pixels)	1920
Horizontal Blanking (pixels)	280
Vertical Active (lines)	1080
Vertical Blanking (lines)	45
Horizontal Sync Offset (pixels)	88
Horizontal Sync Pulse Width (pixels)	44
Vertical Sync Offset (lines)	4
Vertical Sync Pulse Width (lines)	5
Horizontal Sync Pulse Polarity	Positive
Vertical Sync Pulse Polarity	Positive
Color Bit Depth (6 bpc or 8 bpc)	8 (24 bpp)

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Typical Application (continued)

Table 34. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
eDP PANEL DPCD INFORMATION	
eDP Version (1.0, 1.1, 1.2, 1.3, or 1.4)	1.3
Number of eDP lanes (1, 2, or 4)	2
Datarate Supported (1.62 Gbps, 2.16 Gbps, 2.43 Gbps, 2.70 Gbps, 3.24 Gbps, 4.32 Gbps, or 5.40 Gbps)	2.70
DSI INFORMATION	
APU or GPU Maximum number of DSI Lanes (1 through 8)	4
APU or GPU Maximum DSI Clock Frequency (MHz)	500
Single or Dual DSI	Single
Dual DSI Configuration (Odd/Even or Left/Right)	NA

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 eDP Design Procedure

The panel, as indicated by the panel EDID information, supports a pixel clock of 148.5 MHz at 8 bpc or 24 bpp. This translates to a stream bit rate of 3.564 Gbps.

Stream Bit Rate = PixelClock × bpp

Stream Bit Rate = 148.5 × 24

Stream Bit Rate = 3.564 Gbps

In order to support the panel stream bit rate, the SN65DSIx6 eDP interface must be programmed so that the total eDP data rate is greater than the stream bit rate. In this example, the total eDP data rate is calculated as:

eDP Total Bit Rate = #_of_eDP_Lanes × DataRate × 0.80

eDP Total Bit Rate = 2 × 2.7 Gbps × 0.80

eDP Total Bit Rate = 4.32 Gbps.

In this example, the eDP panel DPCD registers indicates eDP1.3 compliant, supports a data rate of 2.7 Gbps per lane, and a lane count of 2. For this panel to operate properly, the SN65DSIx6 would need to be programmed to enable two lanes at a data rate of 2.7 Gbps each.

In portable and mobile applications, total power consumption is a key care-about. In this example, the panel chosen is eDP 1.3 compliant and supports a data rate of 2.7 Gbps per lane. The SN65DSIx6 power consumption is a function of the data rate and number of active DP lanes. By reducing the number of active lanes and/or data rate, the total power consumption of the SN65DSIx6 is reduced as well. If a panel which supported data rate of 5.4 Gbps was chosen over the example panel, the number of lanes could be reduced from two lanes to one lane. Or if a panel which was eDP1.4 compliant and support 2.43 Gbps data rate was chosen over the example panel, the data rate could be reduced from 2.7 Gbps to 2.43 Gbps.

Once the eDP interface parameters are known, the video resolution parameters required by the panel need to be programmed into the SN65DSIx6. For this example, the parameters programmed would be the following:

Horizontal Active = 1920 or 0x780

CHA_ACTIVE_LINE_LENGTH_LOW = 0x80

CHA_ACTIVE_LINE_LENGTH_HIGH = 0x07

Vertical Active = 1080 or 0x438

CHA_VERTICAL_DISPLAY_SIZE_LOW = 0x38

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CHA_VERTICAL_DISPLAY_SIZE_HIGH = 0x04

Horizontal Pulse Width = 44 or 0x2C

HORIZONTAL_PULSE_WIDTH_LOW = 0x2C

HORIZONTAL_PULSE_WIDTH_HIGH = 0x00

Vertical Pulse Width = 5

VERTICAL_PULSE_WIDTH_LOW = 0x05

VERTICAL_PULSE_WIDTH_HIGH = 0x00

Horizontal Backporch = HorizontalBlanking – (HorizontalSyncOffset + HorizontalSyncPulseWidth)

Horizontal Backporch = 280 – (88 + 44)

CHA_HORIZONTAL_BACK_PORCH = 0x94

Horizontal Backporch = 148 or 0x94

Vertical Backporch = VerticalBlanking – (VerticalSyncOffset + VerticalSyncPulseWidth)

Vertical Backporch = 45 – (4 + 5)

Vertical Backporch = 36 or 0x24

CHA_VERTICAL_BACK_PORCH = 0x24

Horizontal Frontporch = HorizontalSyncOffset

Horizontal Frontporch = 88 or 0x58

CHA_HORIZONTAL_FRONT_PORCH = 0x58

Vertical Frontporch = VerticalSyncOffset

Vertical Frontporch = 4

CHA_VERTICAL_FRONT_PORCH = 0x04

9.2.1.2.2 DSI Design Procedure

The APU or GPU must provide a stream bit rate as required by the eDP panel. In this particular example, the eDP panel stream rate is 3.564 Gbps. Because the SN65DSIx6 can support a DSI clock rate of up to 750 MHz (or 1.5 Gbps), the minimum number of required DSI lanes to meet the stream bit rate is three lanes. But in this example, the APU/GPU maximum DSI Clock frequency is 500 MHz. This means the number of required DSI lanes will need to be increased to four lanes.

Min number of DSI Lanes = StreamBitRate / MaxDSIClock

Min number of DSI Lanes = 3564 MBps / (500 × 2)

Min number of DSI Lanes = 3.564 lanes

Min number of DSI Lanes = 4 lanes

After determining the number of required DSI lanes, the next step is to determine the minimum required DSI clock frequency to support the stream bit rate of the eDP panel. For 24 bpp, the calculation for determining the DSI clock frequency is as follows:

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Min Required DSI Clock Frequency = StreamBitRate / (Min_Number_DSI_Lanes × 2)

Min Required DSI Clock Frequency = 3564 / (4 × 2)

Min Required DSI Clock Frequency = 445.5 MHz

In this example, the clock source for the SN65DSIx6 is the REFCLK pin. When using the REFCLK as the clock source, any DSI Clock frequency is supported. But if the clock source was instead the DSI A clock, then the required DSI Clock frequency would need to change to a frequency supported by the SN65DSIx6. When operating in this mode, any one of the following DSI A clock frequencies can be used: 384 MHz, 416 MHz, 460.8 MHz, 468 MHz, or 486 MHz. In most cases, a eDP panel would support some variation from the ideal pixel clock frequency. For this example either 416 MHz or 460.8 MHz could be tried.

The DSI mode, number of lanes, and DSI Clock frequency needs to be programmed into the SN65DSIx6.

DSI_CHANNEL_MODE = 1 (Single DSI Channel)

CHA_DSI_LANES = 3 (for 4 lanes)

CHA_DSI_CLK_RANGE = 0x59 (equates to 445 MHz)

REFCLK_FREQ = 0x06 (27 MHz)

9.2.1.2.3 Example Script

This example configures the SN65DSIx6 for the following configuration:

```
<aardvark>
<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0" />
<i2c_bitrate khz="100" />

======REFCLK 27MHz ======
<i2c_write addr="0x2D" count="1" radix="16">0A 06</i2c_write> />

======Single 4 DSI lanes======
<i2c_write addr="0x2D" count="1" radix="16">10 26</i2c_write> />

======DSIA CLK FREQ 445MHz======
<i2c_write addr="0x2D" count="1" radix="16">12 59</i2c_write> />

======enhanced framing and ASSR======
<i2c_write addr="0x2D" count="1" radix="16">5A 05</i2c_write> />

======2 DP lanes no SSC======
<i2c_write addr="0x2D" count="1" radix="16">93 20</i2c_write> />

======HBR (2.7Gbps)======
<i2c_write addr="0x2D" count="1" radix="16">94 80</i2c_write> />

======PLL ENABLE======
<i2c_write addr="0x2D" count="1" radix="16">0D 01</i2c_write> <sleep ms="10" />

======Verify PLL is locked======
<i2c_write addr="0x2D" count="0" radix="16">0A</i2c_write> />
<i2c_read addr="0x2D" count="2" radix="16">00</i2c_read> <sleep ms="10" />

======POST-Cursor2 0dB ======
<i2c_write addr="0x2D" count="1" radix="16">95 00</i2c_write> />

======Write DPCD Register 0x0010A in Sink to Enable ASSR======
<i2c_write addr="0x2D" count="1" radix="16">64 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">74 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">75 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">76 0A</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">77 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">78 81</i2c_write> <sleep ms="10" />

======Semi-Auto TRAIN ======
<i2c_write addr="0x2D" count="1" radix="16">96 0A</i2c_write> <sleep ms="20" />
```

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```
======Verify Training was successful======
<i2c_write addr="0x2D" count="0" radix="16">96</i2c_write> />
<i2c_read addr="0x2D" count="1" radix="16">00</i2c_read> <sleep ms="10" />

=====CHA_ACTIVE_LINE_LENGTH is 1920 =======
<i2c_write addr="0x2D" count="2" radix="16">20 80 07</i2c_write> />

=====CHA_VERTICAL_DISPLAY_SIZE is 1080 =======
<i2c_write addr="0x2D" count="2" radix="16">24 38 04</i2c_write> />

=====CHA_HSYNC_PULSE_WIDTH is 44 positive =======
<i2c_write addr="0x2D" count="2" radix="16">2C 2C 00</i2c_write> />

=====CHA_VSYNC_PULSE_WIDTH is 5 positive=======
<i2c_write addr="0x2D" count="2" radix="16">30 05 80</i2c_write> />

=====CHA_HORIZONTAL_BACK_PORCH is 148=======
<i2c_write addr="0x2D" count="1" radix="16">34 94</i2c_write> />

=====CHA_VERTICAL_BACK_PORCH is 36=======
<i2c_write addr="0x2D" count="1" radix="16">36 24</i2c_write> />

=====CHA_HORIZONTAL_FRONT_PORCH is 88=======
<i2c_write addr="0x2D" count="1" radix="16">38 58</i2c_write> />

=====CHA_VERTICAL_FRONT_PORCH is 4=======
<i2c_write addr="0x2D" count="1" radix="16">3A 04</i2c_write> />

======DP- 24bpp======
<i2c_write addr="0x2D" count="1" radix="16">5B 00</i2c_write> />

=====COLOR BAR disabled=======
<i2c_write addr="0x2D" count="1" radix="16">3C 00</i2c_write> />

======enhanced framing, ASSR, and Vstream enable======
<i2c_write addr="0x2D" count="1" radix="16">5A 0D</i2c_write> />

</aardvark>
```


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9.2.1.3 Application Curve

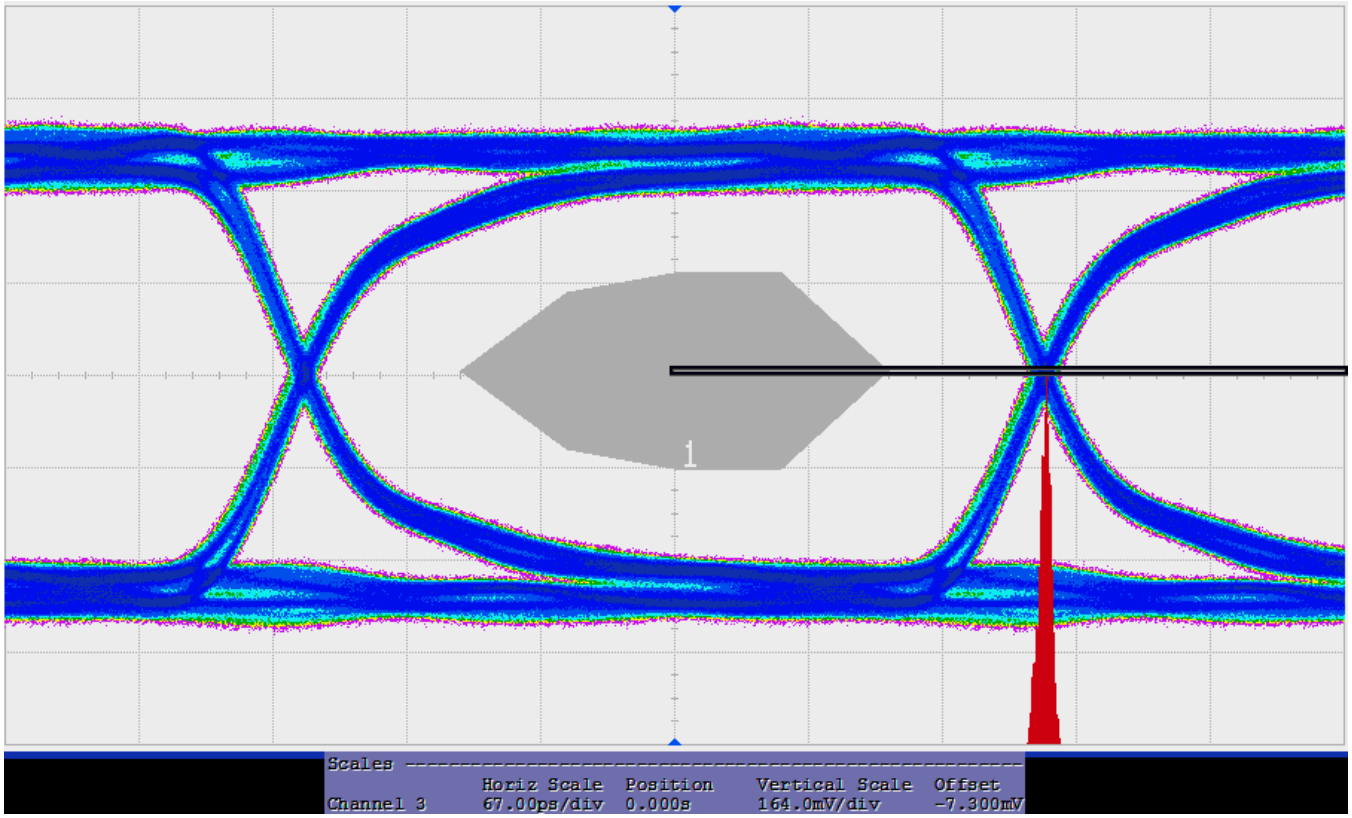


Figure 21. HBR Eye Diagram

10 Power Supply Recommendations

10.1 V_{CC} Power Supply

Each V_{CC} power supply pin should have a 100-nF capacitor to ground connected as close as possible to SN65DSIx6. TI recommends to have one bulk capacitor (1 µF to 10 µF) on it. TI recommends to have the pins connected to a solid power plane

10.2 V_{CCA} Power supply

Each V_{CCA} power supply pin should have a 100-nF capacitor to ground connected as close as possible to SN65DSIx6. TI recommends to have one bulk capacitor (1 µF to 10 µF) on it. TI recommends to have the pins connected to a solid power plane.

10.3 V_{PLL} and V_{CCIO} Power Supplies

The V_{PLL} and V_{CCIO} pins can be tied together or isolated. Regardless of how these two supplies are connected, a 100-nF capacitor to ground should be placed as close as possible to each power pin. TI recommends to have a bulk capacitor (1 µF) near the V_{PLL} pin.

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11 Layout

11.1 Layout Guidelines

To minimize the power supply noise floor, provide good decoupling near the SN65DSIx6 power pins. The use of four ceramic capacitors (2 × 0.1 μF and 2 × 0.1 μF) provides good performance. At the very least, TI recommends to install one 0.1-μF and one 0.01-μF capacitors near the SN65DSIx6. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized. Placing the capacitor underneath the SN65DSIx6 on the bottom of the PCB is often a good choice.
Note: The power supplies V_{PLL}, V_{CCIO}, V_{CCA}, and V_{CC} can be applied simultaneously.

11.1.1 DSI Guidelines

1. DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (± 20%) or 50-Ω single-ended impedance (±15%).
2. Keep away from other high speed signals.
3. Keep lengths to within 5 mils of each other.
4. Length matching should be near the location of mismatch. See Figure 4 for an example.
5. Each pair should be separated at least by 3 times the signal trace width.
6. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135°. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
7. Route all differential pairs on the same of layer.
8. The number of VIAS should be kept to a minimum. TI recommends to keep the VIAS count to 2 or less.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane split.
11. Adding Test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.
12. The maximum trace length over FR4 between SN65DSI86 and the GPU is 25 to 30 cm.

11.1.2 eDP Guidelines

1. ML*P/N pairs should be routed with controlled 100-Ω differential impedance (± 20%) or 50-Ω single-ended impedance (± 15%).
2. Keep away from other high speed signals.
3. Keep lengths to within 5 mils of each other.
4. Length matching should be near the location of mismatch. See Figure 4 for an example.
5. Each pair should be separated at least by 3 times the signal trace width.
6. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135°. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI
7. Route all differential pairs on the same of layer.
8. The number of VIAS should be kept to a minimum. TI recommends to keep the VIAS count to 2 or less.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane split.
11. Adding Test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.
12. The maximum trace length over FR4 between SN65DSIx6 and the eDP receptacle is 4 inches for data rates less than or equal to HBR (2.7 Gbps) and 2 inches for HBR2 (5.4 Gbps).

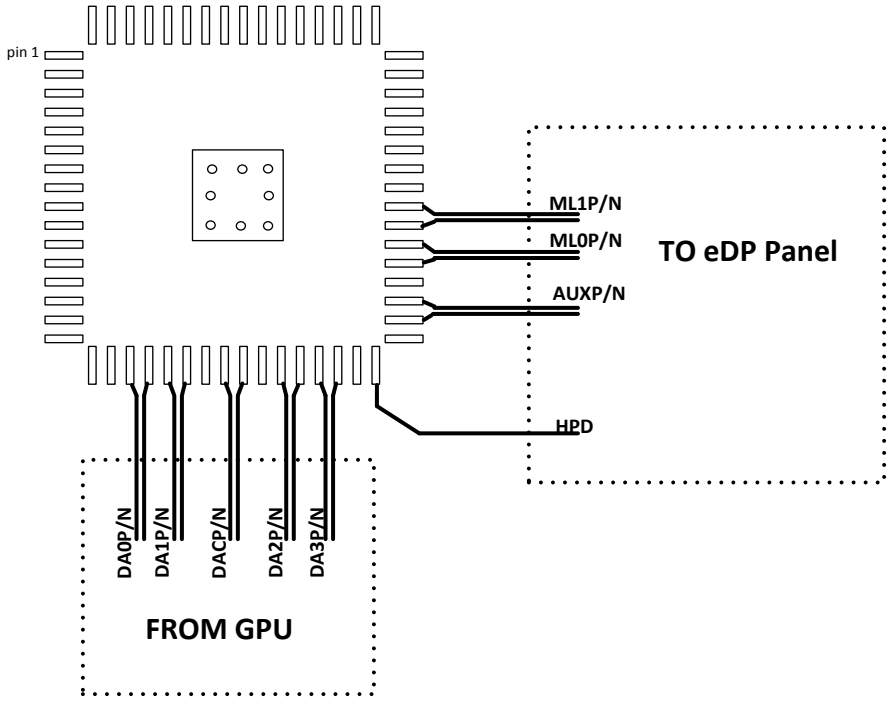
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Layout Guidelines (continued)

11.1.3 Ground

TI recommends that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the SN65DSIx6 should be connected to this plane with vias.

11.2 Layout Example



12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

《SN65DSI86 和 SN65DSI96 硬件实现指南》（文献编号：SLLA343）
《SN65DSI86/SN65DSI96 EVM 用户手册》（文献编号：SLLU204）

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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VESA is a registered trademark of Video Electronics Standards Association (VESA).
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12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65DSI86IPAPQ1	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DSI86IQ1
SN65DSI86IPAPQ1.A	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DSI86IQ1
SN65DSI86IPAPRQ1	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DSI86IQ1
SN65DSI86IPAPRQ1.A	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DSI86IQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN65DSI86-Q1 :

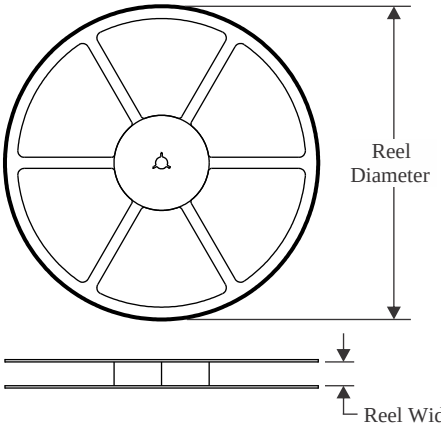
- Catalog : SN65DSI86

NOTE: Qualified Version Definitions:

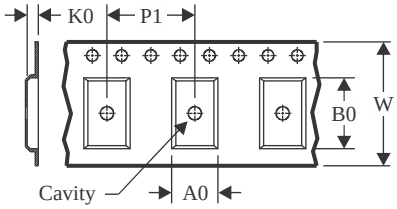
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

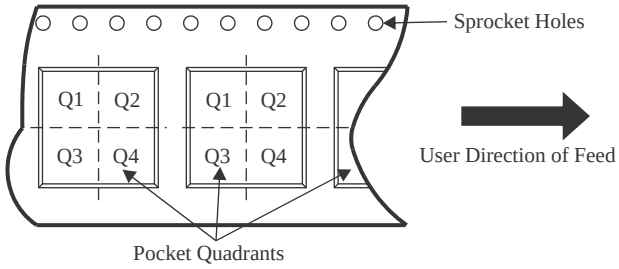


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

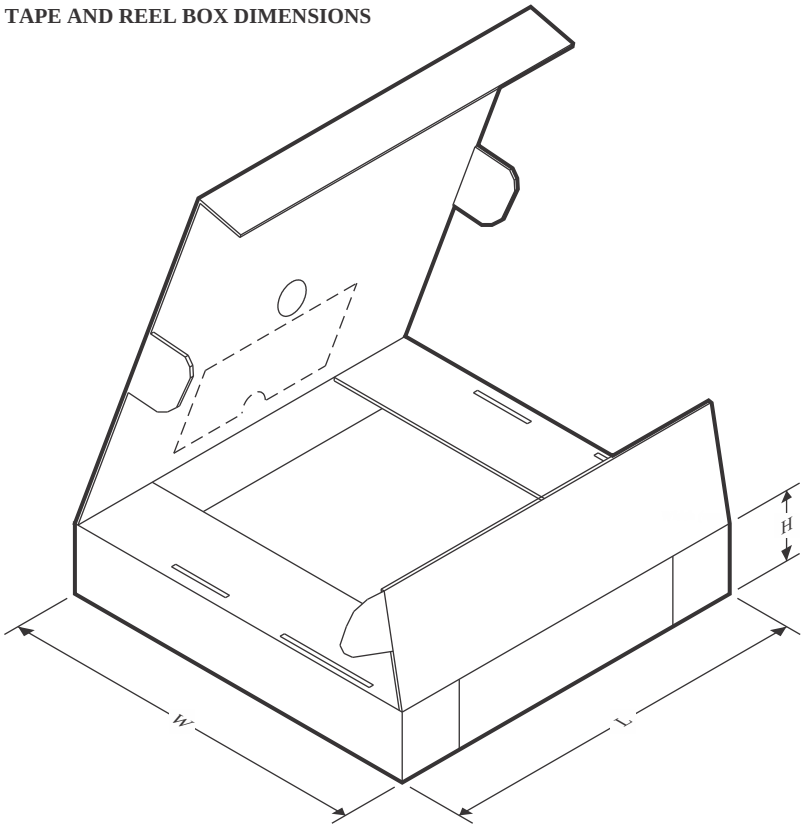
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65DSI86IPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

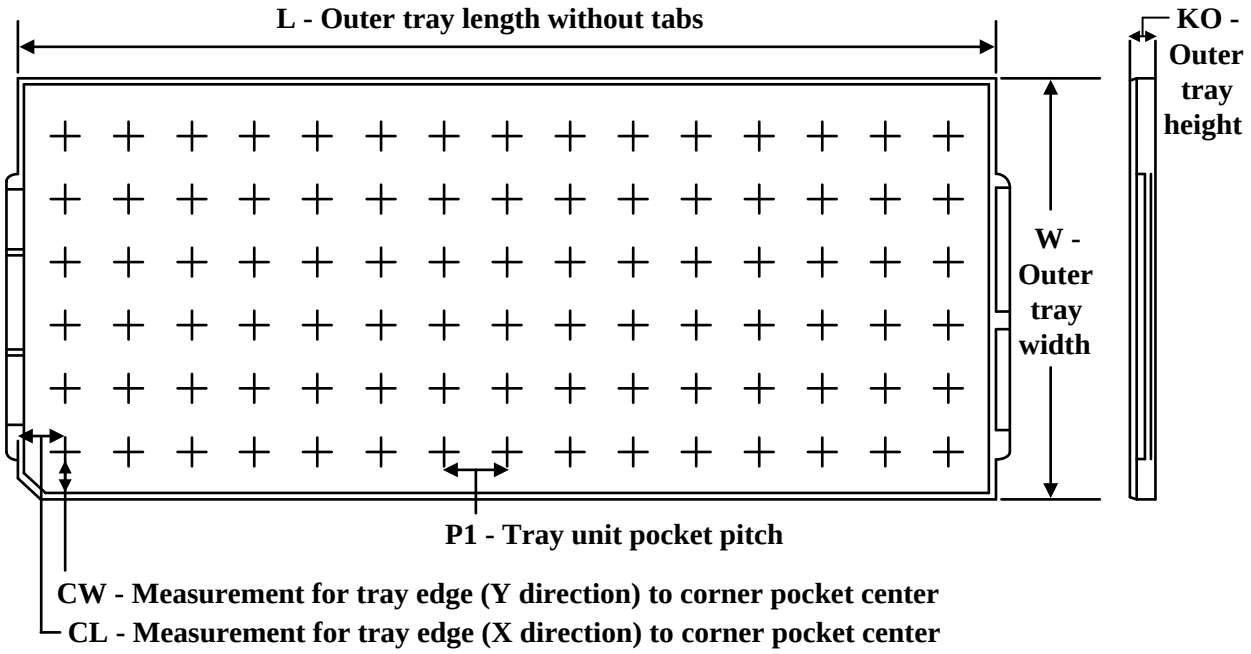
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65DSI86IPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN65DSI86IPAPQ1	PAP	HTQFP	64	160	8 X 20	150	322.6	135.9	7620	15.2	13.1	13
SN65DSI86IPAPQ1.A	PAP	HTQFP	64	160	8 X 20	150	322.6	135.9	7620	15.2	13.1	13

GENERIC PACKAGE VIEW

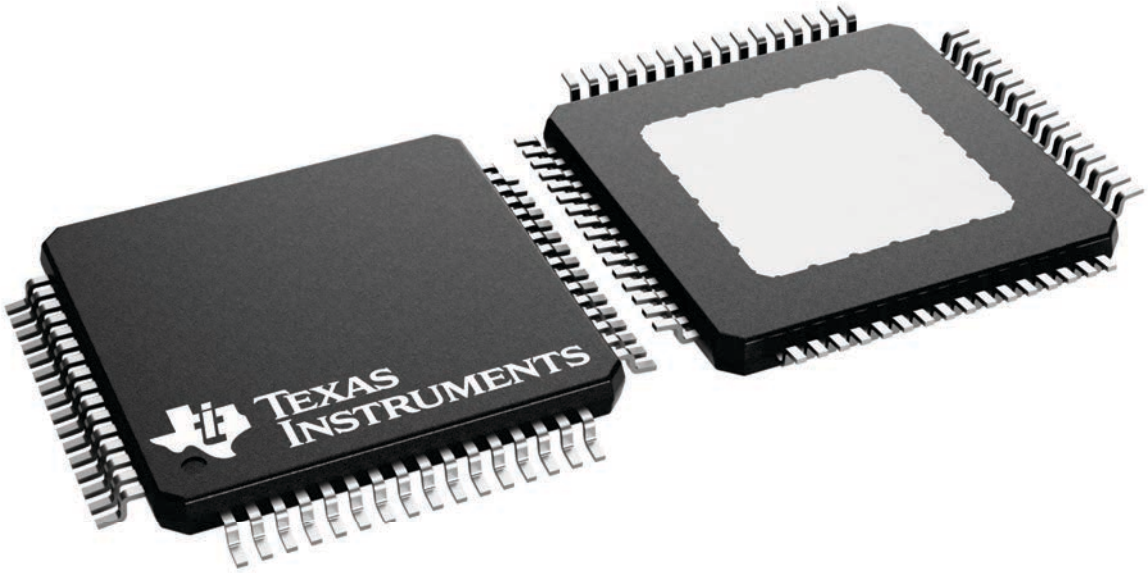
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



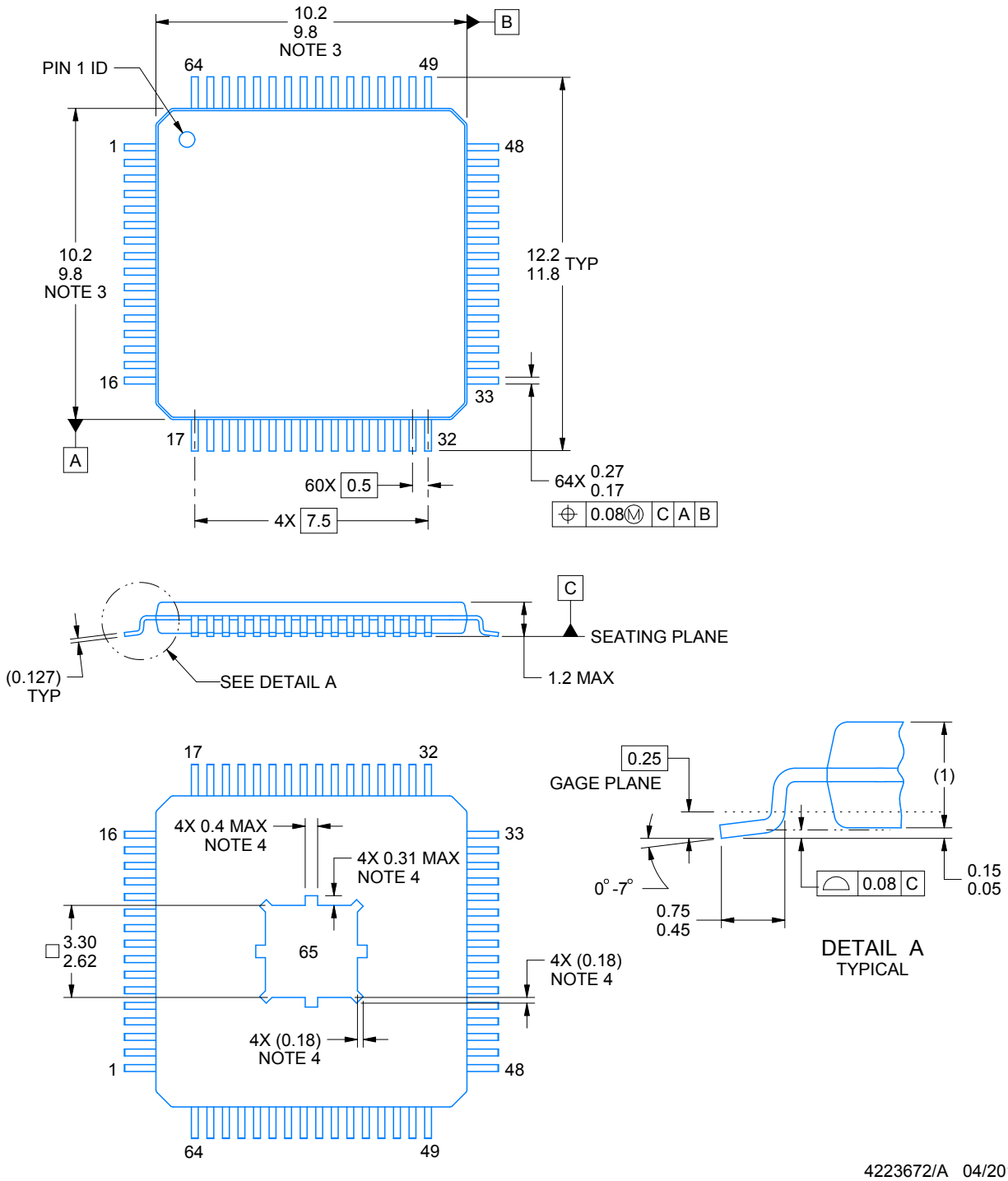
4226442/A

PACKAGE OUTLINE

PAP0064Q

PowerPAD™ TQFP - 1.2 mm max height

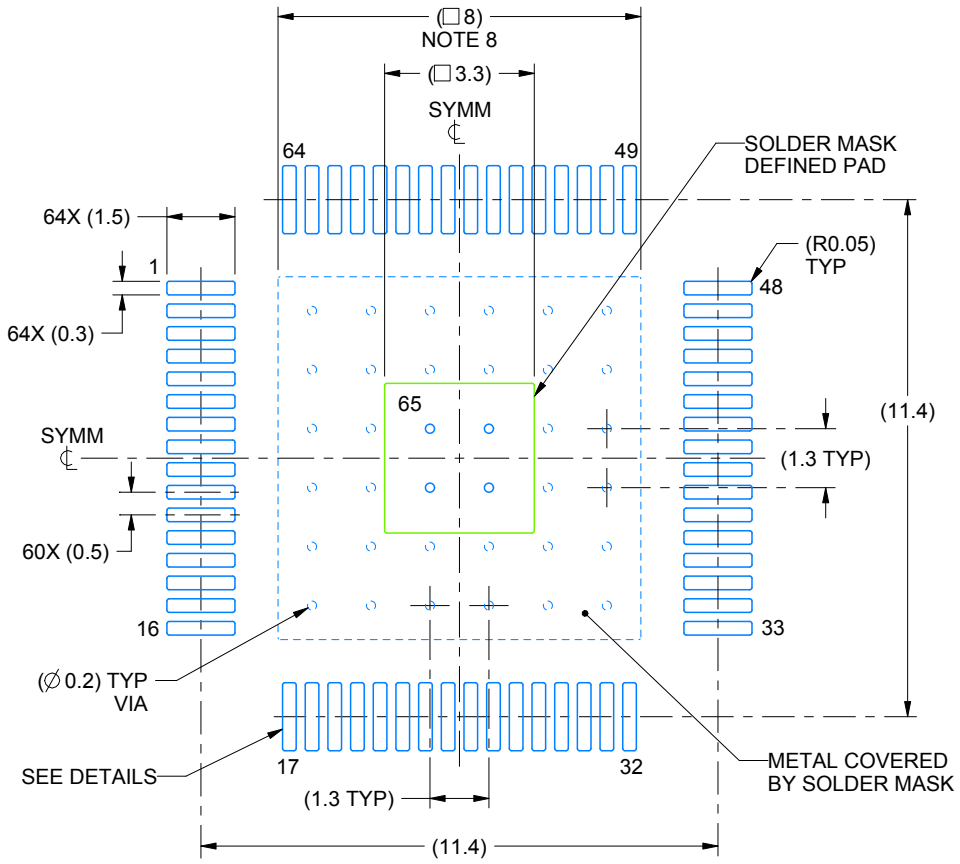
PLASTIC QUAD FLATPACK



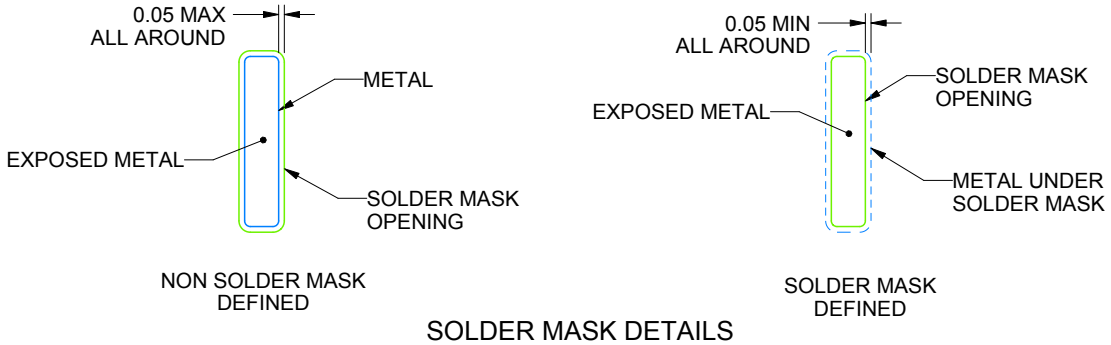
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

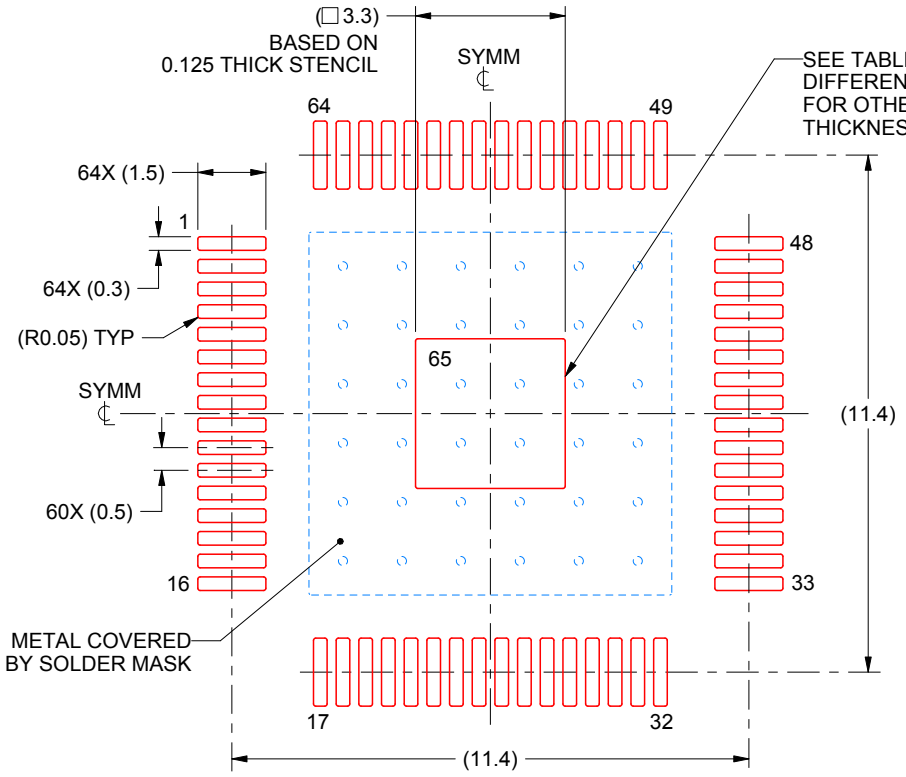


SOLDER MASK DETAILS

4223672/A 04/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4223672/A 04/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月