SN65DSI84-Q1 汽车用单通道 MIPI® DSI 转双链路 LVDS 桥接器

1 特性

- 符合汽车类应用的 要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 2：-40°C 至 105°C 的环境运行温度范围
  - 器件 HBM ESD 分类等级 3A
  - 器件 CDM ESD 分类等级 C6
- 实现了 MIPI D-PHY 版本 1.00.00 物理层前端和显示屏串行接口 (DSI) 版本 1.02.00
- 单通道 DSI 接收器每通道可配置 1、2、3 或 4 条 D-PHY 数据信道，每条信道的运行速率高达 1Gbps
- 支持 RGB666 和 RGB888 格式的 18bpp 与 24bpp DSI 视频流
- 适合 60fps WUXGA 1920 × 1200 分辨率（18bpp 和 24bpp 颜色），以及 60fps 1366 × 768 分辨率（18bpp 和 24bpp 颜色）
- 针对单链路或双链路 LVDS 的输出配置
- 支持单通道 DSI 转单链路 LVDS 的操作模式
- 双链路或单链路模式下 LVDS 输出时钟范围为 25MHz 到 154MHz
- LVDS 像素时钟可采用自由运行持续 D-PHY 时钟或外部基准时钟 (REFCLK)
- 1.8V 主 V_{CC} 电源
- 低功耗 特性 包括关断模式、低 LVDS 输出电压摆幅、共模以及 MIPI 超低功耗状态 (ULPS) 支持
- 针对简化印刷电路板 (PCB) 走线的 LVDS 通道交换 (SWAP)，LVDS 引脚顺序反向特性
- 采用 64 引脚 10mm × 10mm HTQFP (PAP) 封装 PowerPAD™IC 封装

2 应用

- 集成显示屏的信息娱乐系统主机
- 具有远程显示屏的信息娱乐系统主机
- 后座信息娱乐系统
- 混合动力汽车仪表板
- 便携式导航设备 (PND)
- 导航
- 工业人机界面 (HMI) 和显示屏

3 说明

SN65DSI84-Q1 DSI 转 LVDS 桥接器 具有 一个单通道 MIPI D-PHY 接收器前端配置，此配置中在每个通道上具有 4 条信道，每条信道的运行速率为 1Gbps，最大输入带宽为 4Gbps。桥接器可解码 MIPI®DSI 18bpp RGB666 和 24bpp RGB888 包，并将格式化视频数据流转换为 LVDS 输出（像素时钟范围为 25MHz 至 154MHz），从而提供双链路 LVDS 或单链路 LVDS（每个链路具有 4 个数据信道）。

SN65DSI84-Q1 器件非常适用于每秒帧数 (fps) 为 60 的 WUXGA (1920 × 1080)，每像素位数 (bpp) 高达 24 位。该器件实现了部分线路缓冲以适应 DSI 与 LVDS 接口间的数据流不匹配的情况。

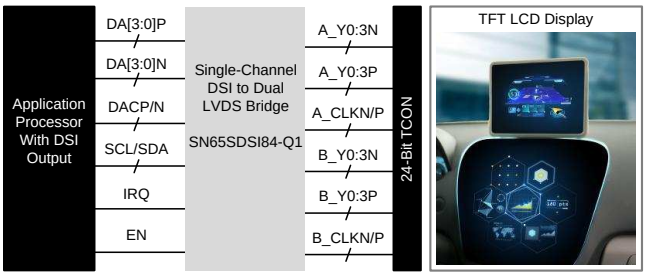
SN65DSI84-Q1 器件采用小外形 10mm × 10mm HTQFP（0.5mm 间距）封装，工作温度范围为 –40ºC 至 +105ºC。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
SN65DSI84-Q1	HTQFP (64)	10.00mm x 10.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

图 1. 典型应用



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目录

1 特性 1
2 应用 1
3 说明 1
4 修订历史记录 2
5 **Pin Configuration and Functions** 3
6 **Specifications** 5
6.1 Absolute Maximum Ratings 5
6.2 ESD Ratings 5
6.3 Recommended Operating Conditions 6
6.4 Thermal Information 6
6.5 Electrical Characteristics 6
6.6 Switching Characteristics 9
7 **Parameter Measurement Information** 9
8 **Detailed Description** 12
8.1 Overview 12
8.2 Functional Block Diagram 12
8.3 Feature Description 13
8.4 Device Functional Modes 14
8.5 Programming 22
8.6 Register Maps 23
9 **Application and Implementation** 38
9.1 Application Information 38
9.2 Typical Application 38
10 **Power Supply Recommendations** 45
10.1 V_{CC} Power Supply 45
10.2 VCORE Power Supply 45
11 **Layout** 45
11.1 Layout Guidelines 45
11.2 Layout Example 46
12 器件和文档支持 47
12.1 文档支持 47
12.2 接收文档更新通知 47
12.3 社区资源 47
12.4 商标 47
12.5 静电放电警告 47
12.6 术语表 47
13 机械、封装和可订购信息 48

4 修订历史记录

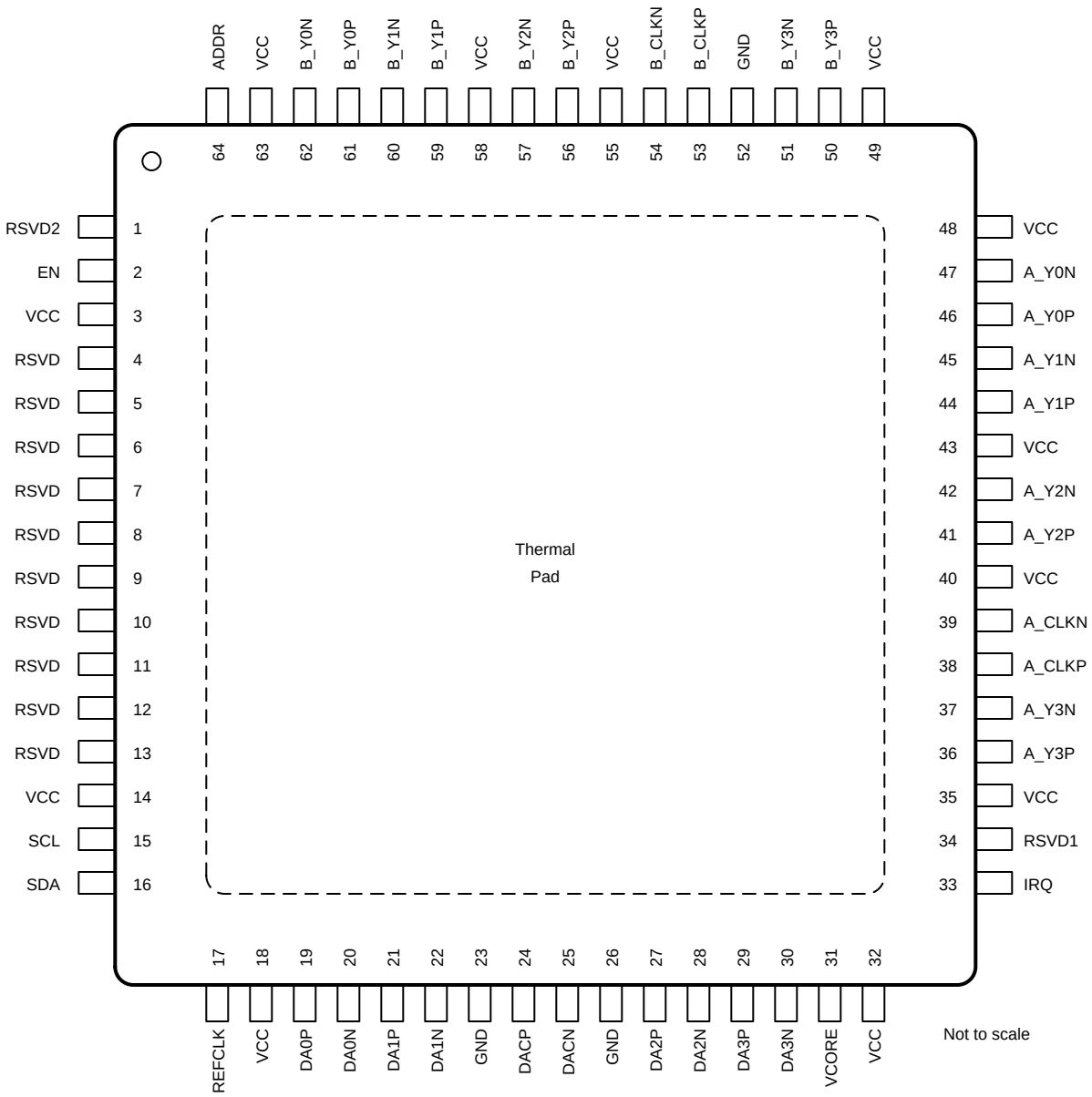
Changes from Original (December 2016) to Revision A **Page**

- Deleted figure *RESET and Initialization Timing Definition While V_{CC} is High* 11
- Changed the paragraph following Figure 8 14
- Changed *Recommended Initialization Sequence* To: *Initialization Sequence* 15
- Changed Table 2 15
- Changed item 3 in *Video Stop and Restart Sequence* From: Drive all DSI input lanes including DSI CLK lane to LP11. To: Drive all DSI data lanes to LP11, but keep the DSI CLK lanes in HS. 38

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5 Pin Configuration and Functions

PAP Package
64-Pin HTQFP With PowerPAD™
Top View



Not to scale

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Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADDR	64	I/O	Local I^2C interface target address select. See Table 4. In normal operation this pin is an input. When the ADDR pin is programmed high, it must be tied to the same 1.8-V power rails where the SN65DSI84-Q1 VCC 1.8-V power rail is connected.
A_Y0P	46	O	LVDS channel A, LVDS data output 0
A_Y0N	47	O	
A_Y1P	44	O	LVDS channel A, LVDS data output 1
A_Y1N	45	O	
A_Y2P	41	O	LVDS channel A, LVDS data output 2
A_Y2N	42	O	
A_Y3P	36	O	LVDS channel A, LVDS data output 3. A_Y3P and A_Y3N must be left not connected (NC) for 18-bpp panels.
A_Y3N	37	O	
A_CLKP	38	O	LVDS channel A, LVDS clock output
A_CLKN	39	O	
B_Y0P	61	O	LVDS channel B, LVDS data output 0
B_Y0N	62	O	
B_Y1P	59	O	LVDS channel B, LVDS data output 1
B_Y1N	60	O	
B_Y2P	56	O	LVDS channel B, LVDS data output 2
B_Y2N	57	O	
B_Y3P	50	O	LVDS channel B, LVDS data output 3. B_Y3P and B_Y3N must be left NC for 18-bpp panels.
B_Y3N	51	O	
B_CLKP	53	O	LVDS channel B, LVDS clock output
B_CLKN	54	O	
DA0P	19	I	MIPI D-PHY channel A, data lane 0; data rate up to 1 Gbps.
DA0N	20	I	
DA1P	21	I	MIPI D-PHY channel A, data lane 1; data rate up to 1 Gbps
DA1N	22	I	
DA2P	27	I	MIPI D-PHY channel A, data lane 2; data rate up to 1 Gbps.
DA2N	28	I	
DA3P	29	I	MIPI D-PHY channel A, data lane 3; data rate up to 1 Gbps.
DA3N	30	I	
DACP	24	I	MIPI D-PHY channel A, clock lane; data rate up to 1 Gbps.
DACN	25	I	
RSVD	4, 5, 6, 7, 8, 9, 10, 11, 12, 13	—	Leave unconnected
EN	2	I	Chip enable and reset. The device is reset (shutdown) when the EN pin is low.
GND	23, 26, 52	G	Reference ground
IRQ	33	O	Interrupt signal
REFCLK	17	I	This pin is an optional external reference clock for the LVDS pixel clock. If an external reference clock is not used, this pin must be pulled to ground with an external resistor. The source of the reference clock must be placed as close as possible with a series resistor near the source to reduce EMI.
RSVD1	34	I/O	Reserved. This pin must be left unconnected for normal operation.
RSVD2	1	I	Reserved. This pin must be left unconnected for normal operation.
SCL	15	I	Local I^2C interface clock.
SDA	16	I/O	Local I^2C interface data

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
V_{CC}	3	—	1.8-V power supply
	14	—	
	18	—	
	32	—	
	35	—	
	40	—	
	43	—	
	48	—	
	49	—	
	55	—	
	58	—	
	63	—	
VCORE	31	P	1.1-V output from the voltage regulator. This pin must have a 1-µF external capacitor to ground.
PowerPAD		—	Reference ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.3	2.175	V
	Input voltage	CMOS input pins	–0.5	2.175	V
		DSI input pins (DAxP, DAxN, DBxP, and DBxN)	–0.4	1.4	V
T_A	Operating free-air temperature		–40	105	°C
T_J	Junction temperature		–40	115	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Procedures*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CC}	V_{CC} power supply	1.65	1.8	1.95	V
V_{PSN}	Supply noise on any V_{CC} pin	$f_{(noise)}$ > 1 MHz		0.05	V
$V_{(DSI)}$	DSI input pin voltage	–50		1350	mV
$f_{(I2C)}$	Local I^2C input frequency			400	kHz
$f_{HS(CLK)}$	DSI high-speed (HS) clock input frequency	40		500	MHz
t_{su}	DSI HS data to clock setup time	0.15			UI(1)
t_h	DSI HS data to clock hold time	0.15			UI(1)
$Z_{OD(LVDS)}$	LVDS output differential impedance	90		132	Ω
T_C	Case temperature			92.2	°C

(1) The unit interval (UI) is one half of the period of the HS clock; at 500 MHz the minimum setup and hold time is 150 ps.

6.4 Thermal Information

THERMAL METRIC(1)		SN65DSI84-Q1 PAP (HTQFP) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IL}	Low-level control signal input voltage				0.3 × VCC	V
V_{IH}	High-level control signal input voltage		0.7 × VCC			V
V_{OH}	High-level output voltage	I_{OH} = –4 mA	1.25			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_{LKG}	Input failsafe leakage current	V_{CC} = 0; $V_{CC(PIN)}$ = 1.8 V			±30	µA
I_{IH}	High level input current	Any input terminal			±30	µA
I_{IL}	Low level input current	Any input terminal			±30	µA
I_{OZ}	High-impedance output current	CMOS output terminals			±10	µA
I_{OS}	Short-circuit output current	Any output driving GND short			±50	mA
I_{CC}	Device active current	See (2)		106	164	mA
I_{ULPS}	Device standby current	All data and clock lanes are in ultra-low power state (ULPS)		7.7	14	mA
I_{RST}	Shutdown current	EN = 0		0.04	130	µA
R_{EN}	EN control input resistor			200		kΩ

(1) All typical values are at V_{CC} = 1.8V and T_A = 25°C
(2) SN65DSI84-Q1: SINGLE Channel DSI to DUAL Channel LVDS, 1400 x 900
(a) number of LVDS lanes = 2 × (3 data lanes + 1 CLK lane)
(b) number of DSI lanes = 2 data lanes + 1 CLK lane
(c) LVDS CLK OUT = 53.25 M
(d) DSI CLK = 500 M
(e) RGB888, LVDS18 bpp
Maximum values are at V_{CC} = 1.95 V and T_A = 105°C

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
MIPI DSI INTERFACE						
V_{IH-LP}	LP receiver input high threshold	See Figure 2	880			mV
V_{IL-LP}	LP receiver input low threshold	See Figure 2			550	mV
$\|V_{ID}\|$	HS differential input voltage		100		270	mV
$\|V_{IDT}\|$	HS differential input voltage threshold				50	mV
$V_{IL-ULPS}$	LP receiver input low threshold; ultra-low power state (ULPS)				300	mV
V_{CM-HS}	HS common mode voltage; steady-state		70		330	mV
ΔV_{CM-HS}	HS common mode peak-to-peak variation including symbol delta and interference				100	mV
V_{IH-HS}	HS single-ended input high voltage	See Figure 2			460	mV
V_{IL-HS}	HS single-ended input low voltage	See Figure 2	–40			mV
$V_{TERM-EN}$	HS termination enable; single-ended input voltage (both Dp AND Dn apply to enable)	Termination is switched simultaneous for Dn and Dp			450	mV
$R_{DIFF-HS}$	HS mode differential input impedance		80		125	Ω
LVDS OUTPUT						
$\|V_{OD}\|$	Steady-state differential output voltage for A_Yx P/N and B_Yx P/N	CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 100 Ω near end termination	180	245	330	mV
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 100 Ω near end termination	215	293	392	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 100 Ω near end termination	250	341	455	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 100 Ω near end termination	290	389	515	
		CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 200 Ω near end termination	150	204	275	
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 200 Ω near end termination	200	271	365	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 200 Ω near end termination	250	337	450	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 200 Ω near end termination	300	402	535	

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Steady-state differential output voltage for A_CLKP/N and B_CLKP/N	CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 100 Ω near end termination	140	191	262	mV
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 100 Ω near end termination	168	229	315	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 100 Ω near end termination	195	266	365	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 100 Ω near end termination	226	303	415	
		CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 200 Ω near end termination	117	159	220	
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 200 Ω near end termination	156	211	295	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 200 Ω near end termination	195	263	362	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 200 Ω near end termination	234	314	435	
$\Delta\|V_{OD}\|$	Change in steady-state differential output voltage between opposite binary states	RL = 100 Ω			35	mV
$V_{OC(SS)}$	Steady state common-mode output voltage(3)	CSR 0x19.6 = 1 and CSR 0x1B.6 = 1; and, or CSR 0x19.4 = 1 and CSR 0x1B.4 = 1; see Figure 3	0.75	0.9	1.13	V
		CSR 0x19.6 = 0 and, or CSR 0x19.4 = 0; see Figure 3	1	1.25	1.5	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	see Figure 3			35	mV
R_{LVDS_DIS}	Pulldown resistance for disabled LVDS outputs			1		kΩ

(3) Tested at V_{CC} = 1.8V , T_A = –40°C for MIN, T_A = 25°C for TYP, T_A = 105°C for MAX.

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DSI						
t_{GS}	DSI LP glitch suppression pulse width				300	ps
LVDS						
t_c	Output clock period		6.49		40	ns
t_w	High-level output clock (CLK) pulse duration			4/7 t_c		ns
t_0	Delay time, CLK↑ to 1st serial bit position	t_c = 6.49 ns; Input clock jitter < 25 ps (REFCLK) See Figure 4	–0.15		0.15	ns
t_1	Delay time, CLK↑ to 2nd serial bit position		1/7 t_c – 0.15		1/7 t_c + 0.15	ns
t_2	Delay time, CLK↑ to 3rd serial bit position		2/7 t_c – 0.15		2/7 t_c + 0.15	ns
t_3	Delay time, CLK↑ to 4th serial bit position		3/7 t_c – 0.15		3/7 t_c + 0.15	ns
t_4	Delay time, CLK↑ to 5th serial bit position		4/7 t_c – 0.15		4/7 t_c + 0.15	ns
t_5	Delay time, CLK↑ to 6th serial bit position		5/7 t_c – 0.15		5/7 t_c + 0.15	ns
t_6	Delay time, CLK↑ to 7th serial bit position		6/7 t_c – 0.15		6/7 t_c + 0.15	ns
t_r	Differential output rise-time	See Figure 4	180		500	ps
t_f	Differential output fall-time					
	LVDS CLK A to CLK B skew		–10		10	ps
EN, ULPS, RESET						
t_{en}	Enable time from EN or ULPS; see	$t_{c(o)}$ = 12.9 ns			1	ms
t_{dis}	Disable time to standby	$t_{c(o)}$ = 12.9 ns			0.1	ms
t_{reset}	Reset Time		10			ms
REFCLK						
F_{REFCLK}	REFCLK Freqeuncy. Supported frequencies: 25 MHz - 15 4MHz		25		154	MHz
t_r, t_f	REFCLK rise and fall time		0.1		1	ns
t_{pj}	REFCLK Peak-to-Peak Phase Jitter				50	ps
Duty	REFCLK Duty Cycle		40%	50%	60%	
REFCLK or DSI CLK (DACP/N, DBCP/N)						
SSC_CLKIN	SSC enabled Input CLK center spread depth(2)		0.5%	1%	2%	
	Modulation Frequency Range		30		60	kHz

(1) All typical values are at V_{CC} = 1.8 V and T_A = 25°C
(2) For EMI reduction purpose, SN65DSI84-Q1 supports the center spreading of the LVDS CLK output through the REFCLK or DSI CLK input. The center spread CLK input to the REFCLK or DSI CLK is passed through to the LVDS CLK output A_CLKP/N and/or B_CLKP/N.

7 Parameter Measurement Information

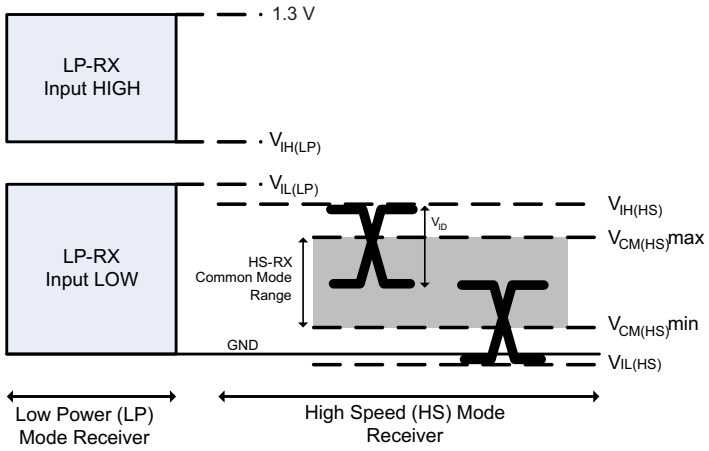


Figure 2. DSI Receiver Voltage Definitions

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Parameter Measurement Information (continued)

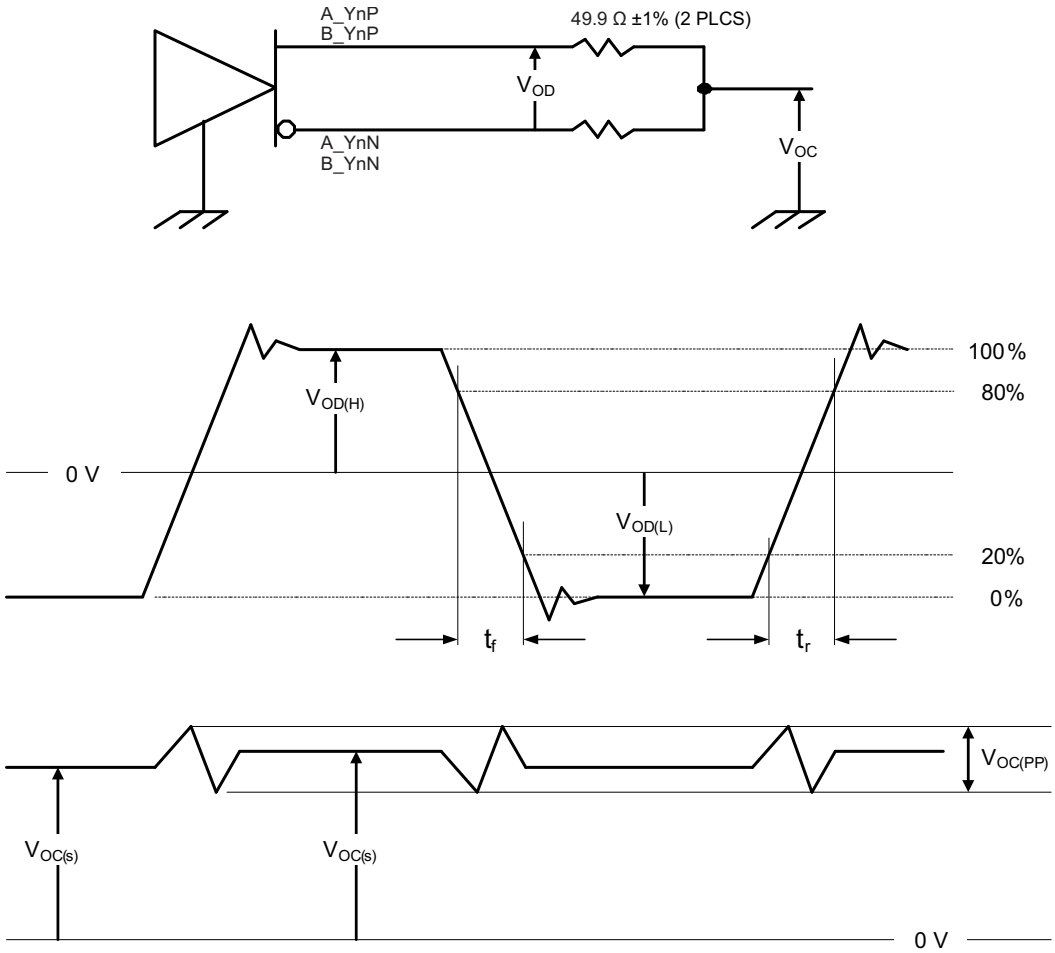


Figure 3. Test Load and Voltage Definitions for LVDS Outputs

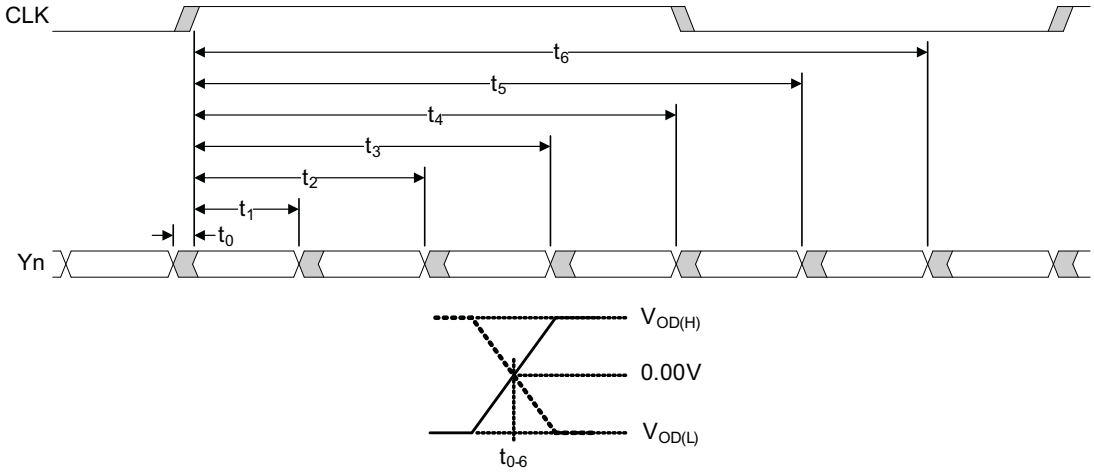
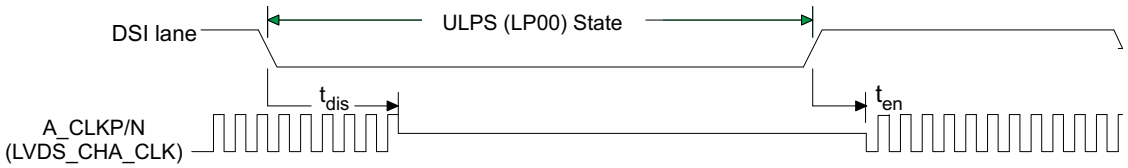


Figure 4. SN65DSI84-Q1 LVDS Timing Definitions

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Parameter Measurement Information (continued)



(1) See the *ULPS* section of the data sheet for the ULPS entry and exit sequence.

(2) ULPS entry and exit protocol and timing requirements must be met according to the MIPI DPHY specification.

Figure 5. ULPS Timing Definition

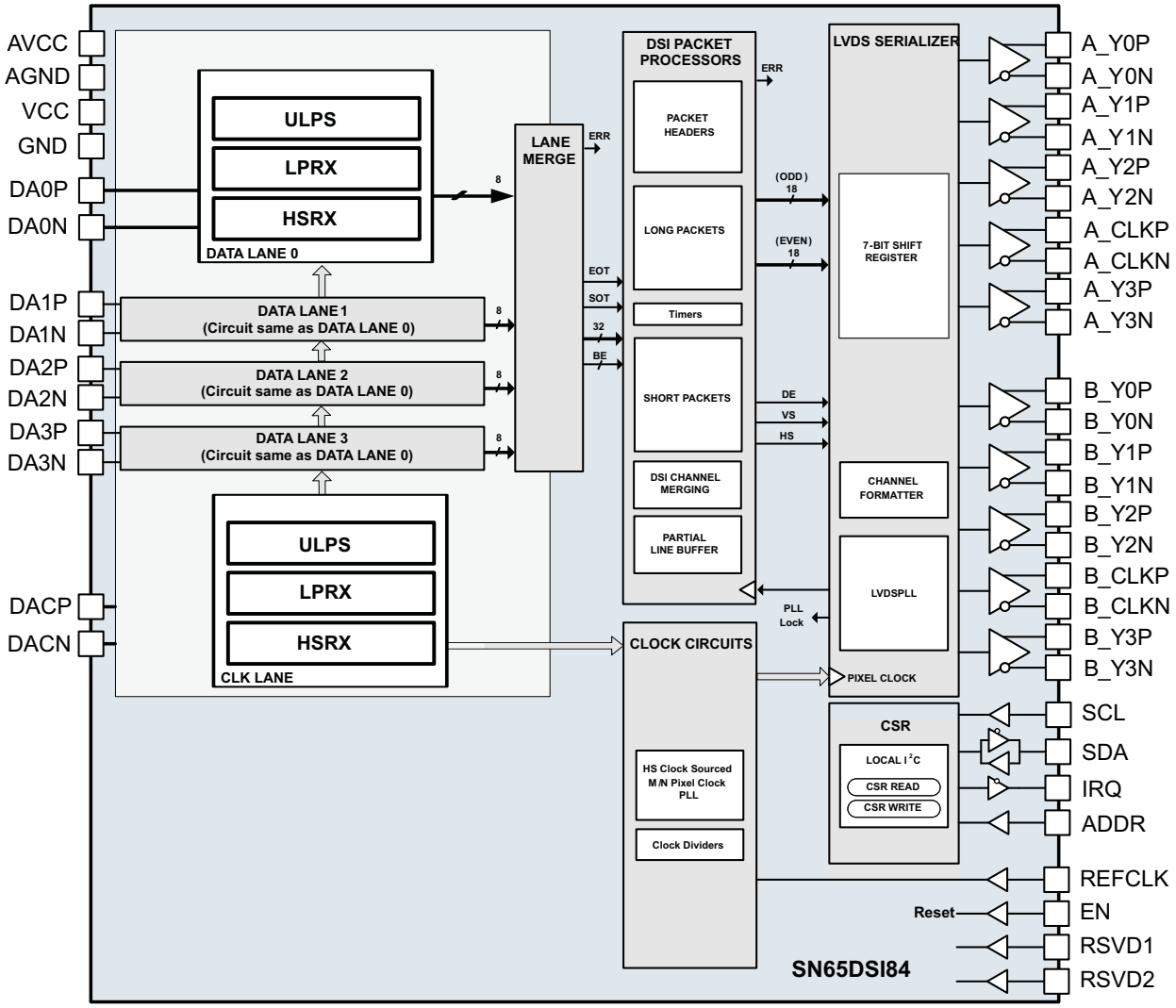
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8 Detailed Description

8.1 Overview

The SN65DSI84-Q1 DSI to LVDS bridge features a single-channel MIPI D-PHY receiver front-end configuration with 4 lanes per channel operating at 1 Gbps per lane; a maximum input bandwidth of 4 Gbps. The bridge decodes MIPI DSI 18-bpp RGB666 and 240-bpp RG888 packets and converts the formatted video data stream to a LVDS compatible LVDS output operating at pixel clocks operating from 25 MHx to 154 MHz, offering a Dual-Link LVDS, Single-Link LVDS interface with four data lanes per link.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Clock Configurations and Multipliers

The LVDS clock may be derived from the DSI channel A clock, or from an external reference clock source. When the MIPI D-PHY channel A HS clock is used as the LVDS clock source, the D-PHY clock lane must operate in HS free-running (continuous) mode; this feature eliminates the requirement for an external reference clock reducing system costs

The reference clock source is selected by HS_CLK_SRC (CSR 0x0A.0) programmed through the local I^2C interface. If an external reference clock is selected, it is multiplied by the factor in REFCLK_MULTIPLIER (CSR 0x0B.1:0) to generate the LVDS output clock. When an external reference clock is selected, it must be between 25 MHz and 154 MHz. If the DSI channel A clock is selected, it is divided by the factor in DSI_CLK_DIVIDER (CSR 0x0B.7:3) to generate the LVDS output clock. Additionally, LVDS_CLK_RANGE (CSR 0x0A.3:1) and CH_DSI_CLK_RANGE(CSR 0x12) must be set to the frequency range of the LVDS output clock for and DSI Channel A input clock respectively the internal PLL to operate correctly. After these settings are programmed, PLL_EN (CSR 0x0D.0) must be set to enable the internal PLL.

8.3.2 ULPS

The SN65DSI84-Q1 supports the MIPI defined ultra-low power state (ULPS). While the device is in the ULPS, the CSR registers are accessible via I2C interface. ULPS sequence should be issued to all active DSI CLK and/or DSI data lanes of the enabled DSI Channels for the SN65DSI84-Q1 enter the ULPS. The Following sequence should be followed to enter and exit the ULPS.

1. Host issues a ULPS entry sequence to all DSI CLK and data lanes enabled.
2. When host is ready to exit the ULPS mode, host issues a ULPS exit sequence to all DSI CLK and data lanes that must be active in normal operation.
3. Wait for a minimum of 3 ms.
4. Set the SOFT_RESET bit (CSR 0x09.0).
5. Device resumes normal operation.(i.e video streaming resumes on the panel).

8.3.3 LVDS Pattern Generation

The SN65DSI84-Q1 supports a pattern generation feature on LVDS Channels. This feature can be used to test the LVDS output path and LVDS panels in a system platform. The pattern generation feature can be enabled by setting the CHA_TEST_PATTERN bit at address 0x3C. No DSI data is received while the pattern generation feature is enabled.

Three modes are available for LVDS test pattern generation. The mode of test pattern generation is determined by register configuration as shown in Table 1.

Table 1. Video Registers

Addr. bit	Register Name
0x20.7:0	CHA_ACTIVE_LINE_LENGTH_LOW
0x21.3:0	CHA_ACTIVE_LINE_LENGTH_HIGH
0x24.7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW
0x25.3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH
0x2C.7:0	CHA_HSYNC_PULSE_WIDTH_LOW
0x2D.1:0	CHA_HSYNC_PULSE_WIDTH_HIGH
0x30.7:0	CHA_VSYNC_PULSE_WIDTH_LOW
0x31.1:0	CHA_VSYNC_PULSE_WIDTH_HIGH
0x34.7:0	CHA_HORIZONTAL_BACK_PORCH
0x36.7:0	CHA_VERTICAL_BACK_PORCH
0x38.7:0	CHA_HORIZONTAL_FRONT_PORCH
0x3A.7:0	CHA_VERTICAL_FRONT_PORCH

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8.4 Device Functional Modes

8.4.1 Reset Implementation

When EN is de-asserted (low), the SN65DSI84-Q1 is in SHUTDOWN or RESET state. In this state, CMOS inputs are ignored, the MIPI® D-PHY inputs are disabled and outputs are high impedance. The EN input must transmit from a low to a high level after the V_{CC} supply has reached the minimum operating voltage as shown in Figure 6. This is achieved by a control signal to the EN input, or by an external capacitor connected between EN and GND.

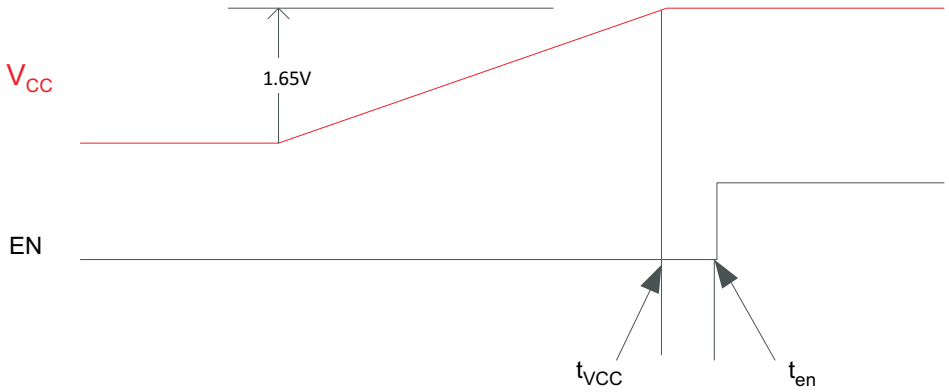


Figure 6. Cold Start V_{CC} Ramp up to EN

When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V_{CC} supply, where a slower ramp-up results in a larger value external capacitor. See the latest reference schematic for the SN65DSI84-Q1 device and, or consider approximately 200 nF capacitor as a reasonable first estimate for the size of the external capacitor.

Both EN implementations are shown in Figure 7 and Figure 8.

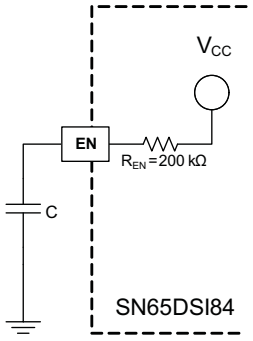


Figure 7. External Capacitor Controlled EN

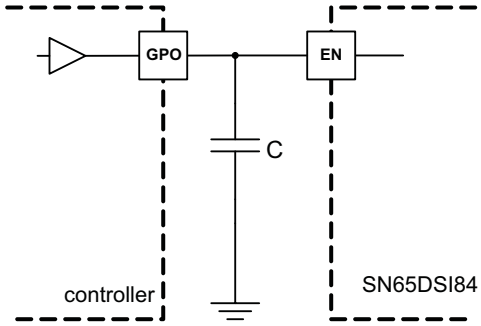


Figure 8. EN Input From Active Controller

When the SN65DSI84-Q1 is reset while V_{CC} is high, the EN pin must be held low for at least 10 ms before being asserted high as described in Table 2 to be sure that the device is properly reset. The DSI CLK lane MUST be in HS and the DSI data lanes MUST be driven to LP11 while the device is in reset before the EN pin is asserted per the timing described in Table 2.

8.4.2 Initialization Sequence

Use the following initialization sequence to setup the SN65DSI84-Q1. This sequence is required for proper operation of the device. Steps 9 through 11 in the sequence are optional.

Also see to Figure 6.

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Device Functional Modes (continued)

Table 2. Initialization Sequence

INITIALIZATION SEQUENCE NUMBER	INITIALIZATION SEQUENCE DESCRIPTION
Init seq 1	Power on
Init seq 2	After power is applied and stable, the DSI CLK lanes MUST be in HS state and the DSI data lanes MUST be driven to LP11 state
Init seq 3	Set EN pin to Low
Wait 10 ms (1)	
Init seq 4	Tie EN pin to High
Wait 10 ms (1)	
Init seq 5	Initialize all CSR registers to their appropriate values based on the implementation (The SN65DSI8x is not functional until the CSR registers are initialized)
Init seq 6	Set the PLL_EN bit (CSR 0x0D.0)
Wait 10 ms (1)	
Init seq 7	Set the SOFT_RESET bit (CSR 0x09.0)
Wait 10 ms (1)	
Init seq 8	Change DSI data lanes to HS state and start DSI video stream
Wait 5 ms (1)	
Init seq 9	Read back all resisters and confirm they were correctly written
Init seq 10	Write 0xFF to CSR 0xE5 to clear the error registers
Wait 1 ms (1)	
Init seq 11	Read CSR 0xE5. If CSR 0xE5!= 0x00, then go back to step #2 and re-initialize

(1) Minimum recommended delay. It is fine to exceed these.

8.4.3 LVDS Output Formats

The SN65DSI84-Q1 processes DSI packets and produces video data driven to the LVDS interface in an industry standard format. Single-Link LVDS and Dual-Link LVDS are supported by the SN65DSI84-Q1; when the LVDS output is implemented in a Dual-Link configuration, channel A carries the odd pixel data, and channel B carries the even pixel data. During conditions such as the default condition, and some video synchronization periods, where no video stream data is passing from the DSI input to the LVDS output, the SN65DSI84-Q1 transmits zero value pixel data on the LVDS outputs while maintaining transmission of the vertical sync and horizontal sync status.

Figure 9 illustrates a Single-Link LVDS 18bpp application.

Figure 10 illustrates a Dual-Link 24 bpp application using Format 2, controlled by CHA_24BPP_FORMAT1 (CSR 0x18.1) and CHB_24BPP_FORMAT1 (CSR 0x18.0). In data Format 2, the two MSB per color are transferred on the Y3P/N LVDS lane.

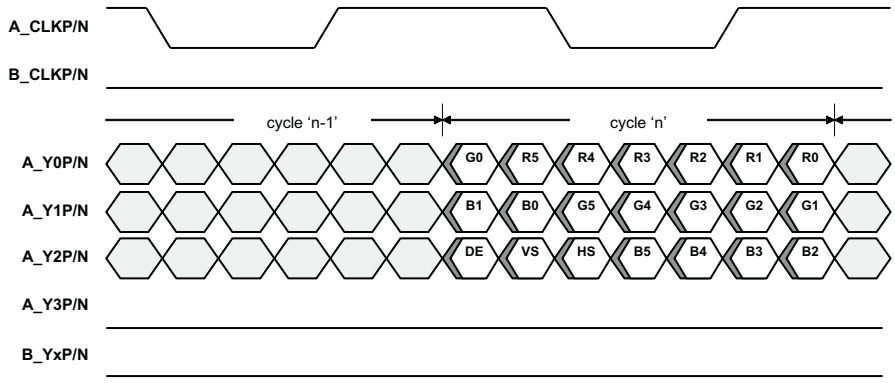
Figure 11 illustrates a 24 bpp Single-Link application using Format 1. In data Format 1, the two LSB per color are transferred on the Y3P/N LVDS lane.

Figure 12 illustrates a Single-Link LVDS application where 24 bpp data is received from DSI and converted to 18 bpp data for transmission to an 18 bpp panel. This application is configured by setting CHA_24BPP_FORMAT1 (CSR 0x18.1) to ‘1’ and CHA_24BPP_MODE (CSR 0x18.3) to ‘0’. In this configuration, the SN65DSI84-Q1 will not transmit the 2 LSB per color because the Y3P/N LVDS lane is disabled.

NOTE

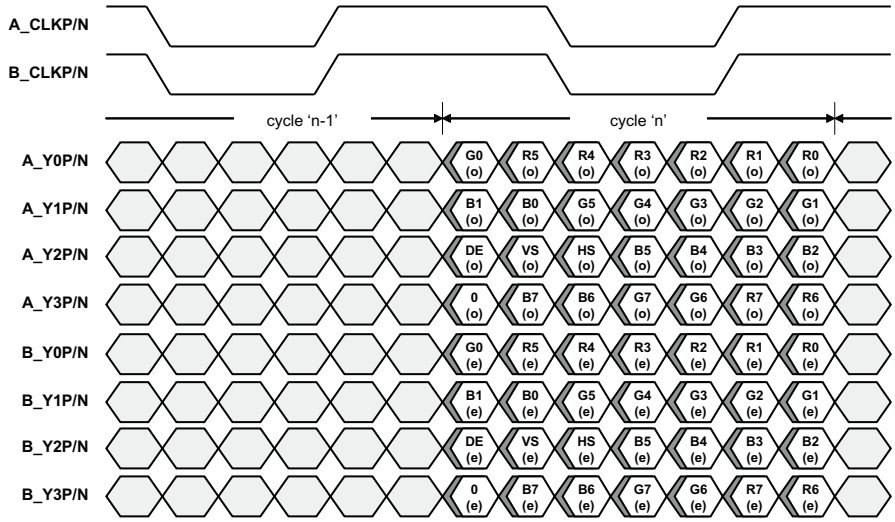
Note: Figure 9, Figure 10, Figure 11, and Figure 12 only illustrate a few example applications for the SN65DSI84-Q1. Other applications are also supported.

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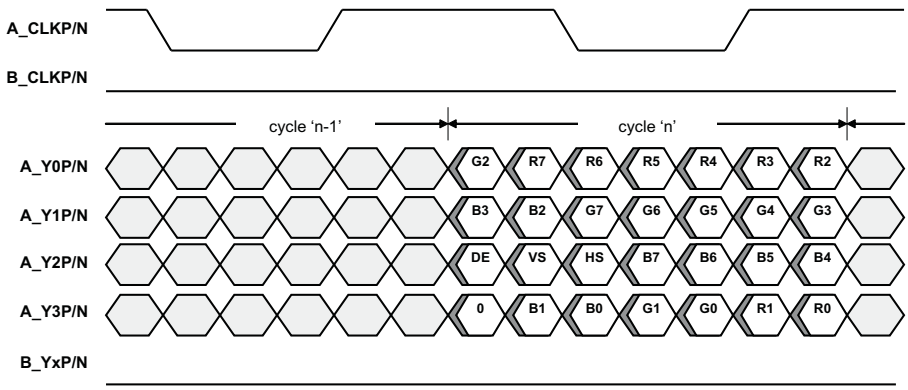
DE = Data Enable; Channel B Clock, Channel B Data, and A_Y3P/N are Output Low

Figure 9. LVDS Output Data; Single-Link 18 Bpp



DE = Data Enable; (o) = Odd Pixels; (e) = Even Pixels

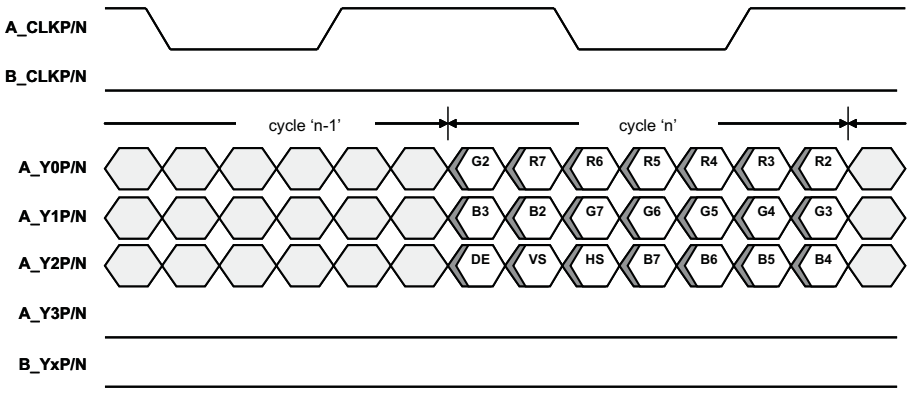
Figure 10. LVDS Output Data (Format 2); Dual-Link 24 Bpp



DE = Data Enable; Channel B Clock and Data are Output Low

Figure 11. LVDS Output Data (Format 1); Single-Link 24 Bpp

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DE = Data Enable; Channel B Clock, Channel B Data, and A_Y3P/N a re Output Low; Channel B Clock, Channel B Data, and A_Y3P/N are Output Low

Figure 12. LVDS Output Data (Format 1); 24-Bpp to Single-Link 18-Bpp Conversion

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8.4.4 DSI Lane Merging

The SN65DSI84-Q1 supports four DSI data lanes per input channel, and may be configured to support one, two, or three DSI data lanes per channel. Unused DSI input pins on the SN65DSI84-Q1 should be left unconnected or driven to LP11 state. The bytes received from the data lanes are merged in HS mode to form packets that carry the video stream. DSI data lanes are bit and byte aligned.

Figure 13 illustrates the lane merging function for each channel; 4-Lane, 3-Lane, and 2-Lane modes are illustrated

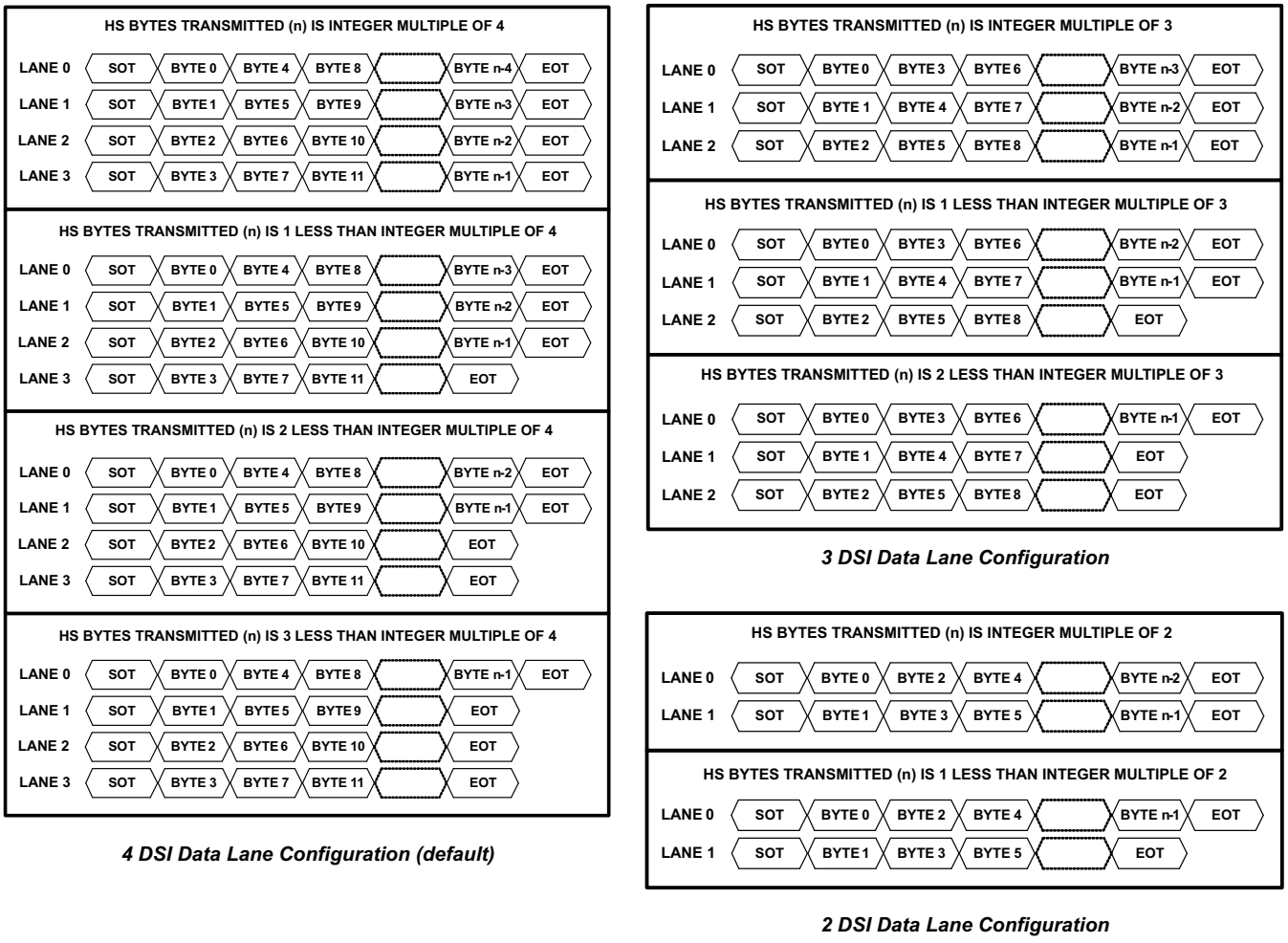


Figure 13. SN65DSI84-Q1 DSI Lane Merging Illustration

8.4.5 DSI Pixel Stream Packets

The SN65DSI84-Q1 processes 18bpp (RGB666) and 24 bpp (RGB888) DSI packets on each channel as shown in Figure 14, Figure 15, andFigure 16.

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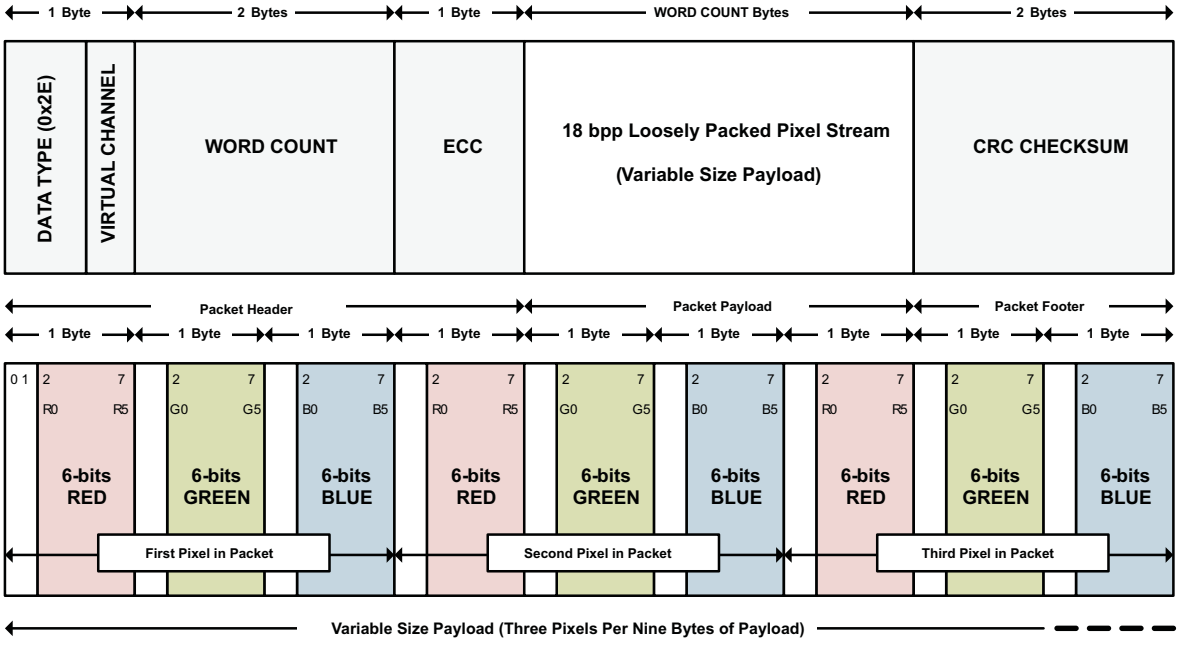


Figure 14. 18 Bpp (Loosely Packed) DSI Packet Structure

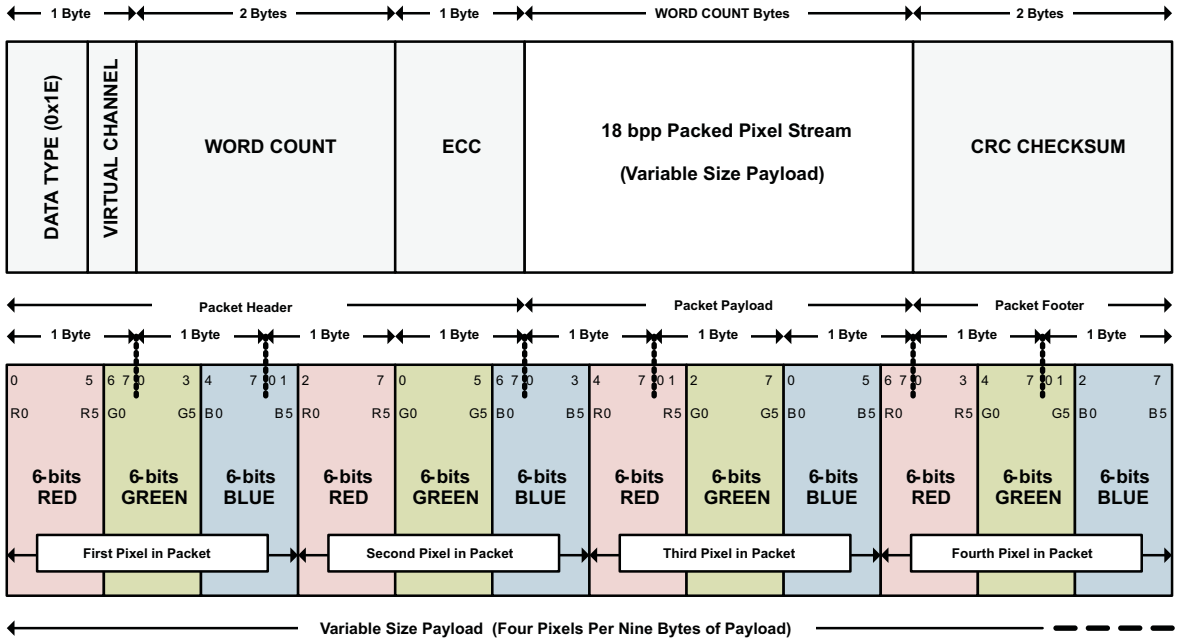


Figure 15. 18-Bpp (Tightly Packed) DSI Packet Structure

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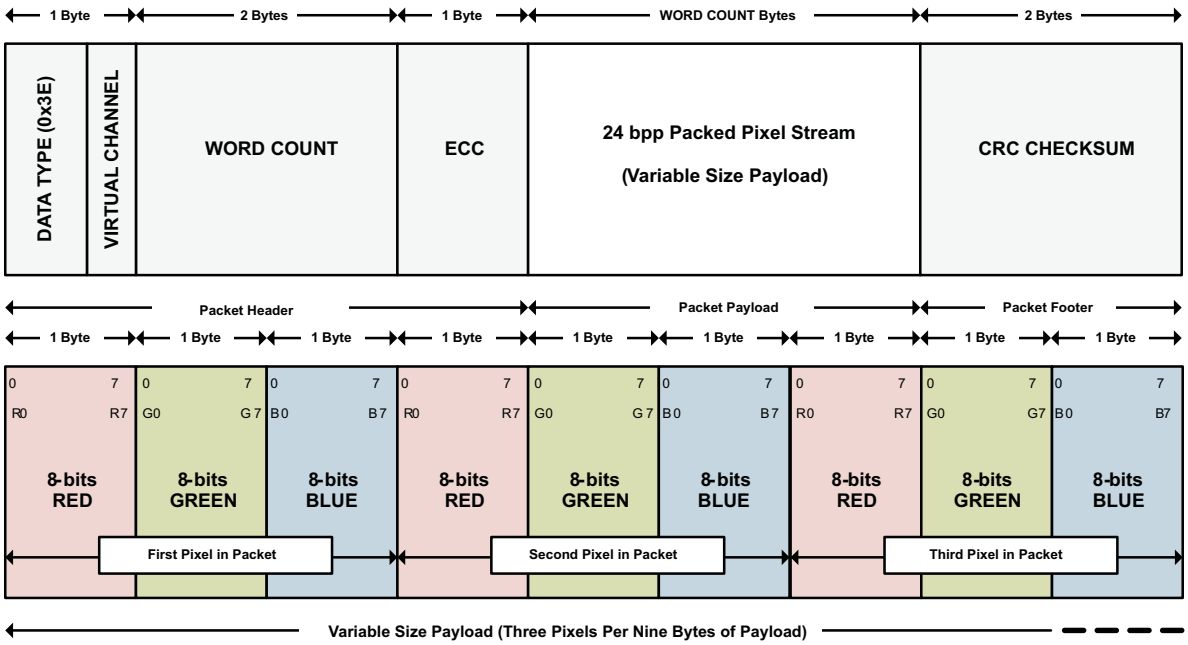


Figure 16. 24-Bpp DSI Packet Structure

8.4.6 DSI Video Transmission Specifications

The SN65DSI84-Q1 supports burst video mode and non-burst video mode with sync events or with sync pulses packet transmission as described in the DSI specification. The burst mode supports time-compressed pixel stream packets that leave added time per scan line for power savings LP mode. The SN65DSI84-Q1 requires a transition to LP mode once per frame to enable PHY synchronization with the DSI host processor; however, for a robust and low-power implementation, the transition to LP mode is recommended on every video line.

Figure 17 illustrates the DSI video transmission applied to SN65DSI84-Q1 applications. In all applications, the LVDS output rate must be less than or equal to the DSI input rate. The first line of a video frame shall start with a VSS packet, and all other lines start with VSE or HSS. The position of the synchronization packets in time is of utmost importance because this has a direct impact on the visual performance of the display panel; that is, these packets generate the HS and VS (horizontal and vertical sync) signals on the LVDS interface after the delay programmed into CHA_SYNC_DELAY_LOW/HIGH (CSR 0x28.7:0 and 0x29.3:0).

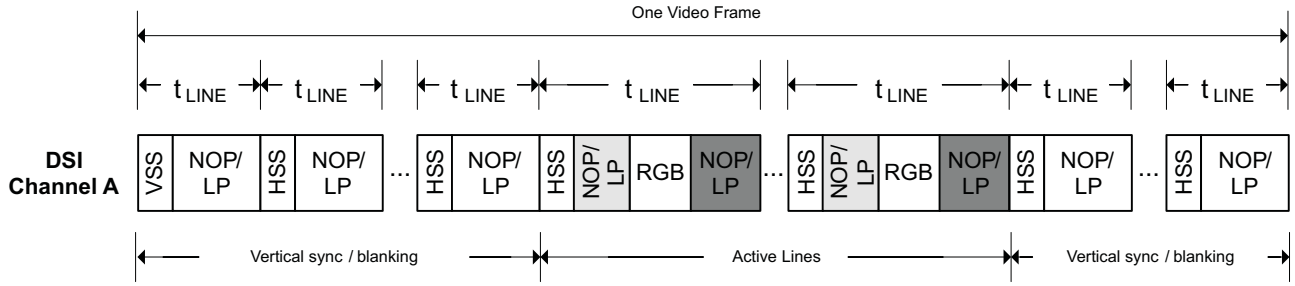
As required in the DSI specification, the SN65DSI84-Q1 requires that pixel stream packets contain an integer number of pixels (i.e. end on a pixel boundary); TI recommends transmitting an entire scan line on one pixel stream packet. When a scan line is broken in to multiple packets, inter-packet latency shall be considered such that the video pipeline (ie. pixel queue or partial line buffer) does not run empty (i.e. under-run); during scan line processing, if the pixel queue runs empty, the SN65DSI84-Q1 transmits zero data (18'b0 or 24'b0) on the LVDS interface.

NOTE

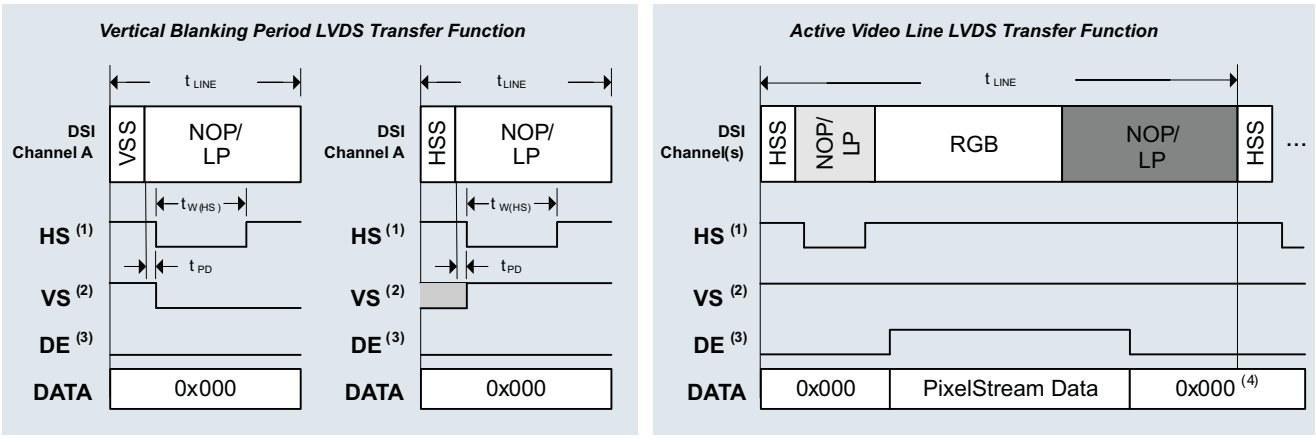
When the HS clock is used as a source for the LVDS pixel clock, the LP mode transitions apply only to the data lanes, and the DSI clock lane remains in the HS mode during the entire video transmission.

The DSI84 does not support the DSI Virtual Channel capability or reverse direction (peripheral to processor) transmissions.

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* VSS and HSS packets are required for DSI Channel B, although LVDS video sync signals are derived from DSI Channel A VSS and HSS packets



(1) The assertion of HS is delayed (t_{PD}) by a programmable number of pixel clocks from the last bit of VSS/HSS packet received on DSI. The HS pulse width ($t_{W(HS)}$) is also programmable. The illustration shows HS active low.

(2) VS is signaled for a programmable number of lines (t_{LINE}) and is asserted when HS is asserted for the first line of the frame . VS is de -asserted when HS is asserted after the number of lines programmed has been reached. The illustration shows VS active low

(3) DE is asserted when active pixel data is transmitted on LVDS, and polarity is set independent to HS/VS. The illustration shows DE active high

(4) After the last pixel in an active line is output to LVDS, the LVDS data is output zero

LEGEND

VSS	**DSI Sync Event Packet: V Sync Start**
HSS	**DSI Sync Event Packet: H Sync Start**
RGB	**A sequence of DSI Pixel Stream Packets and Null Packets**
NOP/LP	**DSI Null Packet , Blanking Packet , or a transition to LP Mode**

Figure 17. DSI Channel Transmission and Transfer Function

8.4.7 Operating Modes

The SN65DSI84-Q1 can be configured for several different operating modes via LVDS_LINK_CFG (CSR 0x18.4), LEFT_RIGHT_PIXELS (CSR 0x10.7), and DSI_CHANNEL_MODE (CSR 0x10.6:5). These modes are summarized in Table 3. In each of the modes, video data can be 18 bpp or 24 bpp.

Table 3. SN65DSI84-Q1 Operating Modes

MODE	CSR 0x18.4 LVDS_LINK_CFG	DESCRIPTION
Single DSI Input to Single-Link LVDS	1	Single DSI Input on Channel A to Single-Link LVDS output on Channel A.
Single DSI Input to Dual-Link LVDS	0	Single DSI Input on Channel A to Dual-Link LVDS output with Odd pixels on Channel A and Even pixels on Channel B.

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8.5 Programming

8.5.1 Local I²C Interface Overview

The SN65DSI84-Q1 local I²C interface is enabled when EN is input high, access to the CSR registers is supported during ultra-low power state (ULPS). The SCL and SDA terminals are used for I²C clock and I²C data respectively. The SN65DSI84-Q1 I²C interface conforms to the two-wire serial interface defined by the I²C Bus Specification, Version 2.1 (January 2000), and supports fast mode transfers up to 400 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for SN65DSI84-Q1 is factory preset to 010110X with the least significant bit being determined by the ADDR control input. Table 4 clarifies the SN65DSI84-Q1 target address.

Table 4. SN65DSI84-Q1 I²C Target Address Description (1)(2)

SN65DSI84-Q1 I2C TARGET ADDRESS							
BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (W/R)
0	1	0	1	1	0	ADDR	0/1

(1) When ADDR=1, Address Cycle is 0x5A (Write) and 0x5B (Read)
(2) When ADDR=0, Address Cycle is 0x58 (Write) and 0x59 (Read)

The following procedure is followed to write to the SN65DSI84-Q1 I²C registers.

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSI84-Q1 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The SN65DSI84-Q1 acknowledges the address cycle.
3. The master presents the sub-address (I2C register within SN65DSI84-Q1) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSI84-Q1 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I²C register.
6. The SN65DSI84-Q1 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SN65DSI84-Q1.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure is followed to read the SN65DSI84-Q1 I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SN65DSI84-Q1 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The SN65DSI84-Q1 acknowledges the address cycle.
3. The SN65DSI84-Q1 transmit the contents of the memory registers MSB-first starting at register 00h. If a write to the SN65DSI84-Q1 I2C register occurred prior to the read, then the SN65DSI84-Q1 will start at the sub-address specified in the write.
4. The SN65DSI84-Q1 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I2C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the SN65DSI84-Q1 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure is followed for setting a starting sub-address for I²C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSI84-Q1 7-bit address and a zero-value “W/R” bit to indicate a write cycle
2. The SN65DSI84-Q1 acknowledges the address cycle.
3. The master presents the sub-address (I²C register within SN65DSI84-Q1) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSI84-Q1 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

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8.6 Register Maps

8.6.1 Control and Status Registers Overview

Many of the SN65DSI84-Q1 functions are controlled by the Control and Status Registers (CSR). All CSR registers are accessible through the local I^2C interface.

See the following tables for the SN65DSI84-Q1 CSR descriptions. Reserved or undefined bit fields should not be modified. Otherwise, the device may operate incorrectly.

8.6.1.1 CSR Bit Field Definitions – ID Registers

8.6.1.1.1 Registers 0x00 – 0x08

Figure 18. Registers 0x00 – 0x08

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Registers 0x00 – 0x08 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R		Reserved Addresses 0x08 - 0x00 = {0x01, 0x20, 0x20, 0x20, 0x44, 0x53, 0x49, 0x38, 0x35}

8.6.1.2 CSR Bit Field Definitions – Reset and Clock Registers

8.6.1.2.1 Register 0x09

Figure 19. Register 0x09

7	6	5	4	3	2	1	0
Reserved							SOFT_RESET
R							W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Register 0x09 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R		Reserved
0	SOFT_RESET	W	0	This bit automatically clears when set to ‘1’ and returns zeros when read. This bit must be set after the CSR’s are updated. This bit must also be set after making any changes to the DIS clock rate or after changing between DSI burst and non-burst modes. 0 – No action (default) 1 – Reset device to default condition excluding the CSR bits.

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8.6.1.2.2 Register 0x0A

Figure 20. Register 0x0A

7	6	5	4	3	2	1	0
PLL_EN_STAT	Reserved			LVDS_CLK_RANGE			HS_CLK_SRC
R	R			R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Register 0x0A Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL_EN_STAT	R	0	0 – PLL not enabled (default) 1 – PLL enabled Note: After PLL_EN_STAT = 1, wait at least 3ms for PLL to lock.
6-4	Reserved	R		
3-1	LVDS_CLK_RANGE	R/W	101	This field selects the frequency range of the LVDS output clock. 000 – 25 MHz ≤ LVDS_CLK < 37.5 MHz 001 – 37.5 MHz ≤ LVDS_CLK < 62.5 MHz 010 – 62.5 MHz ≤ LVDS_CLK < 87.5 MHz 011 – 87.5 MHz ≤ LVDS_CLK < 112.5 MHz 100 – 112.5 MHz ≤ LVDS_CLK < 137.5 MHz 101 – 137.5 MHz ≤ LVDS_CLK ≤ 154 MHz (default) 110 – Reserved 111 – Reserved
0	HS_CLK_SRC	R/W	0	0 – LVDS pixel clock derived from input REFCLK (default) 1 – LVDS pixel clock derived from MIPI D-PHY channel A HS continuous clock

8.6.1.2.3 Register 0x0B

Figure 21. Register 0x0B

7	6	5	4	3	2	1	0
DSI_CLK_DIVIDER					Reserved	REFCLK_MULTIPLIER	
R/W					R	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Register 0x0B Field Descriptions

Bit	Field	Type	Reset	Description
7-3	DSI_CLK_DIVIDER	R/W	00000	When CSR 0x0A.0 = ‘1’, this field controls the divider used to generate the LVDS output clock from the MIPI D-PHY Channel A HS continuous clock. When CSR 0x0A.0 = ‘0’, this field must be programmed to 00000. 00000 – LVDS clock = source clock (default) 00001 – Divide by 2 00010 – Divide by 3 00011 – Divide by 4 • • • 10111 – Divide by 24 11000 – Divide by 25 11001 through 11111 – Reserved
2	Reserved	R		
1-0	REFCLK_MULTIPLIER	R/W	00	When CSR 0x0A.0 = ‘0’, this field controls the multiplier used to generate the LVDS output clock from the input REFCLK. When CSR 0x0A.0 = ‘1’, this field must be programmed to 00. 00 – LVDS clock = source clock (default) 01 – Multiply by 2 10 – Multiply by 3 11 – Multiply by 4

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8.6.1.2.4 Register 0x0D

Figure 22. Register 0x0D

7	6	5	4	3	2	1	0
Reserved							PLL_EN
R							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Register 0x0D Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R		Reserved
0	PLL_EN	R/W	0	When this bit is set, the PLL is enabled with the settings programmed into CSR 0x0A and CSR 0x0B. The PLL should be disabled before changing any of the settings in CSR 0x0A and CSR 0x0B. The input clock source must be active and stable before the PLL is enabled. 0 – PLL disabled (default) 1 – PLL enabled

8.6.1.3 CSR Bit Field Definitions – DSI Registers

8.6.1.3.1 Register 0x10

Figure 23. Register 0x10

7	6	5	4	3	2	1	0
Reserved			CHA_DSI_LANES		Reserved		SOT_ERR_TOL_DIS
R			R/W		R		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Register 0x10 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R		Reserved
4-3	CHA_DSI_LANES	R/W	11	This field controls the number of lanes that are enabled for DSI Channel A. 00 – Four lanes are enabled 01 – Three lanes are enabled 10 – Two lanes are enabled 11 – One lane is enabled (default) Note: Unused DSI input pins on the SN65DSI84-Q1 should be left unconnected.
2-1	Reserved	R		Reserved
0	SOT_ERR_TOL_DIS	R/W	0	0 – Single bit errors are tolerated for the start of transaction SoT leader sequence (default) 1 – No SoT bit errors are tolerated

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8.6.1.3.2 Register 0x11

Figure 24. Register 0x11

7	6	5	4	3	2	1	0
CHA_DSI_DATA_EQ		Reserved		CHA_DSI_CLK_EQ		Reserved	
R/W		R		R/W		R	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Register 0x11 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CHA_DSI_DATA_EQ	R/W	00	This field controls the equalization for the DSI Channel A Data Lanes 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization
5-4	Reserved	R		Reserved
3-2	CHA_DSI_CLK_EQ	R/W	00	This field controls the equalization for the DSI Channel A Clock 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization
1-0	Reserved	R		Reserved

8.6.1.3.3 Register 0x12

Figure 25. Register 0x12

7	6	5	4	3	2	1	0
CHA_DSI_CLK_RANGE							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Register 0x12 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHA_DSI_CLK_RANGE	R/W	0	This field specifies the DSI Clock frequency range in 5 MHz increments for the DSI Channel A Clock 0x00 through 0x07 – Reserved 0x08 – 40 ≤ frequency < 45 MHz 0x09 – 45 ≤ frequency < 50 MHz ... 0x63 – 495 ≤ frequency < 500 MHz 0x64 – 500 MHz 0x65 through 0xFF – Reserved

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8.6.1.4 CSR Bit Field Definitions – LVDS Registers

8.6.1.4.1 Register 0x18

Figure 26. Register 0x18

7	6	5	4	3	2	1	0
DE_NEG_POLARITY	HS_NEG_POLARITY	VS_NEG_POLARITY	LVDS_LINK_CFG	CHA_24BPP_MODE	CHB_24BPP_MODE	CHA_24BPP_FORMAT1	CHB_24BPP_FORMAT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. Register 0x18 Field Descriptions

Bit	Field	Type	Reset	Description
7	DE_NEG_POLARITY	R/W	0	0 – DE is positive polarity driven ‘1’ during active pixel transmission on LVDS (default) 1 – DE is negative polarity driven ‘0’ during active pixel transmission on LVDS
6	HS_NEG_POLARITY	R/W	1	0 – HS is positive polarity driven ‘1’ during corresponding sync conditions 1 – HS is negative polarity driven ‘0’ during corresponding sync (default)
5	VS_NEG_POLARITY	R/W	1	0 – VS is positive polarity driven ‘1’ during corresponding sync conditions 1 – VS is negative polarity driven ‘0’ during corresponding sync (default)
4	LVDS_LINK_CFG	R/W	1	0 – LVDS Channel A and Channel B outputs enabled When CSR 0x10.6:5 = ’00’ or ‘01’, the LVDS is in Dual-Link configuration When CSR 0x10.6:5 = ‘10’, the LVDS is in two Single-Link configuration 1 – LVDS Single-Link configuration; Channel A output enabled and Channel B output disabled (default)
3	CHA_24BPP_MODE	R/W	0	0 – Force 18bpp; LVDS channel A lane 4 (A_Y3P/N) is disabled (default) 1 – Force 24bpp; LVDS channel A lane 4 (B_Y3P/N) is enabled
2	CHB_24BPP_MODE	R/W	0	CHB_24BPP_MODE 0 – Force 18bpp; LVDS channel B lane 4 (A_Y3P/N) is disabled (default) 1 – Force 24bpp; LVDS channel B lane 4 (B_Y3P/N) is enabled
1	CHA_24BPP_FORMAT1	R/W	0	This field selects the 24bpp data format 0 – LVDS channel A lane A_Y3P/N transmits the 2 most significant bits (MSB) per color; Format 2 (default) 1 – LVDS channel B lane A_Y3P/N transmits the 2 least significant bits (LSB) per color; Format 1 Note1: This field must be ‘0’ when 18bpp data is received from DSI. Note2: If this field is set to ‘1’ and CHA_24BPP_MODE is ‘0’, the SN65DSI84-Q1 will convert 24bpp data to 18bpp data for transmission to an 18bpp panel. In this configuration, the SN65DSI84-Q1 will not transmit the 2 LSB per color on LVDS channel A, because LVDS channel A lane A_Y3P/N is disabled.
0	CHB_24BPP_FORMAT	R/W	0	This field selects the 24bpp data format 0 – LVDS channel B lane B_Y3P/N transmits the 2 most significant bits (MSB) per color; Format 2 (default) 1 – LVDS channel B lane B_Y3P/N transmits the 2 least significant bits (LSB) per color; Format 1 Note1: This field must be ‘0’ when 18bpp data is received from DSI. Note2: If this field is set to ‘1’ and CHB_24BPP_MODE is ‘0’, the SN65DSI84-Q1 will convert 24bpp data to 18bpp data for transmission to an 18bpp panel. In this configuration, the SN65DSI84-Q1 will not transmit the 2 LSB per color on LVDS channel B, because LVDS channel B lane B_Y3P/Nis disabled.

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8.6.1.4.2 Register 0x19

Figure 27. Register 0x19

7	6	5	4	3	2	1	0
Reserved	CHA_LVDS_VOCM	Reserved	CHB_LVDS_VOCM	CHA_LVDS_VOD_SWING		CHB_LVDS_VOD_SWING	
R/W			R/W	R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Register 0x19 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R		Reserved
6	CHA_LVDS_VOCM	R/W	0	This field controls the common mode output voltage for LVDS Channel A 0 – 1.2V (default) 1 – 0.9V (CSR 0x1B.5:4 CHA_LVDS_CM_ADJUST must be set to '01b')
5	Reserved	R		Reserved
4	CHB_LVDS_VOCM	R/W	0	This field controls the common mode output voltage for LVDS Channel B 0 – 1.2V (default) 1 – 0.9V (CSR 0x1B.1:0 CHB_LVDS_CM_ADJUST must be set to '01b')
3-2	CHA_LVDS_VOD_SWING	R/W	01	This field controls the differential output voltage for LVDS Channel A. See the *Electrical Characteristics table* for $\|V_{OD}\|$ for each setting: 00, 01 (default), 10, 11.
1-0	CHB_LVDS_VOD_SWING	R/W	01	This field controls the differential output voltage for LVDS Channel B. See the *Electrical Characteristics table* for $\|V_{OD}\|$ for each setting: 00, 01 (default), 10, 11.

8.6.1.4.3 Register 0x1A

Figure 28. Register 0x1A

7	6	5	4	3	2	1	0
Reserved	EVEN_ODD_SWAP	CHA_REVERSE_LVDS	CHB_REVERSE_LVDS	Reserved		CHA_LVDS_TERM	CHB_LVDS_TERM
R	R/W	R/W	R/W	R		R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. Register 0x1A Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R		Reserved
6	EVEN_ODD_SWAP	R/W	0	0 – Odd pixels routed to LVDS Channel A and Even pixels routed to LVDS Channel B (default) 1 – Odd pixels routed to LVDS Channel B and Even pixels routed to LVDS Channel A Note: When the SN65DSI84-Q1 is in two stream mode (CSR 0x10.6:5 = '10'), setting this bit to '1' will cause the video stream from DSI Channel A to be routed to LVDS Channel B and the video stream from DSI Channel B to be routed to LVDS Channel A.

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Table 15. Register 0x1A Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CHA_REVERSE_LVDS	R/W	0	This bit controls the order of the LVDS pins for Channel A. 0 – Normal LVDS Channel A pin order. LVDS Channel A pin order is the same as listed in the Terminal Assignments Section. (default) 1 – Reversed LVDS Channel A pin order. LVDS Channel A pin order is remapped as follows: • A_Y0P → A_Y3P • A_Y0N → A_Y3N • A_Y1P → A_CLKP • A_Y1N → A_CLKN • A_Y2P → A_Y2P • A_Y2N → A_Y2N • A_CLKP → A_Y1P • A_CLKN → A_Y1N • A_Y3P → A_Y0P • A_Y3N → A_Y0N
4	CHB_REVERSE_LVDS	R/W	0	This bit controls the order of the LVDS pins for Channel B. 0 – Normal LVDS Channel B pin order. LVDS Channel B pin order is the same as listed in the Terminal Assignments Section. (default) 1 – Reversed LVDS Channel B pin order. LVDS Channel B pin order is remapped as follows: • B_Y0P → B_Y3P • B_Y0N → B_Y3N • B_Y1P → B_CLKP • B_Y1N → B_CLKN • B_Y2P → B_Y2P • B_Y2N → B_Y2N • B_CLKP → B_Y1P • B_CLKN → B_Y1N • B_Y3P → B_Y0P • B_Y3N → B_Y0N
3-2	Reserved	R		Reserved
1	CHA_LVDS_TERM	R/W	1	This bit controls the near end differential termination for LVDS Channel A. This bit also affects the output voltage for LVDS Channel A. 0 – 100Ω differential termination 1 – 200Ω differential termination (default)
0	CHB_LVDS_TERM	R/W	1	This bit controls the near end differential termination for LVDS Channel B. This bit also affects the output voltage for LVDS Channel B. 0 – 100Ω differential termination 1 – 200Ω differential termination (default)

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8.6.1.4.4 Register 0x1B

Figure 29. Register 0x1B

7	6	5	4	3	2	1	0
Reserved		CHA_LVDS_CM_ADJUST		Reserved		CHB_LVDS_CM_ADJUST	
R		R/W		R		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Register 0x1B Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R		Reserved
5-4	CHA_LVDS_CM_ADJUST	R/W	00	This field can be used to adjust the common mode output voltage for LVDS Channel A. 00 – No change to common mode voltage (default) 01 – Adjust common mode voltage down 3% 10 – Adjust common mode voltage up 3% 11 – Adjust common mode voltage up 6%
3-2	Reserved	R		Reserved
1-0	CHB_LVDS_CM_ADJUST	R/W	00	This field can be used to adjust the common mode output voltage for LVDS Channel B. 00 – No change to common mode voltage (default) 01 – Adjust common mode voltage down 3% 10 – Adjust common mode voltage up 3% 11 – Adjust common mode voltage up 6%

Note for all video registers:

1. TEST PATTERN GENERATION PURPOSE ONLY registers are for test pattern generation use only. Others are for normal operation unless the test pattern generation feature is enabled.

8.6.1.5 CSR Bit Field Definitions – Video Registers

8.6.1.5.1 Register 0x20

Figure 30. Register 0x20

7	6	5	4	3	2	1	0
CHA_ACTIVE_LINE_LENGTH_LOW							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Register 0x20 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHA_ACTIVE_LINE_LENGTH_LOW	R/W	0	This field controls the length in pixels of the active horizontal line line that are received on DSI Channel A and output to LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length.

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8.6.1.5.2 Register 0x21

Figure 31. Register 0x21

7	6	5	4	3	2	1	0
Reserved				CHA_ACTIVE_LINE_LENGTH_HIGH			
R				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Register 0x21 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R		Reserved
3-0	CHA_ACTIVE_LINE_LENGTH_HIGH	R/W	0	This field controls the length in pixels of the active horizontal line that are received on DSI Channel A and output to LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length.

8.6.1.5.3 Register 0x24

Figure 32. Register 0x24

7	6	5	4	3	2	1	0
CHA_VERTICAL_DISPLAY_SIZE_LOW							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Register 0x24 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHA_VERTICAL_DISPLAY_SIZE_LOW	R/W	0	TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size.

8.6.1.5.4 Register 0x25

Figure 33. Register 0x25

7	6	5	4	3	2	1	0
Reserved				CHA_VERTICAL_DISPLAY_SIZE_HIGH			
R				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Register 0x25 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R		Reserved
3-0	CHA_VERTICAL_DISPLAY_SIZE_HIGH	R/W	0	TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 4 bits of the 12-bit value for the vertical display size

8.6.1.5.5 Register 0x28

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Figure 34. Register 0x28

7	6	5	4	3	2	1	0
CHA_SYNC_DELAY_LOW							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. Register 0x28 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHA_SYNC_DELAY_LOW	R/W	0	This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI84-Q1. The additional delay is approximately 10 pixel clocks. The Sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the lower 8 bits of the 12-bit value for the Sync delay.

8.6.1.5.6 Register 0x29

Figure 35. Register 0x29

7	6	5	4	3	2	1	0
Reserved				CHA_SYNC_DELAY_HIGH			
R				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. Register 0x29 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R		Reserved
3-0	CHA_SYNC_DELAY_HIGH	R/W	0	This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI84-Q1. The additional delay is approximately 10 pixel clocks. The Sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the upper 4 bits of the 12-bit value for the Sync delay.

8.6.1.5.7 Register 0x2C

Figure 36. Register 0x2C

7	6	5	4	3	2	1	0
CHA_HSYNC_PULSE_WIDTH_LOW							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. Register 0x2C Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHA_HSYNC_PULSE_WIDTH_LOW	R/W	0	This field controls the width in pixel clocks of the HSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the lower 8 bits of the 10-bit value for the HSync Pulse Width.

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8.6.1.5.8 Register 0x2D

Figure 37. Register 0x2D

7	6	5	4	3	2	1	0
Reserved						CHA_HSYNC_PULSE_WIDTH_HIGH	
R						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Register 0x2D Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R		Reserved
1-0	CHA_HSYNC_PULSE_WIDTH_HIGH	R/W	0	This field controls the width in pixel clocks of the HSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 2 bits of the 10-bit value for the HSync Pulse Width.

8.6.1.5.9 Register 0x30

Figure 38. Register 0x30

7	6	5	4	3	2	1	0
CHA_VSYNC_PULSE_WIDTH_LOW							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Register 0x30 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHA_VSYNC_PULSE_WIDTH_LOW	R/W	0	This field controls the length in lines of the VSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the lower 8 bits of the 10-bit value for the VSync Pulse Width.

8.6.1.5.10 Register 0x31

Figure 39. Register 0x31

7	6	5	4	3	2	1	0
Reserved						CHA_VSYNC_PULSE_WIDTH_HIGH	
R						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Register 0x31 Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R		Reserved
1-0	CHA_VSYNC_PULSE_WIDTH_HIGH	R/W	0	This field controls the length in lines of the VSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 2 bits of the 10-bit value for the VSync Pulse Width.

8.6.1.5.11 Register 0x34

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Figure 40. Register 0x34

7	6	5	4	3	2	1	0
CHA_HORIZONTAL_BACK_PORCH							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. Register 0x34 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHA_HORIZONTAL_BACK_PORCH	R/W	0	This field controls the time in pixel clocks between the end of the HSync Pulse and the start of the active video data for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).

8.6.1.5.12 Register 0x36

Figure 41. Register 0x36

7	6	5	4	3	2	1	0
CHA_VERTICAL_BACK_PORCH							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Register 0x36 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHA_VERTICAL_BACK_PORCH	R/W	0	TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the VSync Pulse and the start of the active video data for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).

8.6.1.5.13 Register 0x38

Figure 42. Register 0x38

7	6	5	4	3	2	1	0
CHA_HORIZONTAL_FRONT_PORCH							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. Register 0x38 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHA_HORIZONTAL_FRONT_PORCH	R/W	0	TEST PATTERN GENERATION PURPOSE ONLY. This field controls the time in pixel clocks between the end of the active video data and the start of the HSync Pulse for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).

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8.6.1.5.14 Register 0x3A

Figure 43. Register 0x3A

7	6	5	4	3	2	1	0
CHA_VERTICAL_FRONT_PORCH							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. Register 0x3A Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHA_VERTICAL_FRONT_PORCH	R/W	0	TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the active video data and the start of the VSync Pulse for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).

8.6.1.5.15 Register 0x3C

Figure 44. Register 0x3C

7	6	5	4	3	2	1	0
Reserved			CHA_TEST_PATTERN	Reserved			
R			R/W	R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. Register 0x3C Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R		Reserved
4	CHA_TEST_PATTERN	R/W	0	TEST PATTERN GENERATION PURPOSE ONLY. When this bit is set, the SN65DSI84-Q1 will generate a video test pattern based on the values programmed into the Video Registers for LDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).
3-0	Reserved	R		Reserved

8.6.1.6 CSR Bit Field Definitions – IRQ Registers

8.6.1.6.1 Register 0xE0

Figure 45. Register 0xE0

7	6	5	4	3	2	1	0
Reserved							IRQ_EN
R							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Register 0xE0 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R		Reserved
0	IRQ_EN	R/W	0	When enabled by this field, the IRQ output is driven high to communicate IRQ events. 0 – IRQ output is high-impedance (default) 1 – IRQ output is driven high when a bit is set in registers 0xE5 that also has the corresponding IRQ_EN bit set to enable the interrupt condition

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8.6.1.6.2 Register 0xE1

Figure 46. Register 0xE1

7	6	5	4	3	2	1	0
CHA_SYNCH_ERR_EN	CHA_CRC_ERR_EN	CHA_UNC_ECC_ERR_EN	CHA_COR_ECC_ERR_EN	CHA_LLP_ERR_EN	CHA_SOT_BIT_ERR_EN	Reserved	PLL_UNLOCK_EN
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. Register 0xE1 Field Descriptions

Bit	Field	Type	Reset	Description
7	CHA_SYNCH_ERR_EN	R/W	0	0 – CHA_SYNCH_ERR is masked 1 – CHA_SYNCH_ERR is enabled to generate IRQ events
6	CHA_CRC_ERR_EN	R/W	0	0 – CHA_CRC_ERR is masked 1 – CHA_CRC_ERR is enabled to generate IRQ events
5	CHA_UNC_ECC_ERR_EN	R/W	0	0 – CHA_UNC_ECC_ERR is masked 1 – CHA_UNC_ECC_ERR is enabled to generate IRQ events
4	CHA_COR_ECC_ERR_EN	R/W	0	0 – CHA_COR_ECC_ERR is masked 1 – CHA_COR_ECC_ERR is enabled to generate IRQ events
3	CHA_LLP_ERR_EN	R/W	0	0 – CHA_LLP_ERR is masked 1 – CHA_ LLP_ERR is enabled to generate IRQ events
2	CHA_SOT_BIT_ERR_EN	R/W	0	0 – CHA_SOT_BIT_ERR is masked 1 – CHA_SOT_BIT_ERR is enabled to generate IRQ events
1	Reserved	R		Reserved
0	PLL_UNLOCK_EN	R/W	0	0 – PLL_UNLOCK is masked 1 – PLL_UNLOCK is enabled to generate IRQ events

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8.6.1.6.3 Register 0xE5

Figure 47. Register 0xE5

7	6	5	4	3	2	1	0
CHA_SYNCH_ERR	CHA_CRC_ERR	CHA_UNC_ECC_ERR	CHA_COR_ECC_ERR	CHA_LLP_ERR	CHA_SOT_BIT_ERR	Reserved	PLL_UNLOCK
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Register 0xE5 Field Descriptions

Bit	Field	Type	Reset	Description
7	CHA_SYNCH_ERR	R/W	0	When the DSI channel A packet processor detects an HS or VS synchronization error, that is, an unexpected sync packet; this bit is set; this bit is cleared by writing a ‘1’ value.
6	CHA_CRC_ERR	R/W	0	When the DSI channel A packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a ‘1’ value.
5	CHA_UNC_ECC_ERR	R/W	0	When the DSI channel A packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a ‘1’ value.
4	CHA_COR_ECC_ERR	R/W	0	When the DSI channel A packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a ‘1’ value.
3	CHA_LLP_ERR	R/W	0	When the DSI channel A packet processor detects a low level protocol error, this bit is set; this bit is cleared by writing a ‘1’ value. Low level protocol errors include SoT and EoT sync errors, Escape Mode entry command errors, LP transmission sync errors, and false control errors. Lane merge errors are reported by this status condition.
2	CHA_SOT_BIT_ERR	R/W	0	When the DSI channel A packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a ‘1’ value.
1	Reserved	R		Reserved
0	PLL_UNLOCK	R/W	1	This bit is set whenever the PLL Lock status transitions from LOCK to UNLOCK.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN65DSI84-Q1 device is primarily targeted for portable applications such as tablets and smart phones that utilize the MIPI DSI video format. The SN65DSI84-Q1 device can be used between a GPU with DSI output and a video panel with LVDS inputs

9.1.1 Video Stop and Restart Sequence

When the system requires to stop outputting video to the display, it is recommended to use the following sequence for the SN65DSI84-Q1:

1. Clear the PLL_EN bit to 0 (CSR 0x0D.0)
2. Stop video streaming on DSI inputs
3. Drive all DSI data lanes to LP11, but keep the DSI CLK lanes in HS.

When the system is ready to restart the video streaming.

1. Start video streaming on DSI inputs.
2. Set the PLL_EN bit to 1(CSR 0x0D.0).
3. Wait for a minimum of 3 ms.
4. Set the SOFT_RESET bit(0x09.0).

9.1.2 Reverse LVDS Pin Order Option

For ease of PCB routing, the SN65DSI84-Q1 supports swapping/reversing the channel or pin order via configuration register programming. The order of the LVDS pin for LVDS Channel A or Channel B can be reversed by setting the address 0x1A bit 5 CHA_REVERSE_LVDS or bit 4 CHB_REVERSE_LVDS. The LVDS Channel A and Channel B can be swapped by setting the 0x1A.6 EVEN_ODD_SWAP bit. See the corresponding register bit definition for details.

9.1.3 IRQ Usage

The SN65DSI84-Q1 provides an IRQ pin that can be used to indicate when certain errors occur on DSI. The IRQ output is enabled through the IRQ_EN bit (CSR 0xE0.0). The IRQ pin will be asserted when an error occurs on DSI, the corresponding error enable bit is set, and the IRQ_EN bit is set. An error is cleared by writing a '1' to the corresponding error status bit.

NOTE

If the SOFT_RESET bit is set while the DSI video stream is active, some of the error status bits may be set.

If the DSI video stream is stopped, some of the error status bits may be set. These error status bits should be cleared before restarting the video stream.

If the DSI video stream starts before the device is configured, some of the error status bits may be set. TI recommends starting streaming after the device is correctly configured as recommended in the initialization sequence in the *Initialization Sequence* section.

9.2 Typical Application

Figure 48 illustrates a typical application using the SN65DSI84-Q1 for a single channel DSI receiver to interface a single-channel DSI application processor to an LVDS Dual-Link 18 bit-per-pixel panel supporting 1920 x 1200 WUXGA resolutions at 60 frames per second.

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Typical Application (continued)

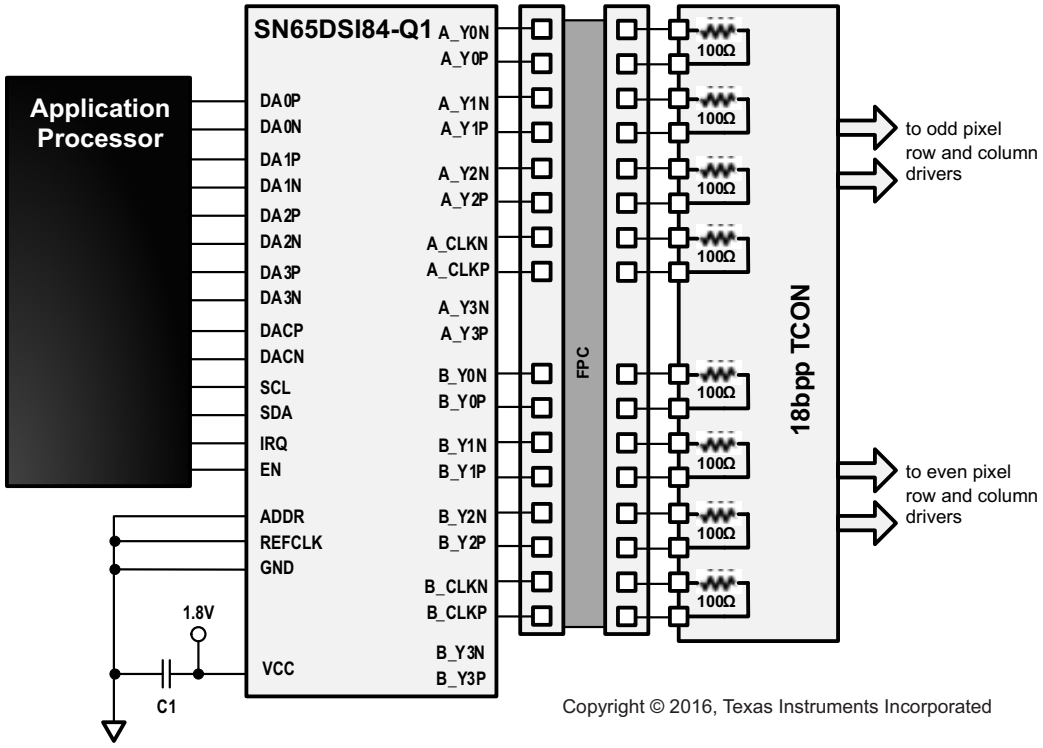


Figure 48. Typical 1920 x 1200 WUXGA 18-bpp Panel Application

9.2.1 Design Requirements

For the 1920 x 1200 WUXGA 18-bpp Panel typical application design parameters, see Table 35.

Table 35. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VCC	1.8V (±5%)
CLOCK	DSIA_CLK
REFCKL Frequency	N/A
DSIA Clock Frequency	490 MHz
PANEL INFORMATION	
LVDS Output Clock Frequency	81 MHz
Resolution	1920 x 1200
Horizontal Active (pixels)	960
Horizontal Blanking (pixels)	144
Vertical Active (lines)	1200
Vertical Blanking (lines)	20
Horizontal Sync Offset (pixels)	50
Horizontal Sync Pulse Width (pixels)	50
Vertical Sync Offset (lines)	1
Vertical Sync Pulse Width (lines)	5
Horizontal Sync Pulse Polarity	Negative
Vertical Sync Pulse Polarity	Negative
Color Bit Depth (6bpc or 8bpc)	6-bit
Number of LVDS Lanes	2 X [3 Data Lanes + 1 Clock Lane]

Typical Application (continued)

Table 35. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
DSI INFORMATION	
Number of DSI Lanes	1 X [4 Data Lanes + 1 Clock Lane]
DSI Input Clock Frequency	490MHz
Dual DSI Configuration(Odd/Even or Left/Right)	N/A

9.2.2 Detailed Design Procedure

The video resolution parameters required by the panel must be programmed into the SN65DSI84-Q1. For this example, the parameters programmed would be the following:

Horizontal active = 1920 or 0x780
CHA_ACTIVE_LINE_LENGTH_LOW = 0X80
CHA_ACTIVE_LINE_LENGTH_HIGH = 0x07

Horizontal pulse Width = 50 or 0x32
CHA_HSYNC_PULSE_WIDTH_LOW = 0x32
CHA_HSYNC_PULSE_WIDTH_HIGH= 0x00

Horizontal back porch = Horizontal blanking – (Horizontal sync offset + Horizontal sync pulse width)
Horizontal back porch = 144– (50 + 50)
Horizontal back porch = 44 or 0x2C
CHA_HORIZONTAL_BACK_PORCH = 0x2C

Vertical pulse width = 5
CHA_VSYNC_PULSE_WIDTH_LOW = 0x05
CHA_VSYNC_PULSE_WIDTH_HIGH= 0x00

The pattern generation feature can be enabled by setting the CHA_TEST_PATTERN bit at address 0x3C and configuring the following TEST PATTERN GENERATION PURPOSE ONLY registers.

Vertical active = 1200 or 0x4B0
CHA_VERTICAL_DISPLAY_SIZE_LOW = 0xB0
CHA_VERTICAL_DISPLAY_SIZE_HIGH = 0x04

Vertical back porch = Vertical blanking – (Vertical sync offset +Vertical sync pulse width)
Vertical back porch = 20 – (1 + 5)
Vertical back porch = 14 or 0x0E
CHA_VERTICAL_BACK_PORCH = 0x0E

Horizontal front porch = Horizontal sync offset
Horizontal front porch = 50 or 0x32
CHA_HORIZONTAL_FRONT_PORCH = 0x32

Vertical front porch = Vertical sync offset
Vertical front porch =1
CHA_VERTICAL_FRONT_PORCH = 0x01

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In this example, the clock source for the SN65DSI84-Q1 is the DSI clock. When the MIPI D-PHY clock is used as the LVDS clock source, it is divided by the factor in DSI_CLK_DIVIDER (CSR 0x0B.7:3) to generate the LVDS output clock. Additionally, LVDS_CLK_RANGE (CSR 0x0A.3:1) and CH_DSI_CLK_RANGE(CSR 0x12) must be set to the frequency range of the LVDS output clock and DSI Channel A input clock respectively for the internal PLL to operate correctly. After these settings are programmed, PLL_EN (CSR 0x0D.0) should be set to enable the internal PLL.

LVDS_CLK_RANGE = 010b-62.5 MHz ≤ LVDS_CLK < 87.5 MHz
HS_CLK_SRC = 1 – LVDS pixel clock derived from MIPI D-PHY channel A HS continuous clock
DSI_CLK_DIVIDER = 0010b – Divide by 6
CHA_DSI_LANES = 00 – Four lanes are enabled
CHA_DSI_CLK_RANGE = 0x62 – 490 MHz ≤ frequency < 495 MHz

9.2.2.1 Example Script

This example configures the SN65DSI84-Q1 for the following configuration:

```
<aardvark>
        <configure i2c="1" spi="1" gpio="0" tpower="1" pullups="1"/>
        <i2c_bitrate khz="100"/>

=====SOFTRESET=======
        <i2c_write addr="0x2D" count="1" radix="16"glt;09 01</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 0D=======
======PLL_EN(bit 0) - Enable LAST after addr 0A and 0B configured======
        <i2c_write addr="0x2D" count="1" radix="16"glt;0D 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 0A=======
======HS_CLK_SRC bit0===
======LVDS_CLK_Range bit 3:1======
        <i2c_write addr="0x2D" count="1" radix="16"glt;0A 05</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 0B=======
======DSI_CLK_DIVIDER bit7:3=====
======RefCLK multiplier(bit1:0)====== ======00 - LVDSclk=source clk, 01 - x2, 10 -x3, 11 - x4======
        <i2c_write addr="0x2D" count="1" radix="16"glt;0B 28</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 10=======
======DSI Ch Confg Left_Right Pixels(bit7 - 0 for A ODD, B EVEN, 1 for the other config)======
======DSI Ch Mode(bit6:5) 00 - Dual, 01 - single, 10 - two single =======
======CHA_DSI_Lanes(bit4:3), CHB_DSI_Lanes(bit2:1), 00 - 4, 01 - 3, 10 - 2, 11 - 1
======SOT_ERR_TOL_DIS(bit0)=======
        <i2c_write addr="0x2D" count="1" radix="16"glt;10 26</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 12=======
        <i2c_write addr="0x2D" count="1" radix="16"glt;12 62</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 18=======
======bit7: DE_Pol, bit6:HS_Pol, bit5:VS_Pol, bit4: LVDS Link Cfg, bit3:CHA 24bpp, bit2: CHB 24bpp,
bit1: CHA 24bpp fmt1, bit0: CHB 24bpp fmt1======
        <i2c_write addr="0x2D" count="1" radix="16"glt;18 63</i2c_writeglt;
        <sleep ms="10"/>

 ======ADDR 19=======
        <i2c_write addr="0x2D" count="1" radix="16"glt;19 00</i2c_writeglt;
        <sleep ms="10"/>

 ======ADDR 1A=======
        <i2c_write addr="0x2D" count="1" radix="16"glt;1A 03</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 20=======
```

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```
======CHA_LINE_LENGTH_LOW========
        <i2c_write addr="0x2D" count="1" radix="16"glt;20 80</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 21=======
======CHA_LINE_LENGTH_HIGH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;21 07</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 22=======
======CHB_LINE_LENGTH_LOW========
        <i2c_write addr="0x2D" count="1" radix="16"glt;22 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 23=======
======CHB_LINE_LENGTH_HIGH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;23 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 24=======
======CHA_VERTICAL_DISPLAY_SIZE_LOW========
        <i2c_write addr="0x2D" count="1" radix="16"glt;24 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 25=======
======CHA_VERTICAL_DISPLAY_SIZE_HIGH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;25 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 26=======
======CHB_VERTICAL_DISPLAY_SIZE_LOW========
        <i2c_write addr="0x2D" count="1" radix="16"glt;26 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 27=======
======CHB_VERTICAL_DISPLAY_SIZE_HIGH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;27 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 28=======
======CHA_SYNC_DELAY_LOW========
        <i2c_write addr="0x2D" count="1" radix="16"glt;28 20</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 29=======
======CHA_SYNC_DELAY_HIGH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;29 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 2A=======
======CHB_SYNC_DELAY_LOW========
        <i2c_write addr="0x2D" count="1" radix="16"glt;2A 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 2B=======
======CHB_SYNC_DELAY_HIGH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;2B 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 2C=======
======CHA_HSYNC_PULSE_WIDTH_LOW========
        <i2c_write addr="0x2D" count="1" radix="16"glt;2C 32</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 2D=======
======CHA_HSYNC_PULSE_WIDTH_HIGH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;2D 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 2E=======
======CHB_HSYNC_PULSE_WIDTH_LOW========
        <i2c_write addr="0x2D" count="1" radix="16"glt;2E 00</i2c_writeglt;
        <sleep ms="10"/>
```


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```
======ADDR 2F=======
======CHB_HSYNC_PULSE_WIDTH_HIGH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;2F 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 30=======
======CHA_VSYNC_PULSE_WIDTH_LOW========
    <i2c_write addr="0x2D" count="1" radix="16"glt;30 05</i2c_writeglt;
    <sleep ms="10"/>

======ADDR 31=======
======CHA_VSYNC_PULSE_WIDTH_HIGH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;31 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 32=======
======CHB_VSYNC_PULSE_WIDTH_LOW========
        <i2c_write addr="0x2D" count="1" radix="16"glt;32 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 33=======
======CHB_VSYNC_PULSE_WIDTH_HIGH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;33 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 34=======
======CHA_HOR_BACK_PORCH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;34 2C</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 35=======
======CHB_HOR_BACK_PORCH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;35 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 36=======
======CHA_VER_BACK_PORCH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;36 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 37=======
======CHB_VER_BACK_PORCH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;37 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 38=======
======CHA_HOR_FRONT_PORCH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;38 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 39=======
======CHB_HOR_FRONT_PORCH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;39 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 3A=======
======CHA_VER_FRONT_PORCH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;3A 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 3B=======
======CHB_VER_FRONT_PORCH========
        <i2c_write addr="0x2D" count="1" radix="16"glt;3B 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 3C=======
======CHA/CHB TEST PATTERN(bit4 CHA, bit0 CHB)========
        <i2c_write addr="0x2D" count="1" radix="16"glt;3C 00</i2c_writeglt;
        <sleep ms="10"/>

======ADDR 0D=======
======PLL_EN(bit 0) - Enable LAST after addr 0A and 0B configured======
```

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```
        <i2c_write addr="0x2D" count="1" radix="16"glt;0D 01</i2c_writeglt;
        <sleep ms="10"/>

=====SOFTRESET=======
        <i2c_write addr="0x2D" count="1" radix="16"glt;09 00</i2c_writeglt;
        <sleep ms="10"/>

======write======
        <i2c_write addr="0x2D" count="196" radix="16"glt;00</i2c_writeglt;
        <sleep ms="10"/>

======Read======
        <i2c_read addr="0x2D" count="256" radix="16"glt;00</i2c_readglt;
        <sleep ms="10"/>
</aardvark>
```

9.2.3 Application Curve

SN65DSI84-Q1: SINGLE Channel DSI to DUAL Channel LVDS, 1440 x 900

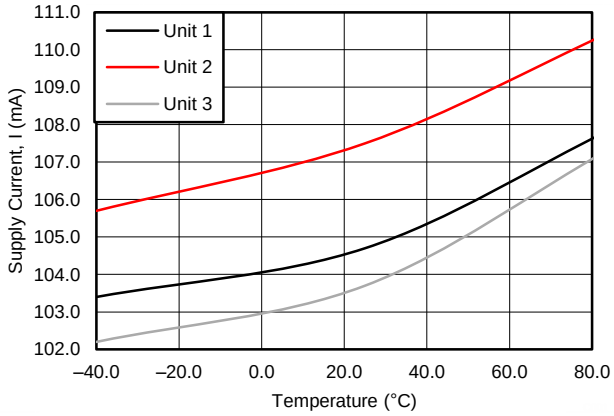


Figure 49. Supply Current vs Temperature

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10 Power Supply Recommendations

10.1 V_{CC} Power Supply

Each VCC power supply pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI84-Q1 device. It is recommended to have one bulk capacitor (1 µF to 10 µF) on it. It is also recommended to have the pins connected to a solid power plane.

10.2 VCORE Power Supply

This pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI84-Q1 device. It is recommended to have one bulk capacitor (1 µF to 10 µF) on it. It is also recommended to have the pins connected to a solid power plane.

11 Layout

11.1 Layout Guidelines

11.1.1 Package Specific

For the ZQE package, to minimize the power supply noise floor, provide good decoupling near the SN65DSI84-Q1 device power pins. The use of four ceramic capacitors (2 × 0.1 µF and 2 × 0.01 µF) provides good performance. At the least, TI recommends to install one 0.1-µF and one 0.01-µF capacitor near the SN65DSI84-Q1 device. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized. Placing the capacitor underneath the SN65DSI84-Q1 device on the bottom of the PCB is often a good choice.

11.1.2 Differential Pairs

- Differential pairs must be routed with controlled 100-Ω differential impedance (± 20%) or 50-Ω single-ended impedance (±15%).
- Keep away from other high speed signals
- Keep lengths to within 5 mils of each other.
- Length matching must be near the location of mismatch.
- Each pair must be separated at least by 3 times the signal trace width.
- The use of bends in differential traces must be kept to a minimum. When bends are used, the number of left and right bends must be as equal as possible and the angle of the bend must be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of vias must be kept to a minimum. It is recommended to keep the via count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- Do NOT route differential pairs over any plane split.
- Adding Test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test points are used, they must be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

11.1.3 Ground

TI recommends that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the SN65DSI84-Q1 must be connected to this plane with vias.

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11.2 Layout Example

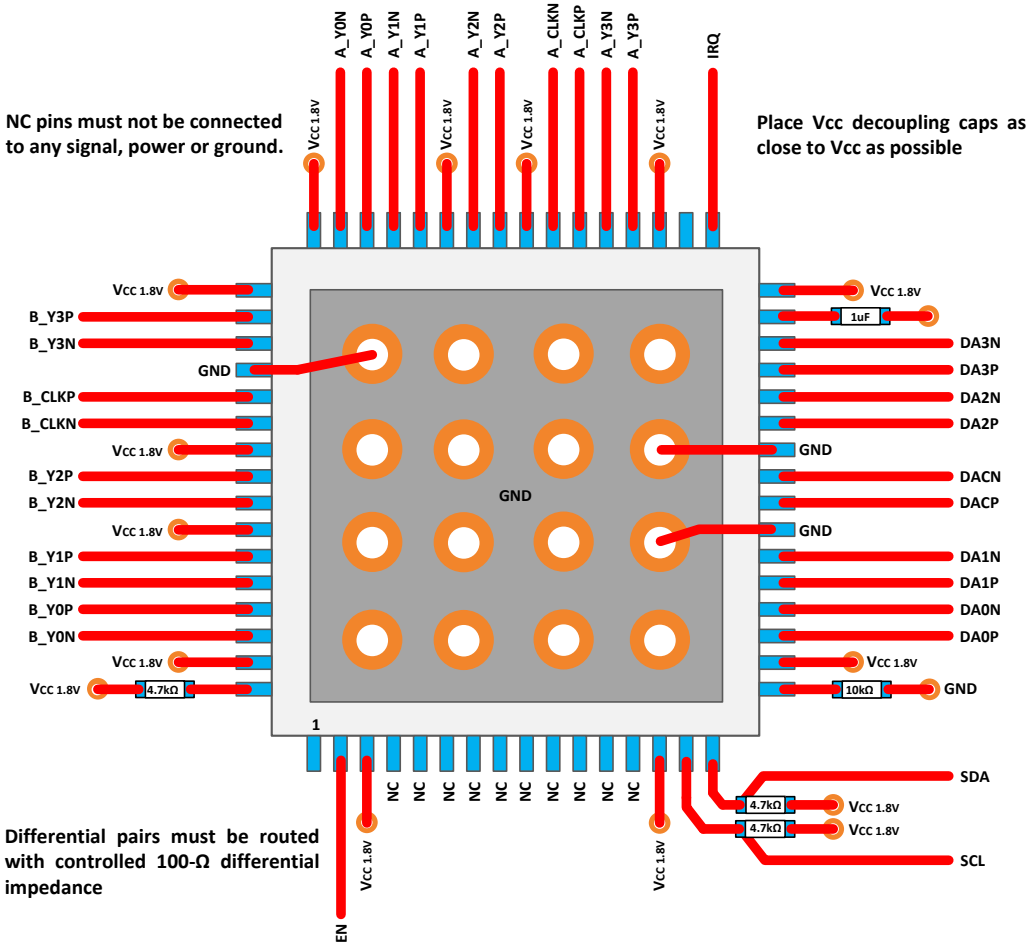


Figure 50. SN65DSI8x Layout Example

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12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《SN65DSI8x 视频配置指南和配置工具用户手册》*（文献编号：SLLA332）
- *《SN65DSI83、SN65DSI84 和 SN65DSI85 硬件实现指南》*（文献编号：SLLA340）

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
MIPI is a registered trademark of Arasan Chip Systems, Inc..
All other trademarks are the property of their respective owners.

12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65DSI84TPAPRQ1	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	DSI84TQ1
SN65DSI84TPAPRQ1.A	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	DSI84TQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN65DSI84-Q1 :

- Catalog : SN65DSI84

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

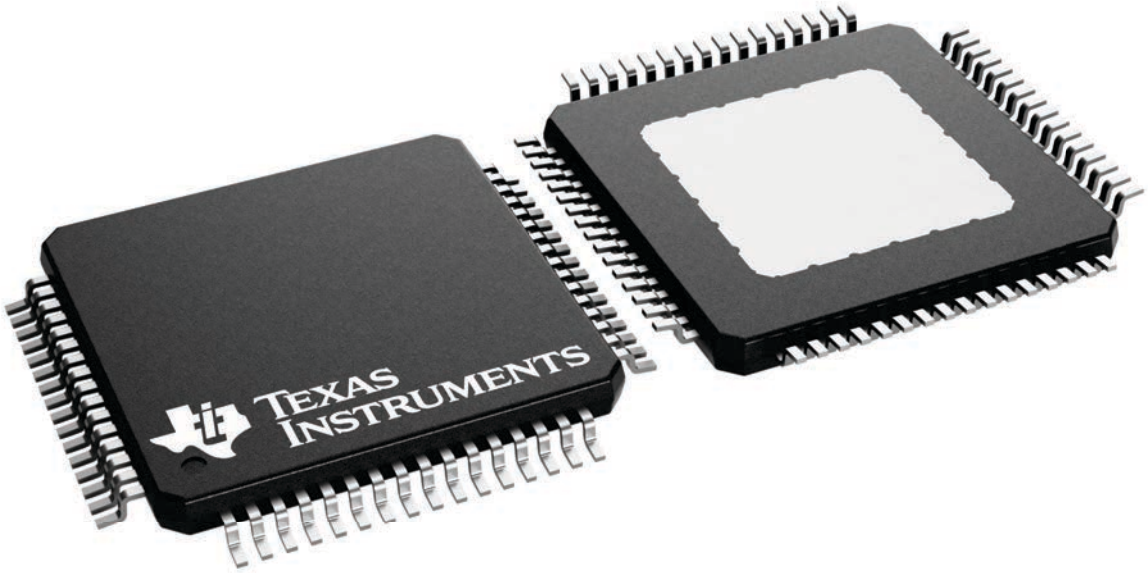
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



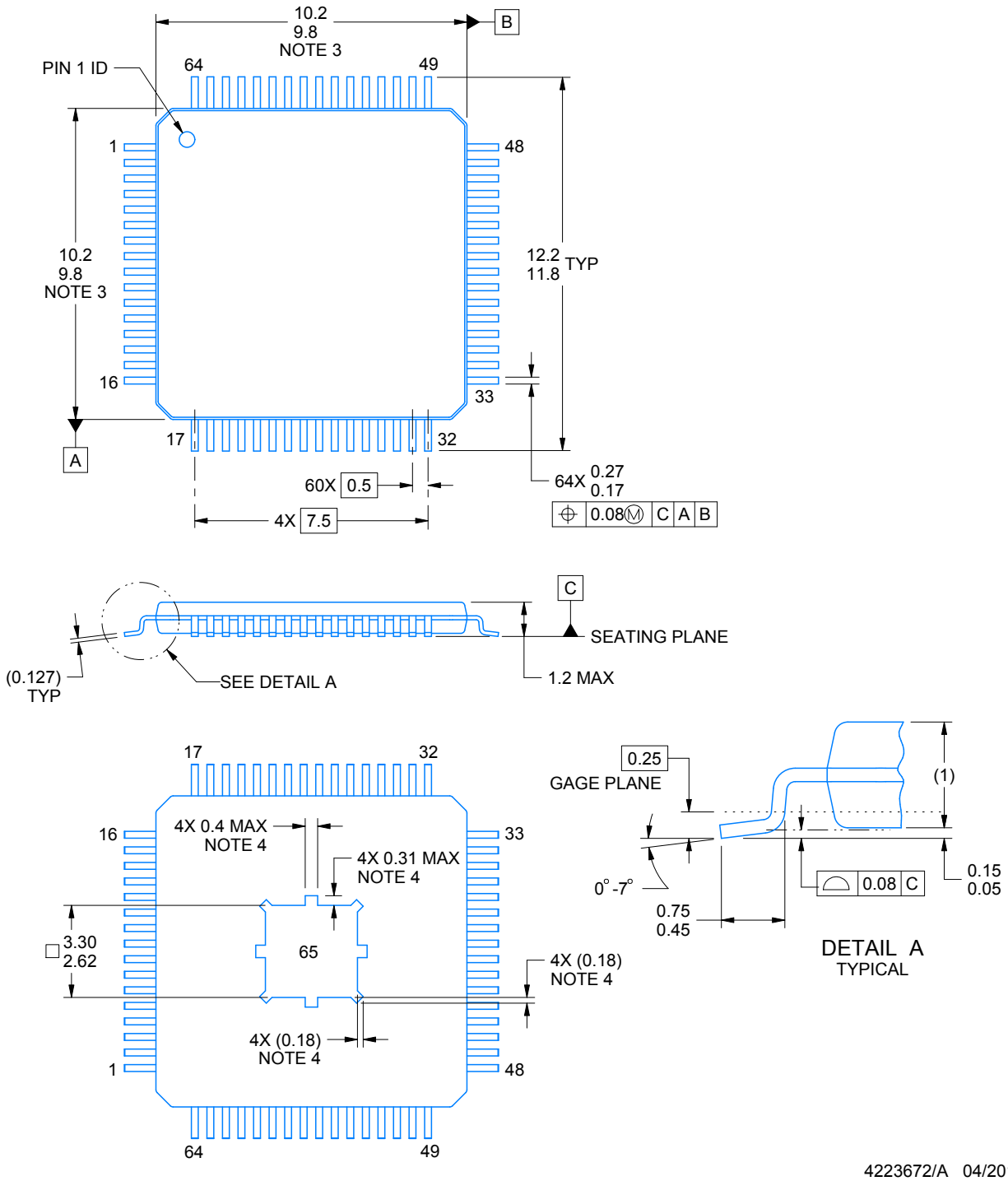
4226442/A

PACKAGE OUTLINE

PAP0064Q

PowerPAD™ TQFP - 1.2 mm max height

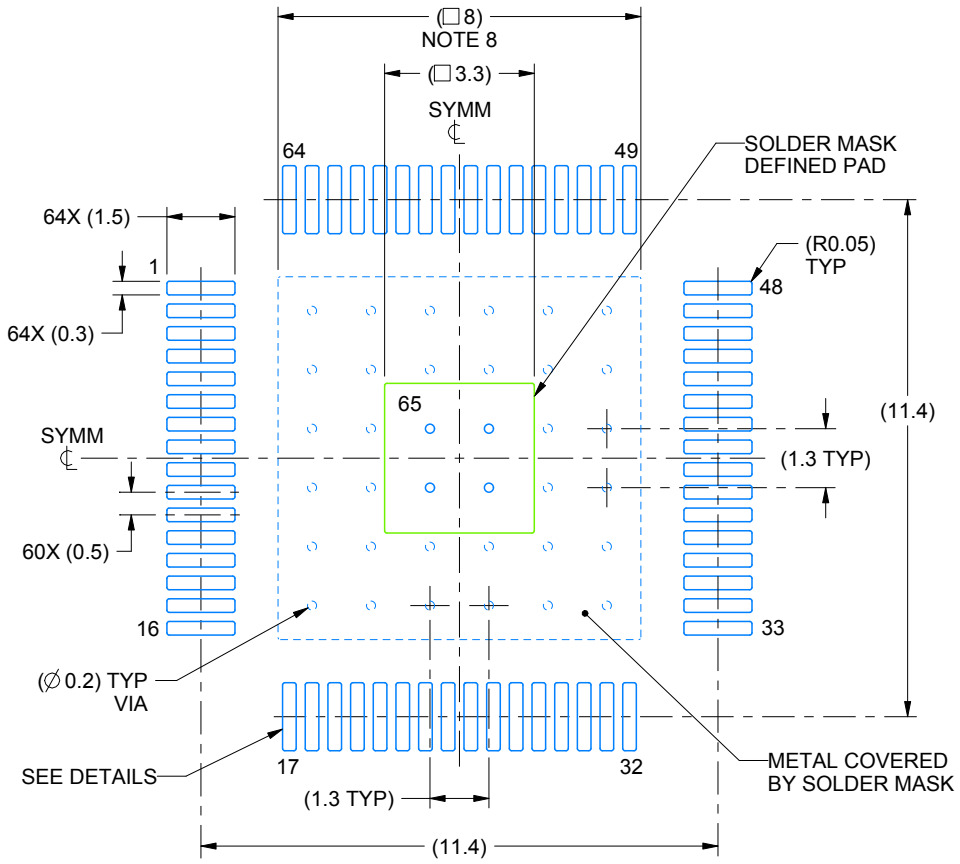
PLASTIC QUAD FLATPACK



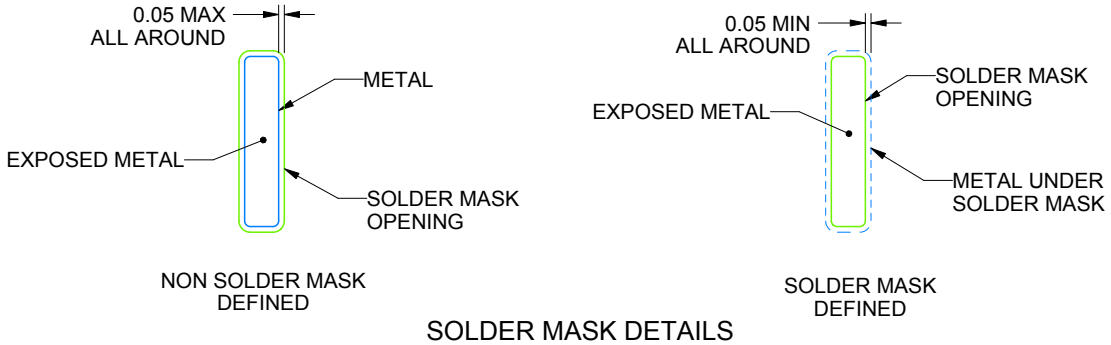
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

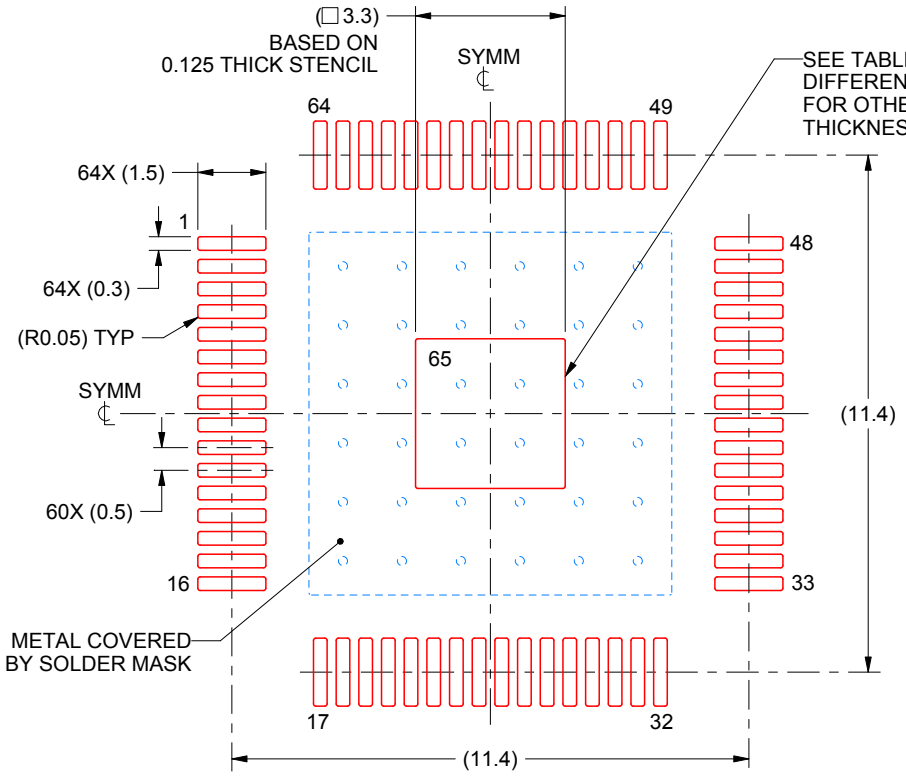


SOLDER MASK DETAILS

4223672/A 04/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4223672/A 04/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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