SN55HVD233-SP 3.3V 耐辐射 CAN 收发器

1 特性

- 符合 MIL-PRF 38535 的 QMLV（QML V 类）耐辐射 (RHA) SMD 5962L1420901VXC
  - 单粒子闩锁 (SEL) 在 125°C 下的抗扰度可达 86MeV-cm^2/mg
  - 电离辐射总剂量 (TID) 在低剂量率下可达 50kRad (Si)
  - 符合军用温度范围（-55°C 至 125°C）
  - 高性能 8 引脚陶瓷扁平封装 (HKX)
- 符合 ISO 11898-2 标准
- 总线引脚故障保护大于 ±16V
- 总线引脚 ESD 保护大于 ±16kV HBM
- 数据传输速率高达 1Mbps
- 扩展级共模范围：–7V 至 12V
- 高输入阻抗，允许连接 120 个节点
- 低电压晶体管-晶体管逻辑电路 (LVTTL) I/O 可耐受 5V 电压
- 可调节的驱动器传输次数，用于改善信号质量
- 未供电节点不会干扰总线
- 低电流待机模式，200μA 典型值
- 诊断回送功能
- 热关断保护
- 加电和断电无干扰总线输入和输出
  - 具有低 V_{CC} 的高输入阻抗
  - 功率循环过程中单片输出

2 应用

- 航天器背板数据总线通信和控制
- CANopen、DeviceNet、CAN Kingdom、ISO 11783、NMEA 2000、SAE J1939 等 CAN 总线标准

3 说明

SN55HVD233-SP 依照 ISO 11898 标准， 用于 使用控制器区域网络 (CAN) 串行通信物理层的航天器应用中。作为 CAN 收发器，此器件在差分 CAN 总线和 CAN 控制器间提供传输和接收能力，信令速度高达 1Mbps。

SN55HVD233-SP 专门用于严苛的辐射环境， 具有 交叉线保护、过压保护、±16V 接地失效保护和过热（热关断）保护。此器件可在 –7V 至 12V 的宽共模范围内运行。此收发器是用于卫星应用的微处理器、FPGA 或 ASIC 的主机 CAN 控制器与差分 CAN 总线之间的接口。

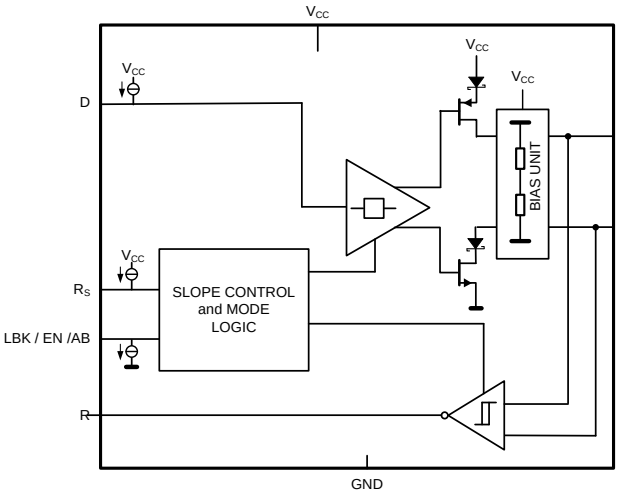
器件信息(1)

器件型号	等级	封装
5962L1420901VXC	QMLV RHA [50kRad]	8 引线 CFP [HKX] 6.48mm × 6.48mm
HVD233HKX/EM(2)	工程样片	8 引线 CFP [HKX] 6.48mm × 6.48mm
SN55HVD233EVM-CVAL	陶瓷评估板	

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 这些部件仅适用于工程评估。部件按照不合规的流程进行加工处理。这些部件不适用于质检、生产、辐射测试或飞行。这些零部件无法在 –55°C 至 125°C 的完整 MIL 额定温度范围内或运行寿命中保证其性能。

简化原理图



Copyright © 2017, Texas Instruments Incorporated

目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 说明 （续） ... 3
6 **Pin Configuration and Functions** ... 3
7 **Specifications** ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 5
7.5 Driver Electrical Characteristics ... 6
7.6 Receiver Electrical Characteristics ... 6
7.7 Driver Switching Characteristics ... 7
7.8 Receiver Switching Characteristics ... 8
7.9 Device Switching Characteristics ... 8
7.10 Typical Characteristics ... 9
8 **Parameter Measurement Information** ... 11
9 **Detailed Description** ... 15
9.1 Overview ... 15
9.2 Functional Block Diagram ... 15
9.3 Feature Description ... 15
9.4 Device Functional Modes ... 19
10 **Application and Implementation** ... 20
10.1 Application Information ... 20
10.2 Typical Application ... 22
11 **Power Supply Recommendations** ... 24
12 **Layout** ... 24
12.1 Layout Guidelines ... 24
12.2 Layout Example ... 26
13 器件和文档支持 ... 27
13.1 接收文档更新通知 ... 27
13.2 社区资源 ... 27
13.3 商标 ... 27
13.4 静电放电警告 ... 27
13.5 Glossary ... 27
14 机械、封装和可订购信息 ... 27

4 修订历史记录

Changes from Original (September 2017) to Revision A **Page**

- 已更改 将器件状态从*高级信息* 更改为*生产数据* ... 1

版权 © 2017, Texas Instruments Incorporated

5 说明（续）

模式：SN55HVD233-SP 的引脚 8 R_S 具有三种运行模式：高速、斜率控制或低功耗待机模式。用户可直接将引脚 8 接地以选择高速运行模式，驱动器输出晶体管将尽快开启和关闭，无上升和下降斜率限制。由于斜率与引脚的输出电流成比例，用户可在引脚 8 连接接地的电阻器以调节上升和下降斜率。斜率控制可通过 0Ω 电阻进行，以实现约 38V/µs 的转换率；最高可通过 50kΩ电阻进行，从而实现约 4V/µs 的转换率。有关斜率控制的更多信息，请参阅*应用和实现* 部分。

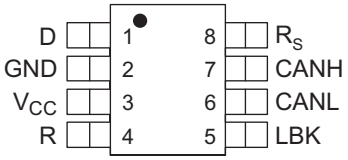
如果引脚 8 具有高模式电平，当驱动器关闭且接收器保持工作状态时，SN55HVD233-SP 将进入低电流待机（只听）模式。当本地协议控制器需要向总线传输时，将会改变此低电流待机模式。有关回送模式的更多信息，请参阅*应用信息* 部分。

回送：SN55HVD233-SP 的回送 LBK 引脚 5 逻辑高电平使总线输出和总线输入处于高阻抗状态。其余电路将保持工作状态，可用于驱动器到接收器的回送和自诊断节点功能，且不会干扰总线。

CAN 总线状态：在器件供电运行期间，CAN 总线具有两种状态：显性和隐性。在总线显性状态下，总线采用差分驱动方式，D 和 R 引脚相应地置为逻辑低电平。在隐性总线状态下，总线通过接收器的高电阻内部输入电阻器 R_{IN} 偏置为 $V_{CC}/2$，D 和 R 引脚相应地偏置为逻辑高电平（请参阅总线状态（物理位表示） 和简化的隐性共模偏置和接收器）。

6 Pin Configuration and Functions

HKX Package
8-Pin CFP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input.
GND	2	GND	Ground connection.
V_{CC}	3	Supply	Transceiver 3.3-V supply voltage.
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output.
LBK	5	I	Loopback mode input pin.
CANL	6	I/O	Low-level CAN bus line.
CANH	7	I/O	High-level CAN bus line.
RS	8	I	Mode select pin: Tie to GND = high-speed mode, Strong pullup to V_{CC} = low power mode, 0-Ω to 50-kΩ pulldown to GND = slope control mode.

Copyright © 2017, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature unless otherwise noted(1)(2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	7	V
	Voltage at any bus pin (CANH or CANL)	–16	16	V
	Voltage input, transient pulse, CANH and CANL, through 100 Ω (see Figure 18)	–100	100	V
V_I	Input voltage, (D, RS, LBK)	–0.5	7	V
V_O	Output voltage, (R)	–0.5	7	V
I_O	Receiver output current	–10	10	mA
T_J	Operating junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground pin.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	CANH, CANL, and GND	±14000	V
			Other pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
	Voltage at any bus pin (separately or common mode)		–7		12	V
V_{IH}	High-level input voltage	D, LBK	2		5.5	V
V_{IL}	Low-level input voltage	D, LBK	0		0.8	V
V_{ID}	Differential input voltage		–6		6	V
	Resistance from RS to ground for slope control		0		50	kΩ
$V_{I(RS)}$	Input voltage at RS for standby		0.75 V_{CC}		5.5	V
I_{OH}	High-level output current	Driver	–50			mA
		Receiver	–10			
I_{OL}	Low-level output current	Driver			50	mA
		Receiver			10	
T_J	Operating junction temperature(1)		–55		125	°C

(1) Maximum junction temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

Copyright © 2017, Texas Instruments Incorporated

7.4 Thermal Information

THERMAL METRIC[1][2]		SN55HVD233-SP HKX (CFP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.0	°C/W

(1) All values except $R_{\theta JC}$ were taken on a JEDEC-51 standard High-K PCB using a nominal lead form. Differences in lead form, component density, or PCB design can affect these values.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2017, Texas Instruments Incorporated

7.5 Driver Electrical Characteristics

The specifications shown below are valid across temperature range of –55°C to 125°C pre-radiation and 25°C post-radiation. When different, the post-radiation values are shown in a separate row specified by the corresponding RHA level (L = 50 krad).

PARAMETER			TEST CONDITIONS		SUBGROUP(1)	MIN	TYP(2)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (dominant)	CANH	$V_{(D)}$ = 0 V, $V_{(RS)}$ = 0 V, see Figure 12 and Figure 13		[1, 2, 3]	2.4		V_{CC}	V
		CANL			[1, 2, 3]	0.5		1.25	
V_O	Bus output voltage (recessive)	CANH	$V_{(D)}$ = 3 V, $V_{(RS)}$ = 0 V, see Figure 12 and Figure 13				2.3		V
		CANL					2.3		
$V_{OD(D)}$	Differential output voltage (dominant)		$V_{(D)}$ = 0 V, $V_{(RS)}$ = 0 V, see Figure 12 and Figure 13		[1, 2, 3]	1.5	2	3	V
				L		1.4			
			$V_{(D)}$ = 0 V, $V_{(RS)}$ = 0 V, see Figure 13 and Figure 14		[1, 2, 3]	1.2	2	3	
V_{OD}	Differential output voltage (recessive)		$V_{(D)}$ = 3 V, $V_{(RS)}$ = 0 V, see Figure 12 and Figure 13		[1, 2, 3]	–120		12	mV
			$V_{(D)}$ = 3 V, $V_{(RS)}$ = 0 V, no load		[1, 2, 3]	–0.5		0.05	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		See Figure 20				1		V
I_{IH}	High-level input current	D, LBK	$V_{(D)}$ = 2 V		[1, 2, 3]	–30		30	µA
I_{IL}	Low-level input current	D, LBK	$V_{(D)}$ = 0.8 V		[1, 2, 3]	–30		30	µA
I_{OS}	Short-circuit output current		$V_{(CANH)}$ = –7 V, CANL open, see Figure 23		[1, 2, 3]	–250			mA
			$V_{(CANH)}$ = 12 V, CANL open, see Figure 23		[1, 2, 3]			1	
			$V_{(CANL)}$ = –7 V, CANH open, see Figure 23		[1, 2, 3]	–1			
			$V_{(CANL)}$ = 12 V, CANH open, see Figure 23		[1, 2, 3]			250	
C_O	Output capacitance		See receiver input capacitance						
$I_{IRS(s)}$	RS input current for standby		$V_{(RS)}$ = 0.75 V_{CC}		[1, 2, 3]	–10			µA
I_{CC}	Supply current	Standby	$V_{(RS)}$ = V_{CC}, $V_{(D)}$ = V_{CC}, $V_{(LBK)}$ = 0 V		[1, 2, 3]		200	600	µA
		Dominant	$V_{(D)}$ = 0 V, no load, $V_{(LBK)}$ = 0 V, RS = 0 V		[1, 2, 3]			6	mA
		Recessive	$V_{(D)}$ = V_{CC}, no load, $V_{(LBK)}$ = 0 V, $V_{(RS)}$ = 0 V		[1, 2, 3]			6	

(1) For subgroup definitions, please see Table 1.
(2) All typical values are at 25°C and with a 3.3-V supply.

7.6 Receiver Electrical Characteristics

The specifications shown below are valid across temperature range of –55°C to 125°C pre-radiation and 25°C post-radiation. When different, the post-radiation values are shown in a separate row specified by the corresponding RHA level (L = 50 krad).

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP(2)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_{(LBK)}$ = 0 V, see Table 2	[1, 2, 3]		750	900	mV
$V_{IT–}$	Negative-going input threshold voltage		[1, 2, 3]	500	650		mV
V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)				100		mV
V_{OH}	High-level output voltage	I_O = –4 mA, see Figure 17	[1, 2, 3]	2.4			V
V_{OL}	Low-level output voltage	I_O = 4 mA, see Figure 17	[1, 2, 3]			0.4	V

(1) For subgroup definitions, please see Table 1.
(2) All typical values are at 25°C and with a 3.3-V supply.

Copyright © 2017, Texas Instruments Incorporated

Receiver Electrical Characteristics (continued)

The specifications shown below are valid across temperature range of –55°C to 125°C pre-radiation and 25°C post-radiation. When different, the post-radiation values are shown in a separate row specified by the corresponding RHA level (L = 50 krad).

PARAMETER			TEST CONDITIONS		SUBGROUP(1)	MIN	TYP(2)	MAX	UNIT
I_I	Bus input current		$V_{(CANH)}$ or $V_{(CANL)}$ = 12 V	Other bus pin = 0 V, $V_{(D)}$ = 3 V, $V_{(LBK)}$ = 0 V, $V_{(RS)}$ = 0 V	[1, 2, 3]	150		500	µA
			$V_{(CANH)}$ or $V_{(CANL)}$ = 12 V, V_{CC} = 0 V		[1, 2, 3]	150		600	
			CANH or CANL = –7 V		[1, 2, 3]	–610		–100	
			CANH or CANL = –7 V, V_{CC} = 0 V		[1, 2, 3]	–450		–100	
C_I	Input capacitance (CANH or CANL)		Pin-to-ground, V_I = 0.4 sin(4E6πt) + 0.5 V, $V_{(D)}$ = 3 V, $V_{(LBK)}$ = 0 V				40		pF
C_{ID}	Differential input capacitance		Pin-to-pin, V_I = 0.4 sin(4E6πt) + 0.5 V, $V_{(D)}$ = 3 V, $V_{(LBK)}$ = 0 V				20		pF
R_{ID}	Differential input resistance		$V_{(D)}$ = 3 V, $V_{(LBK)}$ = 0 V		[4, 5, 6]	40		105	kΩ
R_{IN}	Input resistance (CANH or CANL)				[4, 5, 6]	20		55	kΩ
I_{CC}	Supply current	Standby	$V_{(RS)}$ = V_{CC}, $V_{(D)}$ = V_{CC}, $V_{(LBK)}$ = 0 V		[1, 2, 3]		200	600	µA
		Dominant	$V_{(D)}$ = 0 V, no load, $V_{(RS)}$ = 0 V, $V_{(LBK)}$ = 0 V		[1, 2, 3]			6	mA
		Recessive	$V_{(D)}$ = V_{CC}, no load, $V_{(RS)}$ = 0 V, $V_{(LBK)}$ = 0 V		[1, 2, 3]			6	mA

7.7 Driver Switching Characteristics

The specifications shown below are valid across temperature range of –55°C to 125°C pre-radiation and 25°C post-radiation. When different, the post-radiation values are shown in a separate row specified by the corresponding RHA level (L = 50 krad).

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP(2)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$V_{(RS)}$ = 0 V, see Figure 15	[9, 10, 11]		35	85	ns
		RS with 10 kΩ to ground, see Figure 15	[9, 10, 11]		70	125	
		RS with 50 kΩ to ground, see Figure 15	[9, 10, 11]		500	870	
t_{PHL}	Propagation delay time, high-to-low-level output	$V_{(RS)}$ = 0 V, see Figure 15	[9, 10, 11]		70	120	ns
		RS with 10 kΩ to ground, see Figure 15	[9, 10, 11]		130	180	
		RS with 50 kΩ to ground, see Figure 15	[9, 10, 11]		870	1200	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	$V_{(RS)}$ = 0 V, see Figure 15			35		ns
		RS with 10 kΩ to ground, see Figure 15			60		
		RS with 50 kΩ to ground, see Figure 15			370		
t_r	Differential output signal rise time	$V_{(RS)}$ = 0 V, see Figure 15	[9, 10, 11]	20		70	ns
t_f	Differential output signal fall time		[9, 10, 11]	20		70	ns
t_r	Differential output signal rise time	RS with 10 kΩ to ground, see Figure 15	[9, 10, 11]	30		135	ns
t_f	Differential output signal fall time		[9, 10, 11]	30		135	ns
t_r	Differential output signal rise time	RS with 50 kΩ to ground, see Figure 15	[9, 10, 11]	350		1400	ns
t_f	Differential output signal fall time		[9, 10, 11]	350		1400	ns
$t_{en(s)}$	Enable time from standby to dominant	See Figure 19	[9, 10, 11]		0.6	1.5	µs

(1) For subgroup definitions, please see Table 1.
(2) All typical values are at 25°C and with a 3.3-V supply.

Copyright © 2017, Texas Instruments Incorporated

7.8 Receiver Switching Characteristics

The specifications shown below are valid across temperature range of –55°C to 125°C pre-radiation and 25°C post-radiation. When different, the post-radiation values are shown in a separate row specified by the corresponding RHA level (L = 50 krad).

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP(2)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 17	[9, 10, 11]		35	105	ns
t_{PHL}	Propagation delay time, high-to-low-level output		[9, 10, 11]		35	105	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				7		ns
t_r	Output signal rise time				2		ns
t_f	Output signal fall time				2		ns

(1) For subgroup definitions, please see Table 1.
(2) All typical values are at 25°C and with a 3.3-V supply.

7.9 Device Switching Characteristics

The specifications shown below are valid across temperature range of –55°C to 125°C pre-radiation and 25°C post-radiation. When different, the post-radiation values are shown in a separate row specified by the corresponding RHA level (L = 50 krad).

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP(2)	MAX	UNIT
$t_{(LBK)}$	Loopback delay, driver input to receiver output	See Figure 22			7.5		ns
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant	$V_{(RS)}$ at 0 V, see Figure 21	[9, 10, 11]		70	150	ns
		$V_{(RS)}$ with 10 kΩ to ground, see Figure 21	[9, 10, 11]		105	225	
		$V_{(RS)}$ with 50 kΩ to ground, see Figure 21	[9, 10, 11]		500	600	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive	$V_{(RS)}$ at 0 V, See Figure 21	[9, 10, 11]		70	150	ns
		$V_{(RS)}$ with 10 kΩ to ground, see Figure 21	[9, 10, 11]		105	225	
		$V_{(RS)}$ with 50 kΩ to ground, see Figure 21	[9, 10, 11]		500	600	

(1) For subgroup definitions, please see Table 1.
(2) All typical values are at 25°C and with a 3.3-V supply.

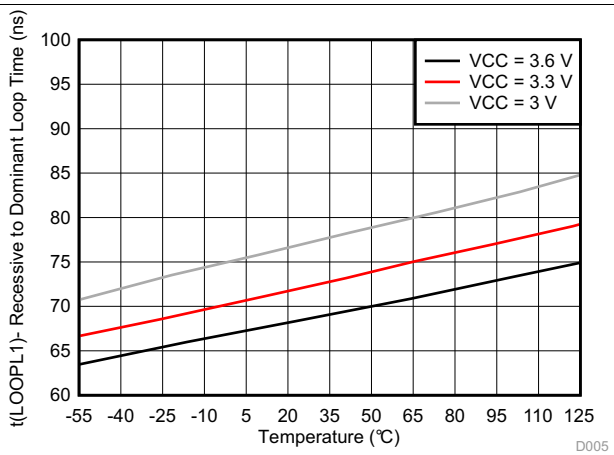
Table 1. Quality Conformance Inspection(1)

SUBGROUP	DESCRIPTION	TEMPERATURE (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

(1) MIL-STD-883, Method 5005 - Group A

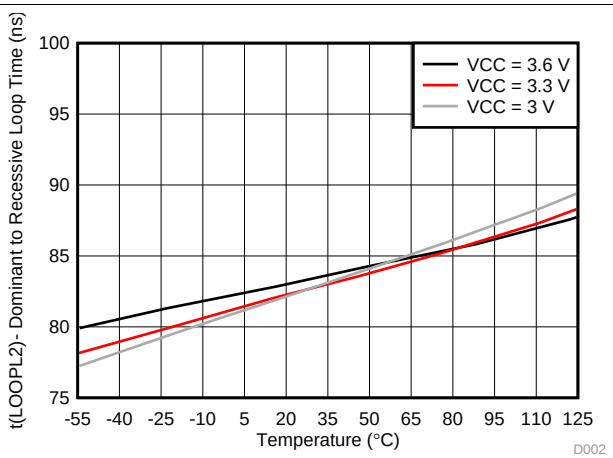
Copyright © 2017, Texas Instruments Incorporated

7.10 Typical Characteristics



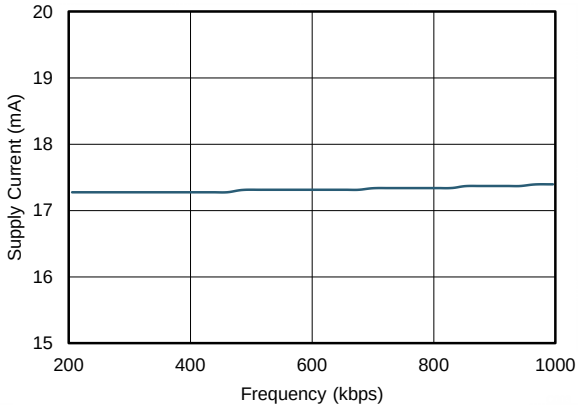
$V_{(RS)}$, $V_{(LBK)}$ = 0 V

Figure 1. Recessive-To-Dominant Loop Time vs Temperature



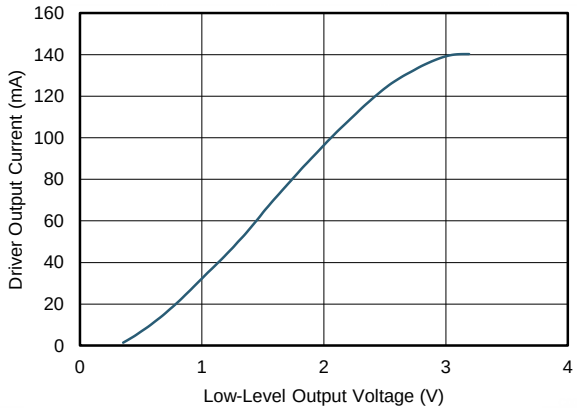
$V_{(RS)}$, $V_{(LBK)}$ = 0 V

Figure 2. Dominant-To-Recessive Loop Time vs Temperature



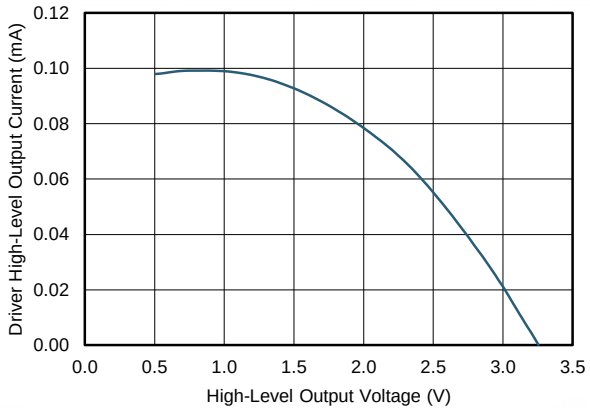
V_{CC} = 3.3 V $V_{(RS)}$, $V_{(LBK)}$ = 0 V T_A = 25°C
60-Ω load

Figure 3. Supply Current vs Frequency



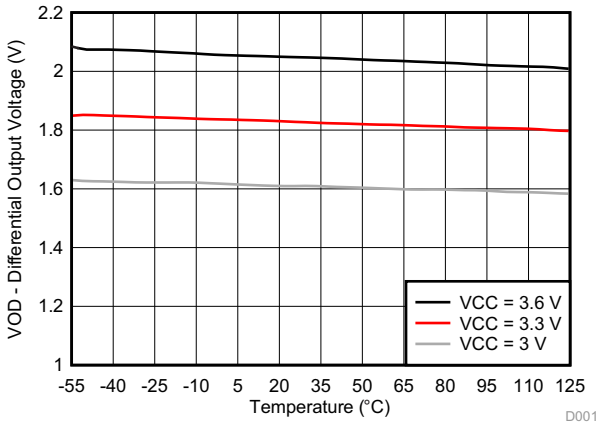
V_{CC} = 3.3 V $V_{(RS)}$, $V_{(LBK)}$ = 0 V T_A = 25°C

Figure 4. Driver Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 3.3 V $V_{(RS)}$, $V_{(LBK)}$ = 0 V T_A = 25°C

Figure 5. Driver High-Level Output Current vs High-Level Output Voltage

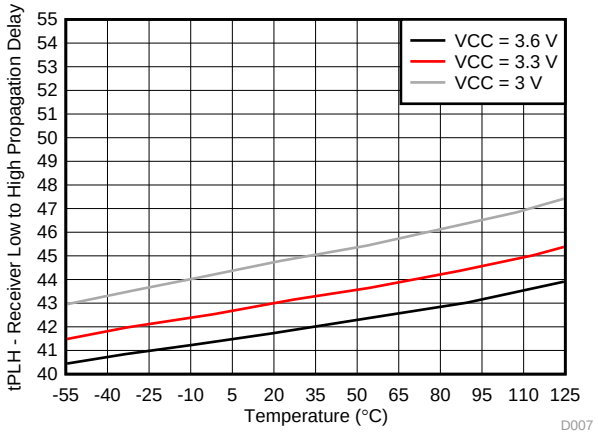


R_L = 60 Ω $V_{(RS)}$, $V_{(LBK)}$ = 0 V

Figure 6. Differential Output Voltage vs Temperature

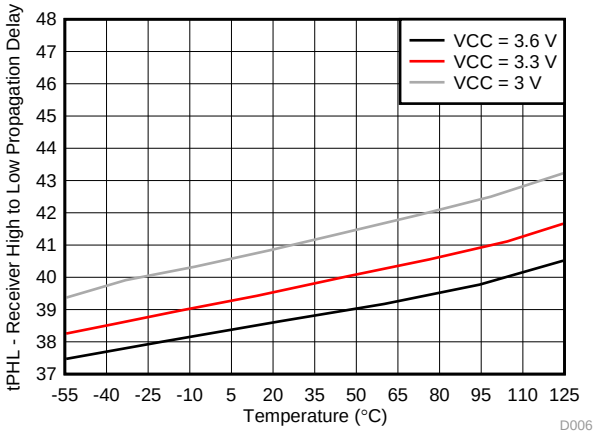
Copyright © 2017, Texas Instruments Incorporated

Typical Characteristics (continued)



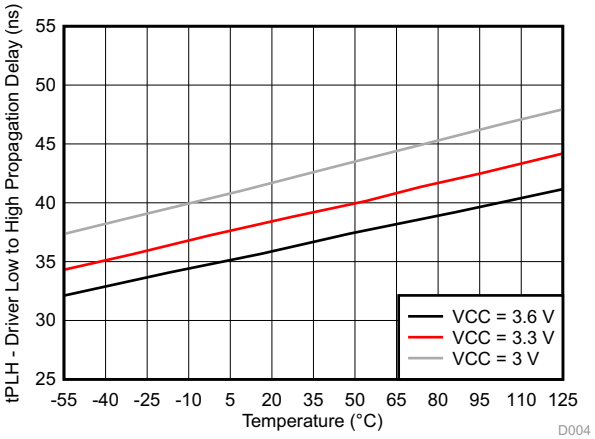
$V_{(RS)}$, $V_{(LBK)}$ = 0 V See Figure 17

Figure 7. Receiver Low-To-High Propagation Delay vs Temperature



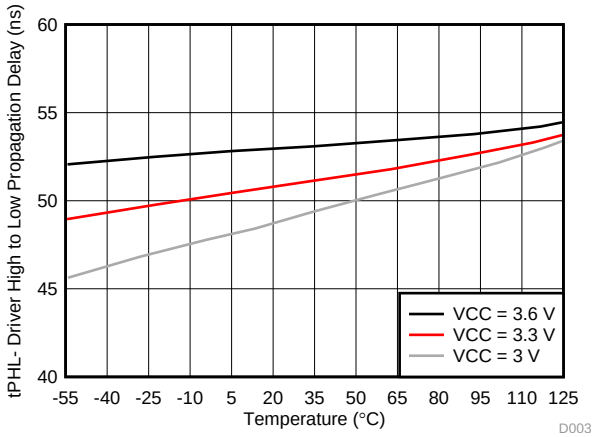
$V_{(RS)}$, $V_{(LBK)}$ = 0 V See Figure 17

Figure 8. Receiver High-To-Low Propagation Delay vs Temperature



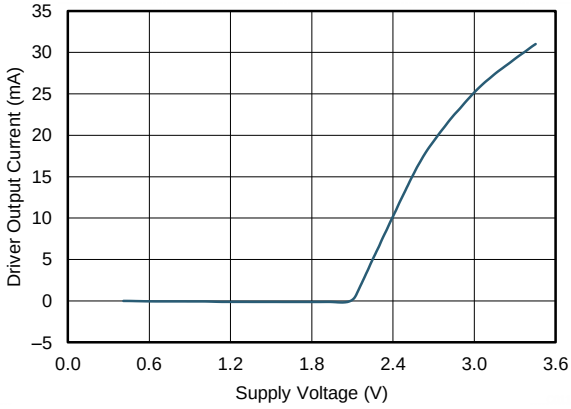
$V_{(RS)}$, $V_{(LBK)}$ = 0 V See Figure 15

Figure 9. Driver Low-To-High Propagation Delay vs Temperature



$V_{(RS)}$, $V_{(LBK)}$ = 0 V See Figure 15

Figure 10. Driver High-To-Low Propagation Delay vs Temperature



$V_{(RS)}$, $V_{(LBK)}$ = 0 V T_A = 25°C R_L = 60 Ω

Figure 11. Driver Output Current vs Supply Voltage

Copyright © 2017, Texas Instruments Incorporated

8 Parameter Measurement Information

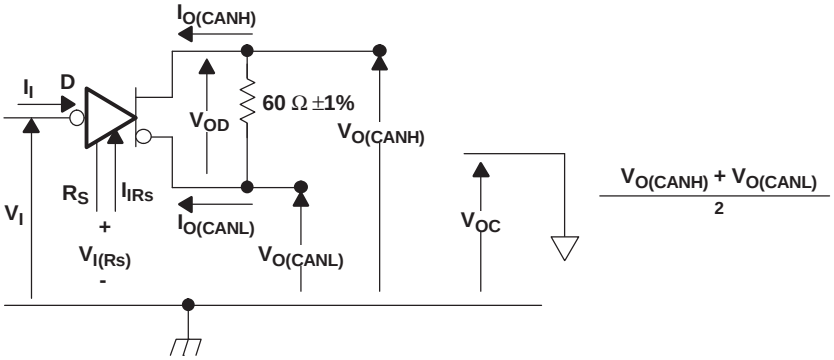


Figure 12. Driver Voltage, Current, and Test Definition

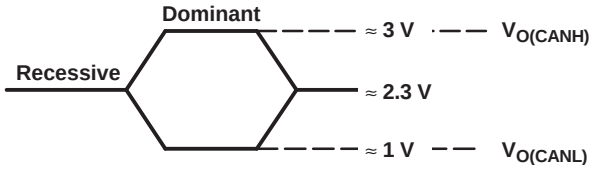


Figure 13. Bus Logic State Voltage Definitions

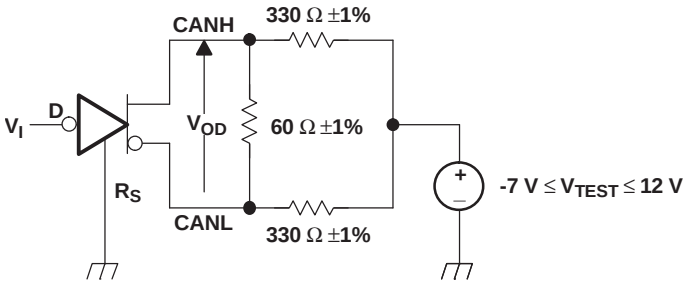
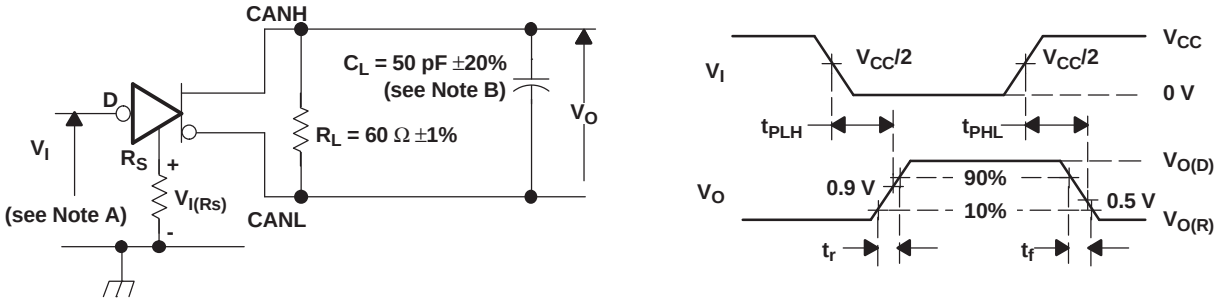


Figure 14. Driver V_{OD}



A. The input pulse is supplied by a generator having the following characteristics:
- Pulse repetition rate (PRR) ≤125 kHz, 50% duty cycle
- t_r ≤ 6 ns
- t_f ≤ 6 ns
- Z_O = 50 Ω

B. C_L includes fixture and instrumentation capacitance.

Figure 15. Driver Test Circuit and Voltage Waveforms

Copyright © 2017, Texas Instruments Incorporated

Parameter Measurement Information (continued)

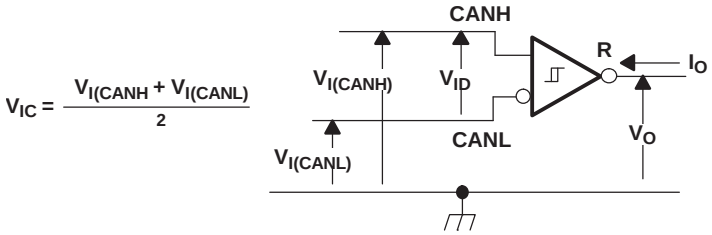
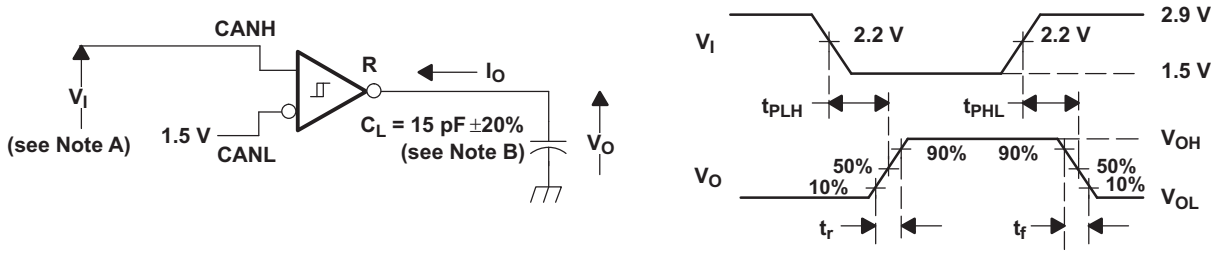


Figure 16. Receiver Voltage and Current Definitions



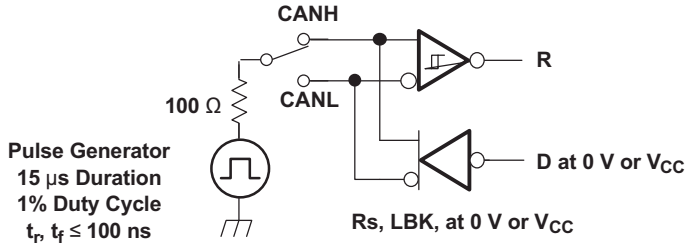
A. The input pulse is supplied by a generator having the following characteristics:
- PRR ≤125 kHz, 50% duty cycle
- t_r ≤ 6 ns
- t_f ≤ 6 ns
- Z_O = 50 Ω

B. C_L includes fixture and instrumentation capacitance.

Figure 17. Receiver Test Circuit and Voltage Waveforms

Table 2. Differential Input Voltage Threshold Test

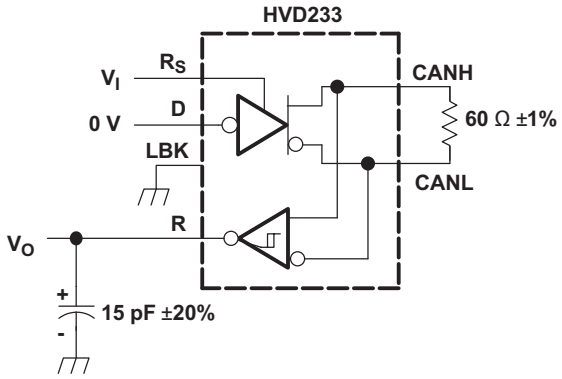
INPUT		OUTPUT		MEASURED
V_{CANH}	V_{CANL}	R		$\lvert V_{ID}\rvert$
–6.1 V	–7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
–1 V	–7 V	L		6 V
12 V	6 V	L		6 V
–6.5 V	–7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
–7 V	–1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X

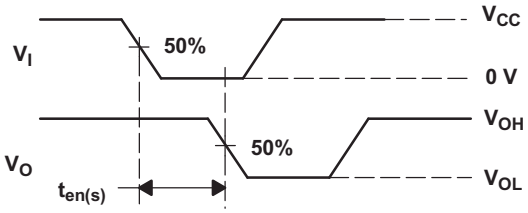


NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 18. Test Circuit, Transient Overvoltage Test

Copyright © 2017, Texas Instruments Incorporated



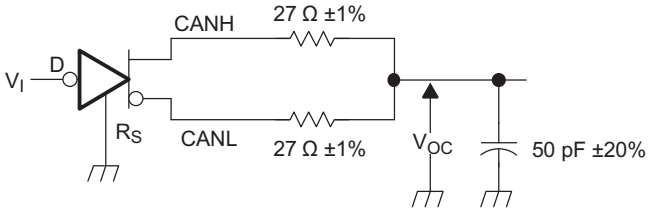


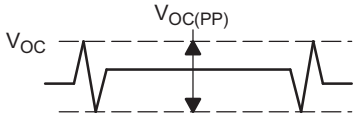
Copyright © 2017, Texas Instruments Incorporated

NOTE: All V_I input pulses are supplied by a generator having the following characteristics:

- t_r or t_f ≤ 6 ns
- PRR = 125 kHz, 50% duty cycle

Figure 19. $T_{en(s)}$ Test Circuit and Voltage Waveforms

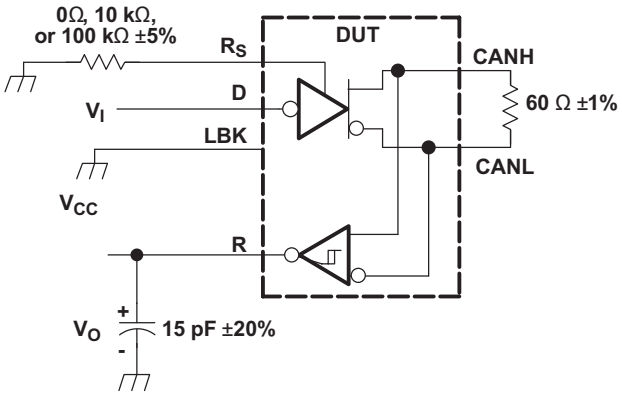




NOTE: All V_I input pulses are supplied by a generator having the following characteristics:

- t_r or t_f ≤ 6 ns
- PRR = 125 kHz, 50% duty cycle

Figure 20. $V_{OC(pp)}$ Test Circuit and Voltage Waveforms



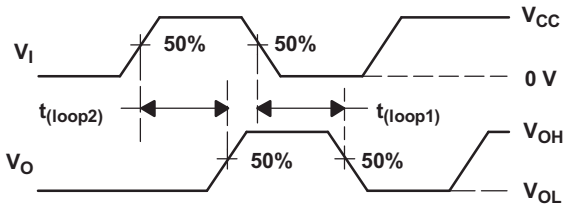
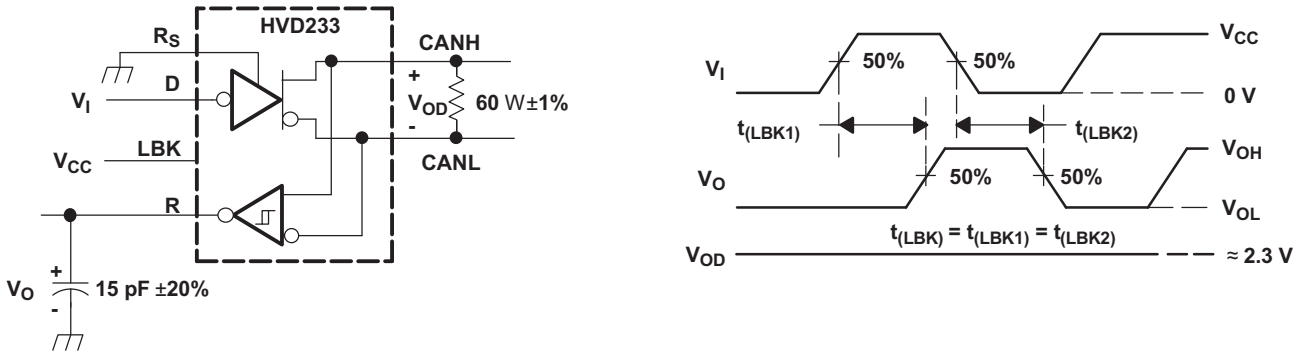


Figure 21. $T_{(loop)}$ Test Circuit and Voltage Waveforms



Copyright © 2017, Texas Instruments Incorporated

Figure 22. $T_{(LBK)}$ Test Circuit and Voltage Waveforms

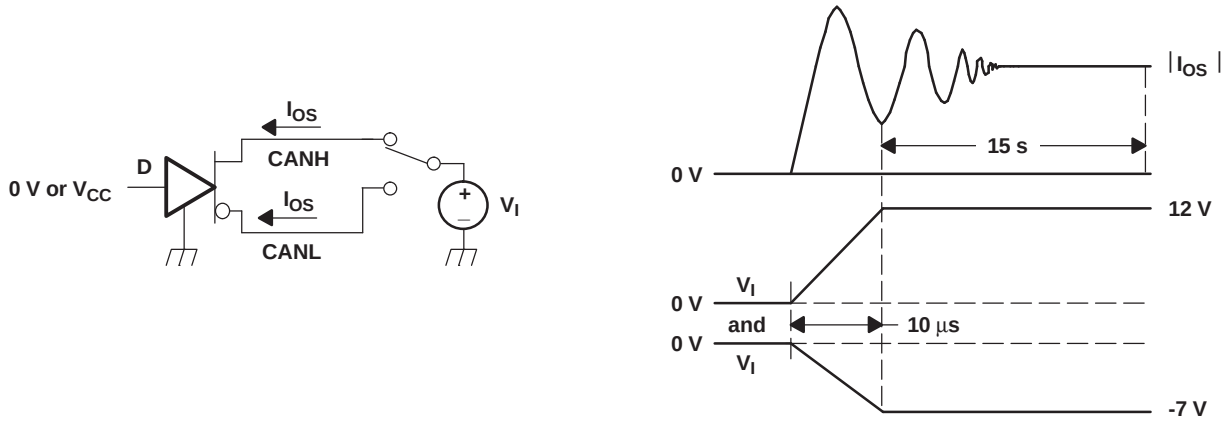
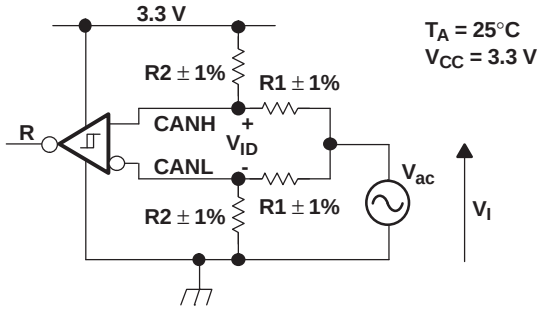
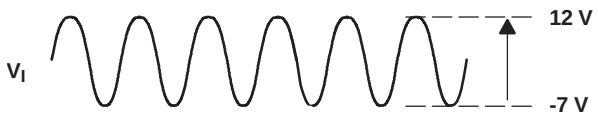


Figure 23. I_{OS} Test Circuit and Waveforms



The R Output State Does Not Change During Application of the Input Waveform.

V_{ID}	R1	R2
500 mV	50 Ω	280 Ω
900 mV	50 Ω	130 Ω



NOTE: All input pulses are supplied by a generator with $f \leq 1.5$ MHz.

Figure 24. Common-Mode Voltage Rejection

Copyright © 2017, Texas Instruments Incorporated

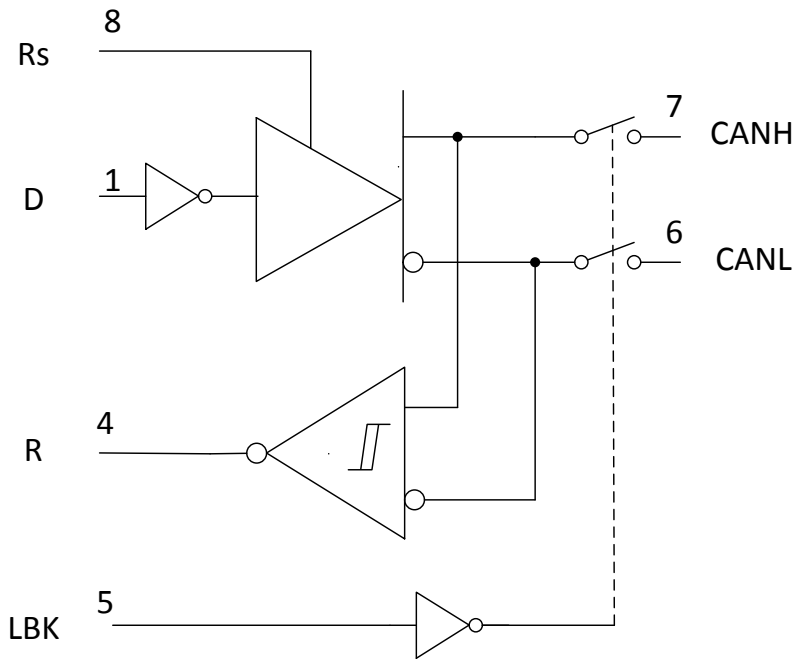
9 Detailed Description

9.1 Overview

The SN55HVD233-SP is used in applications employing the CAN serial communication physical layer in accordance with the ISO 11898 standard. As a CAN transceiver, the device provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

Designed for operation in especially harsh environments, the SN55HVD233-SP features cross-wire, overvoltage, and loss of ground protection to ±16 V, overtemperature (thermal shutdown) protection, and common-mode transient protection of ±100 V. This device operates over a wide –7-V to 12-V common mode range. This transceiver is the interface between the host CAN controller on the microprocessor, FPGA, or ASIC, and the differential CAN bus used in satellite applications.

9.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

9.3 Feature Description

9.3.1 Modes

The R_S, pin 8 of the SN55HVD233-SP, provides for three modes of operation: high-speed, slope control, or low-power standby mode. The user selects the high-speed mode of operation by connecting pin 8 directly to ground, allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. The user can adjust the rise and fall slope by connecting a resistor to ground at pin 8, because the slope is proportional to the pin's output current. Slope control is implemented with a resistor values of 0 Ω to achieve a single ended slew rate of approximately 38 V/μs up to a value of 50 kΩ to achieve approximately 4 V/μs slew rate. For more information about slope control, refer to *Application and Implementation*.

The SN55HVD233-SP enters a low-current standby (listen-only) mode during which the driver is switched off and the receiver remains active if a high logic level is applied to pin 8. The local protocol controller reverses this low-current standby mode when it needs to transmit to the bus.

Feature Description (continued)

9.3.2 Loopback

A logic high on the loopback LBK pin 5 of the SN55HVD233-SP places the bus output and bus input in a high-impedance state. The remaining circuit remains active and available for driver-to-receiver loopback, self-diagnostic node functions without disturbing the bus. For more information on the loopback mode, refer to the *Application Information*.

Copyright © 2017, Texas Instruments Incorporated

Feature Description (continued)

9.3.3 CAN Bus States

The CAN bus has two states during powered operation of the device: dominant and recessive. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to V_{CC} / 2 through the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the D and R pins (see Figure 25 and Figure 26).

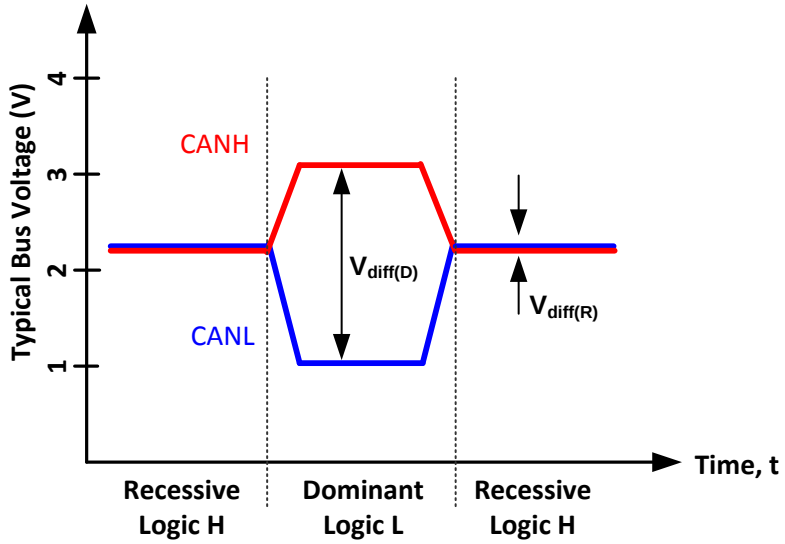


Figure 25. Bus States (Physical Bit Representation)

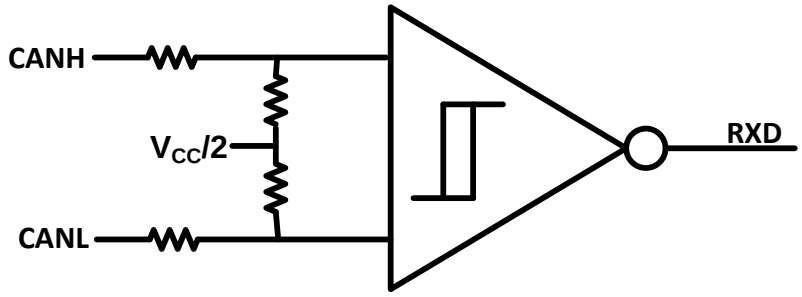


Figure 26. Simplified Recessive Common Mode Bias and Receiver

9.3.4 ISO 11898 Compliance of SN55HVD233-SP

9.3.4.1 Introduction

Many users value the low-power consumption of operating their CAN transceivers from a 3.3-V supply. However, some users are concerned about the interoperability with 5-V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

9.3.4.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single-ended output signal.

Copyright © 2017, Texas Instruments Incorporated

Feature Description (continued)

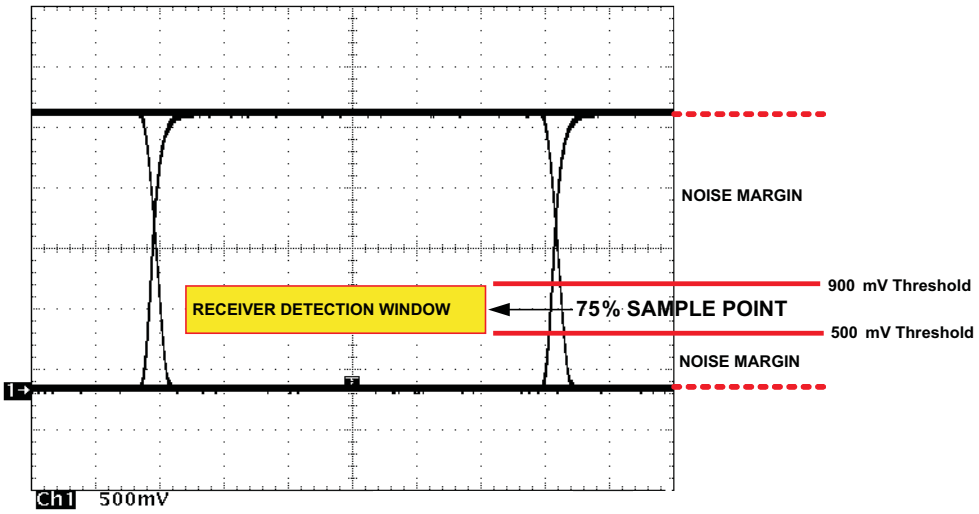


Figure 27. Typical SN55HVD233-SP Differential Output Voltage Waveform

The CAN driver creates the difference in voltage between CANH and CANL in the dominant state. The dominant differential output of the SN55HVD233-SP is greater than 1.5 V and less than 3 V across a 60-Ω load. The minimum required by ISO 11898 is 1.5 V and maximum is 3 V. These are the same limiting values for 5-V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state with less than 500 mV and a dominant state with more than 900 mV difference voltage on its bus inputs. The CAN receiver must do this with common-mode input voltages from –2 V to 7 V. The SN55HVD233-SP receiver meets these same input specifications as 5-V supplied receivers.

9.3.4.2.1 Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. The supply voltage of the CAN transceiver has nothing to do with noise. The SN55HVD233-SP driver lowers the common-mode output in a dominant bit by a couple hundred millivolts from that of most 5-V drivers. While this does not fully comply with ISO 11898, this small variation in the driver common-mode output is rejected by differential receivers and does not effect data, signal noise margins, or error rates.

9.3.4.3 Interoperability of 3.3-V CAN in 5-V CAN Systems

The 3.3-V supplied CAN transceivers are electrically interchangeable with 5-V CAN transceivers. The differential output is the same. The recessive common mode output is the same. The dominant common mode output voltage is a couple hundred millivolts lower than 5 V supplied drivers, while the receivers exhibit identical specifications as 5-V devices.

To help ensure the widest interoperability possible, the SN55HVD233-SP successfully passed the internationally recognized GIFT ICT conformance and interoperability testing for CAN transceivers. Electrical interoperability does not always assure interchangeability, however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure full interchangeability. Interchangeability is ensured with thorough equipment testing.

Copyright © 2017, Texas Instruments Incorporated

Feature Description (continued)

9.3.5 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold, the device turns off the CAN driver circuits thus blocking the D pin to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device. The CAN bus pins are high-impedance biased to recessive level during a thermal shutdown, and the receiver-to-R pin path remains operational.

9.4 Device Functional Modes

Table 3. Driver I/O

DRIVER(1)					
INPUTS			OUTPUTS		
D	LBK	RS	CANH	CANL	BUS STATE
X	X	> 0.75 V_{CC}	Z	Z	Recessive
L	L or open	≤ 0.33 V_{CC}	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	≤ 0.33 V_{CC}	Z	Z	Recessive

(1) H = High level; L = Low level; Z = High impedance; X = Irrelevant

Table 4. Receiver I/O

RECEIVER(1)			
INPUTS			OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	D	R
Dominant	V_{ID} ≥ 0.9 V	X	L
Recessive	V_{ID} ≤ 0.5 V or open	H or open	H
?	0.5 V < V_{ID} < 0.9 V	H or open	?
Dominant	V_{ID} ≥ 0.9 V	X	L
Recessive	V_{ID} ≤ 0.5 V or open	H	H
Recessive	V_{ID} ≤ 0.5 V or open	L	L
?	0.5 V < V_{ID} < 0.9 V	L	L

(1) H = High level; L = Low level; Z = High impedance; X = Irrelevant; ? = Indeterminate

Copyright © 2017, Texas Instruments Incorporated

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

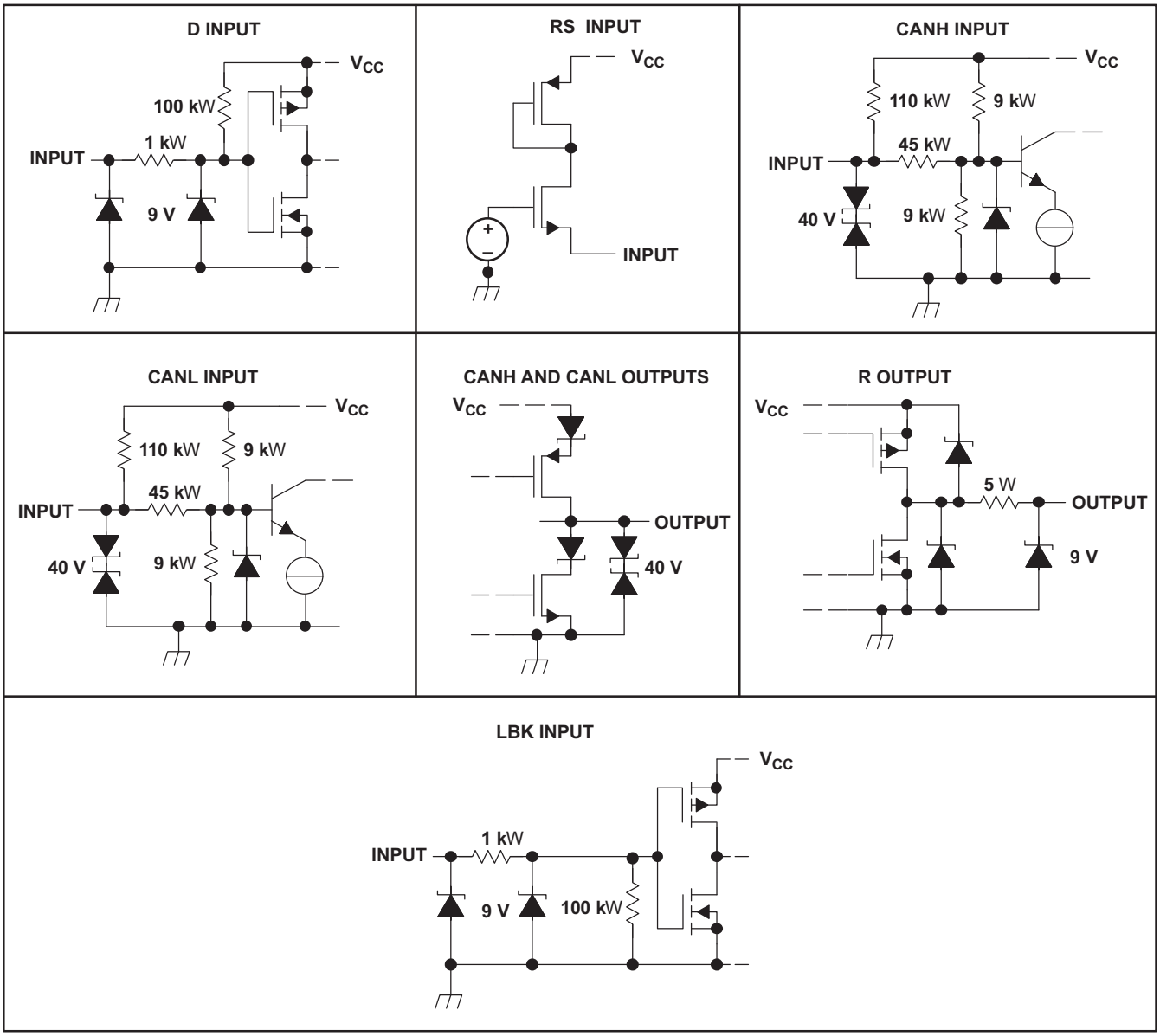
10.1.1 Diagnostic Loopback

The diagnostic loopback or internal loopback function of the SN55HVD233-SP is enabled with a high-level input on pin 7, LBK. This mode disables the driver output while keeping the bus pins biased to the recessive state. This mode also redirects the D data input (transmit data) through logic to the received data output (R), thus creating an internal loopback of the transmit-to-receive data path. This mimics the loopback that occurs normally with a CAN transceiver because the receiver loops back the driven output to the R (receive data) pin. This mode allows the host microprocessor to input and read back a bit sequence or CAN messages to perform diagnostic routines without disturbing the CAN bus. Figure 33 shows a typical CAN bus application.

If the LBK pin is not used, it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

Copyright © 2017, Texas Instruments Incorporated

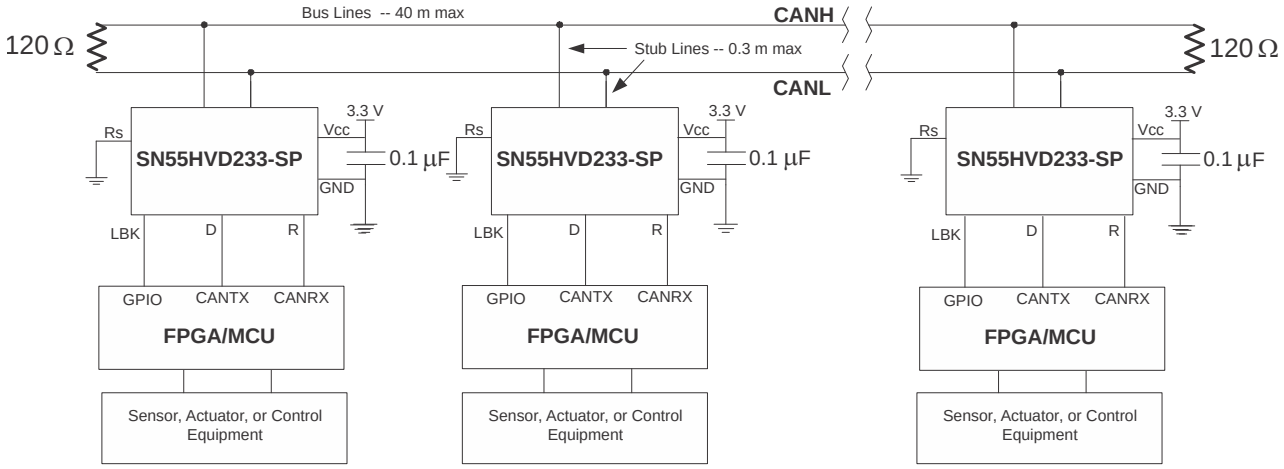
Application Information (continued)



Copyright © 2017, Texas Instruments Incorporated

Figure 28. Equivalent Input and Output Schematic Diagrams

10.2 Typical Application



Copyright © 2017, Texas Instruments Incorporated

Figure 29. Typical Application Schematic

10.2.1 Design Requirements

The High-Speed ISO 11898 Standard specifications are given for a maximum signaling rate of 1 Mbps with a bus length of 40 m and a maximum of 30 nodes. It also recommends a maximum unterminated stub length of 0.3 m. The cable is specified to be a shielded or unshielded twisted-pair with a 120-Ω characteristic impedance (ZO). The standard defines a single line of twisted-pair cable with the network topology as shown in Figure 29. It is terminated at both ends with 120-Ω resistors, which match the characteristic impedance of the line to prevent signal reflections. According to ISO 11898, placing RL on a node should be avoided because the bus lines lose termination if the node is disconnected from the bus.

10.2.2 Detailed Design Procedure

Table 5. Suggested Cable Length vs Signaling Rate

BUS LENGTH (m)	SIGNALING RATE (Mbps)
40	1
100	0.5
200	0.25
500	0.1
1000	0.05

Basically, the maximum bus length is determined by, or rather is a trade-off with the selected signaling rate as listed in Table 5.

A signaling rate decreases as transmission distance increases. While steady-state losses may become a factor at the longest transmission distances, the major factors limiting signaling rate as distance is increased are time varying. Cable bandwidth limitations, which degrade the signal transition time and introduce inter-symbol interference (ISI), are primary factors reducing the achievable signaling rate when transmission distance is increased.

For a CAN bus, the signaling rate is also determined from the total system delay – down and back between the two most distant nodes of a system and the sum of the delays into and out of the nodes on a bus with the typical 5 ns/m prop delay of a twisted-pair cable. Also, consideration must be given the signal amplitude loss due to resistance of the cable and the input resistance of the transceivers. Under strict analysis, skin effects, proximity to other circuitry, dielectric loss, and radiation loss effects all act to influence the primary line parameters and degrade the signal.

A conservative rule of thumb for bus lengths over 100 m is derived from the product of the signaling rate in Mbps and the bus length in meters, which should be less than or equal to 50.

Copyright © 2017, Texas Instruments Incorporated

Signaling Rate (Mbps) × Bus Length (m) ≤ 50. Operation at extreme temperatures should employ additional conservatism.

10.2.2.1 Slope Control

Adjust the rise and fall slope of the SN55HVD233-SP driver output by connecting a resistor from the RS (pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 30.

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value ranging from 0 Ω to achieve a ≈38 V/µs single ended slew rate, and up to 50 kΩ to achieve a ≈4 V/µs slew rate as displayed in Figure 31. Figure 32 shows typical driver output waveforms with slope control.

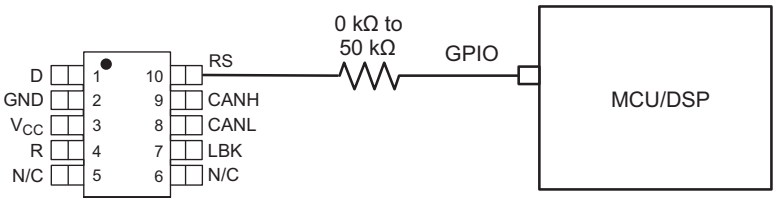


Figure 30. Slope Control/Standby Connection to a DSP

10.2.2.2 Standby

If a high-level input (> 0.75 V_{CC}) is applied to RS (pin 8), the circuit enters a low-current, listen-only standby mode during which the driver is switched off and the receiver remains active. The local controller can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage > 900-mV typical) occurs on the bus.

10.2.3 Application Curves

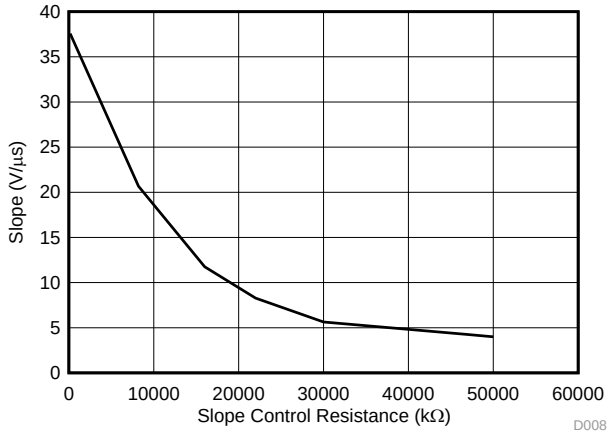


Figure 31. HVD233 Driver Output Signal Slope vs Slope Control Resistance Value

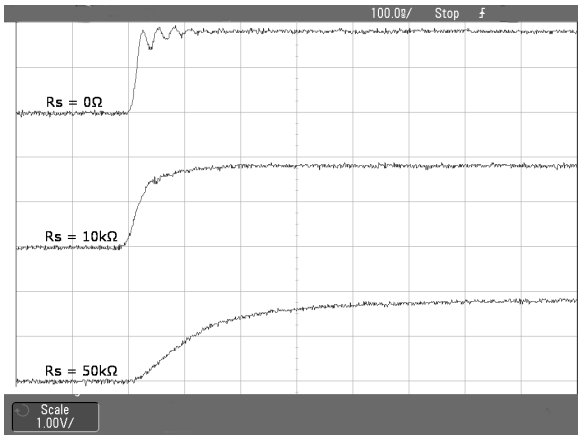


Figure 32. Typical SN55HVD233-SP 250-Kbps Output Pulse Waveforms With Slope Control

11 Power Supply Recommendations

TI recommends to have localized capacitive decoupling near device VCC pin to GND. Values of 4.7 µF at VCC pin and 10 µF, 1 µF, and 0.1 µF at supply have tested well on evaluation modules.

12 Layout

12.1 Layout Guidelines

Minimize stub length from node insertion to bus.

12.1.1 Bus Loading, Length, and Number of Nodes

The ISO11898 standard specifies up to 1-Mbps data rate, maximum bus length of 40 m, maximum drop line (stub) length of 0.3 m, and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898 standard. They made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet, and NMEA200.

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the SN55HVD233-SP CAN. ISO11898-2 specifies the driver differential output with a 60-Ω load (two 120-Ω termination resistors in parallel), and the differential output must be greater than 1.5 V. The SN55HVD233-SP is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common mode range of –2 to 7 V through a 330-Ω coupling network. This network represents the bus loading of 120 SN55HVD233-SP transceivers based on their minimum differential input resistance of 40 kΩ. Therefore, the SN55HVD233-SP supports up to 120 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node. For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets, and signal integrity; thus, a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes, and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO11898 CAN standard. Using this flexibility requires good network design.

12.1.2 CAN Termination

The ISO11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Use resistors equal to the characteristic impedance of the line to terminate both ends of the cable to prevent signal reflections. Keep unterminated drop lines (stubs) connecting nodes to the bus as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that it is not removed from the bus.

Copyright © 2017, Texas Instruments Incorporated

Layout Guidelines (continued)

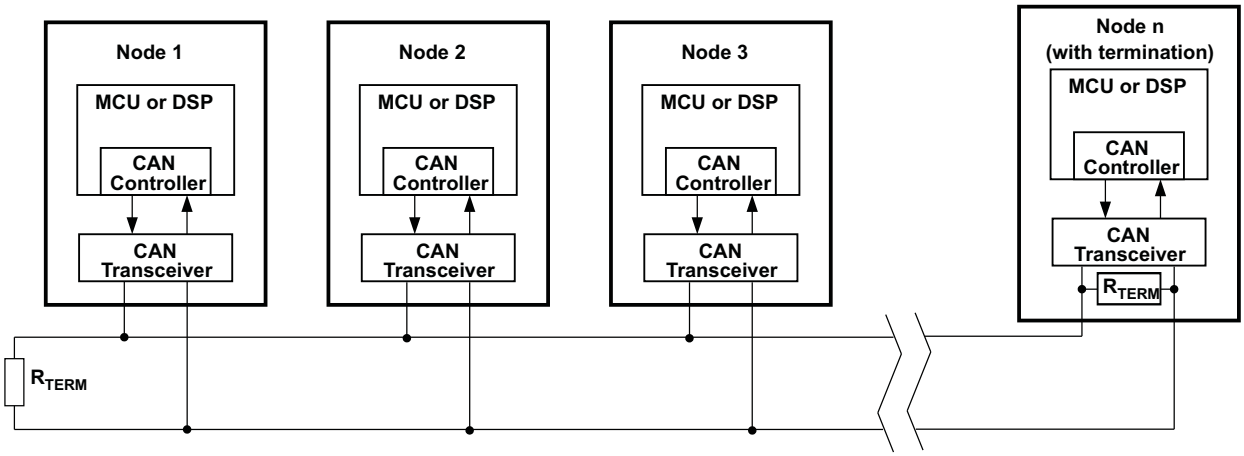


Figure 33. Typical CAN Bus

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then the user may use split termination (see Figure 34). Split termination uses two 60-Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Take care with the power ratings of the termination resistors used, especially for the worst-case condition (if a system power supply is shorted across the termination resistance to ground). In most cases, under the worst-case condition, much higher current passes through the termination resistance than the CAN transceiver's current limit.

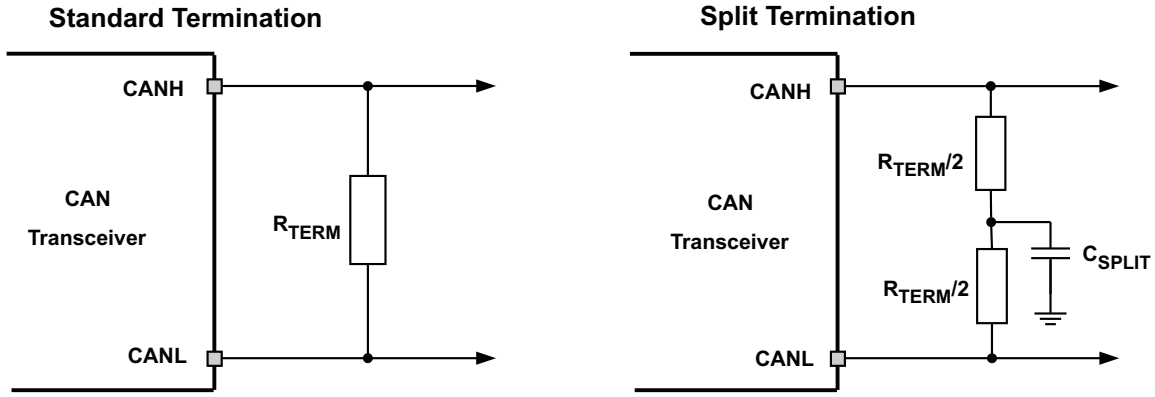


Figure 34. CAN Bus Termination Concepts

12.2 Layout Example

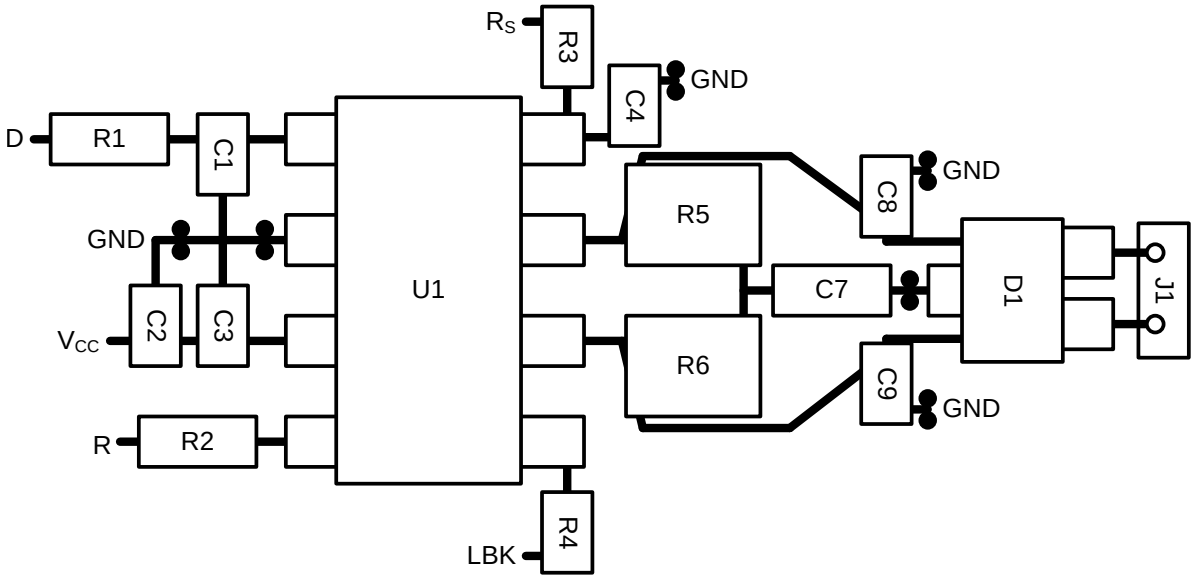


Figure 35. Board Layout Example

版权 © 2017, Texas Instruments Incorporated

13 器件和文档支持

13.1 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

13.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

版权 © 2017, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962L1420901VXC	Active	Production	CFP (HKX) | 8	25 | TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 125	L1420901VXC HVD233-SP
5962L1420901VXC.A	Active	Production	CFP (HKX) | 8	25 | TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 125	L1420901VXC HVD233-SP
HVD233HKX/EM	Active	Production	CFP (HKX) | 8	25 | TUBE	Yes	NIAU	N/A for Pkg Type	25 to 25	HVD233HKX/EM EVAL ONLY
HVD233HKX/EM.A	Active	Production	CFP (HKX) | 8	25 | TUBE	Yes	NIAU	N/A for Pkg Type	25 to 25	HVD233HKX/EM EVAL ONLY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

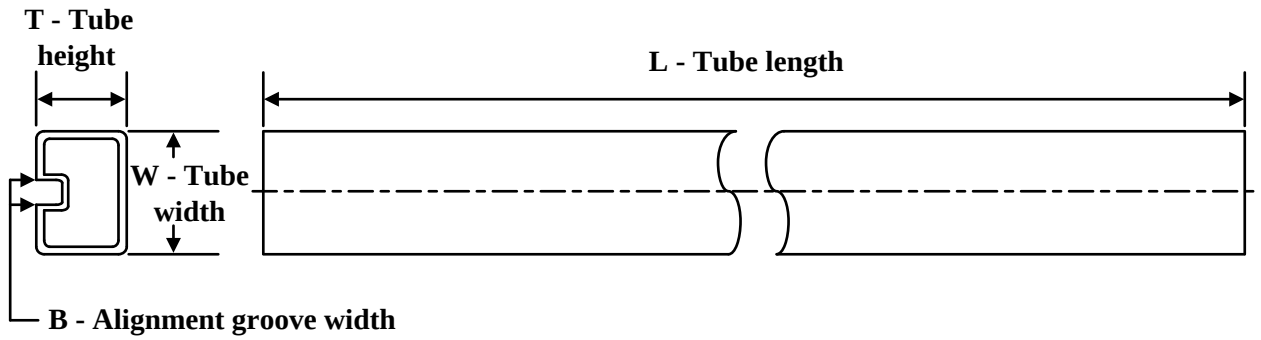
OTHER QUALIFIED VERSIONS OF SN55HVD233-SP :

- Catalog : SN55HVD233-SEP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962L1420901VXC	HKX	CFP (HSL)	8	25	506.98	26.16	6220	NA
5962L1420901VXC.A	HKX	CFP (HSL)	8	25	506.98	26.16	6220	NA
HVD233HKX/EM	HKX	CFP (HSL)	8	25	506.98	26.16	6220	NA
HVD233HKX/EM.A	HKX	CFP (HSL)	8	25	506.98	26.16	6220	NA

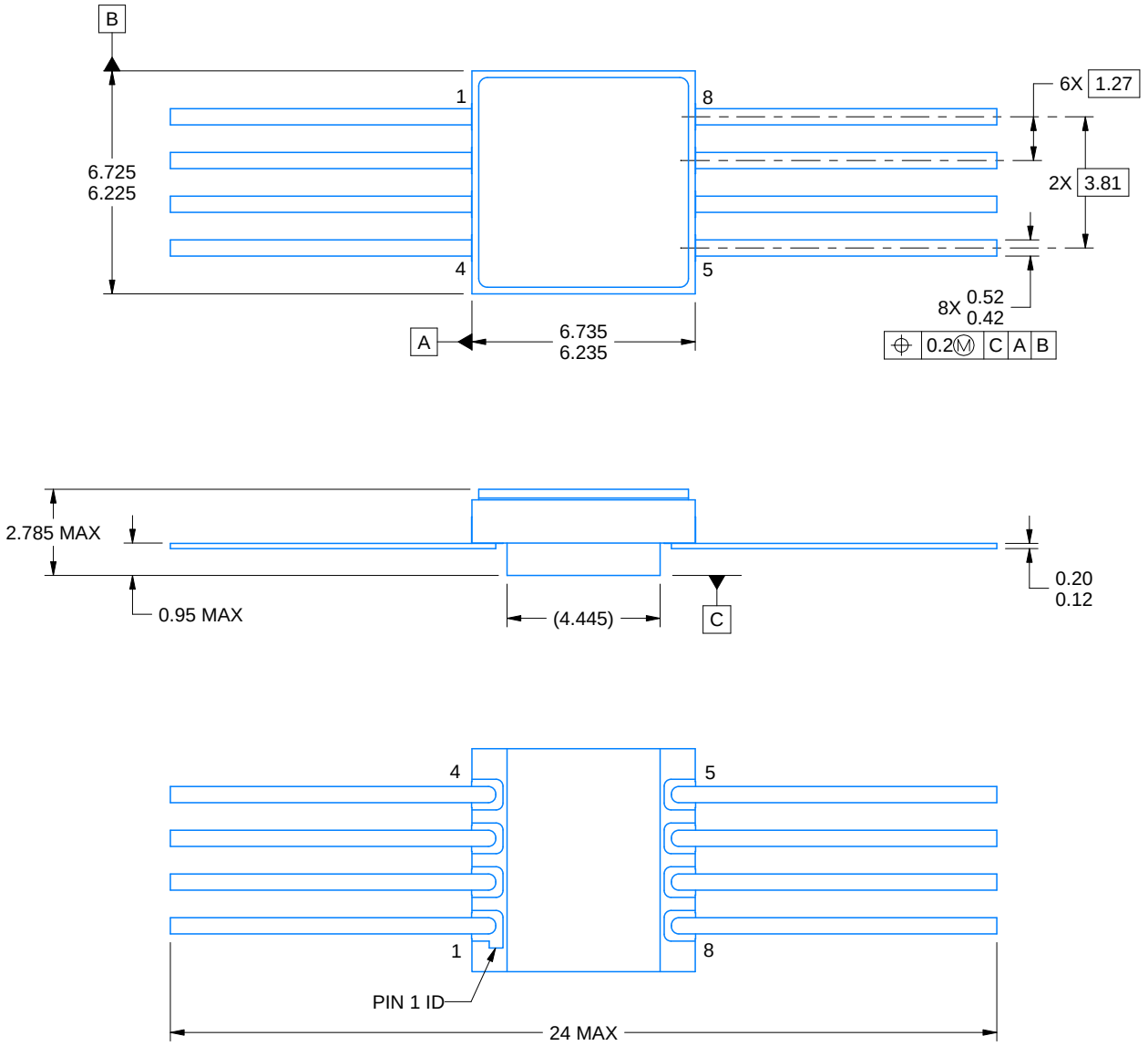


PACKAGE OUTLINE

HKX0008A

CFP - 2.785 mm max height

CERAMIC FLATPACK



4223439/C 08/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The leads are gold plated.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月