

# SN54ALS243A, SN74ALS243A QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS069B – DECEMBER 1982 – REVISED DECEMBER 1994

- Two-Way Asynchronous Communication Between Data Buses
- pnp Inputs Reduce dc Loading
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

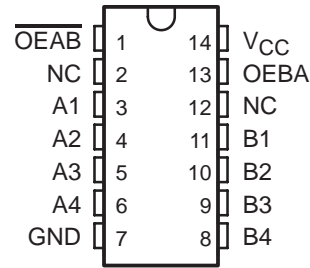
## description

These quadruple bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEBA and OEAB) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

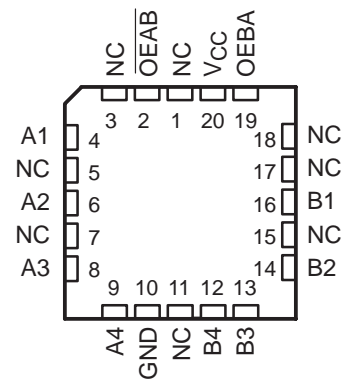
The dual-enable configuration gives the quadruple bus transceivers the capability to store data by simultaneously enabling OEBA and OEAB. Each output reinforces its input in this transceiver configuration. When both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (eight in all) retain their states. The 4-bit codes appearing on the two sets of buses are identical.

The SN54ALS243A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS243A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS243A . . . J PACKAGE  
SN74ALS243A . . . D OR N PACKAGE  
(TOP VIEW)



SN54ALS243A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

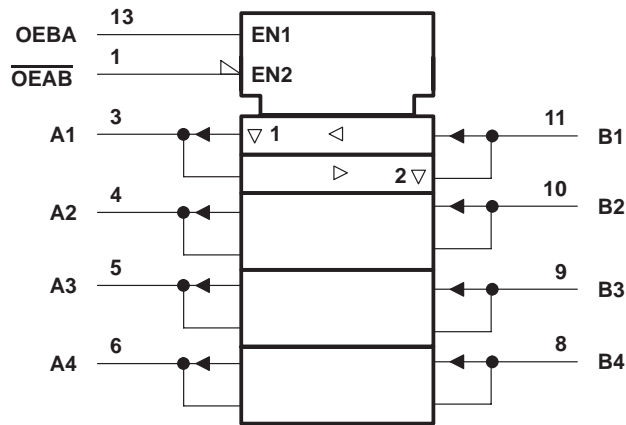
FUNCTION TABLE

INPUTS		FUNCTION
OEAB	OEBA	
L	L	A to B
H	H	B to A
H	L	Isolation
L	H	Latch A and B (A = B)

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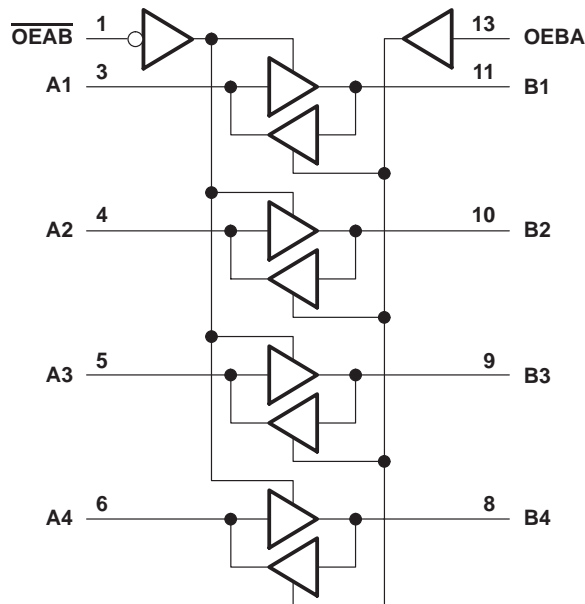
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS243A	–55°C to 125°C
SN74ALS243A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54ALS243A			SN74ALS243A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			12			24	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

# SN54ALS243A, SN74ALS243A QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS243A		SN74ALS243A		UNIT
				MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA		−1.2		−1.2		V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = −0.4 mA		V <sub>CC</sub> − 2		V <sub>CC</sub> − 2		V
		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = −3 mA	2.4	3.2	2.4	3.2	
			I <sub>OH</sub> = −12 mA	2				
			I <sub>OH</sub> = −15 mA			2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4	V
			I <sub>OL</sub> = 24 mA			0.35	0.5	
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 7 V	0.1		0.1		mA
	A or B ports		V <sub>I</sub> = 5.5 V	0.1		0.1		
I <sub>IH</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V	20		20		μA	
	A or B ports‡		20		20			
I <sub>IL</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V	−0.1		−0.1		mA	
	A or B ports‡		−0.1		−0.1			
I <sub>O</sub> §		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	−20	−112	−30	−112	mA	
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V	Outputs high	15	30	15	25	mA
			Outputs low	20	35	20	30	
			Outputs disabled	21	37	21	32	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS243A		SN74ALS243A		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	4	15	4	11	ns
t <sub>PHL</sub>			4	15	4	11	
t <sub>PZH</sub>	$\overline{\text{OEAB}}$	B	7	25	7	20	ns
t <sub>PZL</sub>			7	25	7	20	
t <sub>PHZ</sub>	$\overline{\text{OEAB}}$	B	2	16	2	14	ns
t <sub>PLZ</sub>			3	27	3	22	
t <sub>PZH</sub>	OEBA	A	7	25	7	20	ns
t <sub>PZL</sub>			7	25	7	20	
t <sub>PHZ</sub>	OEBA	A	2	16	2	14	ns
t <sub>PLZ</sub>			3	27	3	22	

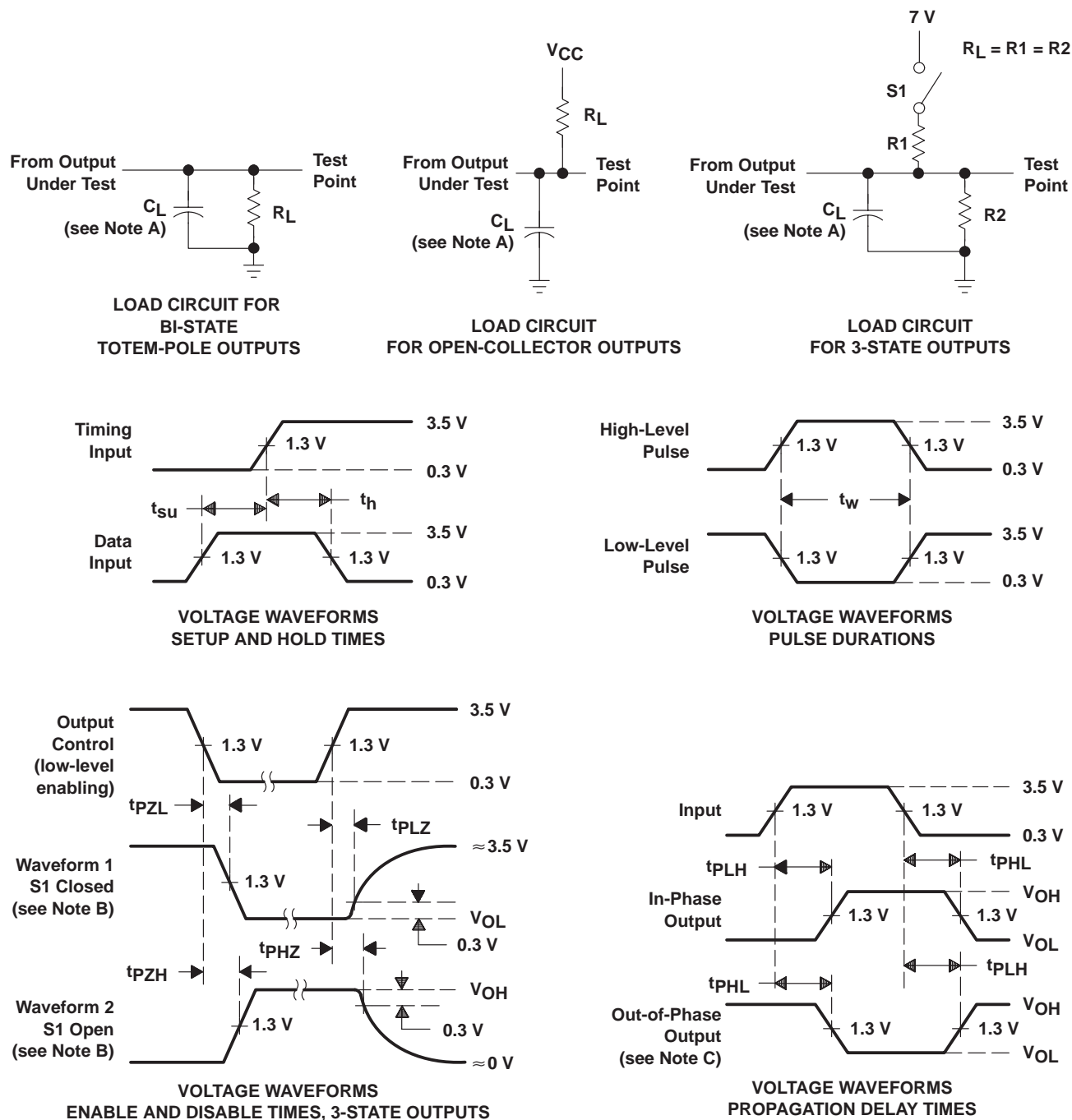
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# SN54ALS243A, SN74ALS243A QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">84013022A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84013022A SNJ54ALS 243AFK
<a href="#">SNJ54ALS243AFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84013022A SNJ54ALS 243AFK
SNJ54ALS243AFK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84013022A SNJ54ALS 243AFK

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

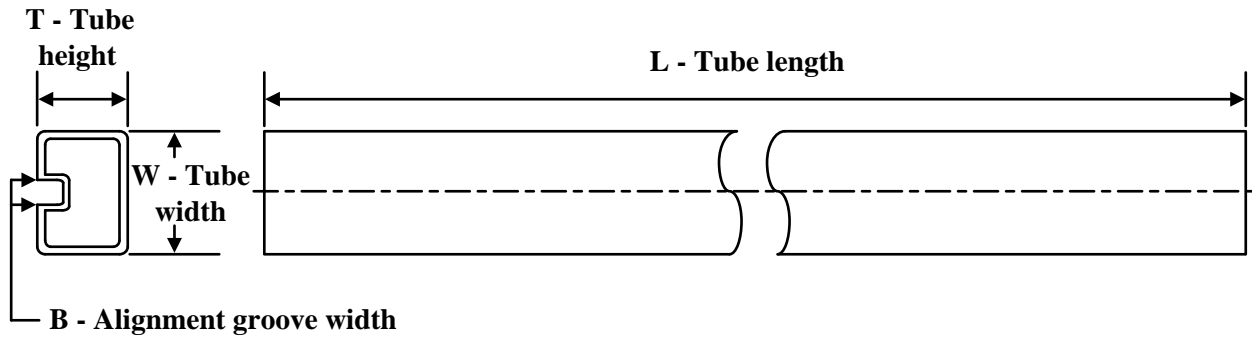
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84013022A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS243AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS243AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

## GENERIC PACKAGE VIEW

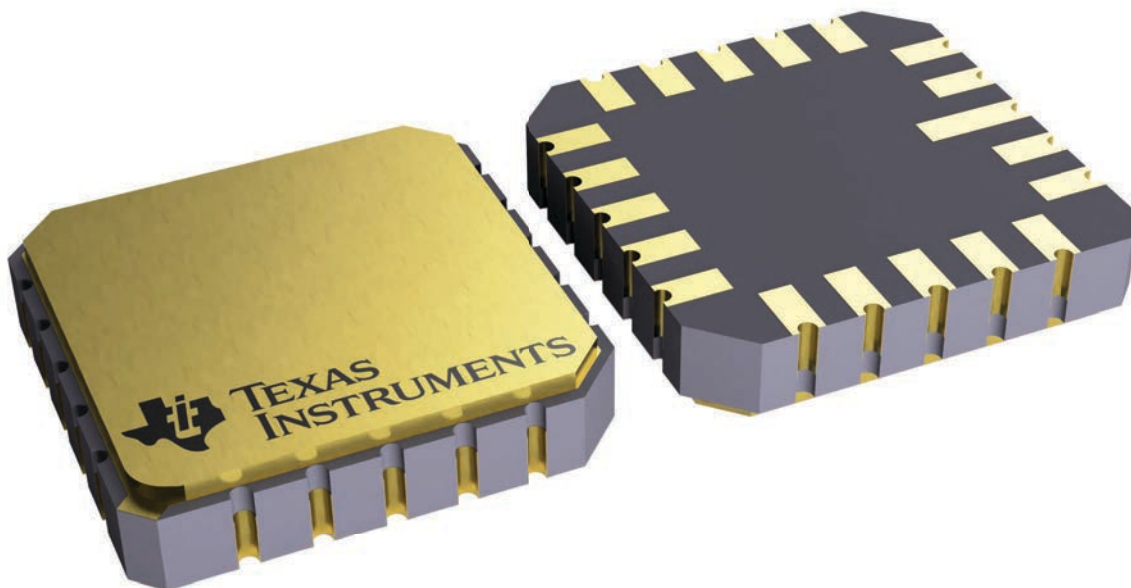
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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