SNx4AHCT00 四路 2 输入正与非门

1 特性

- 工作电压范围为 4.5 V 至 5.5V
- 低功耗，I_{CC} 最大值为 10μA
- 5 V 下的输出驱动为 ±8mA
- 输入兼容 TTL 电压
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 启用或禁用数字信号
- 控制指示灯 LED
- 通信模块和系统控制器之间的转换

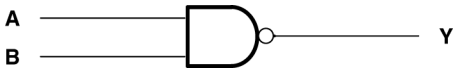
3 说明

’AHCT00 器件以正逻辑执行布尔函数 $Y = \overline{A \cdot B}$ 或 $Y = \overline{A} + \overline{B}$。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
SN54AHCT00	J（CDIP，14）	19.56mm × 6.67mm
	W（CFP，14）	9.21mm × 5.97mm
	FK（LCCC，20）	8.89mm × 8.89mm
SN74AHCT00	D（SOIC，14）	8.65mm × 3.91mm
	DB（SSOP，14）	6.20mm × 5.30mm
	DGV（TVSOP，14）	3.60mm × 4.40mm
	N（PDIP，14）	19.30mm x 6.35mm
	NS（SOP，14）	10.30mm × 5.30mm
	RGY（QFN，14）	3.50mm × 3.50mm
	BQA（WQFN，14）	3.00mm x 2.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图，每个逻辑门（正逻辑）

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision K (July 2003) to Revision L (May 2023)	Page
• 更新了*特性* 部分	1
• 更新了*应用* 部分	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 添加了 BQA (WQFN) 封装信息	1
• 添加了*封装信息* 表	1
• Added the *Test and SI* table	8
• Added the *Detailed Description* sections	9
• Added the *Application and Implementation* sections	11

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5 Pin Configuration and Functions

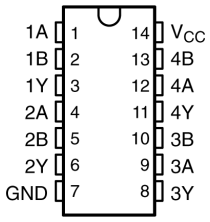


图 5-1. SN54AHCT00 J or W Package, 14-Pin CDIP or CFP SN74AHCT00 D, DB, DGV, N, NS, or PW Package, 14-Pin SOIC, SSOP, TVSOP, PDIP, SOP, or TSSOP (Top View)

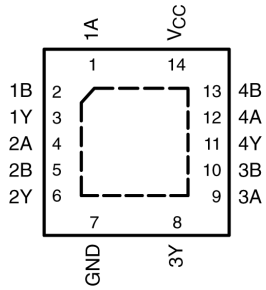


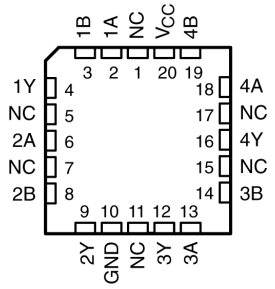
图 5-2. SN74AHCT00 RGY, BQA Package, 14-Pin QFN, WQFN (Transparent Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1, Input A
1B	2	I	Channel 1, Input B
1Y	3	O	Channel 1, Output Y
2A	4	I	Channel 2, Input A
2B	5	I	Channel 2, Input B
2Y	6	O	Channel 2, Output Y
3A	9	O	Channel 3, Output Y
3B	10	I	Channel 3, Input A
3Y	8	I	Channel 3, Input B
4A	12	O	Channel 4, Output Y
4B	13	I	Channel 4, Input A
4Y	11	I	Channel 4, Input B
GND	7	G	Ground
V_{CC}	14	P	Positive Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power Supply, G = Ground.

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NC – No internal connection

图 5-3. SN54AHCT00 FK Package, 14-Pin LCCC (Top View)

表 5-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	2	I	Channel 1, Input A
1B	3	I	Channel 1, Input B
1Y	4	O	Channel 1, Output Y
2A	6	I	Channel 2, Input A
2B	8	I	Channel 2, Input B
2Y	9	O	Channel 2, Output Y
3A	13	O	Channel 3, Output Y
3B	14	I	Channel 3, Input A
3Y	12	I	Channel 3, Input B
4A	18	O	Channel 4, Output Y
4B	19	I	Channel 4, Input A
4Y	16	I	Channel 4, Input B
NC	1, 5, 7, 11, 15, 17	—	No Connection
GND	10	G	Ground
V_{CC}	20	P	Positive Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power Supply, G = Ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	7	V
V_I	Input voltage range(2)		– 0.5	7	V
V_O	Output voltage range(2)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5 V		-20	mA
I_{OK}	Output clamp current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1))

		SN54AHCT00		SN74AHCT00		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		- 8		- 8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	- 55	125	- 40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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6.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT00								UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP	NS (SOP)	PW (TSSOP)	RGY (VQFN)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	96	127	80	76	113	47	88.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A= 25°C			SN54AHCT00		SN74AHCT00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = -50 µA		4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = -8 mA			3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 µA		4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44		0.44	
I_I	V_I = 5.5 V or GND		0 V to 5.5 V			±0.1		±1[1]		±1	µA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	5.5 V			2		20		20	µA
ΔI_{CC} [2]	One input at 3.4 V, Other inputs at V_{CC} or GND		5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND		5 V		2	10				10	pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A= 25°C			SN54AHCT00		SN74AHCT00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF		5[1]	6.9[1]	1[1]	8[1]	1	8	ns
t_{PHL}					5[1]	6.9[1]	1[1]	8[1]	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	1	9	ns
t_{PHL}					5.5	7.9	1	9	1	9	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see [1])

PARAMETER		SN74AHCT00			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.4	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

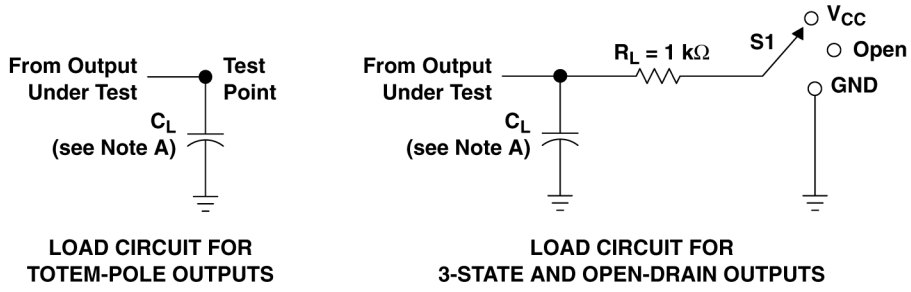
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6.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

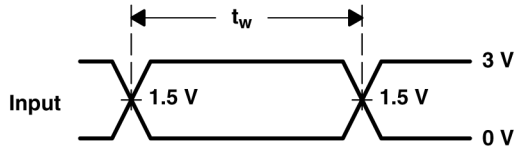
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	10.5	pF

7 Parameter Measurement Information

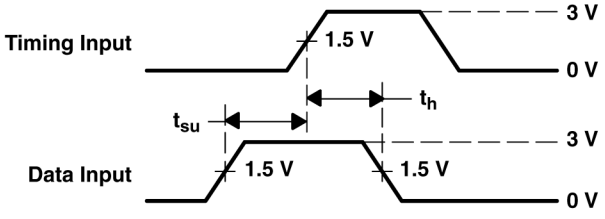


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

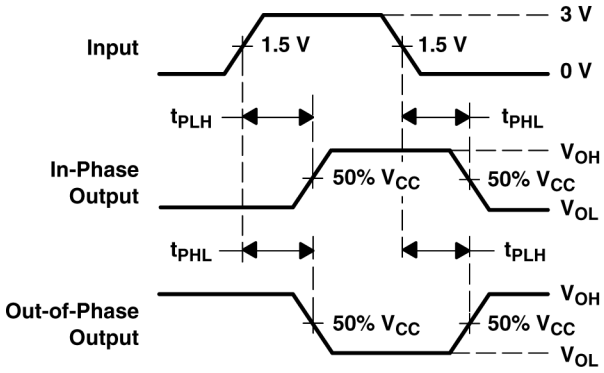
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



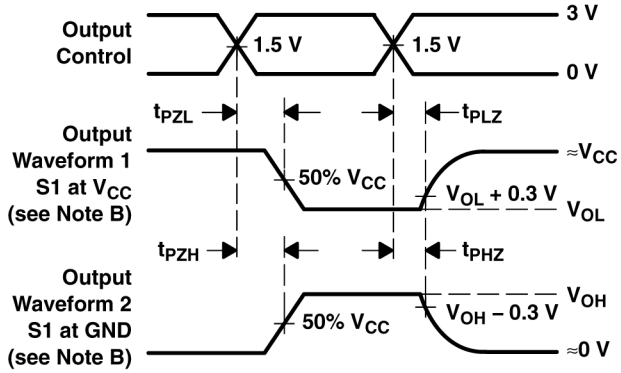
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω, t_r ⩽3 ns, t_f ⩽ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

表 7-1. Test and SI

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

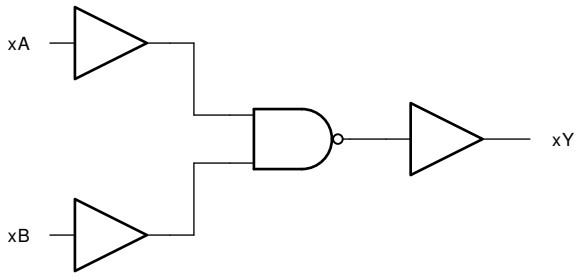
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8 Detailed Description

8.1 Overview

This device contains four independent 2-input NAND Gates. Each gate performs the Boolean function $Y = \overline{A \bullet B}$ in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 TTL 兼容型 CMOS 输入

此器件包括 TTL 兼容型 CMOS 输入。这些输入专门设计为通过降低的输入电压阈值与 TTL 逻辑器件连接。

TTL 兼容型 CMOS 输入为高阻抗，通常建模为与输入电容并联的电阻器，如*电气特性* 中所示。最坏情况下的电阻是根据*绝对最大额定值* 中给出的最大输入电压和*电气特性* 中给出的最大输入漏电流，使用欧姆定律 (R = V ÷ I) 计算得出的。

TTL 兼容型 CMOS 输入要求输入信号在有效逻辑状态之间快速转换，如*建议运行条件* 表中的输入转换时间或速率所定义。不符合此规范将导致功耗过大并可能导致振荡。有关更多详细信息，请参阅 *CMOS 输入缓慢变化或悬空的影响* 应用报告。

在运行期间，任何时候都不要让 TTL 兼容型 CMOS 输入悬空。未使用的输入必须在 V_{CC} 或 GND 端接。如果系统不会一直主动驱动输入，可以添加上拉或下拉电阻器，以在这些时间段提供有效的输入电压。电阻值将取决于多种因素；但建议使用 10kΩ 电阻器，这通常可以满足所有要求。

8.3.3 Clamp Diode Structure

As 图 8-1 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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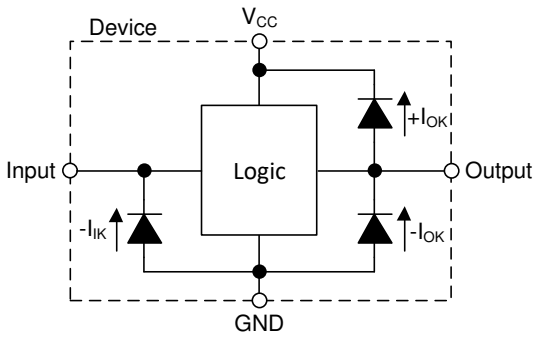


图 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 8-1. Function Table (Each Gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

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9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

In this application, two 2-input NAND gates are used to create an active-low SR latch as shown in 图 9-1. The two additional gates can be used for a second SR latch, or the inputs can be grounded and both channels left unused.

The AHCT00 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the $\overline{R}$ input which returns the Q output back to LOW.

The inputs of this active-low SR latch can often be driven by open-drain outputs which can produce slow input transition rates when they transition from LOW to Hi-Z. This makes the AHCT00 ideal for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

9.2 Typical Application

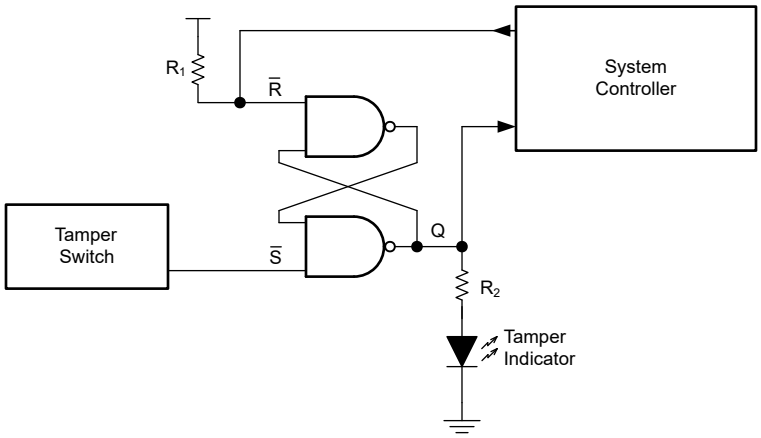


图 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

9.2.1.1 电源注意事项

确保所需电源电压在*建议运行条件*中规定的范围内。电源电压按照*电气特性*部分所述设置器件的电气特性。

正电压电源必须能够提供的电流等于 AHCT00 所有输出端拉出的总电流加上最大静态电源电流 I_{CC}（在*电气特性*中列出）以及开关所需的任何瞬态电流之和。逻辑器件只能拉出与正电源提供的大小相同的电流。确保不要超过*绝对最大额定值*中列出的通过 V_{CC} 的最大总电流。

接地端必须能够灌入的电流等于 AHCT00 所有输出端灌入的总电流加上最大电源电流 I_{CC}（在*电气特性*中列出）以及开关所需的任何瞬态电流之和。逻辑器件只能灌入其所接的地可灌入的大小相同的电流。确保不要超过*绝对最大额定值*中列出的通过 GND 的最大总电流。

AHCT00 可以驱动总电容小于或等于 50pF 的负载，同时仍满足所有数据表规格。可以施加更大的容性负载；但建议不要超过 50pF。

AHCT00 可以驱动由 $R_L \geq V_O/I_O$ 描述的总电阻负载，输出电压和电流在*电气特性*表中用 V_{OH} 和 V_{OL} 定义。在高电平状态下输出时，公式中的输出电压定义为测量的输出电压与 V_{CC} 引脚处的电源电压之间的差值。

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总功耗可以使用 *CMOS 功耗与 Cpd 计算*中提供的信息进行计算。

可以使用*标准线性和逻辑 (SLL) 封装和器件的热特性*中提供的信息计算热增量。

CAUTION

绝对最大额定值 中列出的最高结温 $T_{J(max)}$ 是防止损坏器件的附加限制。请勿违反*绝对最大额定值* 中列出的任何值。提供这些限制是为了防止损坏器件。

9.2.1.2 输入注意事项

输入信号必须超过 $V_{IL(max)}$ 才能被视为逻辑低电平，超过 $V_{IH(min)}$ 才能被视为逻辑高电平。不要超过*绝对最大额定值* 中的最大输入电压范围。

未使用的输入必须端接至 V_{CC} 或地。如果输入完全不使用，则可以直接端接未使用的输入，如果有时要使用输入，但并非始终使用，则可以使用上拉或下拉电阻器连接输入。上拉电阻用于默认高电平状态，下拉电阻用于默认低电平状态。控制器的驱动电流、进入 AHCT00 的漏电流（如*电气特性* 中所规定）以及所需输入转换率会限制电阻大小。由于这些因素，通常使用 10kΩ 的电阻值。

AHCT00 具有 CMOS 输入，因此需要进行快速输入转换才能正常工作，如*建议运行条件* 表中所定义。缓慢的输入转换会导致振荡、额外的功耗以及器件可靠性下降。

有关此器件的输入的附加信息，请参阅*特性描述* 部分。

9.2.1.3 输出注意事项

正电源电压用于产生输出高电平电压。根据*电气特性* 中 V_{OH} 规范的规定，从输出端汲取电流将降低输出电压。接地电压用于产生输出低电平电压。根据*电气特性* 中 V_{OL} 规范的规定，向输出端灌入电流将提高输出电压。

可能处于相反状态的推挽输出始终不应直接连接在一起，即使时间很短也不例外。否则可能会导致电流过大并损坏器件。

同一器件内具有相同输入信号的两个通道可以并联，以获得额外的输出驱动强度。

未使用的输出可以保持悬空状态。不要将输出直接连接到 V_{CC} 或地。

有关此器件的输出的附加信息，请参阅*特性描述* 部分。

9.2.2 详细设计过程

1. 在 V_{CC} 至 GND 之间添加一个去耦电容器。此电容器需要在物理上靠近器件，在电气上靠近 V_{CC} 和 GND 引脚。*布局* 部分中显示了示例布局。
2. 确保输出端的容性负载 ≤ 50pF。这不是硬性限制；但是它将确保更佳的性能。这可以通过从 AHCT00 向一个或多个接收器件提供适当大小的短布线来实现。
3. 确保输出端的电阻负载大于 $(V_{CC}/I_{O(max)})$ Ω。这将确保不会违反*绝对最大额定值* 中的最大输出电流。大多数 CMOS 输入具有以 MΩ 为单位的电阻负载；远大于之前计算的最小值。
4. 逻辑门很少关注热问题；然而，可以使用应用报告 *CMOS 功耗与 Cpd 计算* 中提供的步骤计算功耗和热增量。

9.2.3 Application Curves

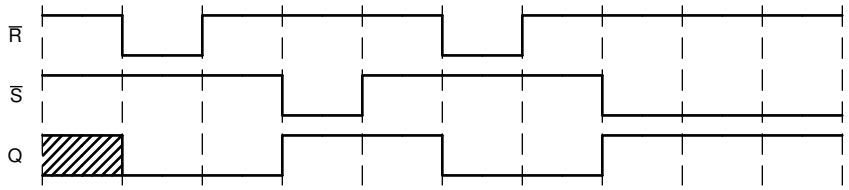


图 9-2. Application Timing Diagram

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9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Layout Example*.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9.4.2 Layout Example

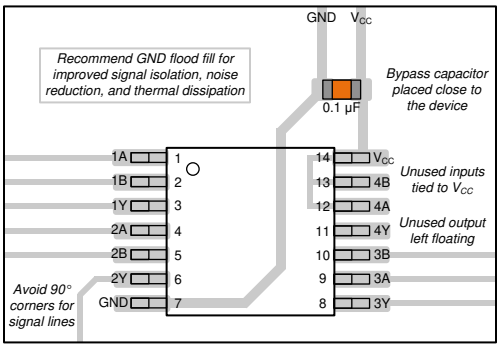


图 9-3. Example Layout for the AHCT00

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9682301Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682301Q2A SNJ54AHCT00FK
5962-9682301QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682301QCA SNJ54AHCT00J
5962-9682301QDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682301QDA SNJ54AHCT00W
SN74AHCT00BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHCT00
SN74AHCT00BQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHCT00
SN74AHCT00D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	AHCT00
SN74AHCT00DBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB00
SN74AHCT00DBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB00
SN74AHCT00DGVR	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB00
SN74AHCT00DGVR.A	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB00
SN74AHCT00DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT00
SN74AHCT00DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT00
SN74AHCT00DRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT00
SN74AHCT00N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCT00N
SN74AHCT00N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCT00N
SN74AHCT00NE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCT00N
SN74AHCT00NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT00
SN74AHCT00NSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT00
SN74AHCT00PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	HB00
SN74AHCT00PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HB00
SN74AHCT00PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB00
SN74AHCT00RGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HB00
SN74AHCT00RGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HB00

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHCT00FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682301Q2A SNJ54AHCT 00FK
SNJ54AHCT00FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682301Q2A SNJ54AHCT 00FK
SNJ54AHCT00J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682301QCA SNJ54AHCT00J
SNJ54AHCT00J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682301QCA SNJ54AHCT00J
SNJ54AHCT00W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682301QDA SNJ54AHCT00W
SNJ54AHCT00W.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9682301QDA SNJ54AHCT00W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54AHCT00, SN74AHCT00 :

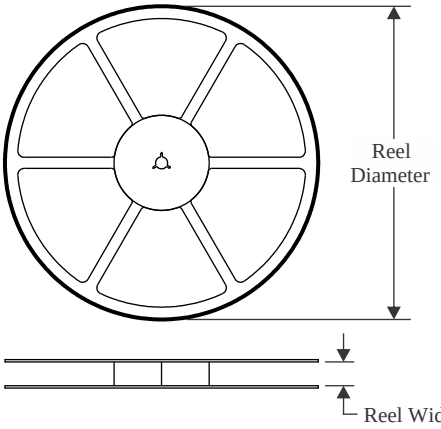
- Catalog : SN74AHCT00
- Enhanced Product : SN74AHCT00-EP, SN74AHCT00-EP
- Military : SN54AHCT00

NOTE: Qualified Version Definitions:

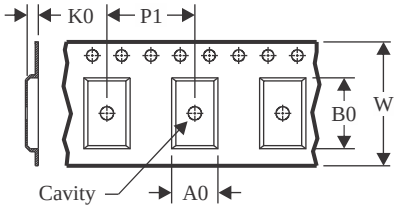
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

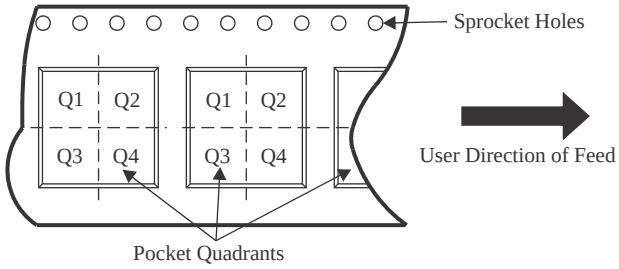


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

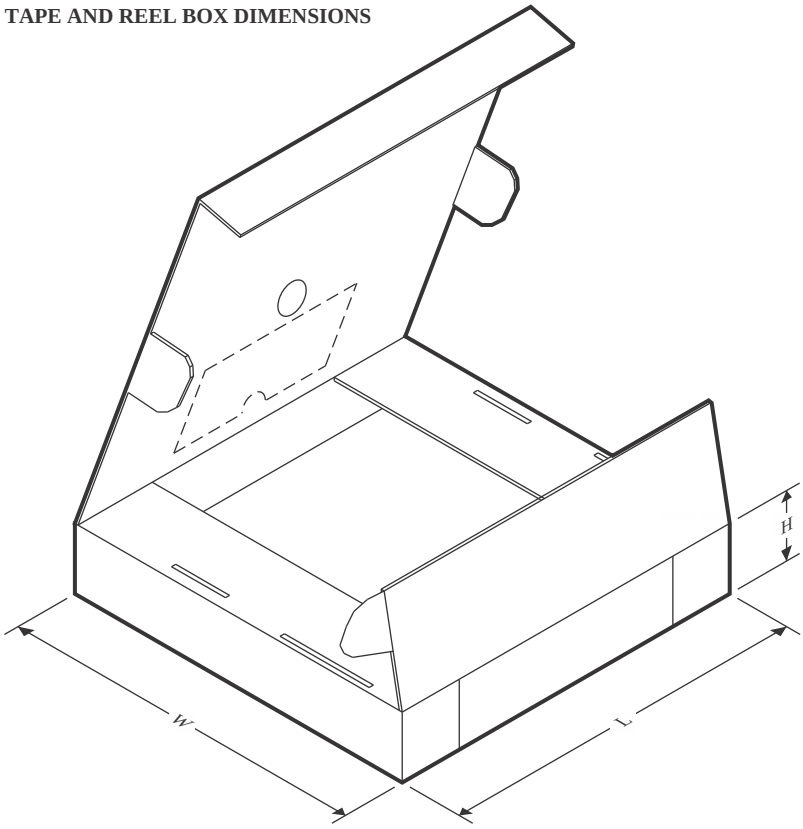
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT00BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHCT00DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT00DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT00DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCT00NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHCT00PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT00RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

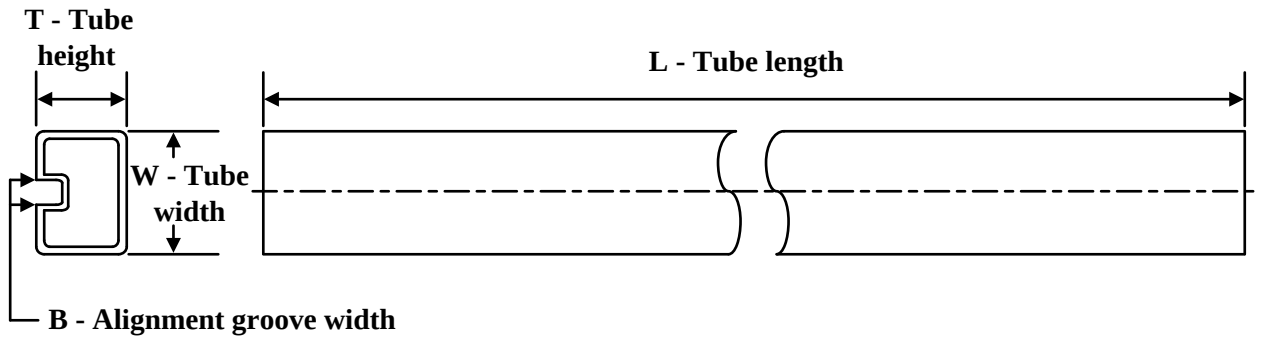
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT00BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHCT00DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHCT00DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHCT00DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHCT00NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHCT00PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT00RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

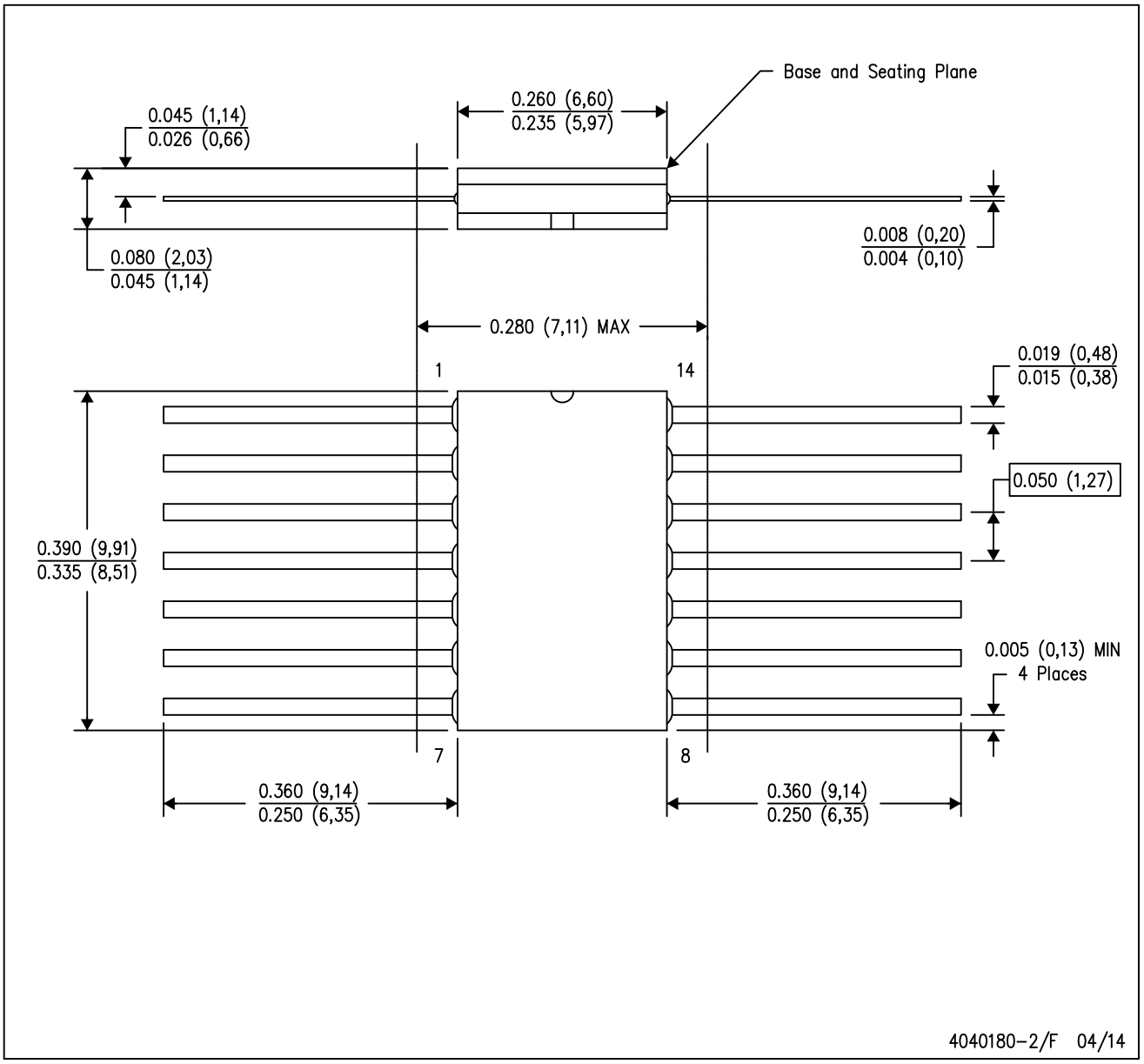
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9682301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9682301QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHCT00N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT00N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT00N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT00N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT00NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT00NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHCT00FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT00FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT00W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54AHCT00W.A	W	CFP	14	25	506.98	26.16	6220	NA

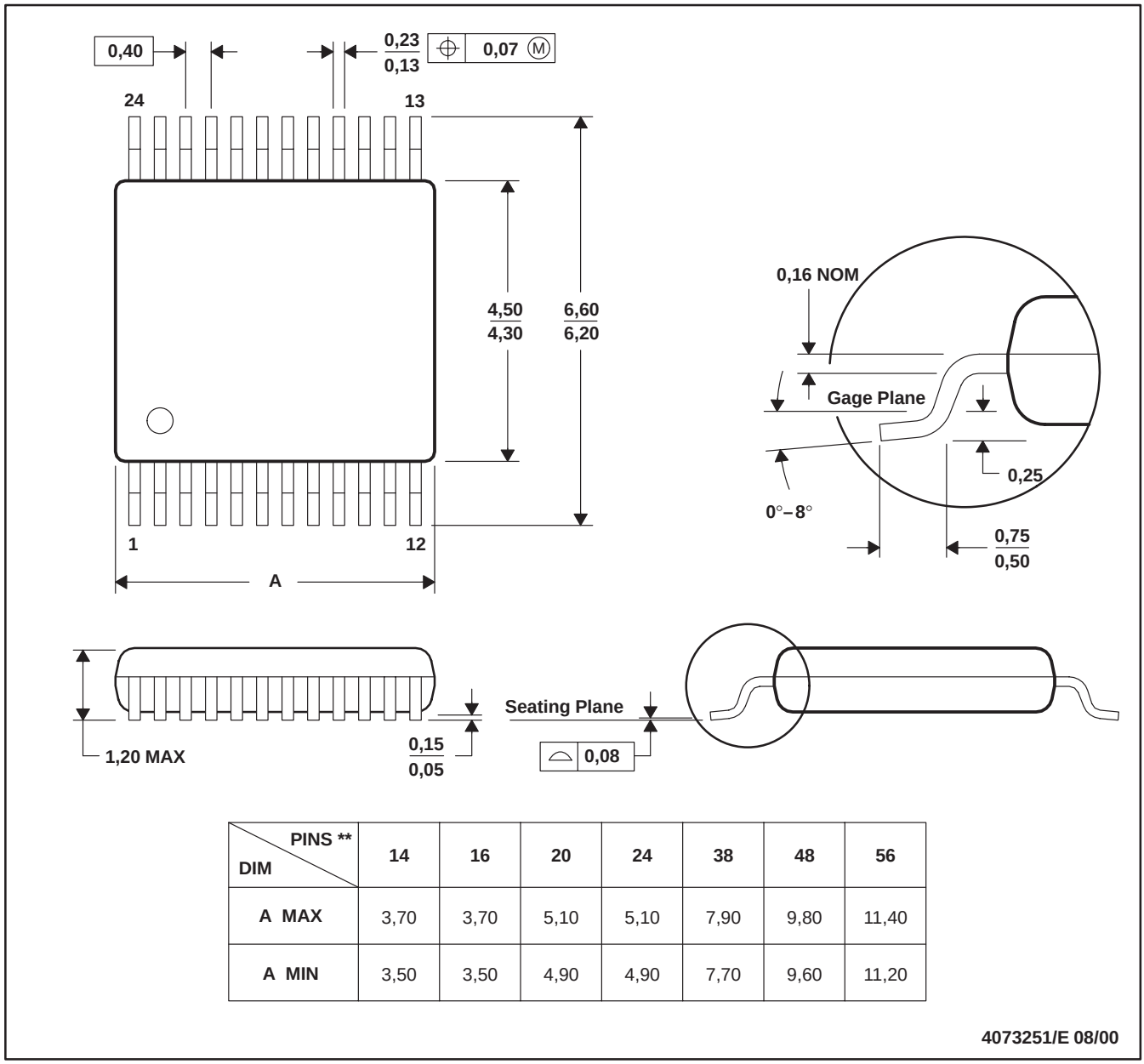
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

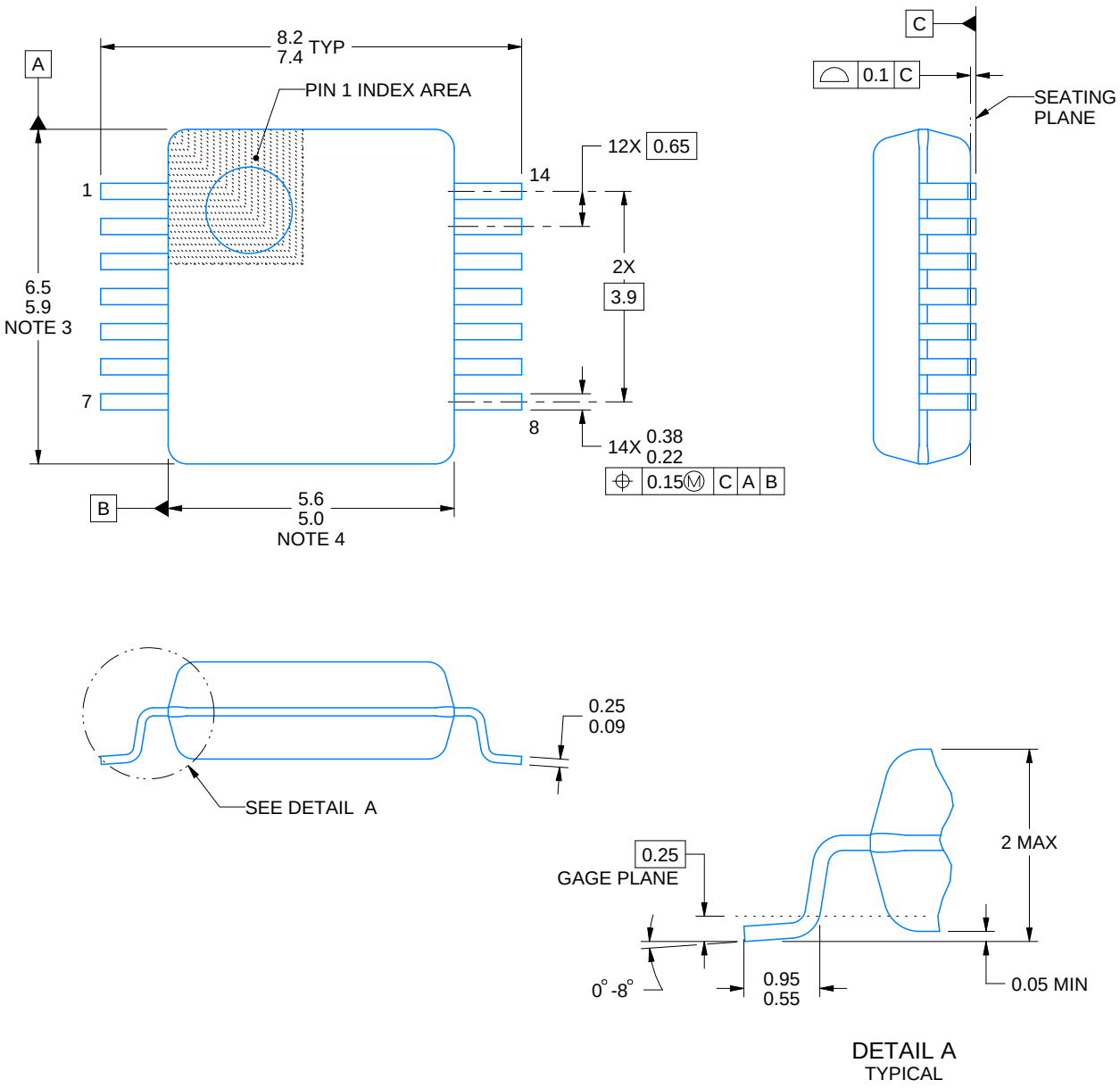
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

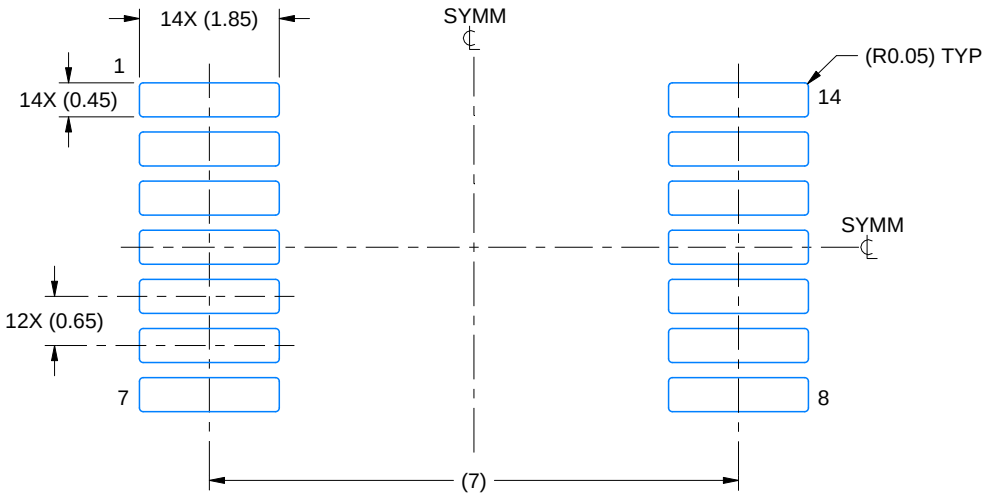
SMALL OUTLINE PACKAGE



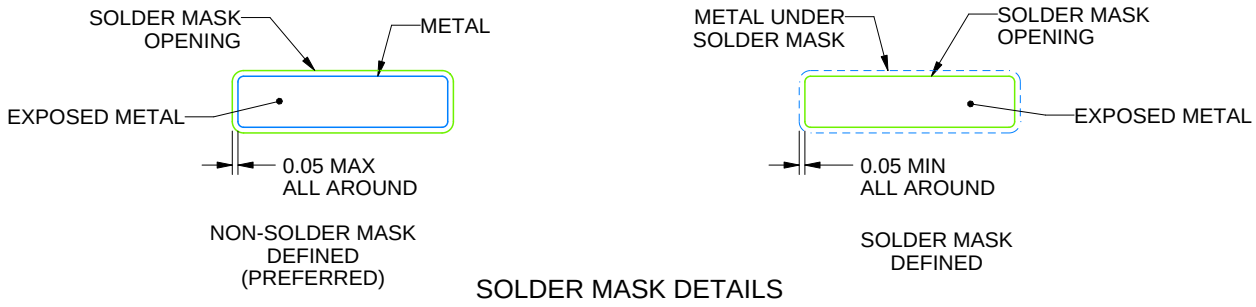
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

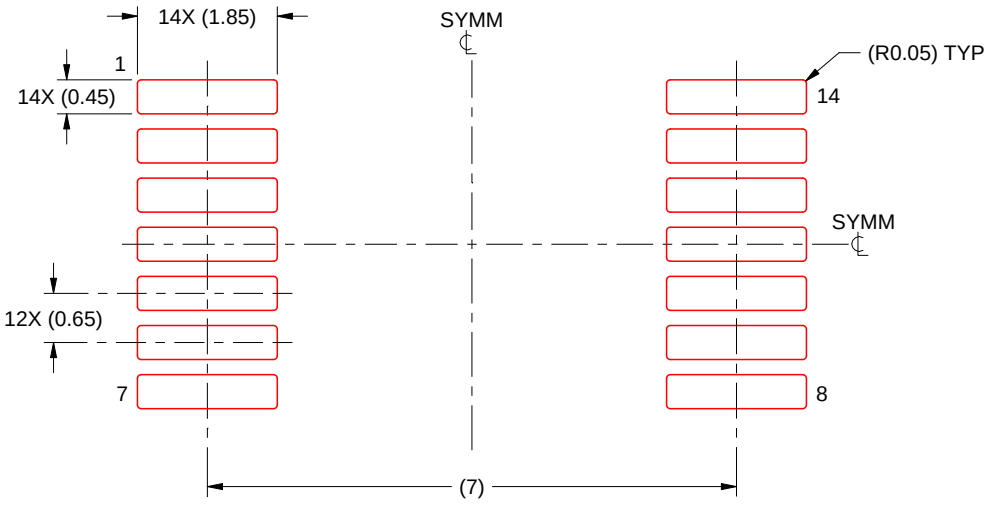


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

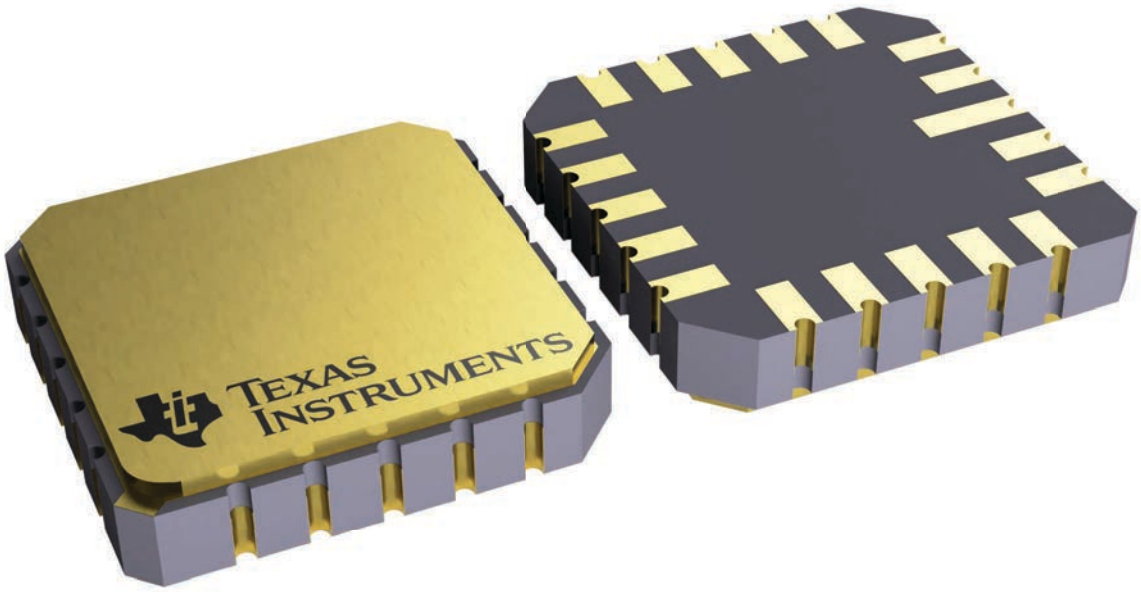
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

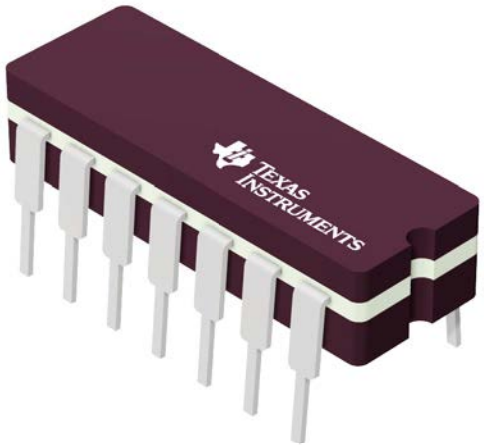


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

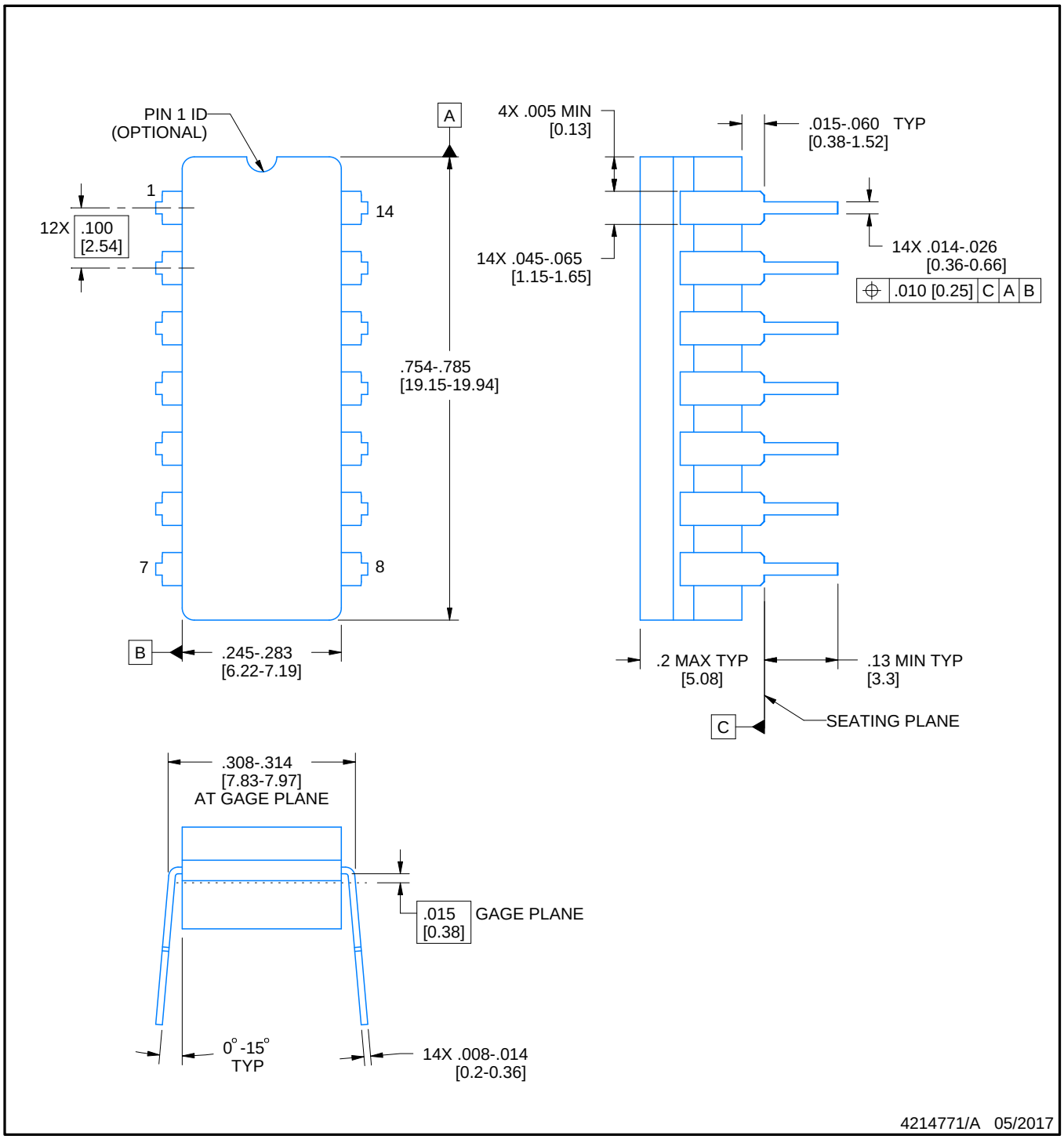


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

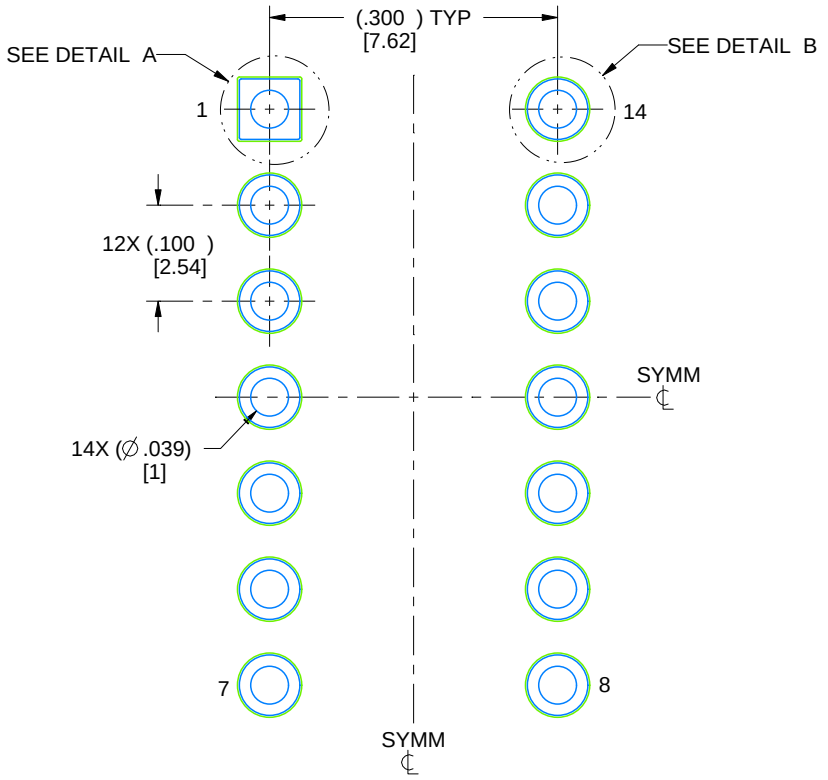
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

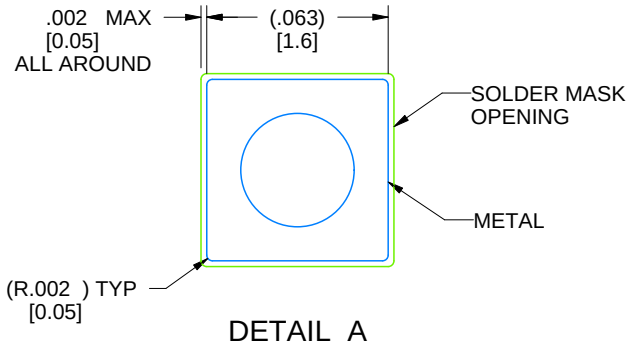
J0014A

CDIP - 5.08 mm max height

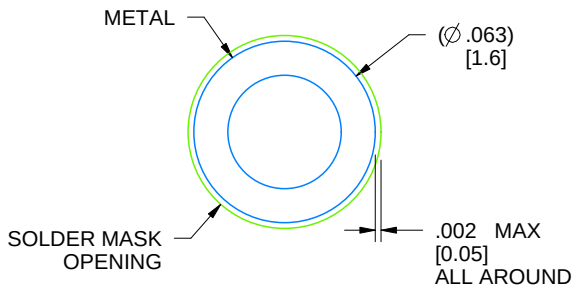
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



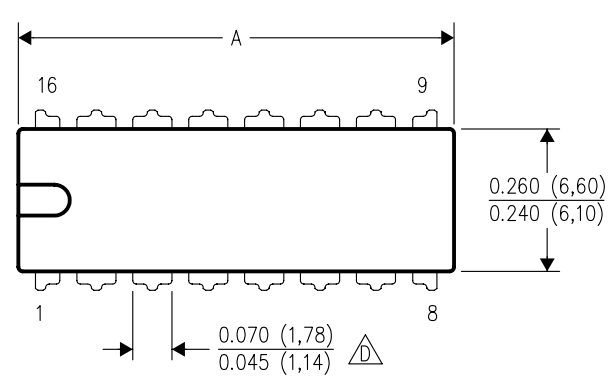
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

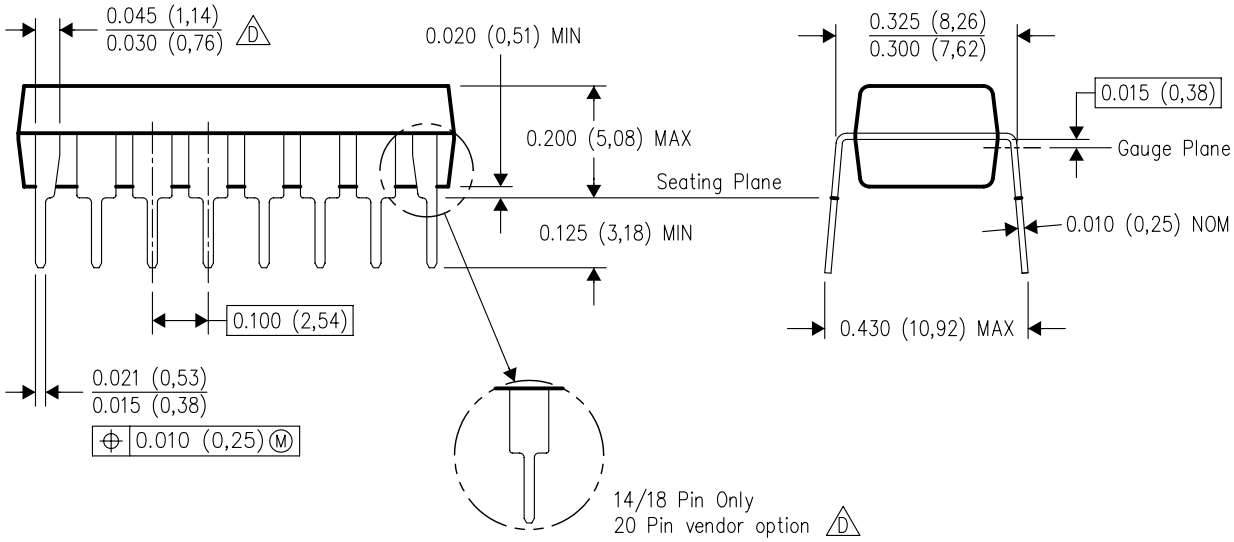
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

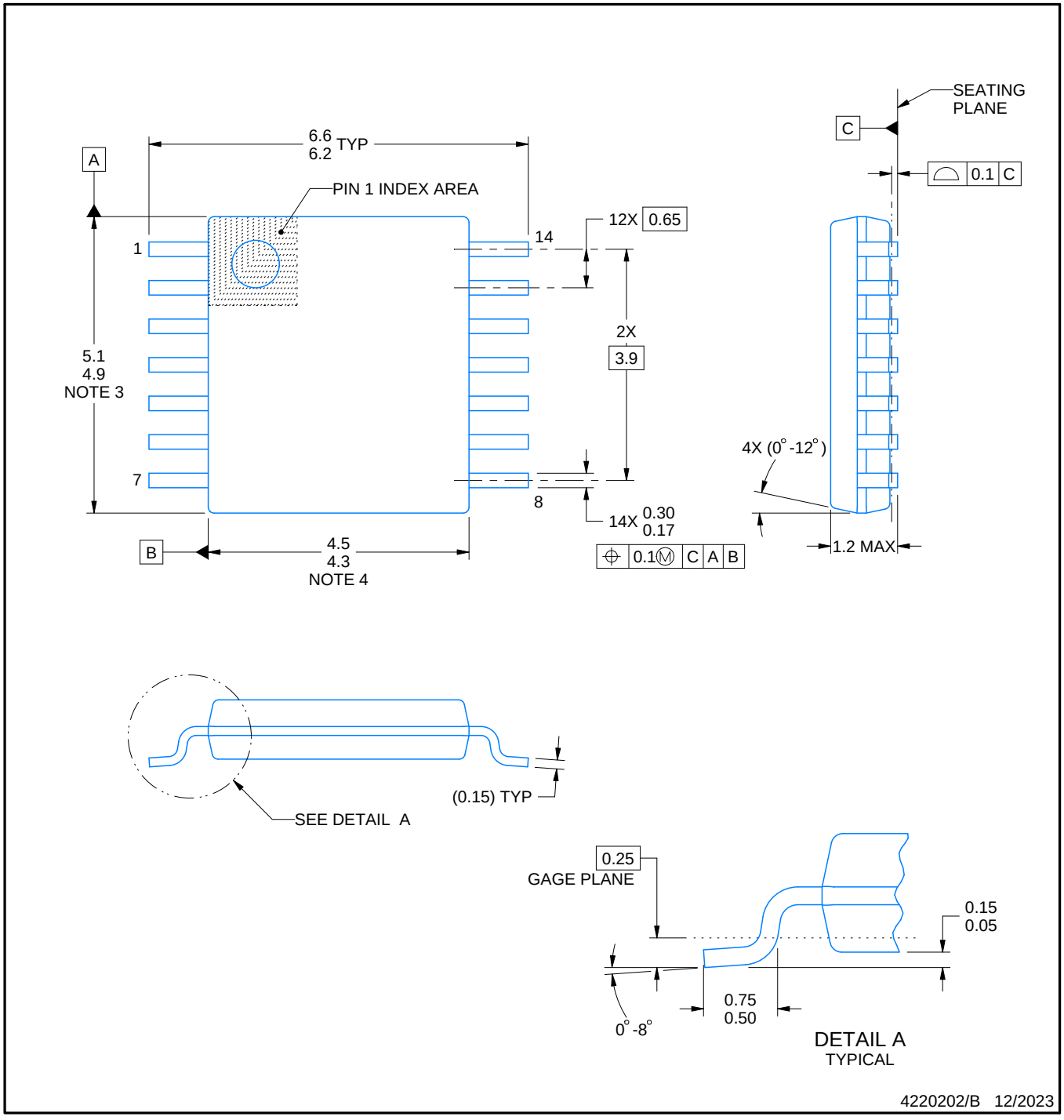
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

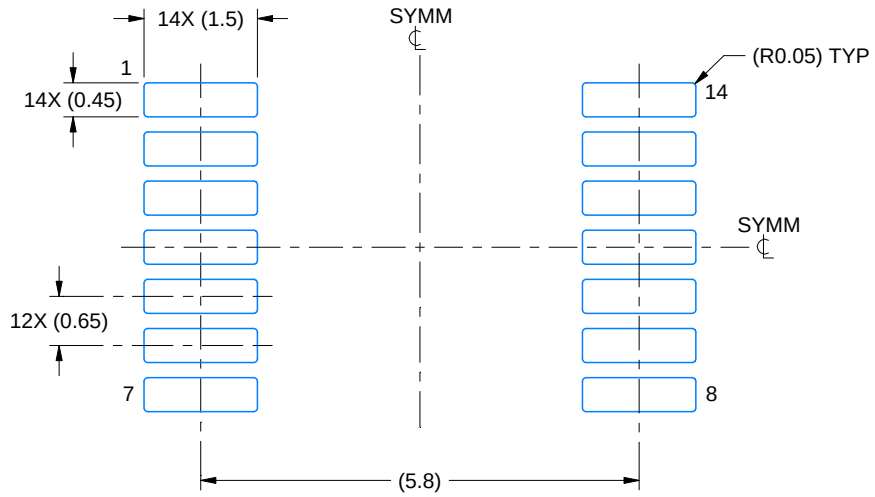
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

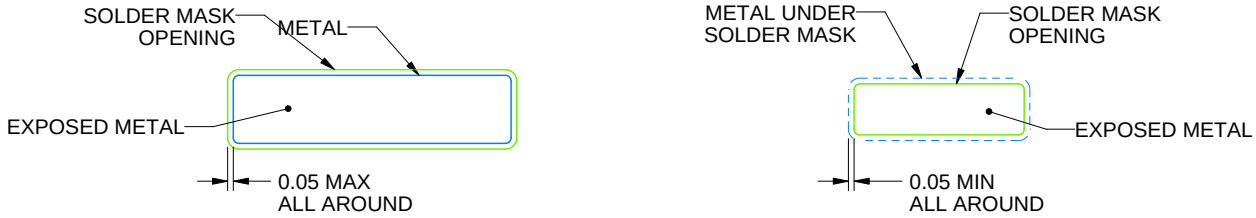


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

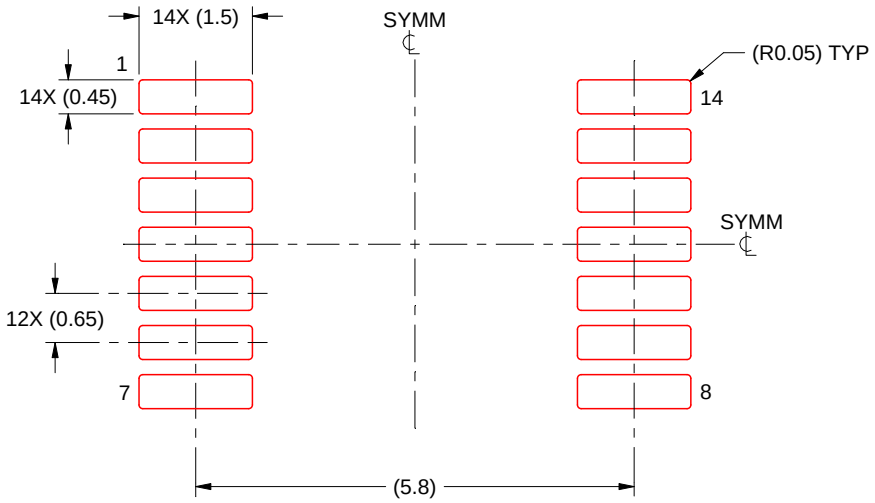


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

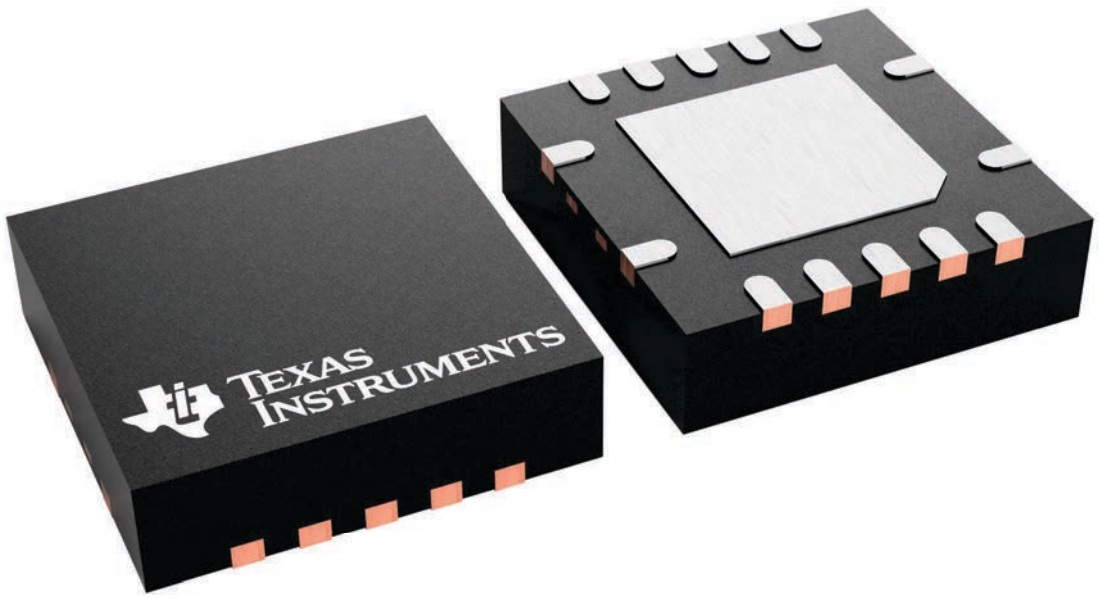
RGY 14

VQFN - 1 mm max height

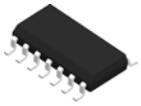
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

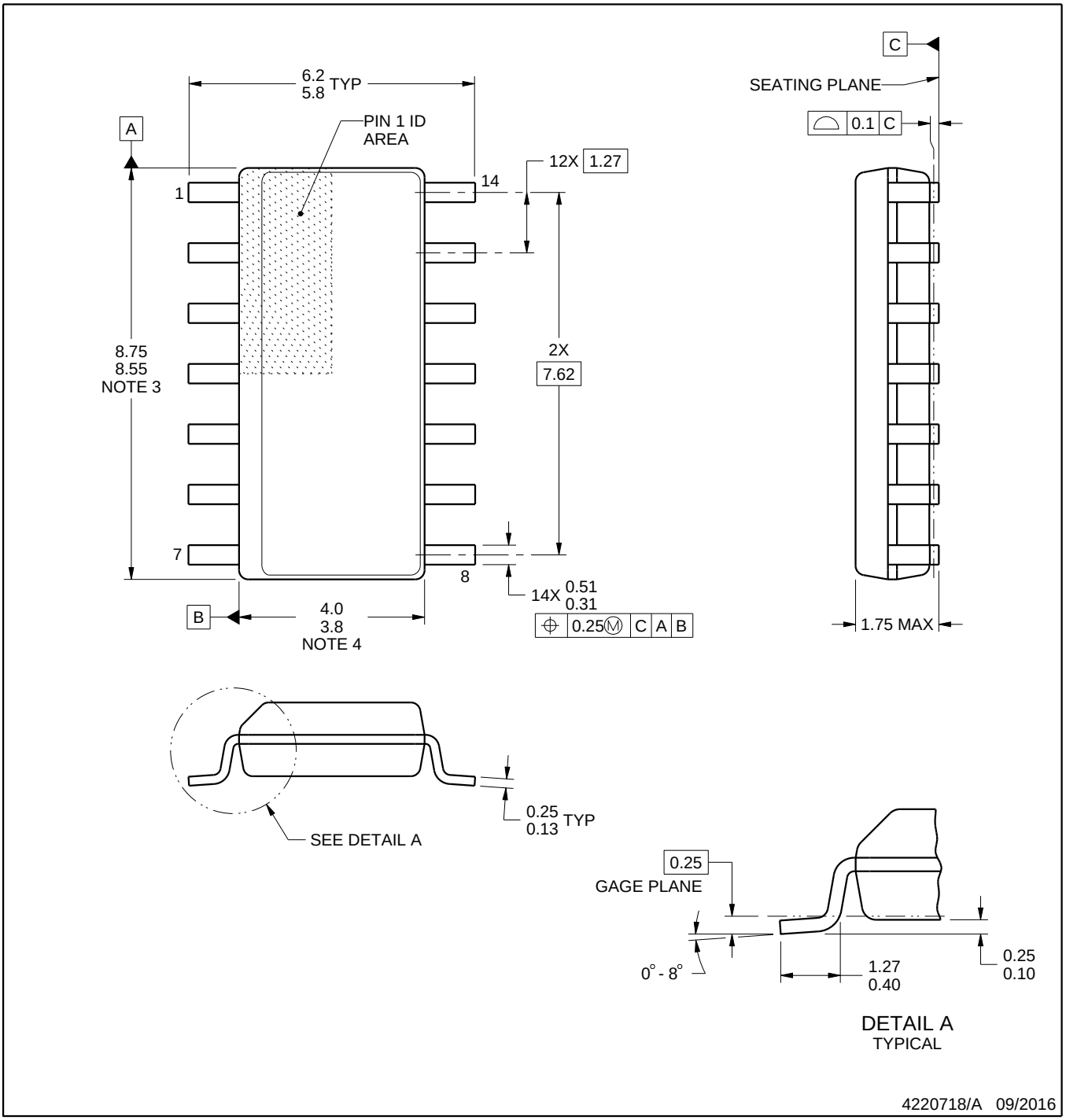


PACKAGE OUTLINE

D0014A

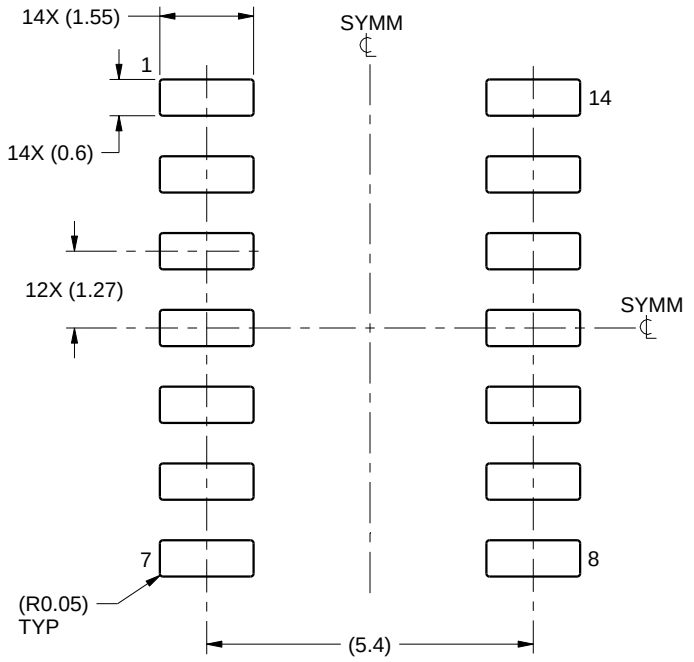
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

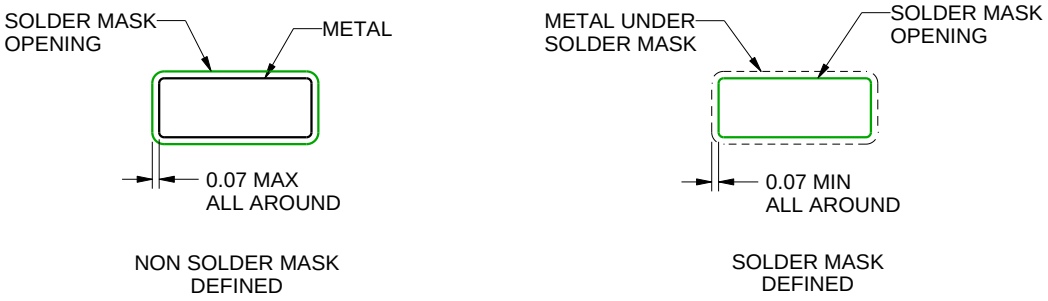


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

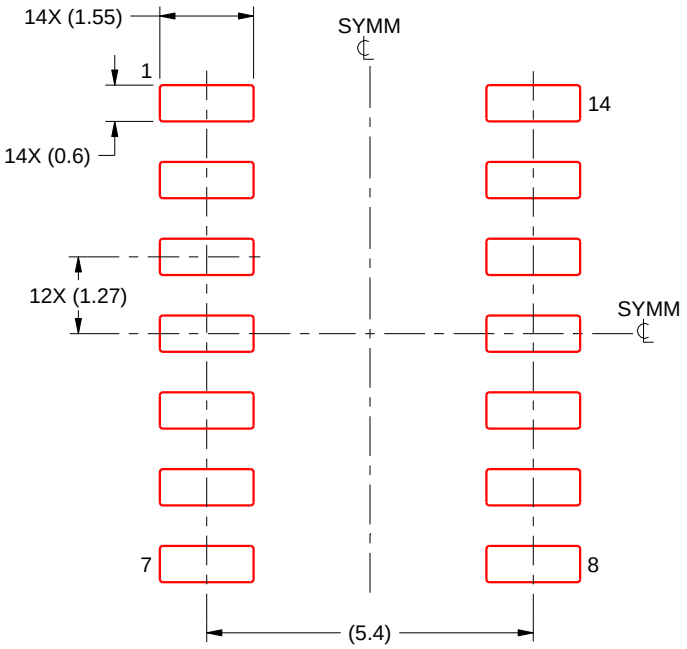
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

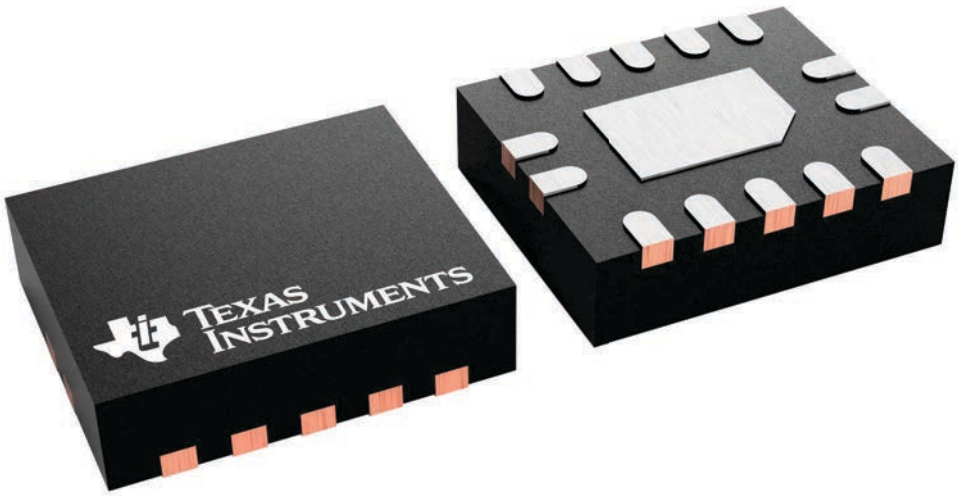
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

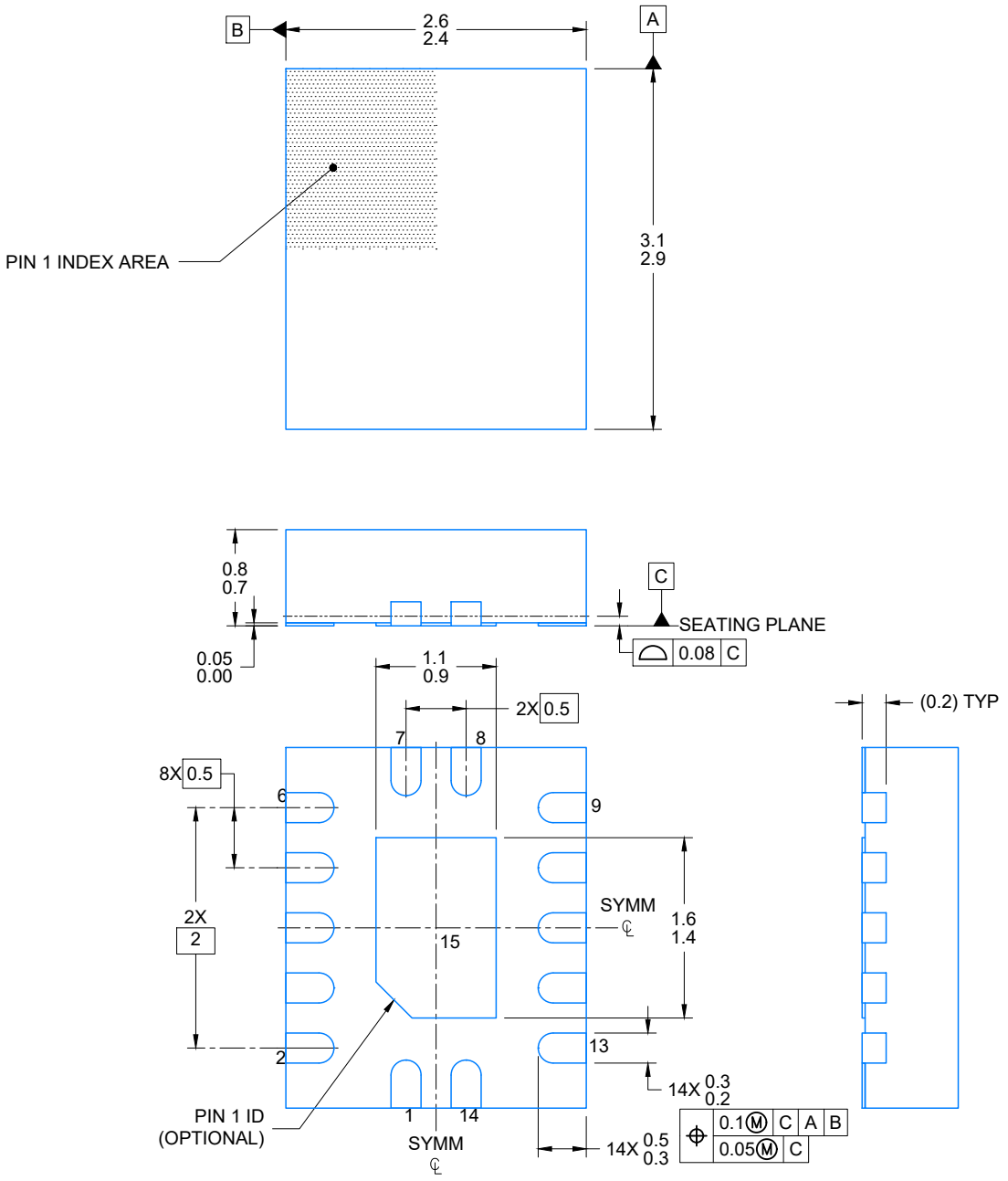


PACKAGE OUTLINE

BQA0014A

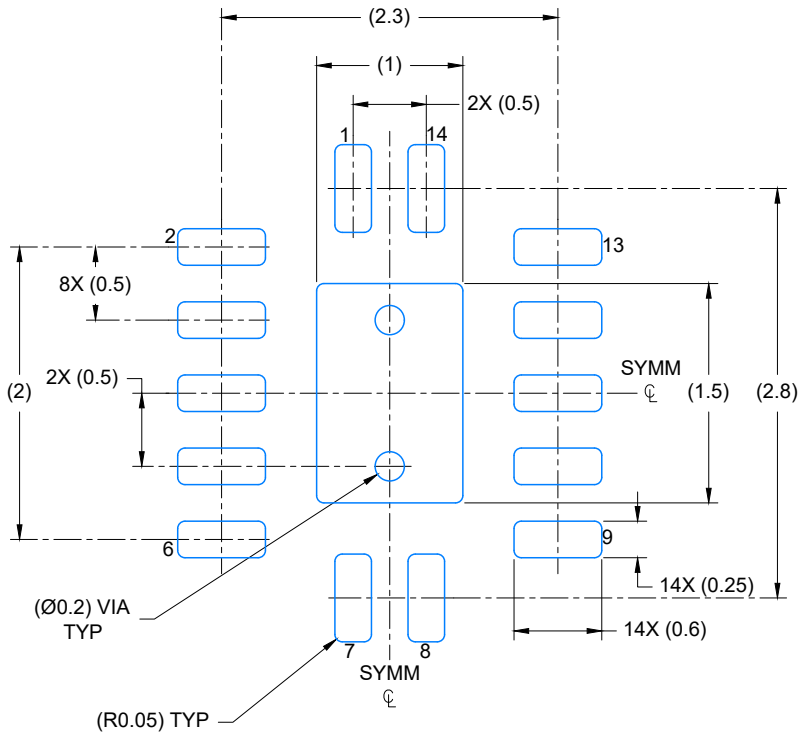
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

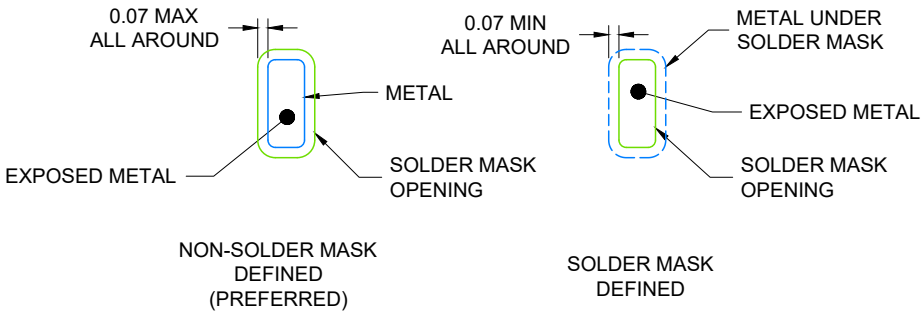


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



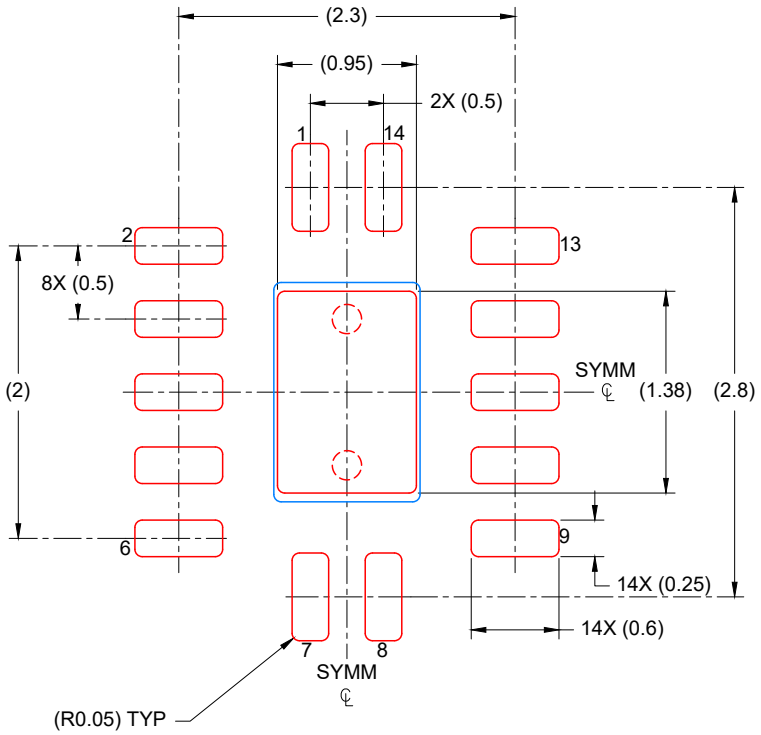
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

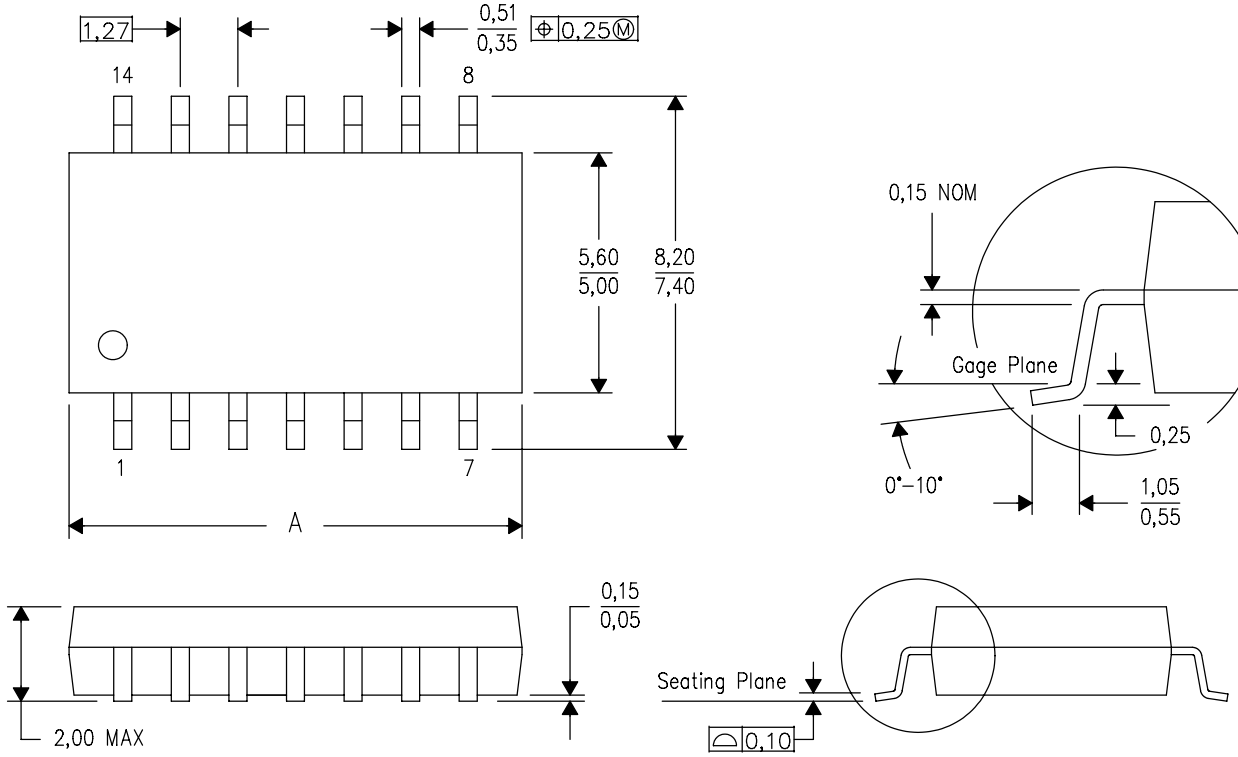
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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最后更新日期：2025 年 10 月