SN54AC00-SP 抗辐射加固型四路 2 输入与非门

1 特性

- 5962R87549：
  - 抗辐射加固保障 (RHA) 高达 100 krad (Si) 总电离剂量 (TID)
  - SEL 抗扰度为 86 MeV×cm^2/mg
- 5962-87549：
  - 总电离剂量为 50 krad (Si)
- 2 V 至 6 V V_{CC} 运行
- 输入电压高达 6 V
- 5V 时 t_{pd} 最大值为 7 ns

2 应用

- 卫星有效载荷
- 卫星上电复位逻辑
- 适用于太空混合动力车的 RHA 已知合格芯片 (KGD) 产品

引脚功能（每个逻辑门）

输入		输出
A	B	Y
H	H	L
L	X	H
X	L	H



逻辑图（正逻辑）

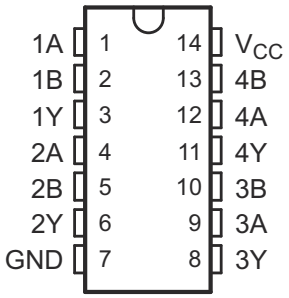
3 说明

SN54AC00 器件包含四个独立双输入与非门。每个逻辑门以正逻辑执行布尔函数 $Y = \overline{A \cdot B}$ 或 $Y = \overline{A} + \overline{B}$。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN54AC00-SP	CDIP (14)	5.97 mm × 9.21 mm
	CFP (14)	6.67 mm × 19.56 mm
	KGD (0)	不可用

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



J 或 W 封装
（顶视图）

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

1 特性.....1
2 应用.....1
3 说明.....1
4 Revision History.....2
5 Bare Die Information.....3
6 Specifications.....4
6.1 Absolute Maximum Ratings.....4
6.2 Recommended Operating Conditions.....4
6.3 Thermal Information.....5
6.4 Electrical Characteristics.....5
6.5 Switching Characteristics, V_{CC} = 3.3 V.....6
6.6 Switching Characteristics, V_{CC} = 5 V.....6
6.7 Operating Characteristics.....6
7 Parameter Measurement Information.....7
8 Device and Documentation Support.....8
8.1 接收文档更新通知.....8
8.2 支持资源.....8
8.3 Trademarks.....8
8.4 Electrostatic Discharge Caution.....8
8.5 术语表.....8
9 Mechanical, Packaging, and Orderable Information.....8

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (October 2015) to Revision C (April 2022) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1
- 删除了*特性* 部分中的 *SEU* 1
- 将 *SEL* 抗扰度更改为 86 MeV×cm^2/mg.....1

Changes from Revision A (December 2013) to Revision B (February 2015) **Page**

- 添加了 KGD 封装信息.....1
- 添加了*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分.....1
- Added *Bare Die Information*, image, and *Bond Pad Coordinates in Microns* 3
- Added parameter information for KGD to *节 6.5* and *节 6.6* 6

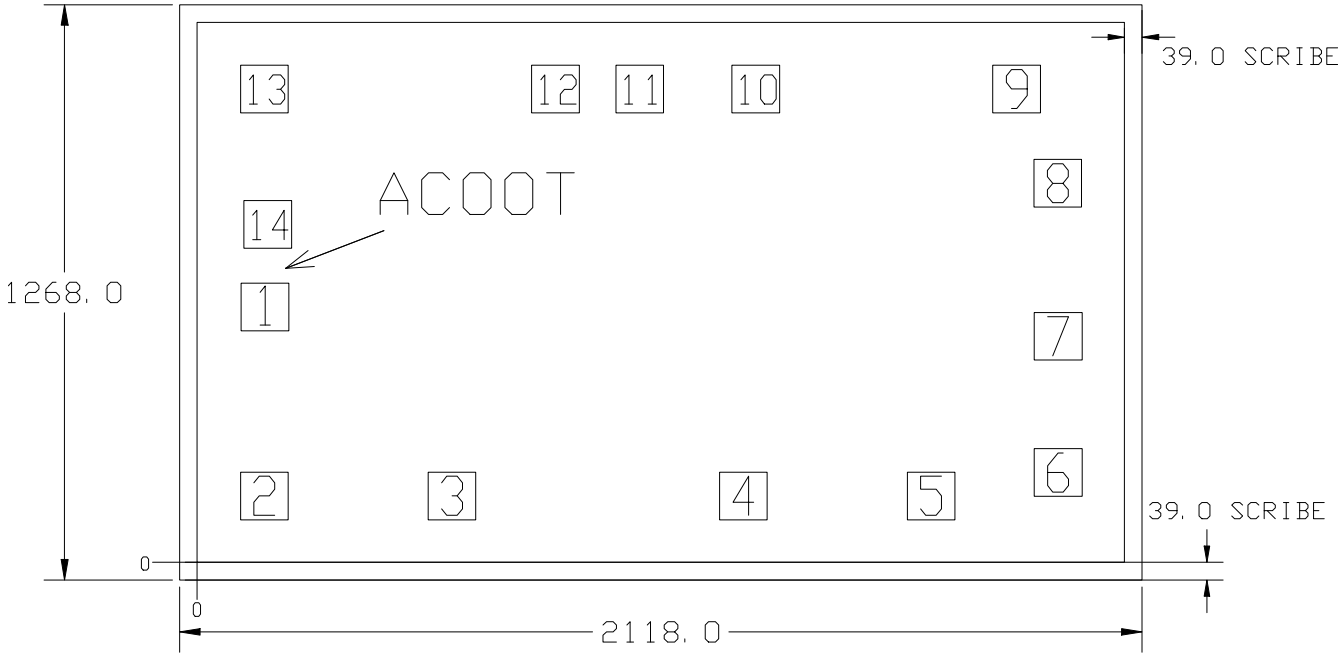
Changes from Revision * (October 2008) to Revision A (December 2013) **Page**

- 更改了*特性* 列表项.....1
- 删除了*订购信息* 表.....1

Copyright © 2022 Texas Instruments Incorporated

5 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Floating	TiW/AlCu2	15800 nm



Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
1A	1	96.3	510.5	201.3	615.5
1B	2	95	94	200	199
1Y	3	508	94	613	199
2A	4	1149	94	1254	199
2B	5	1562	94	1667	199
2Y	6	1841.5	145.5	1946.5	250.5
GND	7	1841.5	445.5	1946.5	550.5
3Y	8	1841	783	1946	888
3A	9	1750.5	991	1855.5	1096
3B	10	1176.5	991	1281.5	1096
4Y	11	921	991	1026	1096
4A	12	736	991	841	1096
4B	13	95	991	200	1096
VCC	14	102.5	692	207.5	797

Copyright © 2022 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		– 0.5	7	V
V_I	Input voltage(2)		– 0.5	V_{CC} + 0.5	V
V_O	Output voltage(2)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 or V_I > V_{CC}		±20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±200	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		12	mA
		V_{CC} = 4.5 V		24	
		V_{CC} = 5.5 V		24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12	mA
		V_{CC} = 4.5 V		24	
		V_{CC} = 5.5 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			8	ns/V
T_A	Operating free-air temperature		– 55	125	°C

Copyright © 2022 Texas Instruments Incorporated

6.3 Thermal Information

THERMAL METRIC(1) (2)		SN54AC00-SP		UNIT
		J	W	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.1	125.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.6	30.85	
$R_{\theta JB}$	Junction-to-board thermal resistance	47.9	43.4	
ψ_{JT}	Junction-to-top characterization parameter	N/A	N/A	
ψ_{JB}	Junction-to-board characterization parameter	N/A	N/A	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7 and Mil Std 883 method 1012.1 (see www.JEDEC.org).

6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = –12 mA	3 V	2.56			2.4		
	I_{OH} = –24 mA	4.5 V	3.86			3.7		
		5.5 V	4.86			4.7		
	I_{OH} = –50 mA(1)	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5	
	I_{OL} = 24 mA	4.5 V			0.36		0.5	
		5.5 V			0.36		0.5	
	I_{OL} = 50 mA(1)	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i	V_I = V_{CC} or GND	5 V		2.6				pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

Copyright © 2022 Texas Instruments Incorporated

6.5 Switching Characteristics, V_{CC} = 3.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ±0.3 V (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	2	7	9.5	1	11	ns
t_{PHL}			1.5	5.5	8	1	9	
t_{PLH} (KGD only)(1)	A or B	Y	1	7	9.5	1	11	ns
t_{PHL} (KGD only)(1)			1	5.5	9.5	1	11	

(1) Specification limits for KGD are based on SMD 5962-8754903

6.6 Switching Characteristics, V_{CC} = 5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	6	8	1	8.5	ns
t_{PHL}			1.5	4.5	6.5	1	7	
t_{PLH} (KGD only)(1)	A or B	Y	1.5	6	8	1	8.5	ns
t_{PHL} (KGD only)(1)			1.5	4.5	8	1	8.5	

(1) Specification limits for KGD are based on SMD 5962-8754903

6.7 Operating Characteristics

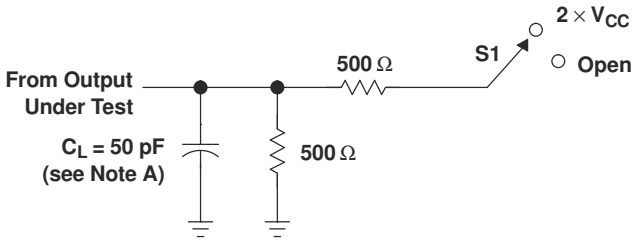
V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	40	pF

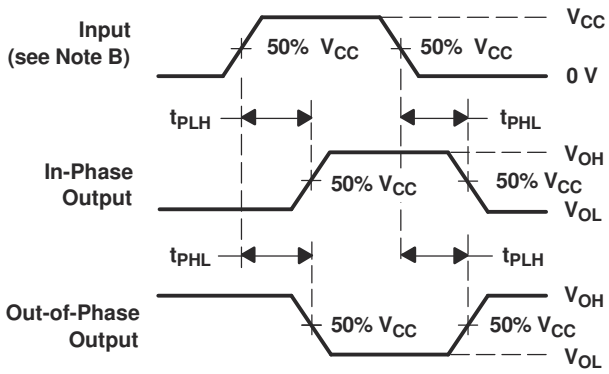
Copyright © 2022 Texas Instruments Incorporated

7 Parameter Measurement Information

TEST	S1
t_{PLH}/t_{PHL}	Open



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

图 7-1. Load Circuit and Voltage Waveforms

Copyright © 2022 Texas Instruments Incorporated

8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2022 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8754903VCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8754903VC A SNV54AC00J
5962-8754903VCA.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8754903VC A SNV54AC00J
5962-8754903VDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8754903VD A SNV54AC00W
5962-8754903VDA.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8754903VD A SNV54AC00W
5962R8754903V9A	Active	Production	XCEPT (KGD) | 0	95 | JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-55 to 125	
5962R8754903V9A.A	Active	Production	XCEPT (KGD) | 0	95 | JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-55 to 125	
5962R8754903VCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962R8754903VC A SNVR54AC00J
5962R8754903VCA.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962R8754903VC A SNVR54AC00J
5962R8754903VDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962R8754903VD A SNVR54AC00W
5962R8754903VDA.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962R8754903VD A SNVR54AC00W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

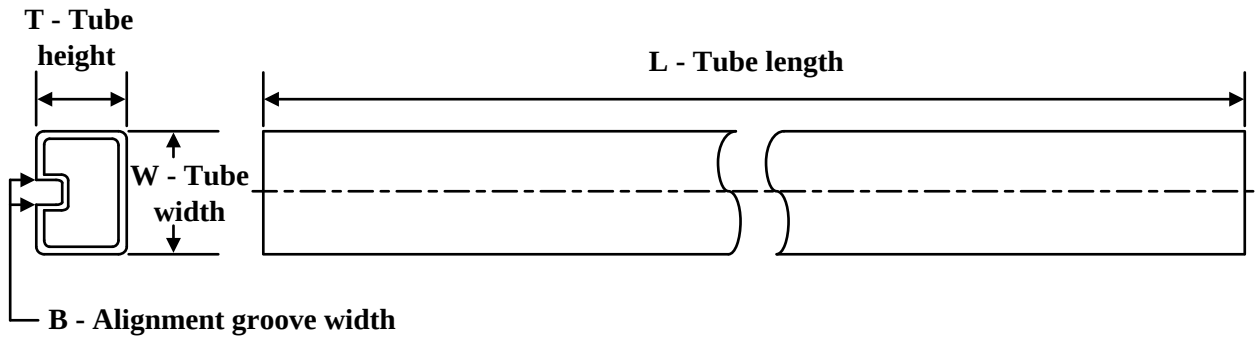
OTHER QUALIFIED VERSIONS OF SN54AC00-SP :

- Catalog : SN54AC00

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

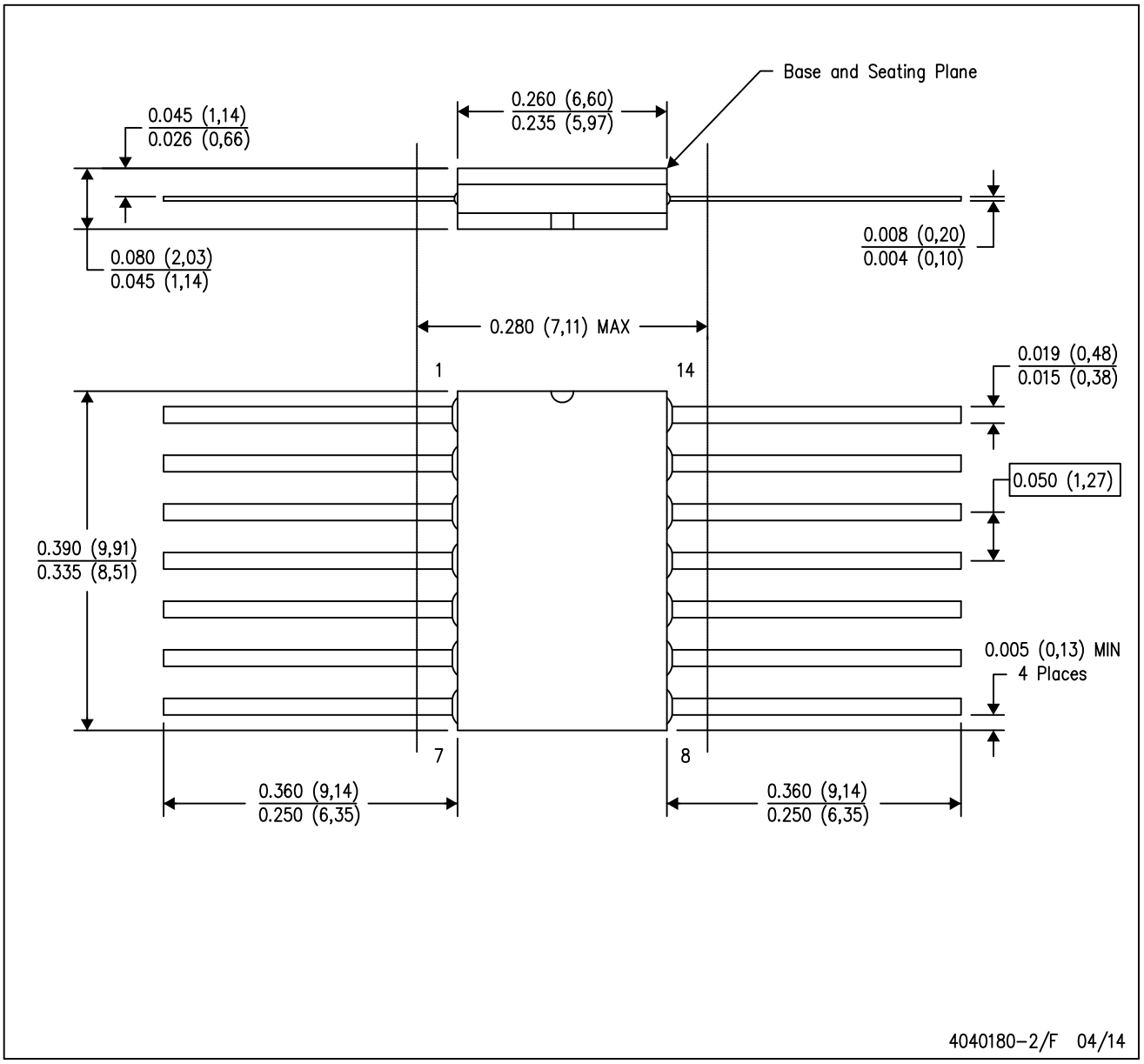
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8754903VDA	W	CFP	14	25	506.98	26.16	6220	NA
5962-8754903VDA.A	W	CFP	14	25	506.98	26.16	6220	NA
5962R8754903VCA	J	CDIP	14	25	506.98	15.24	13440	NA
5962R8754903VCA.A	J	CDIP	14	25	506.98	15.24	13440	NA
5962R8754903VDA	W	CFP	14	25	506.98	26.16	6220	NA
5962R8754903VDA.A	W	CFP	14	25	506.98	26.16	6220	NA

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

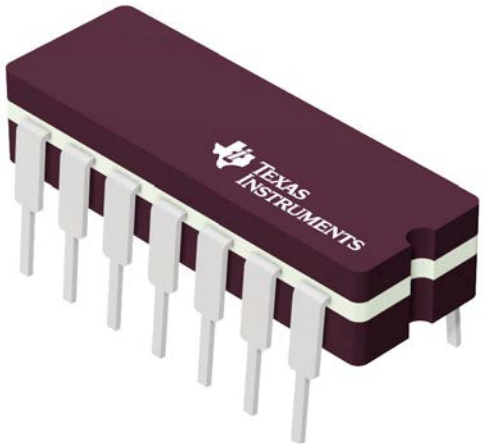


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

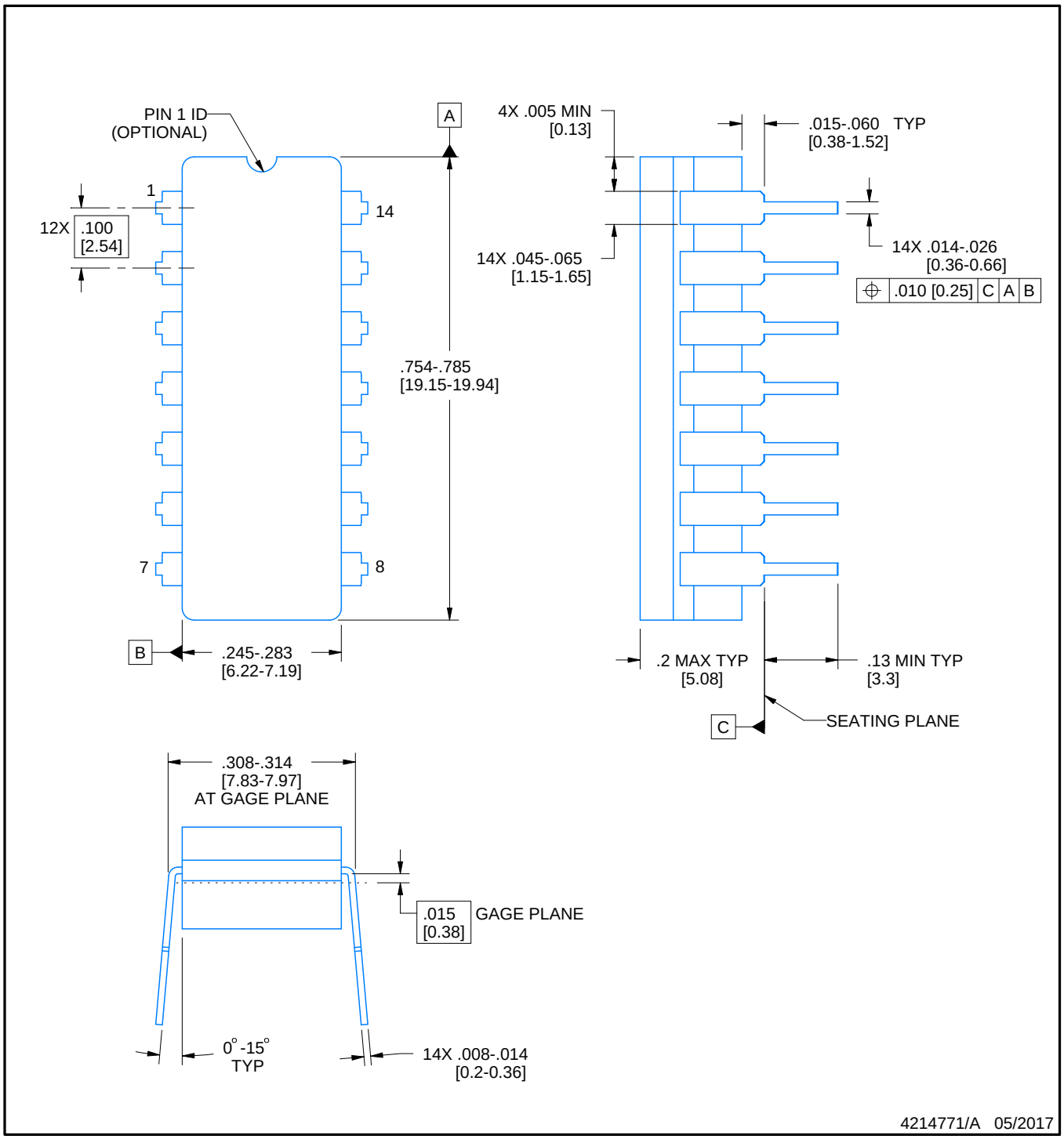


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

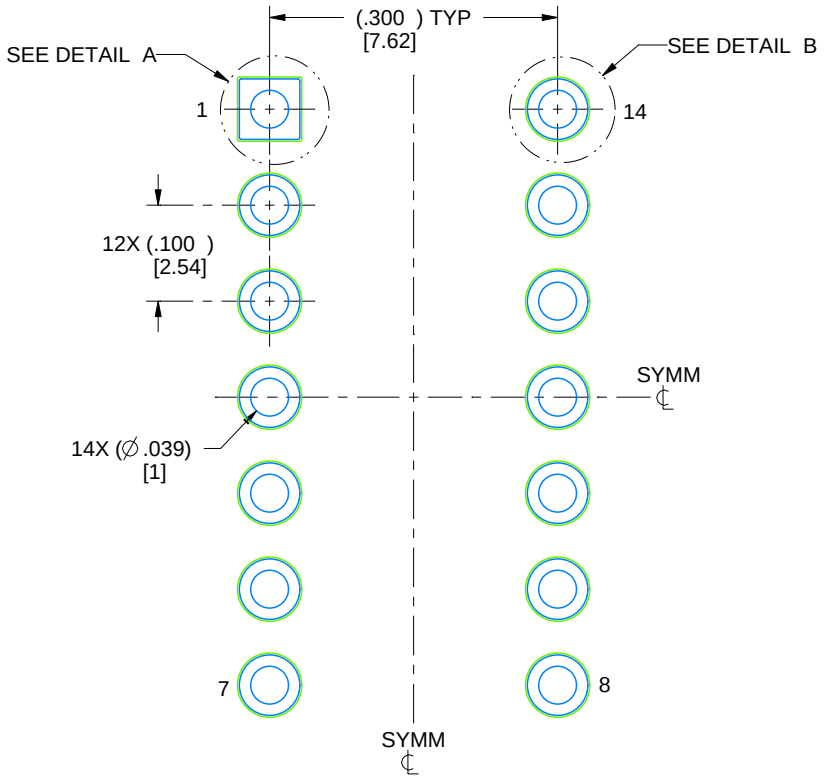
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

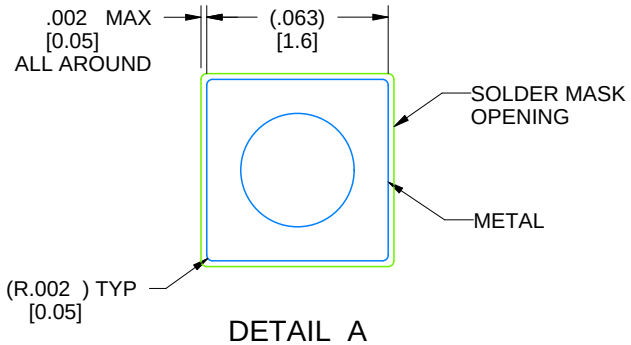
J0014A

CDIP - 5.08 mm max height

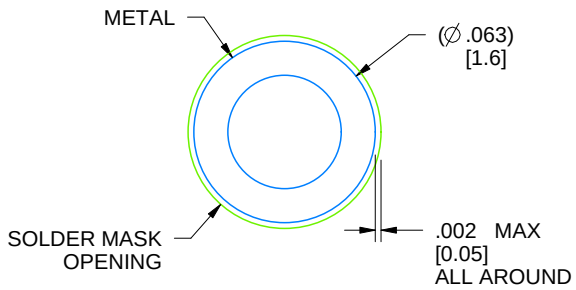
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月