# 精密、零漂移、高压、可编程增益仪表放大器

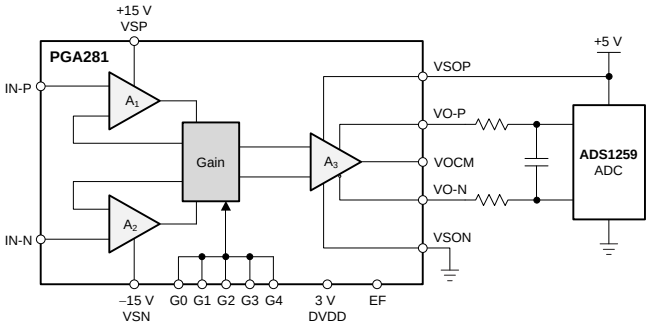
查询样品: **PGA281**

## 特性

- 宽输入电压范围：在使用 **±18V** 电源时为 **±15.5V**
- 二进制增益步长：**128V/V** 至 **⅛V/V**
- 额外比例缩放因子：**1V/V** 和 **1⅜V/V**
- 低偏移电压：在 **G=128** 时为 **5μV**
- 偏移电压的近零长期漂移
- 近零增益漂移：**0.5ppm/°C**
- 出色的线性：**1.5ppm**
- 出色的共模抑制比 **(CMRR)**：**140dB**
- 高输入阻抗
- 极低 **1/f** 噪声
- 差分信号输出
- 过载检测
- 薄型小外形尺寸 **(TSSOP)-16** 封装

## 应用范围

- 高精度信号仪表
- 并行多数据采集
- 医疗仪表
- 测试和测量仪器
- 差分或单端模数转换器 **(ADC)** 驱动器
- 应力计放大器
- 工业过程控制




## 说明

PGA281 是一款高精度仪表放大器，此放大器具有数控增益和信号完整性测试功能。 这个器件使用已获专利的自动归零技术来提供低偏移电压、近零偏移和增益漂移、出色的线性，并且几乎没有 1/f 噪声。

对 PGA281 进行了优化，从而在一个宽频率范围内提供大于 110dB (G = 1) 的出色共模抑制。 较好的共模和电源抑制提供了高分辨率、精准测量。 36V 电源能力和宽、高阻抗输入范围符合一般信号测量的需要。

PGA281 提供 ⅛V/V（衰减）至 176V/V 范围内的多个内部增益选项，这使得这款器件成为适用于多种应用的通用、高性能模拟前端。 完全差分、轨到轨输出被设计成可将宽范围输入信号与高分辨率模数转换器 (ADC) 的低压域轻松对接。

PGA281 采用薄型小外形尺寸 (TSSOP)-16 封装并且额定温度范围介于 -40°C 至 +105°C 之间。

相关产品

| 产品 | 特性 |
|---|---|
| ADS1259 | 23 位分辨率，三角积分 (ΔΣ) 模数转换器 |
| INA333 | 斩波稳定仪表放大器，RR I/O，5V 单电源 |
| PGA204 | 高精度可编程增益放大器 (PGA)；G = 1，10，100 和 1000 |
| PGA280 | 零漂移，36V，PGA，串行外设接口 (SPI)，通用输入输出接口 (GPIO)，输入开关阵列 |

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION(1)

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

| | | VALUE | UNIT |
|---|---|---|---|
| Supply voltage | VSN to VSP | 40 | V |
| | VSON to VSOP, and VSON to DVDD | 6 | V |
| Signal input terminals, voltage(2) | | VSN – 0.5 to VSP + 0.5 | V |
| Signal input terminals, current(2) | | ±10 | mA |
| Output short-circuit(3) | | Continuous | |
| Operating temperature | | –55 to +140 | °C |
| Storage temperature | | –65 to +150 | °C |
| Junction temperature | | +150 | °C |
| Electrostatic discharge (ESD) ratings | Human body model (HBM) | 2000 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Terminals are diode-clamped to the power-supply (VON and VOP) rails. Signals that can swing more than 0.5 V beyond the supply rails must be current-limited.
(3) Short-circuit to VSON or VSOP, respectively, VSON or DVDD.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | PGA281 PW (TSSOP) 16 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 92.6 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 23.7 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 37.9 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.0 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 37.3 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## ELECTRICAL CHARACTERISTICS

At $T_A$ = +25°C, VSP = +15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = +3 V, $R_L$ = 2.5 kΩ to VSOP / 2 = VOCM, G = 1 V/V, $V_{CM}$ = 0 V, and differential output, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | PGA281 MIN | PGA281 TYP | PGA281 MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT** | | | | | | |
| $V_{OS}$ | Offset voltage, RTI(1) | All gains | | ±(5 + 45/G) | ±(20 + 235/G) | µV |
| $dV_{OS}/dT$ | vs temperature(2) | All gains | | ±(0.03 + 0.18/G) | ±(0.17 + 0.45/G) | µV/°C |
| PSR | vs power supply, RTI | VSP – VSN = 10 V and 36 V, gain = 1 V/V, 128 V/V | | ±0.3 | ±3 | µV/V |
| | Long-term stability(3) | Gain = 128 V/V | | 3.5 | | nV/month |
| | Input impedance | Single-ended (SE) and differential | | >1 | | GΩ |
| | Input capacitance | SE | | 12 | | pF |
| | Input voltage range | $T_A$ = –40°C to +105°C | (VSN) + 2.5 | | (VSP) – 2.5 | V |
| CMR | Common-mode rejection, RTI | Gain = 1 V/V, $T_A$ = –40°C to +105°C | 110 | 130 | | dB |
| | | Gain = 128 V/V | 121 | 142 | | dB |
| | | Gain = 128 V/V, $T_A$ = –40°C to +105°C | 116 | 140 | | dB |
| **SINGLE-ENDED OUTPUT CONNECTION** (4) | | | | | | |
| $V_{OS}$ | Offset voltage, RTI, SE | Gain = 1 V/V, 1.375 V/V | | ±120 | | µV |
| | | Gain = 64 V/V | | ±3 | | µV |
| $dV_{OS}/dT$ | vs temperature, SE | Gain = 1 V/V, $T_A$ = –40°C to +105°C | | 0.6 | | µV/°C |
| | | Gain = 64 V/V, $T_A$ = –40°C to +105°C | | 0.05 | | µV/°C |
| **INPUT BIAS CURRENT**(5) | | | | | | |
| $I_B$ | Bias current | Gain = 1 V/V | | ±0.3 | ±1 | nA |
| | | Gain = 128 V/V | | ±0.8 | ±2 | nA |
| | | Gain = 1 V/V, gain = 128 V/V, $T_A$ = –40°C to +105°C | | ±0.6 | ±2 | nA |
| $I_{OS}$ | Offset current | Gain = 1 V/V, gain = 128 V/V | | ±0.1 | ±0.5 | nA |
| | | Gain = 1 V/V, gain = 128 V/V, $T_A$ = –40°C to +105°C | | ±0.9 | ±2 | nA |
| **NOISE** | | | | | | |
| $e_{NI}$ | Voltage noise, RTI; target | f = 0.01 Hz to 10 Hz, gain = 128 V/V | | 420 | | $nV_{PP}$ |
| | | f = 1 kHz, gain = 128 V/V | | 22 | | $nV/\sqrt{Hz}$ |
| | | f = 0.01 Hz to 10 Hz, gain = 1 V/V | | 4.5 | | $\mu V_{PP}$ |
| | | f = 1 kHz, gain = 1 V/V | | 240 | | $nV/\sqrt{Hz}$ |
| $I_N$ | Current noise, RTI | f = 0.01 Hz to 10 Hz, gain = 128 V/V | | 1.7 | | $pA_{PP}$ |
| | | f = 1 kHz, gain = 128 V/V | | 90 | | $fA/\sqrt{Hz}$ |

(1) RTI: Referred to input.
(2) Specified by design; not production tested.
(3) 300-hour life test at +150°C demonstrated randomly distributed variation in the range of measurement limits.
(4) For single-ended (SE) output mode, see *Application Information* section and Typical Characteristic graphs; signal between VOP and VOCM.
(5) See *Application Information* section and Typical Characteristic graphs.

## ELECTRICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, VSP = +15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = +3 V, $R_L$ = 2.5 kΩ to VSOP / 2 = VOCM, G = 1 V/V, $V_{CM}$ = 0 V, and differential output, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | PGA281 MIN | PGA281 TYP | PGA281 MAX | UNIT |
|---|---|---|---|---|---|---|
| **GAIN (Output Swing = ±4.5 V(6))** | | | | | | |
| | Range of input gain | | ⅛ | | 128 | V/V |
| | Output gain | | | 1 or 1⅜ | | V/V |
| | Gain error, all binary steps | All gains | | ±0.03% | ±0.15% | |
| | | $T_A$ = –40°C to +105°C, no load, all gains except gain = 128 V/V(7) (8) | | -0.5 | ±2 | ppm/°C |
| | | $T_A$ = –40°C to +105°C, no load, gain = 128 V/V(7)(8) | | -1 | ±3 | ppm/°C |
| | Gain step matching(9) (gain to gain) | No load, all gains | See Typical Characteristics | | | |
| | Nonlinearity | No load, all gains(10) | | 1.5 | 10 | ppm |
| | | No load, all gains, $T_A$ = –40°C to +105°C(7) | | 3 | | ppm |
| **OUTPUT** | | | | | | |
| | Voltage output swing from rail(9) | VSOP = 5 V, load current 2 mA $T_A$ = –40°C to +105°C | | 40 | 100 | mV |
| | | VSOP = 2.7 V, load current 1.5 mA $T_A$ = –40°C to +105°C | | | 100 | mV |
| | Capacitive load drive | | | 500 | | pF |
| $I_{SC}$ | Short-circuit current | To VSOP / 2, gain = 1.375 V/V | 7 | 15 | 25 | mA |
| | Output resistance | Both VOP and VON outputs | | 200 | | mΩ |
| **VOCM** | | | | | | |
| | Voltage range for VOCM | VSP – 2 V > VOCM, $T_A$ = –40°C to +105°C | (VSON) + 0.1 | | (VSOP) – 0.1 | V |
| $I_{B(VOCM)}$ | Bias current into VOCM | | | 3 | 100 | nA |
| | VOCM input resistance | | | 1 | | GΩ |
| **FREQUENCY RESPONSE** | | | | | | |
| GBP | Gain bandwidth product(9) | Gain > 4 V/V | | 6 | | MHz |
| SR | Slew rate(9) | Gain = 1 V/V, 4-$V_{PP}$ output step, $C_L$ = 100 pF | | 1 | | V/µs |
| | | Gain = 8 V/V, 4-$V_{PP}$ output step, $C_L$ = 100 pF | | 2 | | V/µs |
| | | Gain = 128 V/V, 4-$V_{PP}$ output step, $C_L$ = 100 pF | | 1 | | V/µs |
| $t_S$ | Settling time(9) | To 0.01%, gain = 8 V/V, $V_O$ = 8-$V_{PP}$ step | | 20 | | µs |
| | | To 0.001%, gain = 8 V/V, $V_O$ = 8-$V_{PP}$ step | | 30 | | µs |
| | | To 0.01%, gain = 128 V/V, $V_O$ = 8-$V_{PP}$ step | | 30 | | µs |
| | | To 0.001%, gain = 128 V/V, $V_O$ = 8-$V_{PP}$ step | | 40 | | µs |
| | Overload recovery, input(9) | 0.5 V over supply, gain = ⅛ V/V to 128 V/V | | 8 | | µs |
| | Overload recovery, output(9) | ±5.5-$V_{PP}$ input, gain = 1 V/V | | 6 | | µs |

(6) Gains smaller than ½ are measured with smaller output swing.
(7) Specified by design; not production tested.
(8) See Figure 10 for typical gain error drift of various gain settings.
(9) See *Application Information* section and Typical Characteristic graphs.
(10) Only gain = 1 is production tested.

## ELECTRICAL CHARACTERISTICS (continued)

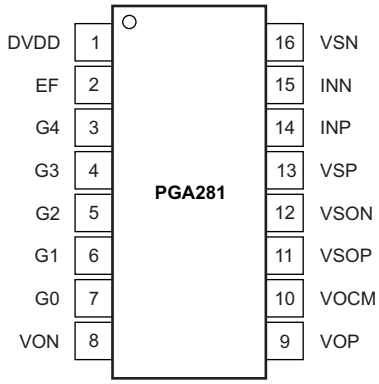
At $T_A$ = +25°C, VSP = +15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = +3 V, $R_L$ = 2.5 kΩ to VSOP / 2 = VOCM, G = 1 V/V, $V_{CM}$ = 0 V, and differential output, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | PGA281 MIN | PGA281 TYP | PGA281 MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL I/O (Supply = 2.7 V to 5.5 V)** | | | | | | |
| | G4:G0 pin input | Logic low threshold | 0.1 | | 0.2(DVDD) | V |
| | | Logic high threshold | 0.8(DVDD) | | DVDD | V |
| | G4:G0 pin input current | | | 0.2 | | µA |
| | Error flag (EF pin) output | Logic low, disable | | | 0.7 | V |
| | | Logic high, alarm | DVDD – 0.5 | | | V |
| | Error flag (EF pin) delay | Alarm → disable (recovery) | | 5 | | µs |
| | | Disable → alarm (response) | | 30 | | µs |
| **POWER SUPPLY: Input Stage (VSP – VSN)** | | | | | | |
| | Specified voltage range | $T_A$ = –40°C to +105°C | 10 (±5) | | 36 (±18) | V |
| | Operating voltage range | | 10 (±5) | | 38 (±19) | V |
| $I_{Q(VSP)}$ | Quiescent current , VSP pin | $T_A$ = –40°C to +105°C | | 2.4 | 3 | mA |
| $I_{Q(VSN)}$ | Quiescent current, VSN pin | $T_A$ = –40°C to +105°C | | 2.1 | 3 | mA |
| **POWER SUPPLY: Output Stage (VSOP – VSON)** | | | | | | |
| | Specified voltage range | VSP – 1.5 V ≥ VSOP, $T_A$ = –40°C to +105°C | 2.7 | | 5.5 | V |
| | Voltage range for VSOP, upper limit | (VSP – 2 V) > VOCM, (VSP – 5 V) > VSON | | (VSP) | | V |
| | Voltage range for VSON | (VSP – 2 V) > VOCM, VSP ≥ VSOP | (VSN) | | (VSP) – 5 | V |
| $I_{Q(VSOP)}$ | Quiescent current, VSOP pin | $T_A$ = –40°C to +105°C | | 0.75 | 1 | mA |
| **POWER SUPPLY: Digital (DVDD – VSON)** | | | | | | |
| | Specified voltage range | $T_A$ = –40°C to +105°C | 2.7 | | 5.5 | V |
| | Voltage range for DVDD, upper limit | | | (VSP) – 1 | | V |
| | Voltage range for VSON, lower limit | | | (VSN) | | V |
| $I_{Q(DVDD)}$ | Quiescent current(11) | Static condition, no external load, DVDD = 3 V, $T_A$ = –40°C to +105°C | | 0.07 | 0.13 | mA |
| **TEMPERATURE** | | | | | | |
| | Specified range | | –40 | | +105 | °C |
| | Operating range | | –55 | | +140 | °C |

(11) See *Application Information* section and Typical Characteristic graphs.

## PIN CONFIGURATION

**TSSOP-16**
**PW PACKAGE**
**(TOP VIEW)**




## PIN DESCRIPTIONS

| PIN | | DESCRIPTION | PIN | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NUMBER | | NAME | NUMBER | |
| DVDD | 1 | Digital supply | INN | 15 | Signal input, inverting |
| EF | 2 | Error flag (output) | INP | 14 | Signal input, noninverting |
| VSON | 12 | Negative output-stage low-voltage supply and negative digital supply | VOCM | 10 | Signal input, output common-mode voltage |
| G0 | 7 | Gain option 1 (see Table 1) | VON | 8 | Inverting signal output |
| G1 | 6 | Gain option 2 (see Table 1) | VOP | 9 | Noninverting signal output |
| G2 | 5 | Gain option 3 (see Table 1) | VSOP | 11 | Positive output-stage low-voltage supply |
| G3 | 4 | Gain option 4 (see Table 1) | VSN | 16 | Negative high-voltage supply |
| G4 | 3 | Gain option 5 (see Table 1) | VSP | 13 | Positive high-voltage supply |

### Table 1. Gain Control

| G3:G0 | G4 = 0 | G4 = 1 |
|---|---|---|
| 0000 | 0.125 | 0.172 |
| 0001 | 0.25 | 0.344 |
| 0010 | 0.5 | 0.688 |
| 0011 | 1 | 1.375 |
| 0100 | 2 | 2.75 |
| 0101 | 4 | 5.5 |
| 0110 | 8 | 11 |
| 0111 | 16 | 22 |
| 1000 | 32 | 44 |
| 1001 | 64 | 88 |
| 1010 | 128 | 176 |
| 1011 | Reserved(1) (0.125) | Reserved(1) (0.172) |
| 1100 | Reserved(1) (0.125) | Reserved(1) (0.172) |
| 1101 | Reserved(1) (0.125) | Reserved(1) (0.172) |
| 1110 | Reserved(1) (0.125) | Reserved(1) (0.172) |
| 1111 | Reserved(1) (0.125) | Reserved(1) (0.172) |

(1) Reserved for test-modes. Default gain in parenthesis.

## TYPICAL CHARACTERISTICS

At $T_A$ = +25°C, VSP = +15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = +3 V, $R_L$ = 2.5 kΩ to VSOP/2 = VOCM, gain = 1 V/V, $V_{CM}$ = 0 V, and differential input and output, unless otherwise noted.

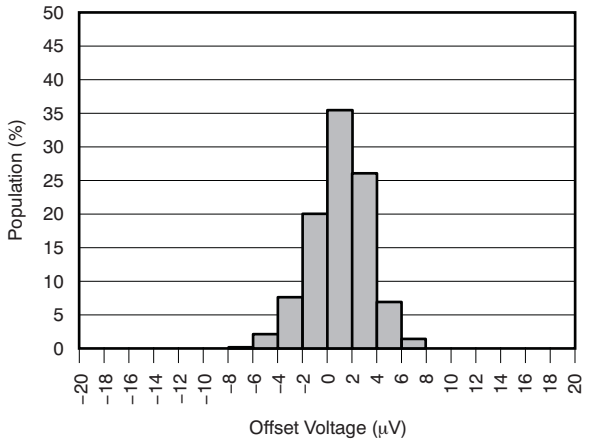



**Figure 1. OFFSET VOLTAGE PRODUCTION DISTRIBUTION (G = 128)**

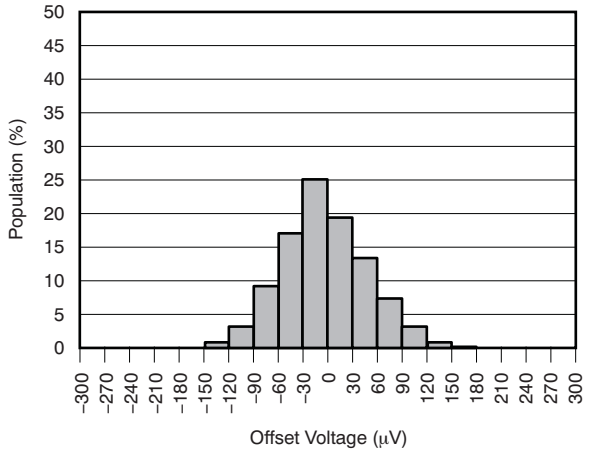



**Figure 2. OFFSET VOLTAGE PRODUCTION DISTRIBUTION (G = 1)**

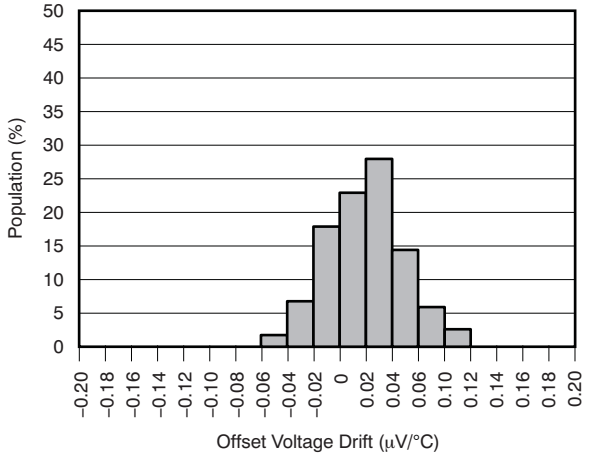



**Figure 3. OFFSET VOLTAGE DRIFT DISTRIBUTION (G = 128)**

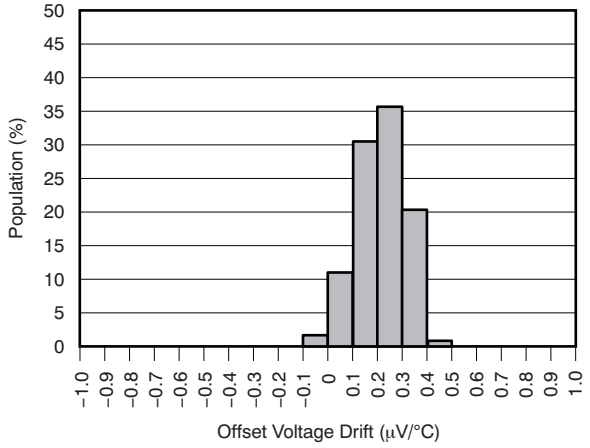



**Figure 4. OFFSET VOLTAGE DRIFT DISTRIBUTION (G = 1)**

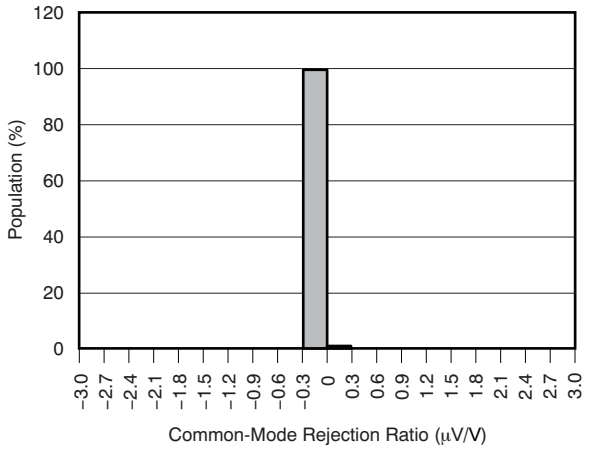



**Figure 5. COMMON-MODE REJECTION DISTRIBUTION (G = 128)**

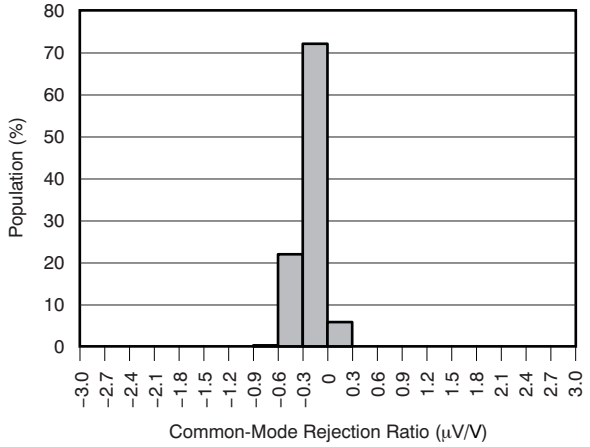



**Figure 6. COMMON-MODE REJECTION DISTRIBUTION (G = 1)**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, VSP = +15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = +3 V, $R_L$ = 2.5 kΩ to VSOP/2 = VOCM, gain = 1 V/V, $V_{CM}$ = 0 V, and differential input and output, unless otherwise noted.

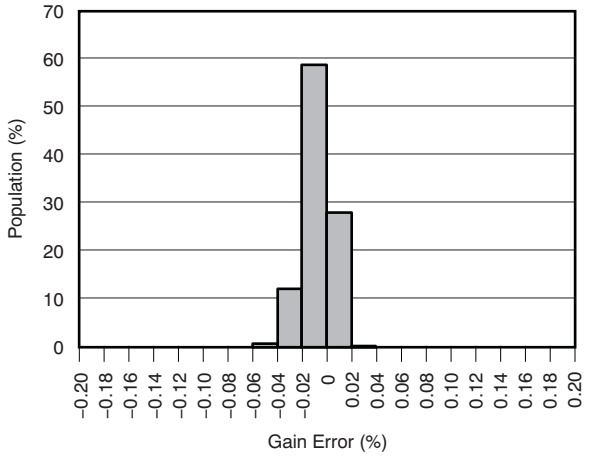



**Figure 7. GAIN ERROR DISTRIBUTION (G = 128)**

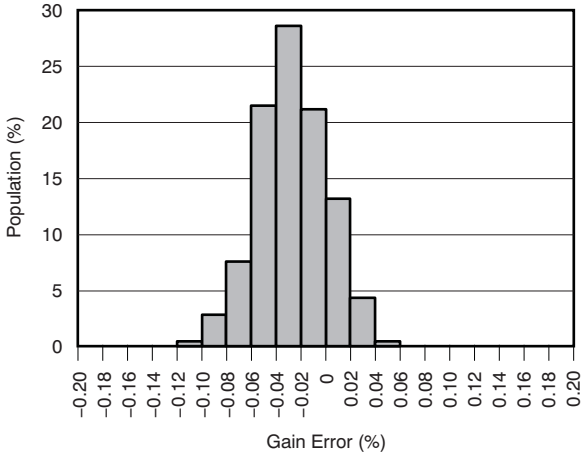



**Figure 8. GAIN ERROR DISTRIBUTION (G = 1)**

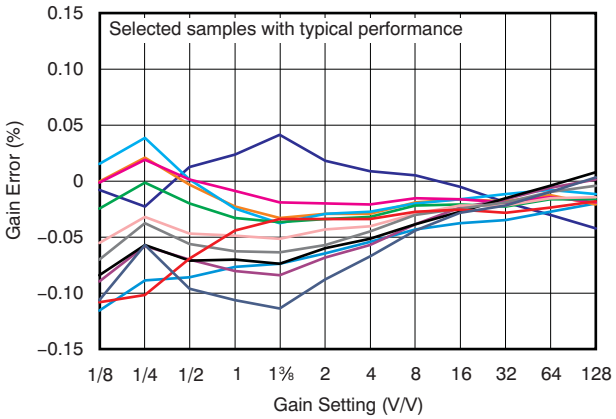



**Figure 9. GAIN ERROR vs GAIN SETTING**

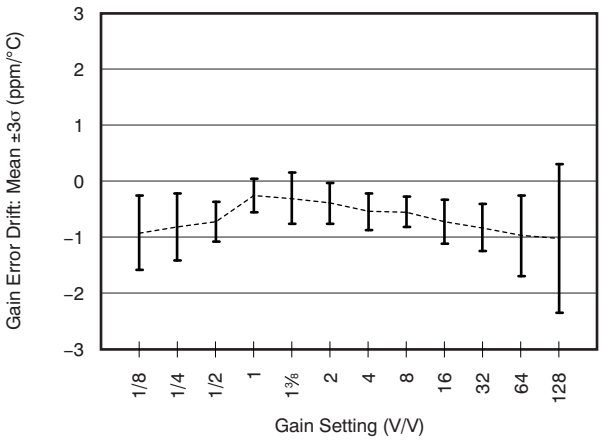



**Figure 10. GAIN ERROR DRIFT DISTRIBUTION vs GAIN SETTING (Mean with ±3 σ)**

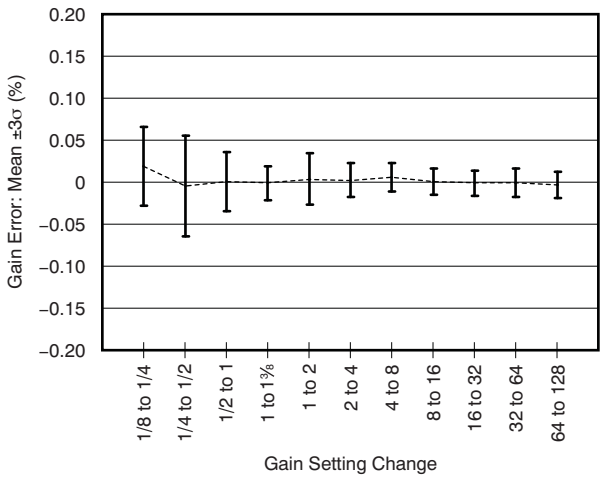



**Figure 11. MAXIMUM GAIN ERROR DEVIATION BETWEEN SEQUENTIAL GAIN SETTINGS (Mean with ±3 σ)**

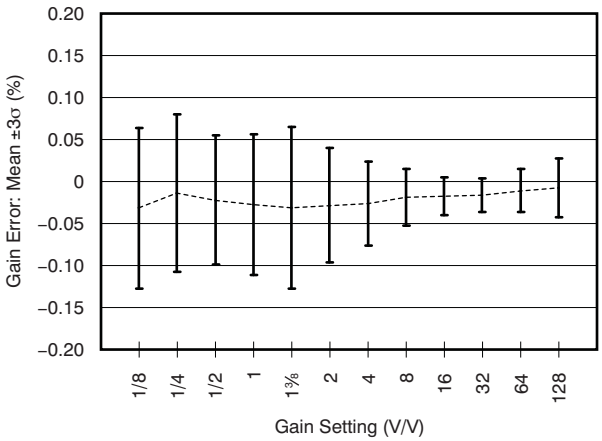



**Figure 12. GAIN ERROR DISTRIBUTION vs GAIN SETTING (MEAN with ±3σ)**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, VSP = +15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = +3 V, $R_L$ = 2.5 kΩ to VSOP/2 = VOCM, gain = 1 V/V, $V_{CM}$ = 0 V, and differential input and output, unless otherwise noted.

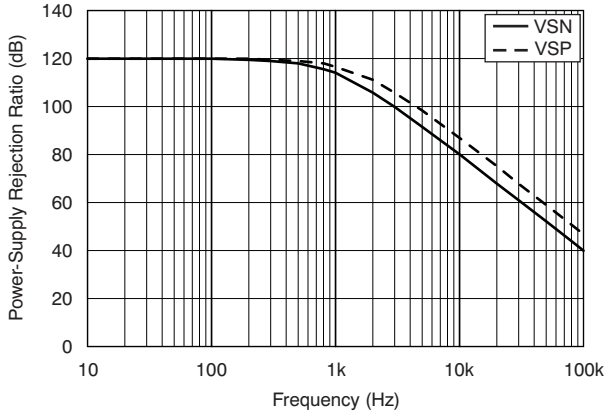



**Figure 13. POWER-SUPPLY REJECTION vs FREQUENCY**

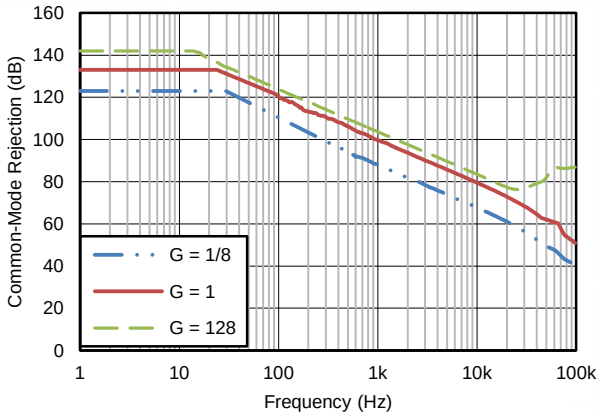



**Figure 14. COMMON-MODE REJECTION vs FREQUENCY**

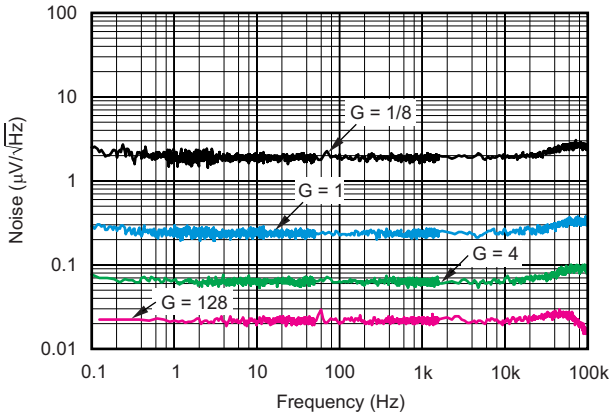



**Figure 15. INPUT-REFERRED NOISE SPECTRUM**

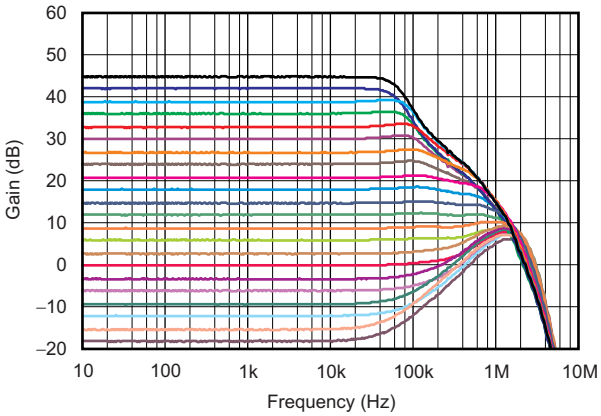



**Figure 16. SMALL-SIGNAL GAIN vs FREQUENCY**

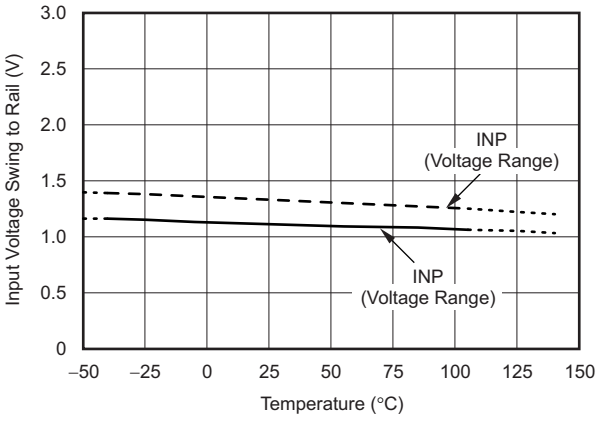



**Figure 17. INPUT VOLTAGE RANGE LIMITS vs TEMPERATURE**

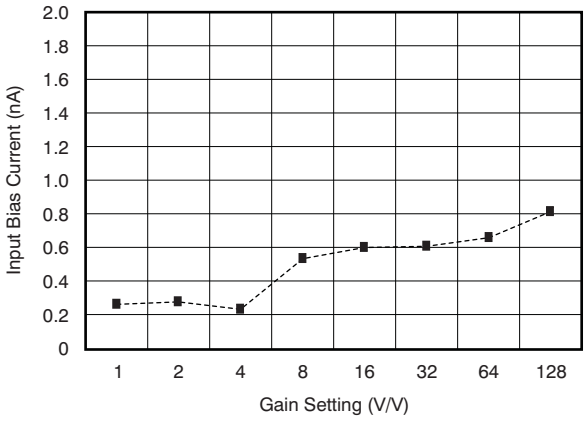



**Figure 18. BIAS CURRENT vs GAIN SETTING**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, VSP = +15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = +3 V, $R_L$ = 2.5 kΩ to VSOP/2 = VOCM, gain = 1 V/V, $V_{CM}$ = 0 V, and differential input and output, unless otherwise noted.

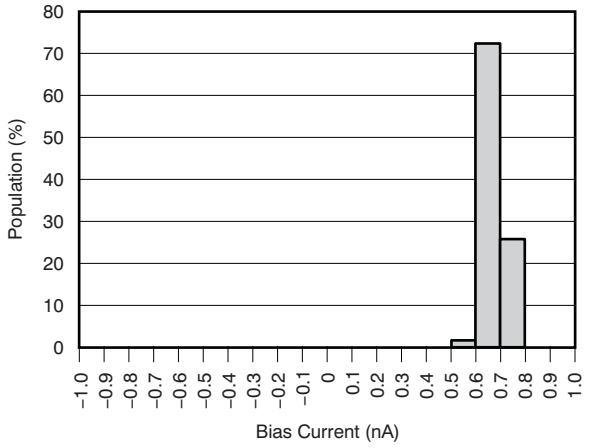



**Figure 19. INPUT BIAS CURRENT DISTRIBUTION (G = 128)**

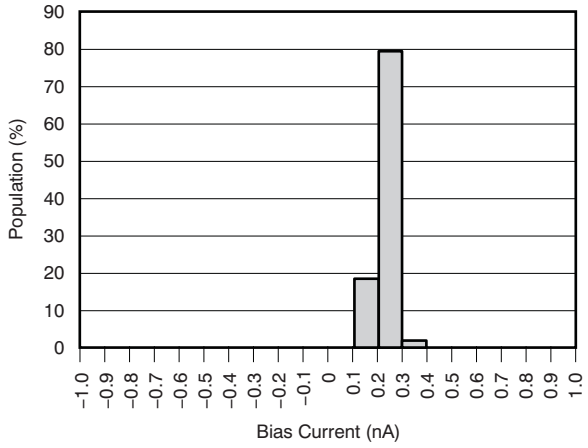



**Figure 20. INPUT BIAS CURRENT DISTRIBUTION (G = 1)**

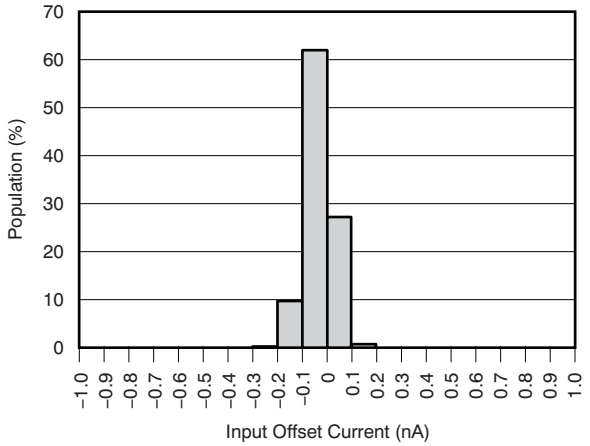



**Figure 21. INPUT OFFSET CURRENT DISTRIBUTION (G = 1, G = 128)**

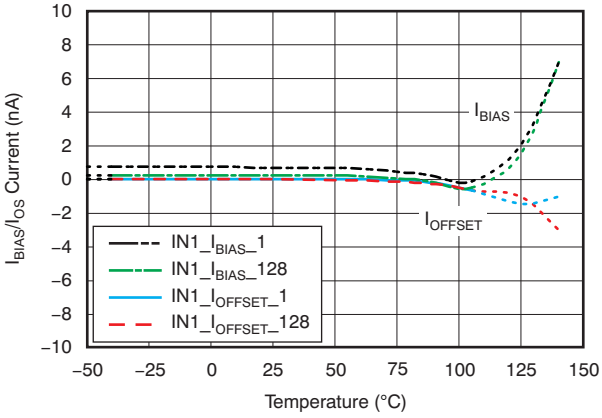



**Figure 22. INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE**

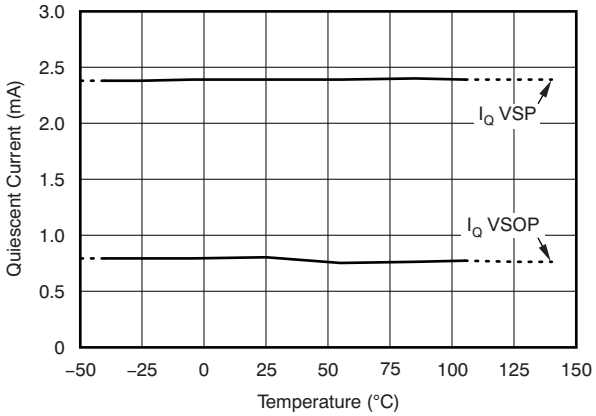



**Figure 23. QUIESCENT CURRENT FROM SUPPLIES (VSP AND VSOP) vs TEMPERATURE**

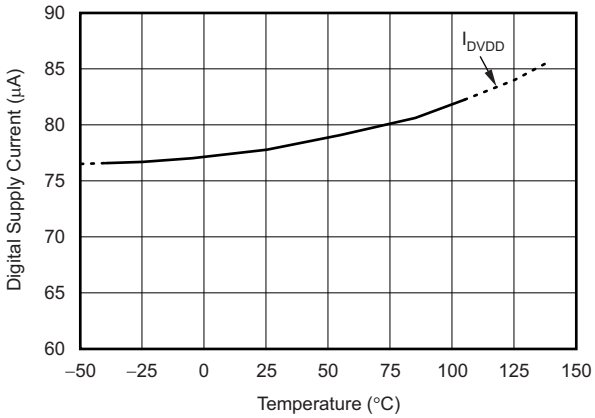



**Figure 24. DIGITAL SUPPLY CURRENT vs TEMPERATURE**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, VSP = +15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = +3 V, $R_L$ = 2.5 kΩ to VSOP/2 = VOCM, gain = 1 V/V, $V_{CM}$ = 0 V, and differential input and output, unless otherwise noted.

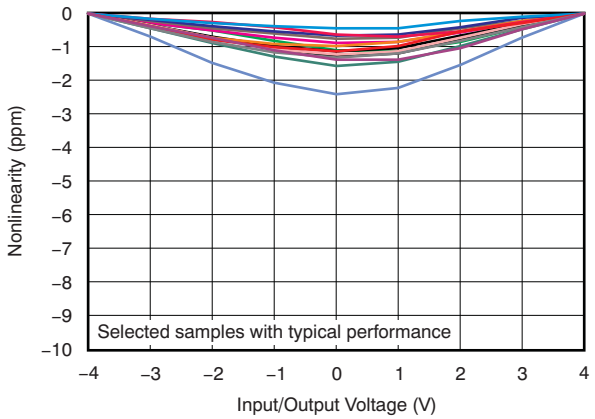



**Figure 25. GAIN NONLINEARITY WITH END-POINT CALIBRATION (G = 1)**

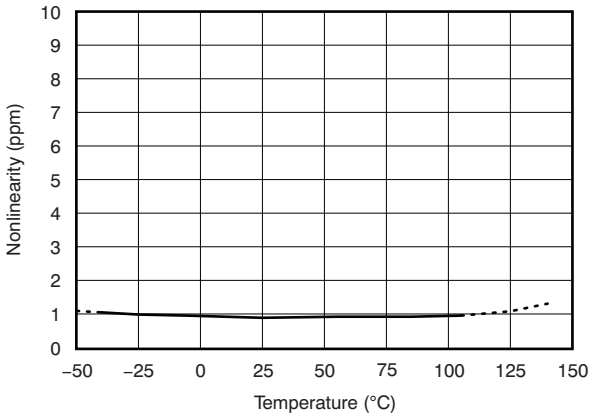



**Figure 26. GAIN NONLINEARITY vs TEMPERATURE**

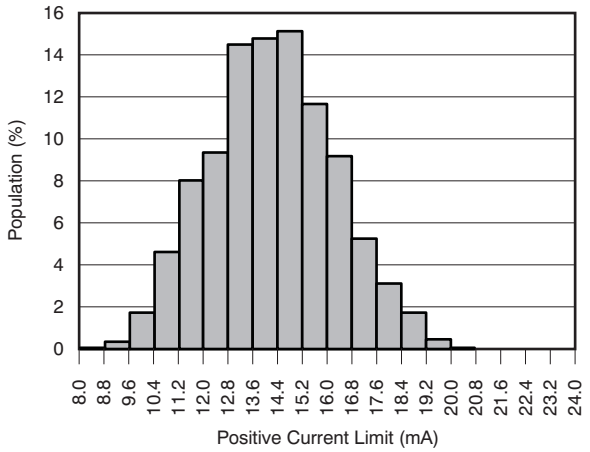



**Figure 27. POSITIVE OUTPUT CURRENT LIMIT DISTRIBUTION**

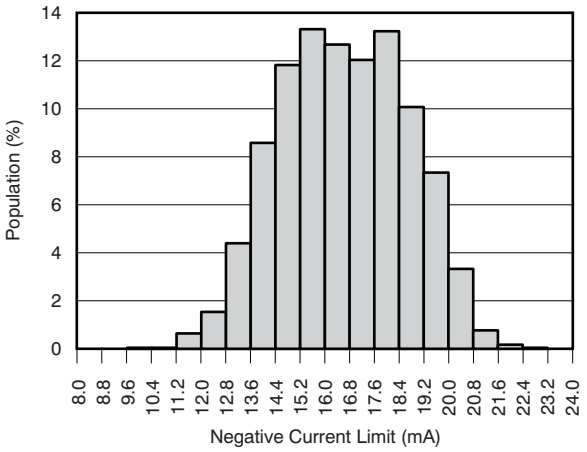



**Figure 28. NEGATIVE OUTPUT CURRENT LIMIT DISTRIBUTION**

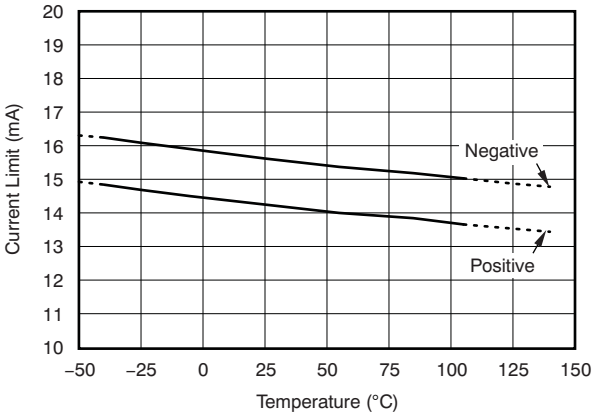



**Figure 29. OUTPUT CURRENT LIMIT vs TEMPERATURE**

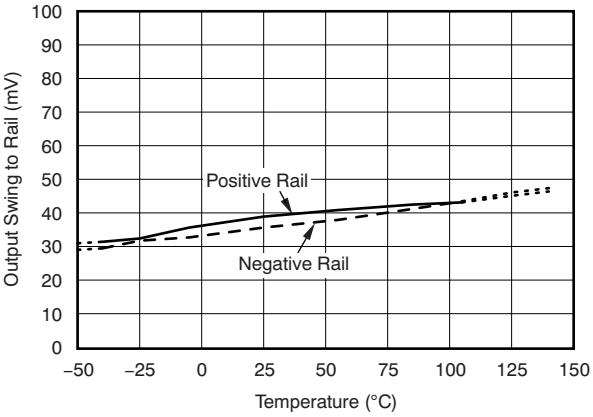



**Figure 30. OUTPUT SWING TO RAIL vs TEMPERATURE (VSOP – VSON = 5 V)**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, VSP = +15 V, VSN = –15 V, VSON = 0 V, VSOP = 5 V, DVDD = +3 V, $R_L$ = 2.5 kΩ to VSOP/2 = VOCM, gain = 1 V/V, $V_{CM}$ = 0 V, and differential input and output, unless otherwise noted.

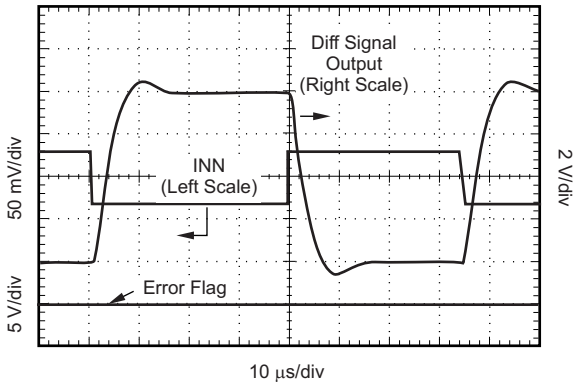



**Figure 31. STEP RESPONSE (G = 128)**

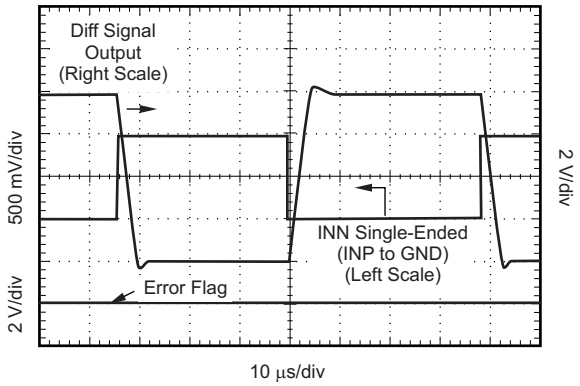



**Figure 32. STEP RESPONSE (G = 8)**

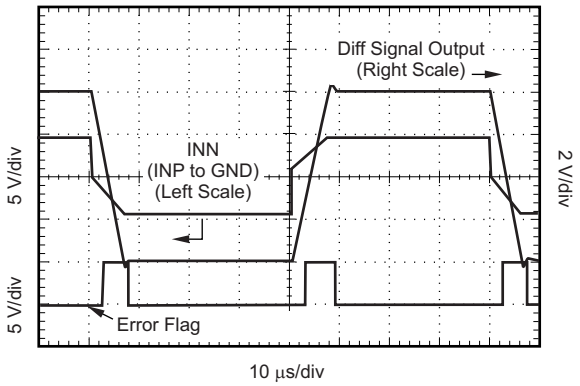



**Figure 33. STEP RESPONSE (G = 1)**

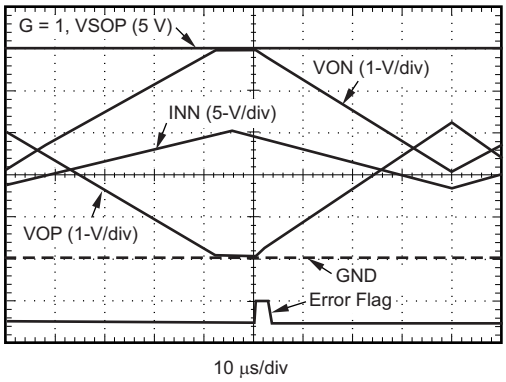



**Figure 34. OUTPUT OVERLOAD RECOVERY**

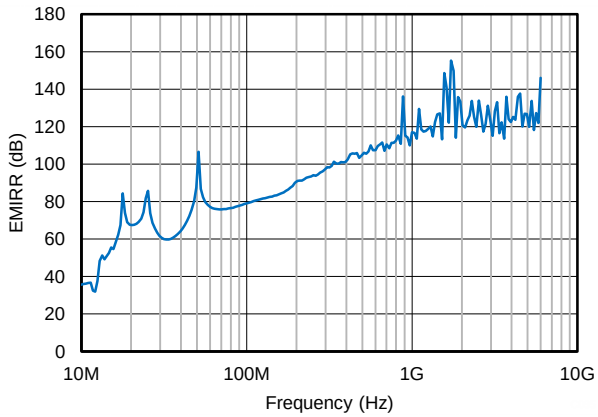



**Figure 35. COMMON MODE EMIRR**

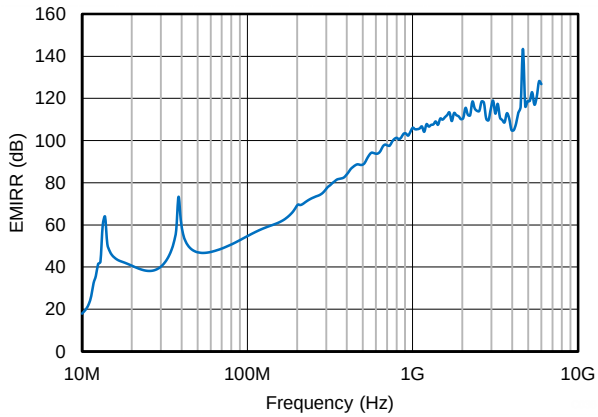



**Figure 36. DIFFERENTIAL MODE EMIRR**

# APPLICATION INFORMATION

## DESCRIPTION

The PGA281 is a universal high-voltage instrumentation amplifier with digital gain control. It offers excellent dc precision and long-term stability using modern chopper technology with internal filters that minimize chopper-related noise. The input gain extends from ⅛ V/V (attenuation) to 128 V/V in binary steps. The output stage offers a gain multiplying factor of 1 V/V or 1⅜ V/V for optimal gain adjustment. The output stage connects to the low-voltage (for example: 5 V or 3 V) supply. Figure 37 shows a block diagram of the PGA281.

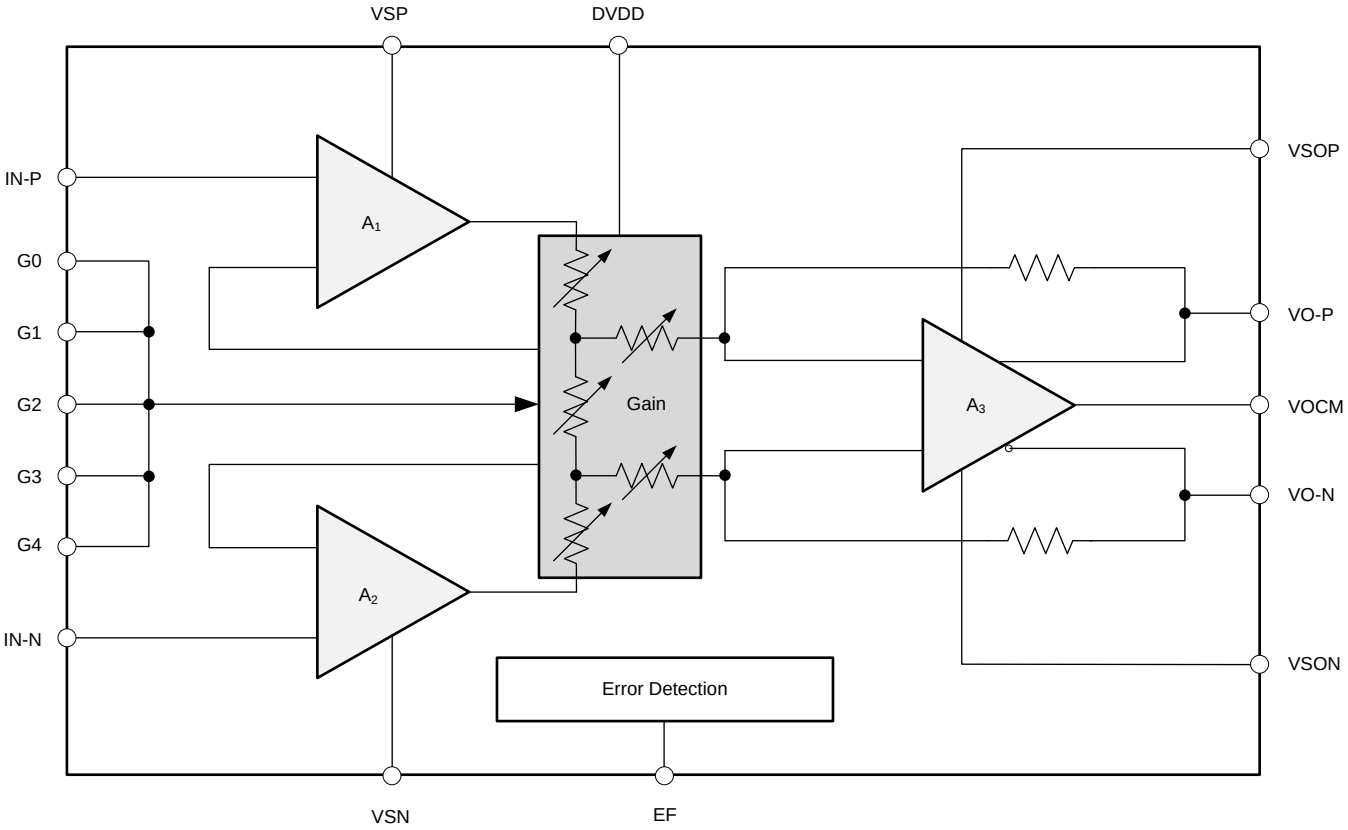



**Figure 37. Block Diagram**

The supply voltage of up to ±18 V offers a wide common-mode range with high input impedance; therefore, large common-mode noise signals and offsets can be suppressed.

The fully differential signal output is compatible with the inputs of modern high-resolution and high-accuracy analog-to-digital converters (ADCs), including delta-sigma (ΔΣ) as well as successive-approximation register (SAR) converters. The supply voltage for the output stage is normally connected to the converter supply, thus preventing signal overloads from the high-voltage analog supply.

Internal error detection in the input and output stage monitors signal integrity and provides information about the input signal condition on the EF pin output.

The gain is set using digital inputs G4:G0 (pins 3, 4, 5, 6, and 7). Select the desired gain according to the settings in Table 1. Logic high and low levels are with respect to the voltage on DVDD (pin 1) and VSON (pin 12). The limits are specified in the *Digital I/O* section of the Electrical Characteristics.

## FUNCTIONAL BLOCKS

The PGA281 has two high-impedance input amplifiers (see Figure 37, $A_1$ and $A_2$) that are symmetrical and low noise, with excellent dc precision. These amplifiers are connected to a resistor network and provide a gain range from 128 V/V down to an attenuation of ⅛ V/V. The PGA281 architecture rejects common-mode offsets and noise over a wide bandwidth.

The signal inputs are diode-clamped to the supply rails. To provide overvoltage protection, place external resistors in series to the inputs. Limit current into the input pins to ≤ 10 mA.

The output stage ($A_3$) provides a fully-differential symmetrical signal around the output reference pin, VOCM. The VOCM pin is a high-impedance input and must be driven with an external voltage, typically close to midsupply. The 3-V or 5-V supply of the converter or amplifier, following the PGA281 outputs, is normally connected to VSOP and VSON; this configuration shares a common supply voltage and protects the circuit from overloads. The fully-differential signal avoids coupling of noise and errors from the supply and ground, and allows large signal swing without the risk of nonlinearities that arise when driving near the supply rails.

The PGA281 signal path has several internal nodes monitored for critical overload conditions. The input amplifiers detect signal overvoltage and overload as a result of high gain. The output stage also detects clipping.

### Input Amplifiers and Gain Network

The high-precision input amplifiers present very low dc error and drift as a result of a modern chopper technology with an embedded synchronous filter that removes nearly all chopping noise. This topology reduces flicker (1/f) noise to a minimum, and therefore enables the precise measurement of small dc-signals with high resolution, accuracy, and repeatability. The chopping frequency of 250 kHz is derived from an internal 1-MHz clock.

The gain network for the binary gain steps connects to the input amplifiers, thus providing the best possible signal-to-noise ratio (SNR) and dc accuracy up to the highest gains. Gain is digitally programmable by pins G4:G0. The input stage provides selectable gains (in V/V): 128, 64, 32, 16, 8, 4, 2, 1, ½, ¼, and ⅛. The G4 pin provides an additional gain multiplication factor on the output stage of 1 V/V or 1⅜ V/V. This allows for optimal gain fine-tuning, and increases the maximum gain of the PGA281 to 176 V/V.

Programmable gain amplifiers such as the PGA281 use internal resistors to set the gain. Consequently, quiescent current is increased by the current that passes through these resistors. The largest amplitude may increase the supply current by ±0.4 mA. For example, in a maximum overload condition, with a gain of 128 V/V, and with each of the inputs connected to the opposite supply voltage, a current of approximately 27 mA is measured. External resistors in series with the input pins are normally present and help to avoid this extreme condition. This current is only limited by the internal 600 Ω.

### Digital Inputs

Digital inputs G0, G1, G2, G3, and G4, select the gain according to the settings shown in Table 1. Logic high and low levels are with respect to the voltage on DVDD (pin 1) and VSON (pin 12). The logic limits are specified in the *Digital I/O* section of the Electrical Characteristics. Approximately 0.2 µA flows out of the digital input pins when a logic '0' is applied. Logic input current is nearly zero with a logic '1' input.

Digital inputs G4:G0 are not latched; a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately 1 µs. The time to respond to gain change is effectively the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see the settling times specified in the *Frequency Response* section of the Electrical Characteristics). Many applications use an external logic latch to access gain control data from a high-speed data bus. Using an external latch isolates the high-speed digital bus from sensitive analog circuitry. Place the latch circuitry as far as practical from analog circuitry.

### Output Stage

The output stage power supply is usually connected to the low-voltage supply (normally 3 V or 5 V) that is used by the subsequent signal path of the system. This design prevents overloading of the low-voltage signal path.

The output signal is fully differential around the common-mode voltage (VOCM). The VOCM input pin is typically connected to the midsupply voltage in order to offer the widest signal amplitude range. VOCM is a high-impedance input that requires an external connection to a voltage within the supply boundaries. If the VOCM pin is left floating, the output common-mode voltage is undefined, and the amplifier will not operate properly. The usable voltage range for the VOCM input is specified in the Electrical Characteristics and must be observed.

The output stage can be set to a gain of 1V/V or 1⅜V/V with the G4 pin logic level. This option allows for additional gain fine tuning.

Figure 38 shows how signal outputs VOP and VON swing symmetrically around VOCM. The signal is represented as the voltage between the two outputs and does not require an accurate VOCM. Therefore, the signal output does not include ground noise or grounding errors. Noise or drift on VOCM is normally rejected by the common-mode rejection capability of the subsequent signal stage. By using a differential output stage, the PGA281 achieves large voltage swings on a single 3-V or 5-V supply.

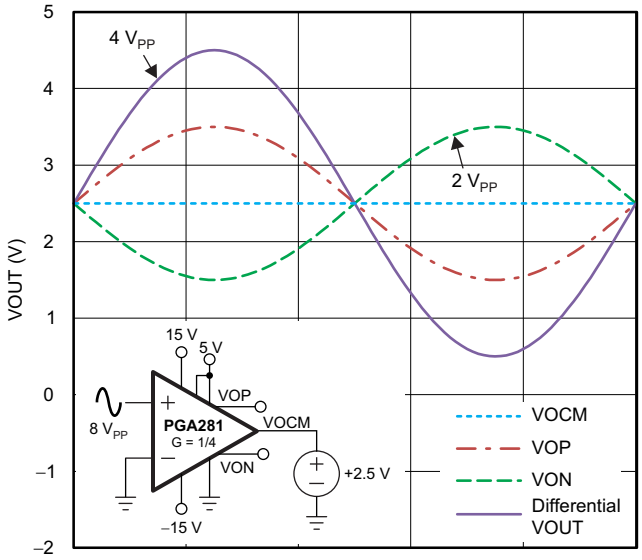



**Figure 38. Differential Output Voltage**

The output signal is internally monitored for two error conditions: clipping of the signal to the supply rail and overcurrent. In fault conditions, an error flag bit is set high until the fault is removed.

### Electrical Overstress

Designers often ask questions about the capability of an amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal ESD protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 39 illustrates the ESD circuits contained in the PGA281. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines. This protection circuitry is intended to remain inactive during normal circuit operation.

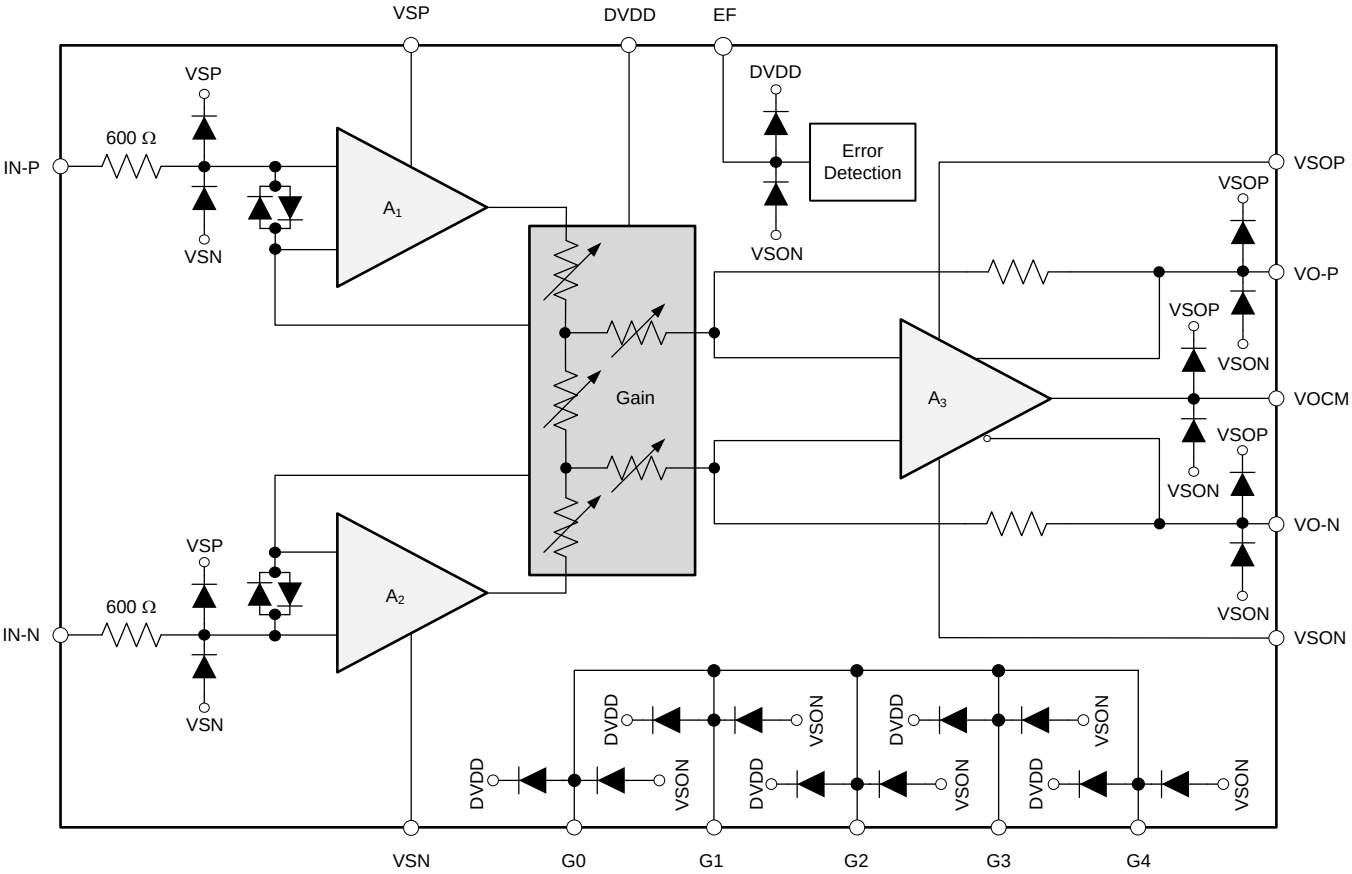



**Figure 39. Equivalent Internal ESD Circuitry**

The PGA281 input terminals are protected with internal diodes connected to VSP and VSN. If the input signal voltage exceeds the power-supply voltage (VSP and VSN), limit the current to less than 10 mA to protect the internal clamp diodes. This current-limiting can usually be accomplished with a series input resistor.

### EMI Rejection

The PGA281 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications, and densely-populated boards with a mix of analog signal chain and digital components. The PGA281 is specifically designed to minimize susceptibility to EMI by incorporating an internal low-pass filter. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system, as well as incorporating known good practices such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing. Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum, extending from 10 MHz to 6 GHz. This method uses EMI rejection ratio (EMIRR) to quantify the PGA281 ability to reject EMI. Figure 40 and Figure 41 show the PGA281 EMIRR graph for both differential and common-mode EMI rejection across this frequency range. Table 2 shows the EMIRR values for the PGA281 at frequencies commonly encountered in real-world applications. Applications listed in Table 2 may be centered on or operated near the particular frequency shown.

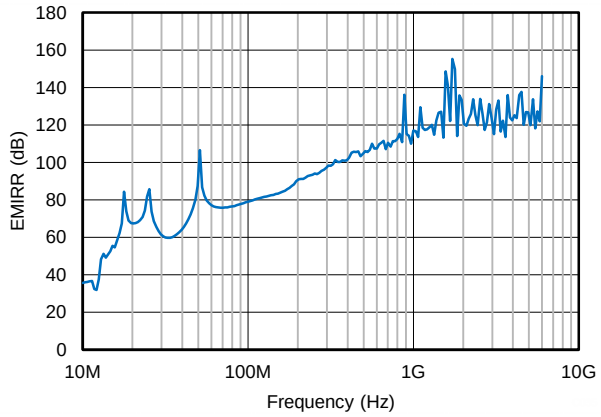



**Figure 40. Common Mode EMIRR Testing**

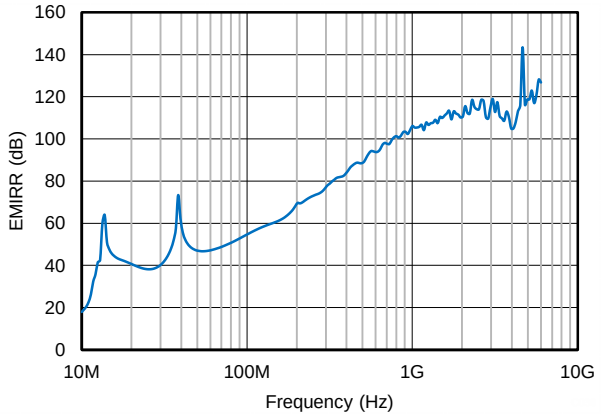



**Figure 41. Differential Mode (IN-P) EMIRR Testing**

**Table 2. PGA281 EMIRR for Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION | DIFFERENTIAL (IN-P) EMIRR | COMMON-MODE EMIRR |
|---|---|---|---|
| 400 MHz | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications | 84.3 dB | 101.8 dB |
| 900 MHz | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications | 103.3 dB | 125.6 dB |
| 1.8 GHz | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz) | 112.5 dB | 131.8 dB |
| 2.4 GHz | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz) | 114.6 dB | 122.4 dB |
| 3.6 GHz | Radiolocation, aero communication and navigation, satellite, mobile, S-band | 108.9 dB | 113.5 dB |
| 5.0 GHz | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz) | 118.7 dB | 123.3 dB |

### Output Filter

The PGA281 uses a chopper-stabilized architecture for excellent dc stability over temperature and life of operation. The device also removes 1/f frequency (flicker) noise, and therefore enables both high resolution and high repeatability for dc measurements. Although the chopper noise components are internally filtered, a minimal residual amount of high-frequency switching noise appears at the signal outputs. Placing an external, passive, low-pass filter after the output stage is recommended to remove this switching noise; Figure 42 shows two examples. This filter can also be used to isolate or decouple the charge switching pulses of an ADC input.

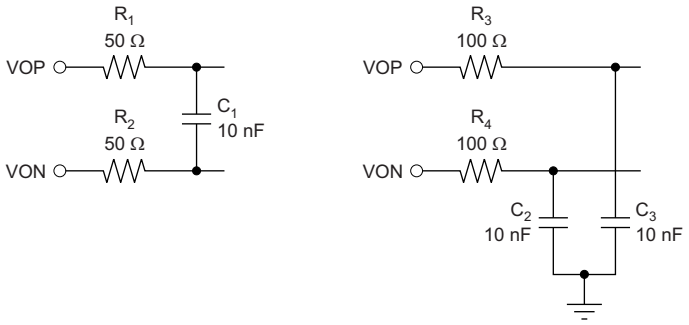



**Figure 42. Typical Examples of Recommended Output Filters**

### Single-Ended Output

The output stage of the PGA281 is designed for highest precision. The fully-differential output avoids grounding errors and noise, and delivers twice the signal amplitude compared to single-ended signals. However, if desired, a single-ended output (VOP or VON) can be measured, referred to the voltage at the VOCM pin. The output stage errors now relate to half the signal amplitude and half the signal gain. Figure 43 shows how the unused output is unconnected, but not disconnected from error detection. The usable voltage range for the VOCM input is specified in the Electrical Characteristics and must be observed; that is, the output swing (of both outputs) should not saturate to the supply. Separate specifications for offset voltage and drift indicate higher offset voltage at lower gains because some error sources are not cancelled in the output stage connected in single-ended mode. Note that the gain is one-half of the gain set in reference to the gain table (see Table 1).

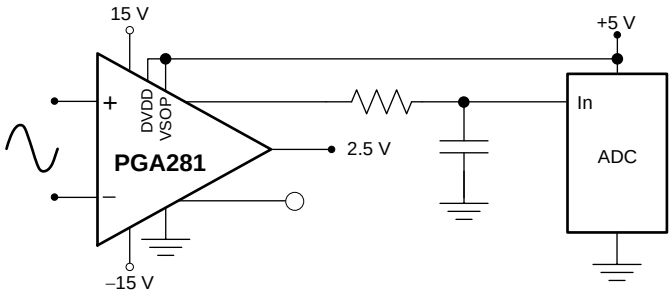



**Figure 43. Single-Ended Connection Example**

## ERROR INDICATORS

### Error Flag Detection

The PGA281 is designed for high dc precision and universal use, but it also allows monitoring of signal integrity. This error flag pin (EF, pin 2) alerts if an error is detected in one of the diagnostic areas specified in Figure 44. The error flag is a logic low during normal operation, but alarms to a logic high level when in an error state. The pin returns to normal operation (logic low) after the error state is removed. This added feature supports fully automated system setup and diagnostic capability while maintaining signal integrity. Figure 44 illustrates the diagnostic points available for error detection in the device architecture.

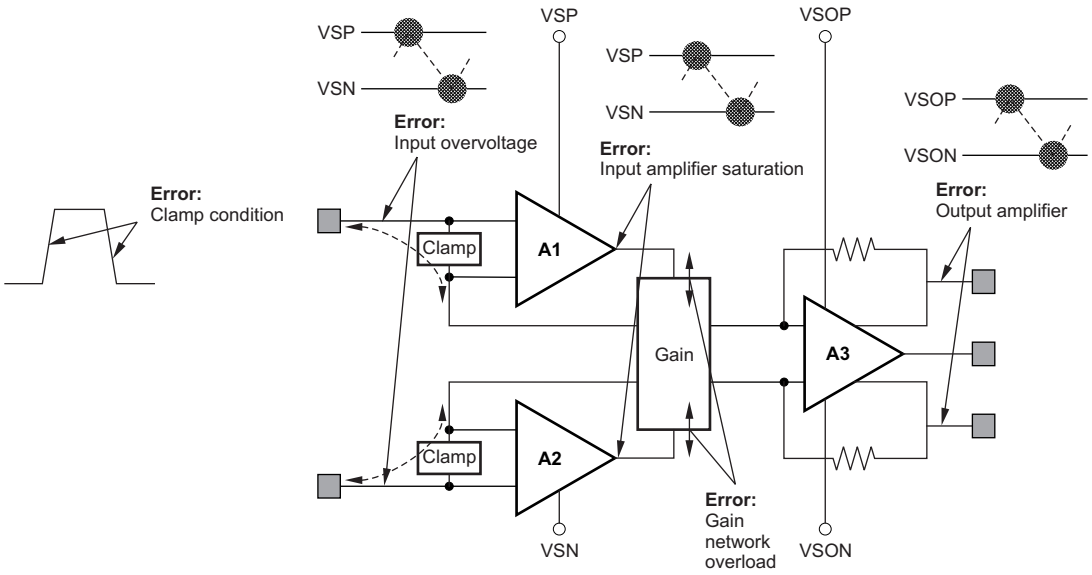



**Figure 44. Diagnostic Points for Error Detection**

### Input Clamp Conduction

The input clamp protects the precision input amplifier from large voltages between the inputs caused by a fast signal slew rate in the input. This clamp circuit conducts current from the input pins during overload. Current flowing through the clamp can influence the signal source and cause long settling delays on passive input signal filters. The current is limited by internal resistors of approximately 600 Ω. Note that dynamic overload can result from the difference signal as well as the common-mode signal.

The input clamp turns on when the input signal slew rate is greater than ±1 V/µs and faster than the amplifier slew rate (specified in the *Frequency Response* section of the Electrical Characteristics). Appropriate input filtering avoids input clamp activation.

### Input Overvoltage

The input amplifier can only operate at high performance within a certain input voltage range inside the supply rail. The error flag (EF pin) alarm indicates a loss of performance as a result of the input voltage or the amplifier output approaching the rail.

### Gain Network Overload

The gain setting network is protected against overcurrent conditions that occur because of an improper gain setting. The current into the resistors is proportional to the voltage between both inputs and the internal resistor; a low resistor value results in high gains. The error flag alarms if such an overload condition results from an improper gain setting.

### Output Amplifier

The output stage is monitored for signal clipping to the supply rail and for overcurrent conditions.

## POWER SUPPLY

The PGA281 requires three supply voltages: the high-voltage analog supply, the low-voltage output amplifier supply, and the digital I/O supply. This architecture allows an optimal interface (level-shift) to the different supply domains.

The high-voltage analog supplies, VSP and VSN, power the high-voltage input stage section. The substrate of the device is connected to VSN; therefore, it must be connected to the most negative potential.

The low-voltage analog output supplies, VSOP and VSON, operate within the high-voltage supply boundaries with two minimal limitations:

1. The usable range for VSON is from a minimum 5 V below VSP to as low as VSN. This 5 V provides the headroom for the output supply voltage of +2.7 V to +5 V. Even with less than a 5-V supply, this voltage difference is required for proper operation.
2. The common-mode control input, VOCM, requires a voltage at least 2 V less than VSP in order to support internal rail-to-rail performance.

These limitations are applicable when using a minimum supply or an extremely asymmetrical high-voltage supply. In most practical cases, VSON is connected to the ground of the system 3-V or 5-V supply.

VSOP can be turned on first or can be higher than VSP without harm, but operation fails if VSP and VSN are not present.

Observe the maximum voltage applied between VSOP and VSON because there is no internal protection.

Positive digital supply DVDD and digital ground VSON can also be set within the boundaries of VSP and VSN. However, DVDD must be 1 V less than VSP. DVDD can be turned on without the analog supply being present and is operational. Observe the maximum supply voltage because there is no internal protection. VSOP can be connected with DVDD if desired.

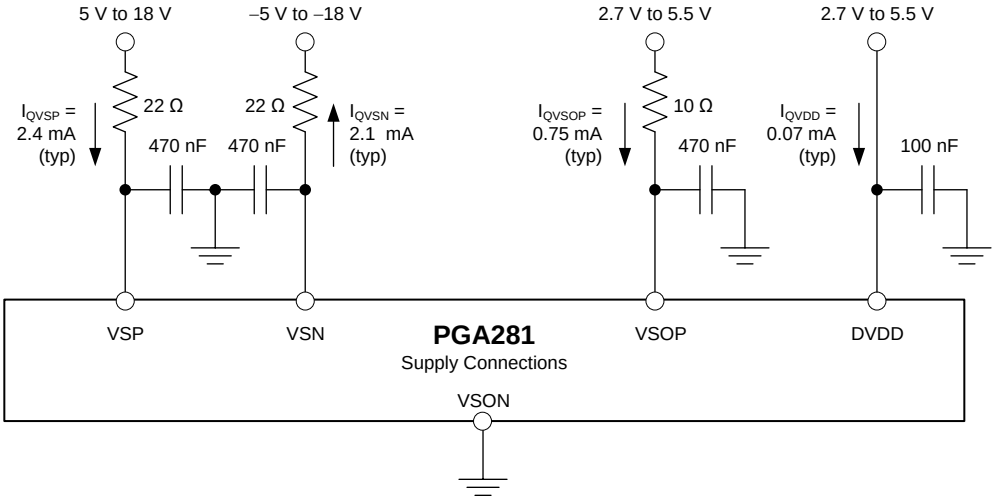
The negative digital supply is connected to the VSON pin. Take care if using split supplies on the VSOP and VSON pin because the logic low and high thresholds are determined by DVDD and VSON. In normal operation, VSON is connected to the system ground.

VSN is connected to the substrate; therefore, the voltage at VSON must not turn on the substrate diode to VSN. Use external Schottky diodes from VSON to VSN to prevent this condition.

The PGA281 uses an internal chopper-stabilized architecture, and requires good supply decoupling. RC decoupling using series resistors in the supply is recommended. Series resistors can be in the range of 15 Ω to 22 Ω. RC decoupling also prevents a very fast rise time of the supply voltage, thus avoiding parasitic currents in the device. Connecting supply wires into an already turned-on supply (very fast rise time) without such a filter can damage the device as a result of voltage overshoot and parasitic charge currents. Figure 45 shows an example of a supply connection using RC bypass filters. DVDD may not need decoupling, but if the digital supply is noisy, a filter is recommended.

**NOTE**

Rise and fall times for the high-voltage supplies must be slower than 1 V/µs.




NOTE: The supply voltages shown are only example values.

**Figure 45. Supply Connection Example Using RC Bypass Filters for Good Decoupling**

## Quiescent Current

The PGA281 uses internal resistor networks and switches to set the signal gain. Consequently, the current through the resistor network may vary with the gain and signal amplitude. Under normal operation, the gain-related current is low (less than 400 µA). However, in signal overload conditions while a high gain is selected, this amount of current may increase.

## Settling Time

The PGA281 provides very low drift and low noise, and therefore allows repeatable settling to a precise value. Signal-related load and power-dissipation variables have minimal effect on device accuracy.

## Overload Recovery

Overload conditions can vary widely and there are multiple points in an instrumentation amplifier that can be overloaded. During input overload, the PGA281 folds the output signal partially back as a result of the differential signal structure and summing, but the error flag indicates such fault conditions. The amplifier recovers safely after removing the overload condition, as long as it is within the specified operating range as shown in Figure 46.

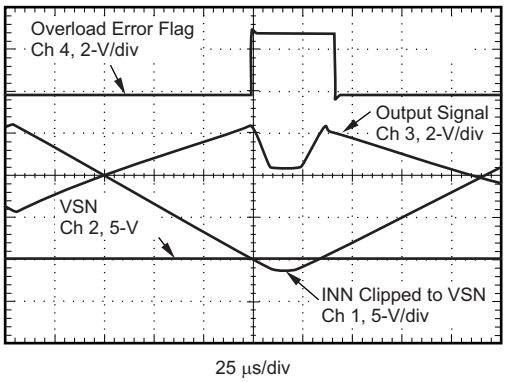



**Figure 46. Input Clipping: Negative Side**

Avoid dynamic overload by using adequate signal filtering that reduces the input slew rate to the slew rate of the amplifier.

## Input Bias Current Return Path

The input impedance of the PGA281 is extremely high; greater than 1 GΩ. However, make sure to provide a path for the input bias current of both inputs. This input bias current is typically 300 pA. A high input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 47 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the PGA281, and the input amplifiers saturate. If the differential source resistance is low, connect the bias current return path to one input (as shown in the thermocouple example in Figure 47). With higher source impedance, using two equal resistors provides a balanced input with the possible advantage of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

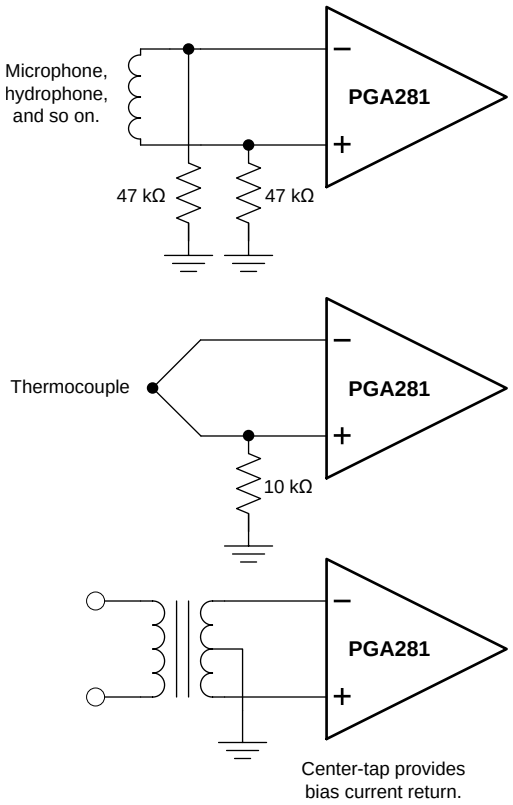



**Figure 47. Providing an Input Common-Mode Current Path**

## Application Examples

### Multiplexed Data Acquisition

Figure 48 shows the PGA281 used in a multiplexed data-acquisition application.

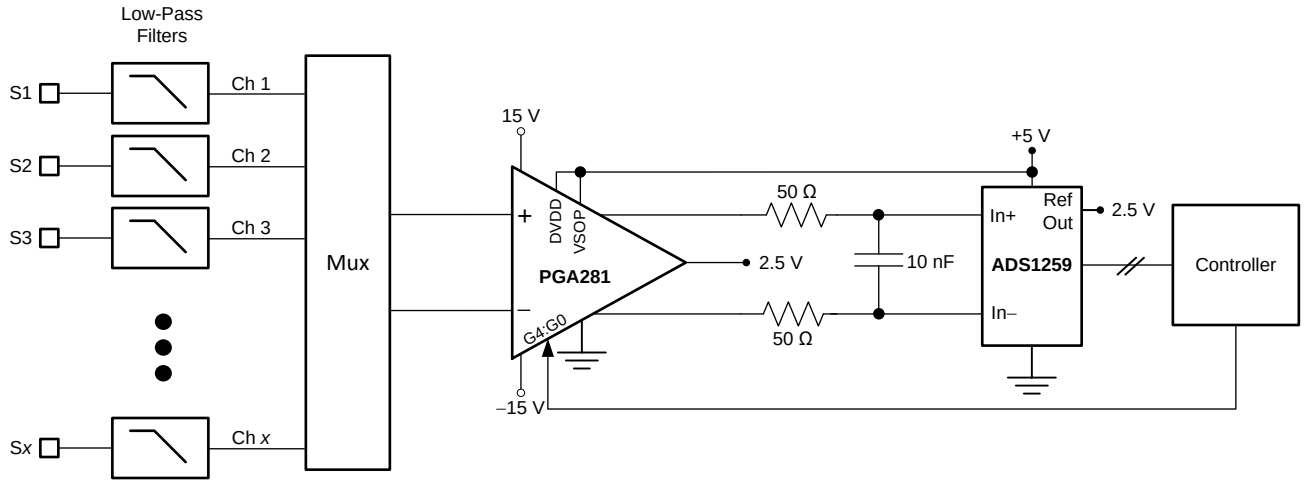



**Figure 48. Typical Block Diagram for Multiplexed Data Acquisition**

### Programmable Logic Controller (PLC) Input

An example of the PGA281 used in a programmable logic controller (PLC) input application is shown in Figure 49 .

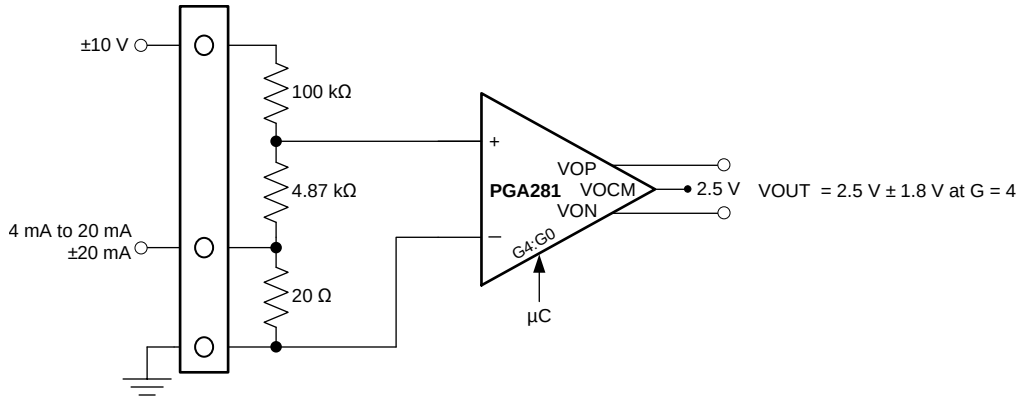



**Figure 49. ±10-V, 4-mA to 20-mA PLC Input**

### SAR ADC Driver

An example of the PGA281 used as a SAR ADC driver with the THS4031 used as input buffers to maximize SNR and THD is shown in Figure 50 .

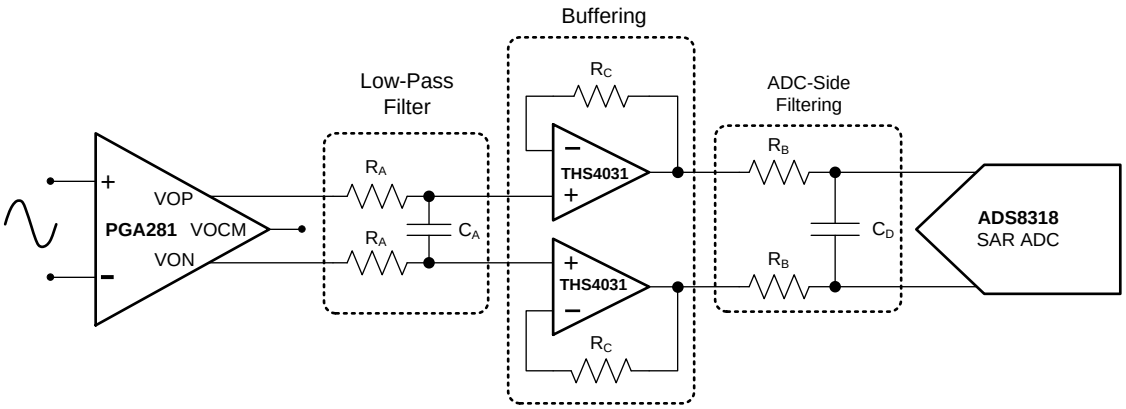



**Figure 50. SAR Driver with Input Buffer**

### Using TINA-TI™ SPICE-Based Analog Simulation Program with the PGA281

TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. It provides all the conventional dc, transient, and frequency-domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways.

Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

**NOTE**

**NOTE:** These files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

### Two-Terminal Programmable Logic Controller

The circuit in Figure 51 is used to convert inputs of ±10 V, ±5 V, or ±20 mA to an output voltage range from 0 V to 5 V. The input selection depends on the settings of the switch and the PGA281 gain. Further explanation, as well as the TINA-TI simulation circuit, is provided in the compressed file that can be downloaded at the following link: PGA281 PLC Circuit.

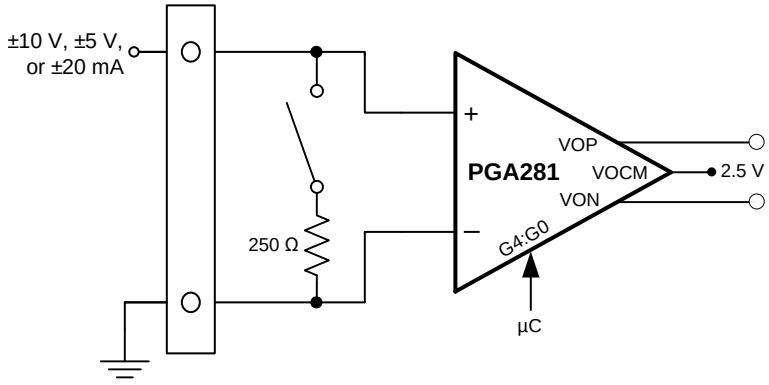
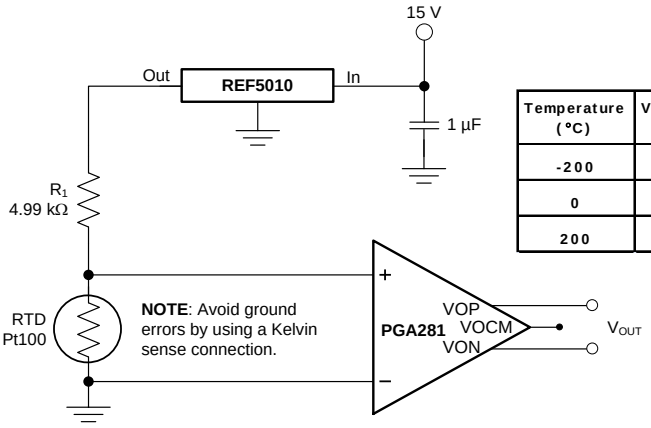



**Figure 51. Two-Terminal, Programmable Logic Controller (PLC) Input**

### RTD Amplifier

An example of the PGA281 used in an RTD-amplification application is shown in Figure 52. Click the following link to download the TINA-TI file: PGA281 RTD.




| Temperature (°C) | VOUT at G = ½ | VOUT at G = 1 | VOUT at G = 2 | VOUT at G = 4 |
|---|---|---|---|---|
| -200 | 0.03 | 0.06 | 0.11 | 0.22 |
| 0 | 0.15 | 0.29 | 0.59 | 1.18 |
| 200 | 0.26 | 0.51 | 1.02 | 2.04 |

**Figure 52. RTD Amplifier**

### High-Side Current Sensing

Figure 53 shows an example of how the PGA281 can be used for high-side current sensing. The load current ($I_{LOAD}$) creates a voltage drop across the shunt resistor ($R_{SHUNT}$). This voltage can be amplified or attenuated by the PGA281. The wide gain options and excellent common-mode rejection of the PGA281 make it ideal for this type of application. Click the following link to download the TINA-TI file: PGA281 Current Sense.

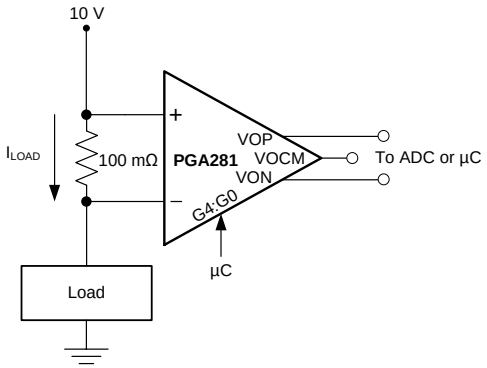



**Figure 53. High-Side Current Sensing**

### Bridge Amplifier

An example of the PGA281 used in a bridge or strain gauge amplification application is shown in Figure 54. Click the following link to download the TINA-TI file: PGA281 Bridge Amplifier.

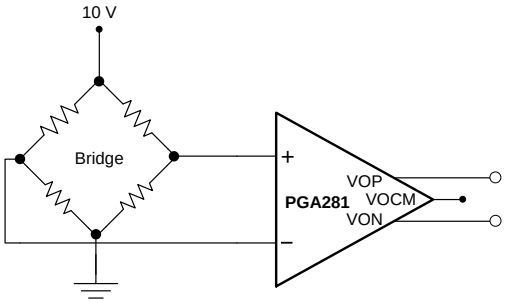



**Figure 54. Programmable Bridge Amplifier**

## Evaluation Module

The PGA281EVM provides basic functional evaluation of the PGA281. A picture of the PGA281EVM is provided in Figure 55.

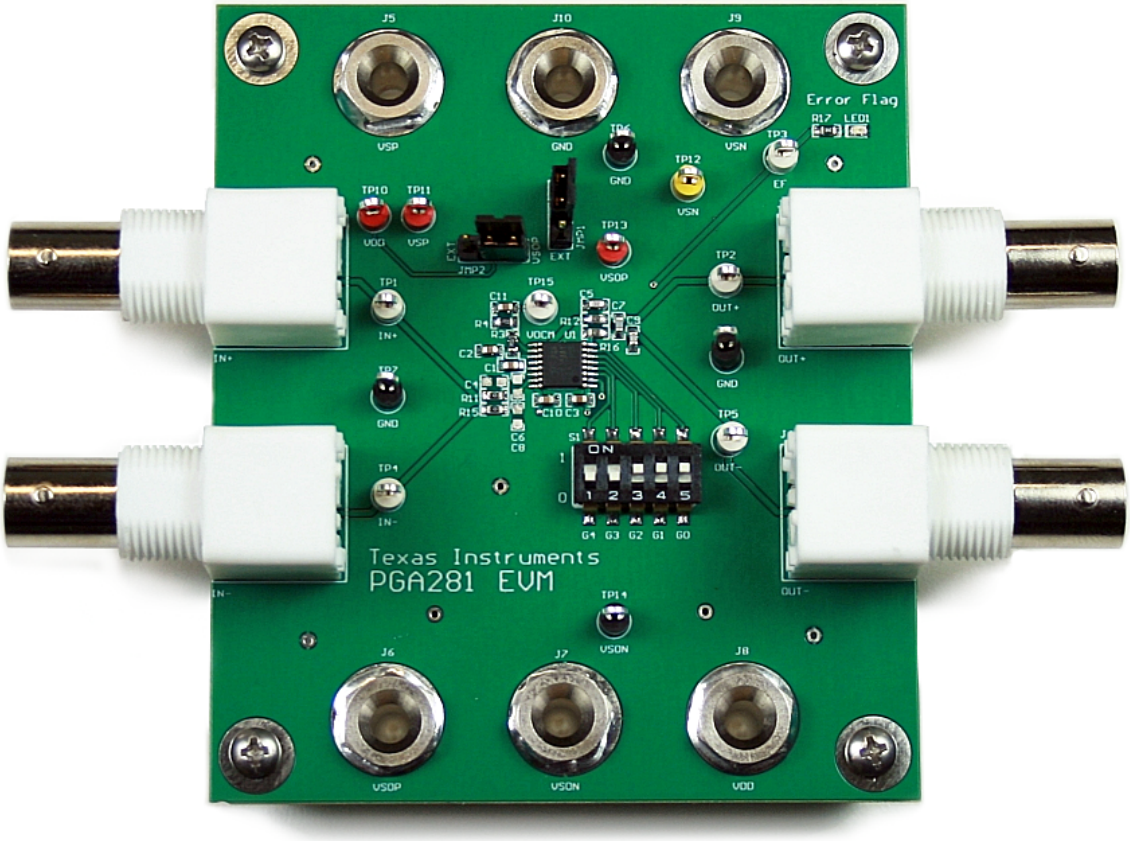



**Figure 55. PGA281 Evaluation Module**

The PGA281 evaluation module provides the following features:

- Easy access to nodes with surface-mount test points
- Convenient input and output filtering
- Simple gain setting and error flag indication

The PGA281EVM User Guide (SBOU130, available for download at www.ti.com) provides instructions on how to set up the device for evaluation. The user guide also includes schematics, layout, and a bill of materials (BOM).

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PGA281AIPW | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PGA 281 |
| PGA281AIPW.A | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PGA 281 |
| PGA281AIPWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PGA 281 |
| PGA281AIPWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PGA 281 |
| PGA281AIPWRG4 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PGA 281 |
| PGA281AIPWRG4.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PGA 281 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

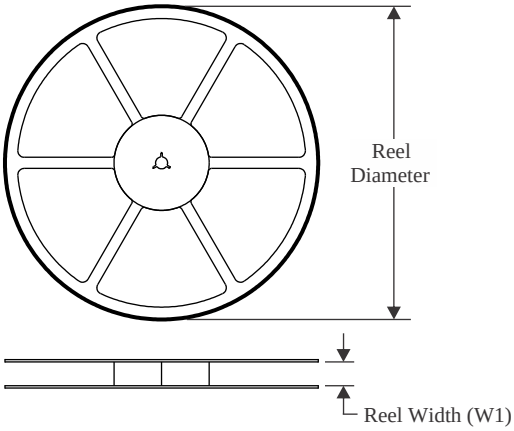
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

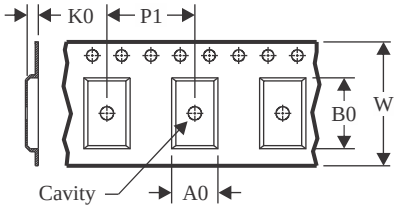
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

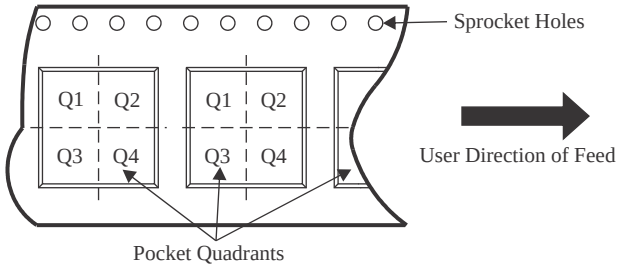



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

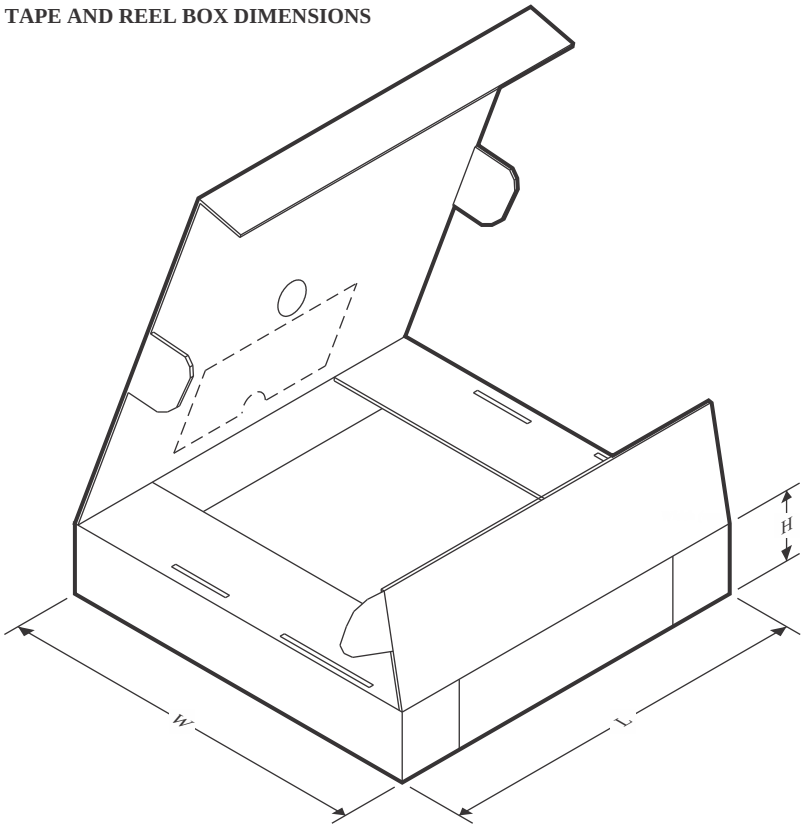
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PGA281AIPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| PGA281AIPWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

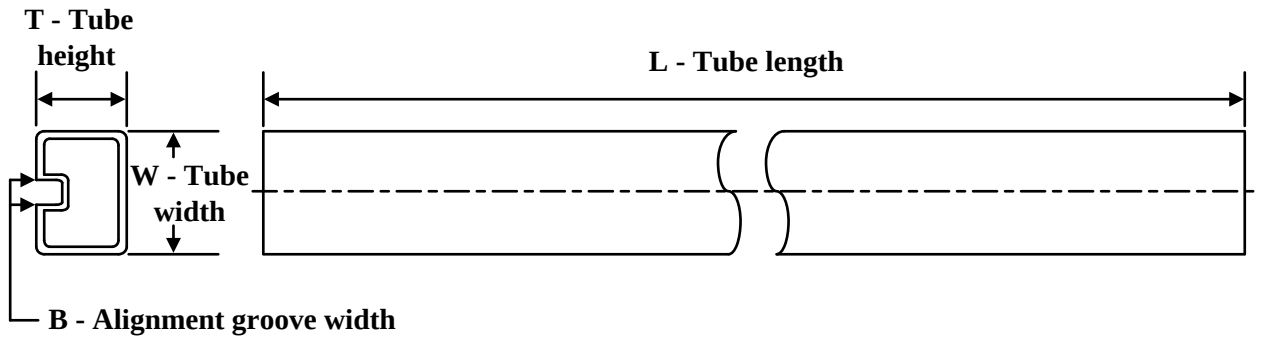
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| PGA281AIPWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| PGA281AIPWRG4 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

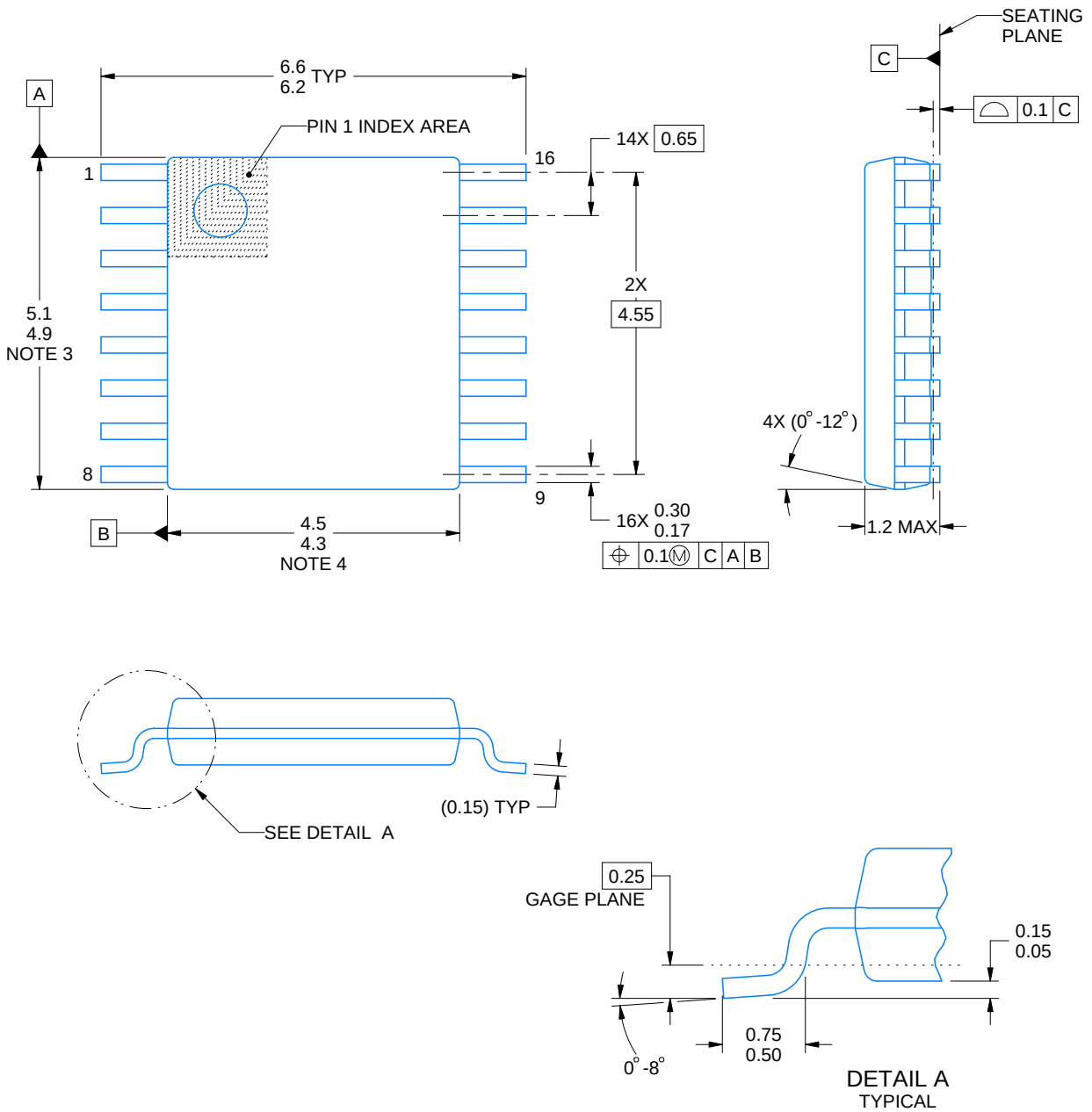
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| PGA281AIPW | PW | TSSOP | 16 | 90 | 508 | 8.5 | 3250 | 2.8 |
| PGA281AIPW.A | PW | TSSOP | 16 | 90 | 508 | 8.5 | 3250 | 2.8 |

# PACKAGE OUTLINE

## PW0016A

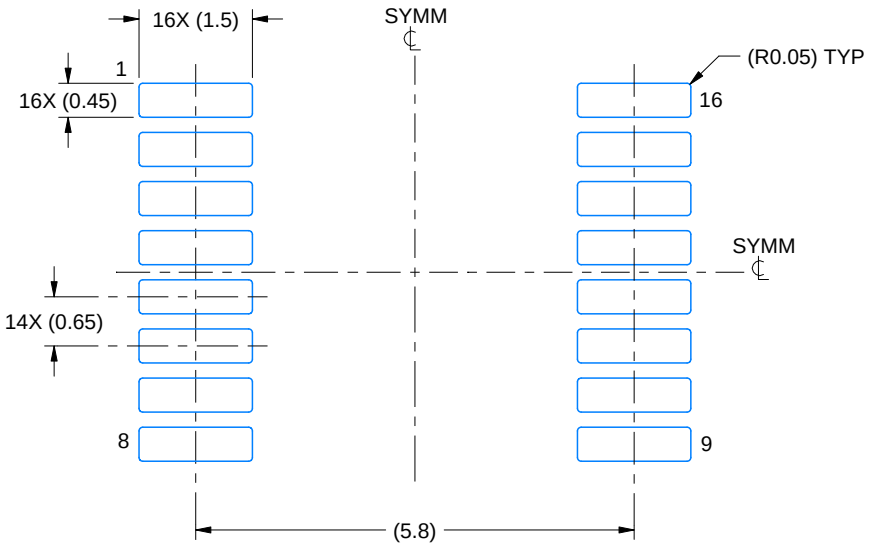
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



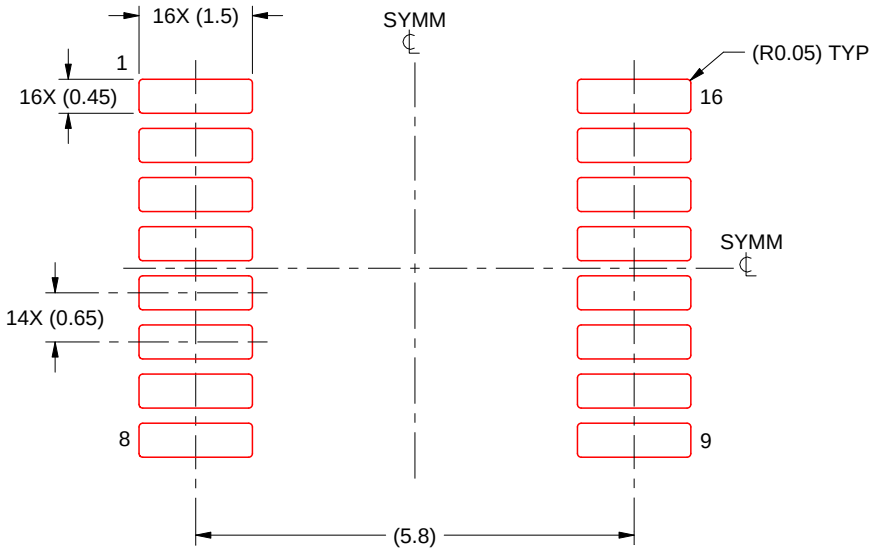

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要通知和免责声明

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