



PCM2903C 具有 USB 接口器、 单端模拟输入/输出 和 S/PDIF 接口的立体声音频编解码器

1 特性

- 片上 USB 接口：
 - 具有全速收发器
 - 完全符合 USB 2.0 规范
 - 经 USB-IF 认证
 - 用于回放的 USB 自适应模式
 - 用于录音的 USB 异步模式
 - 自供电
- 16 位三角积分 (Δ - Σ) 模数转换器 (ADC) 和 数模转换器 (DAC)
- 采样速率：
 - DAC: 32, 44.1, 48kHz
 - ADC: 8, 11.025, 16, 22.05, 32, 44.1, 48 kHz
- 带有单一 12MHz 时钟源的片载时钟生成器
- S/PDIF 输入/输出
- 单电源：
 - 典型值 3.3V
- 立体声 ADC：
 - 在 $V_{CC} = V_{CCP1} = V_{CCP2} = V_{CCX} = V_{DD} = 3.3\text{ V}$ 时的模拟性能：
 - 总谐波失真 (THD)+N=0.01%
 - 信噪比 (SNR)=89dB
 - 动态范围 = 89dB
 - 数字抽取滤波器：
 - 通带纹波 = $\pm 0.05\text{dB}$
 - 抑制频带衰减: -65dB
 - 单端电压输入
 - 包含抗混叠滤波器
 - 包含数字高通滤波器 (HPF)
- 立体声 DAC：
 - $V_{CC} = V_{CCP1} = V_{CCP2} = V_{CCX} = V_{DD} = 3.3\text{ V}$ 时的模拟性能：

– THD+N=0.005%

– SNR=96dB

– 动态范围 = 93dB

– 过采样数字滤波器：

– 通带纹波 = $\pm 0.1\text{dB}$

– 抑制频带衰减 = -43dB

– 单端电压输出

– 包含模拟低通滤波器 (LPF)

• 多功能：

– 人机接口器件 (HID) 功能：

– 音量和静音控制

– 挂起标志功能

• 28 引脚窄间距小外形尺寸 (SSOP) 封装

2 应用

- USB 音频扬声器
- USB 耳机
- USB 监控器
- USB 音频接口盒

3 说明

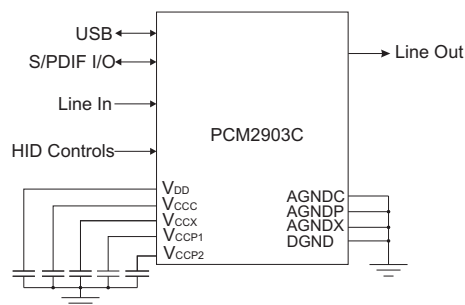
PCM2903C 是德州仪器 (TI) 的一款单芯片、USB、立体声音频编解码器，此解码器带有一个与 USB 兼容的全速协议控制器和 S/PDIF。USB 协议控制器无需软件代码。PCM2903C 采用 SpAct™ 架构，此架构为 TI 将音频时钟从 USB 数据包中恢复的独特系统。使用 SpAct 的片载模拟锁相环路 (PLL) 启用回放和带有低时钟抖动、以及独立回放和录音采样速率的录音功能。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
PCM2903C	SSOP (28)	10.20mm x 5.30mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化图表



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4 修订历史记录

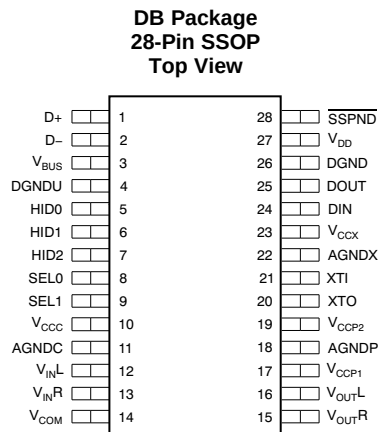
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (June 2011) to Revision A	Page
• 已添加 ESD 额定值表，特性 描述 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分	1
• Removed <i>Package/Ordering Information</i> table	5

5 Device Comparison Table

	PCM2900C	PCM2902C	PCM2903C	PCM2906C
Supply Voltage	5 V (Bus-Powered)	5 V (Bus-Powered)	3.3 V (Self-Powered)	5 V (Bus-Powered)
Additional Features	—	S/PDIF I/O	S/PDIF I/O	S/PDIF I/O 500 mA Max Power Configuration

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGNDC	11	–	Analog ground for codec
AGNDP	18	–	Analog ground for PLL
AGNDX	22	–	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus ⁽¹⁾
D+	1	I/O	USB differential input/output plus ⁽¹⁾
DGND	26	–	Digital ground
DGNDU	4	–	Digital ground for USB transceiver
DIN	24	I	S/PDIF input ⁽²⁾
DOUT	25	O	S/PDIF output
HID0	5	I	HID key state input (mute), active-high ⁽³⁾
HID1	6	I	HID key state input (volume up), active-high ⁽³⁾
HID2	7	I	HID key state input (volume down), active-high ⁽³⁾
SEL0	8	I	Must be set to high ⁽⁴⁾
SEL1	9	I	Connected to the USB port of V _{BUS} ⁽⁴⁾
SSPND	28	O	Suspend flag, active-low (Low: suspend, High: operational)
V _{BUS}	3	–	Must be connected to V _{DD}
V _{CCC}	10	–	Analog power supply for codec ⁽⁵⁾
V _{CCP1}	17	–	Analog power supply for PLL ⁽⁵⁾
V _{CCP2}	19	–	Analog power supply for PLL ⁽⁵⁾
V _{CCX}	23	–	Analog power supply for oscillator ⁽⁵⁾
V _{COM}	14	–	Common for ADC/DAC (V _{CCC} /2) ⁽⁵⁾
V _{DD}	27	–	Digital power supply ⁽⁵⁾
V _{INL}	12	I	ADC analog input for L-channel
V _{INR}	13	I	ADC analog input for R-channel
V _{OUTL}	16	O	DAC analog output for L-channel
V _{OUTR}	15	O	DAC analog output for R-channel
XTI	21	I	Crystal oscillator input ⁽⁶⁾
XTO	20	O	Crystal oscillator output

- (1) LV-TTL level.
- (2) 3.3-V CMOS-level input with internal pulldown, 5-V tolerant.
- (3) 3.3-V CMOS-level input with internal pulldown. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which have no direct connection with the internal DAC or ADC. See the [Interface Number 3](#) and [End-Points](#) sections.
- (4) TTL Schmitt trigger, 5-V tolerant.
- (5) Connect a decoupling capacitor to GND.
- (6) 3.3-V CMOS-level input.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, V_{CC} , V_{CCP1} , V_{CCP2} , V_{CCX} , V_{DD}		−0.3	4	V
Supply voltage differences, V_{CC} , V_{CCP1} , V_{CCP2} , V_{CCX} , V_{DD}			±0.1	V
Ground voltage differences, AGND, AGNDP, AGNDX, DGND, DGNDU			±0.1	V
Digital input voltage	SEL0, SEL1, DIN	−0.3	6.5	V
	D+, D−, HID0, HID1, HID2, XTI, XTO, DOUT, $\overline{SSPND}$	−0.3	$(V_{DD} + 0.3) < 4$	V
Analog input voltage V_{INL} , V_{INR} , V_{COM} , V_{OUTR} , V_{OUTL}		−0.3	$(V_{CC} + 0.3) < 4$	V
Input current (any pins except supplies)			±10	mA
Ambient temperature under bias		−40	125	°C
Junction temperature T_J			150	°C
Lead temperature (soldering, 5 s)			260	°C
Package temperature (IR reflow, peak)			250	°C
Storage temperature, T_{stg}		−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage		3	3.3	3.6	V
Supply current	ADC, DAC operation		54	70	mA
	USB suspend state		250		μA
Ambient temperature		0	25	85	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		PCM2903C	UNIT
		DB (SSOP)	
		28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

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7.5 Electrical Characteristics

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{CCP1} = V_{CCP2} = V_{CCX} = V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
Host interface		Apply USB Revision 2.0, full speed				
Audio data format		USB isochronous data format				
INPUT LOGIC						
V _{IH}	High-level input voltage	D+, D–	2		V _{DD}	VDC
		XTI, HID0, HID1, and HID2	0.7 V _{DD}		V _{DD}	
		SEL0, SEL1	2		5.25	
		DIN	0.7 V _{DD}		5.25	
V _{IL}	Low-level input voltage	D+, D–			0.8	VDC
		XTI, HID0, HID1, and HID2			0.3 V _{DD}	
		SEL0, SEL1			0.8	
		DIN			0.3 V _{DD}	
I _{IH}	High-level input current	D+, D–, XTI, SEL0, SEL1	V _{IN} = 3.3 V		±10	µA
		HID0, HID1, and HID2	V _{IN} = 3.3 V	50	80	
		DIN	V _{IN} = 3.3 V	65	100	
I _{IL}	Low-level input current	D+, D–, XTI, SEL0, SEL1	V _{IN} = 0 V		±10	µA
		HID0, HID1, and HID2	V _{IN} = 0 V		±10	
		DIN	V _{IN} = 0 V		±10	
OUTPUT LOGIC						
V _{OH}	High-level output voltage	D+, D–	2.8			VDC
		DOUT	I _{OH} = –4 mA	2.8		
		SSPND	I _{OH} = –2 mA	2.8		
V _{OL}	Low-level output voltage	D+, D–			0.3	VDC
		DOUT	I _{OL} = 4 mA		0.5	
		SSPND	I _{OL} = 2 mA		0.5	
CLOCK FREQUENCY						
Input clock frequency, XTI			11.994	12	12.006	MHz
ADC CHARACTERISTICS						
Resolution				8, 16		Bits
Audio data channel				1, 2		Channel
ADC CLOCK FREQUENCY						
f _S	Sampling frequencies		8, 11.025, 16, 22.05, 32, 44.1, 48			kHz
ADC DC ACCURACY						
Gain mismatch, channel-to-channel				±1	±5	% of FSR
Gain error				±2	±10	% of FSR
Bipolar zero error				±0		% of FSR
ADC DYNAMIC PERFORMANCE ⁽¹⁾						
THD+N	Total harmonic distortion plus noise	V _{IN} = –1 dB		0.01%	0.02%	
		V _{IN} = –60 dB		5%		

(1) $f_{IN} = 1\text{ kHz}$, using a System Two™ audio measurement system by Audio Precision™ in RMS mode with a 20-kHz LPF and 400-Hz HPF in the calculation.

Electrical Characteristics (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range	A-weighted	81	89		dB
SNR	Signal-to-noise ratio	A-weighted	81	89		dB
	Channel separation		80	85		dB
ANALOG INPUT						
	Input voltage		0.6 V _{CCC}			V _{PP}
	Center voltage		0.5 V _{CCC}			V
	Input impedance		30			kΩ
	Antialiasing filter frequency response	−3 dB	150			kHz
		f _{IN} = 20 kHz	−0.08			dB
ADC DIGITAL FILTER PERFORMANCE						
	Passband		0.454 f _S			Hz
	Stop band		0.583 f _S			Hz
	Passband ripple		±0.05			dB
	Stop-band attenuation		−65			dB
t _d	Delay time		17.4/f _S			s
	HPF frequency response	−3 dB	0.078 f _S /1000			Hz
DAC CHARACTERISTICS						
	Resolution		8, 16			Bits
	Audio data channel		1, 2			Channel
DAC CLOCK FREQUENCY						
f _S	Sampling frequencies		32, 44.1, 48			kHz
DAC DC ACCURACY						
	Gain mismatch channel-to-channel		±1 ±5			% of FSR
	Gain error		±2 ±10			% of FSR
	Bipolar zero error		±2			% of FSR
DAC DYNAMIC PERFORMANCE ⁽²⁾						
THD+N	Total harmonic distortion plus noise	V _{OUT} = 0 dB	0.005% 0.016%			
		V _{OUT} = −60 dB	3%			
	Dynamic range	EIAJ, A-weighted	87	93		dB
SNR	Signal-to-noise ratio	EIAJ, A-weighted	90	96		dB
	Channel separation		86	92		dB
ANALOG OUTPUT						
V _O	Output voltage		0.6 V _{CCC}			V _{PP}
	Center voltage		0.5 V _{CCC}			V
	Load impedance	AC coupling	10			kΩ
	LPF frequency response	−3 dB	250			kHz
		f = 20 kHz	−0.03			dB
DAC DIGITAL FILTER PERFORMANCE						
	Passband		0.445 f _S			Hz
	Stop band		0.555 f _S			Hz
	Passband ripple		±0.1			dB
	Stop-band attenuation		−43			dB

(2) $f_{OUT} = 1\text{ kHz}$, using a System Two audio measurement system by Audio Precision in RMS mode with a 20-kHz LPF and 400-Hz HPF.

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Electrical Characteristics (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = V_{DD} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d Delay time			$14.3/f_S$		s
POWER-SUPPLY REQUIREMENTS					
V_{DD} , V_{CCC} , V_{CCP1} , V_{CCP2} , V_{CCX} Voltage range		3	3.3	3.6	VDC
Supply current	ADC, DAC operation		54	70	mA
	Suspend mode ⁽³⁾		250		μA
P_D Power dissipation	ADC, DAC operation		178	252	mW
	Suspend mode ⁽³⁾		0.83		mW
TEMPERATURE RANGE					
Operating temperature range		–25		85	$^\circ\text{C}$

(3) Under USB suspend state.

7.6 Typical Characteristics

7.6.1 Typical Characteristics: ADC

All specifications at $T_A = +25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCx} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.

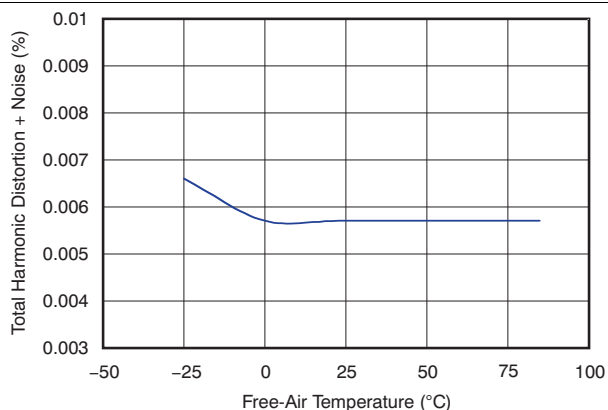


Figure 1. Total Harmonic Distortion + Noise at -1 dB vs Free-Air Temperature

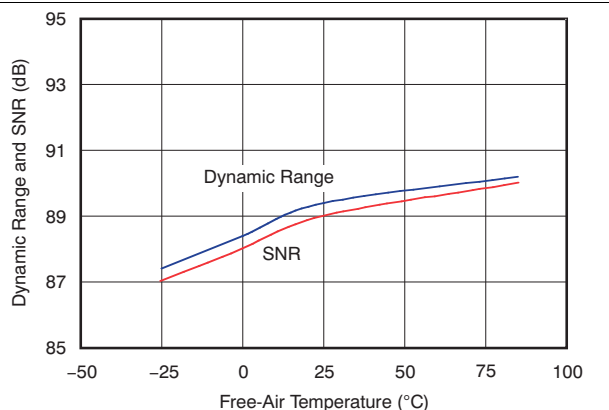


Figure 2. Dynamic Range and SNR vs Free-Air Temperature

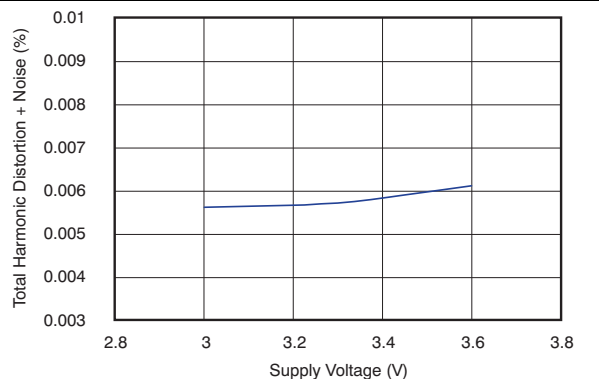


Figure 3. Total Harmonic Distortion + Noise at -1 dB vs Supply Voltage

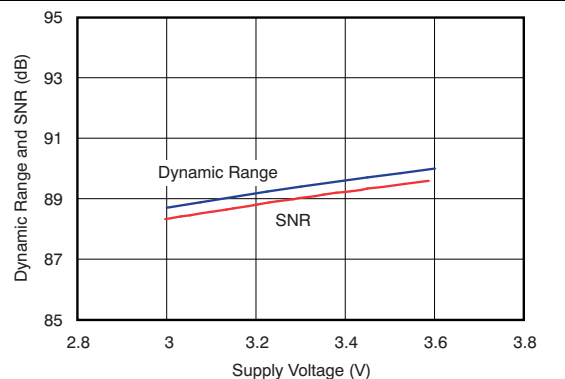


Figure 4. Dynamic Range and SNR vs Supply Voltage

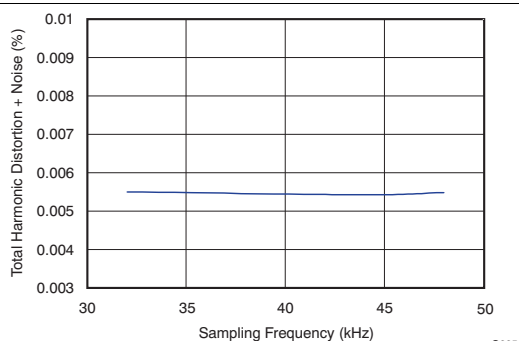


Figure 5. Total Harmonic Distortion + Noise at -1 dB vs Sampling Frequency

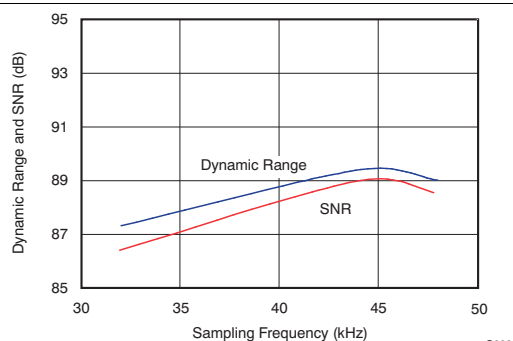


Figure 6. Dynamic Range and SNR vs Sampling Frequency

7.6.2 Typical Characteristics: DAC

All specifications at $T_A = +25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.

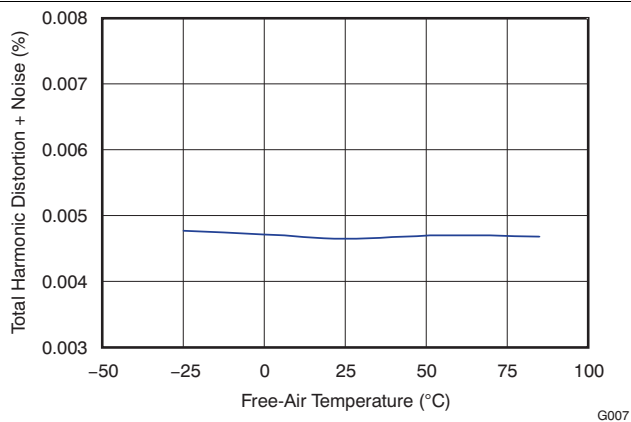


Figure 7. Total Harmonic Distortion + Noise at 0 dB vs Free-Air Temperature

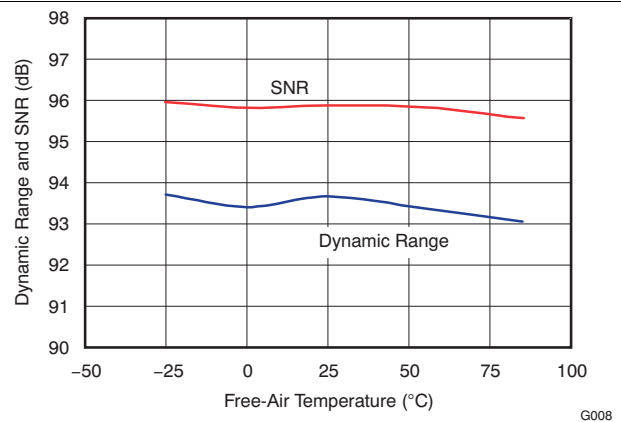


Figure 8. Dynamic Range and SNR vs Free-Air Temperature

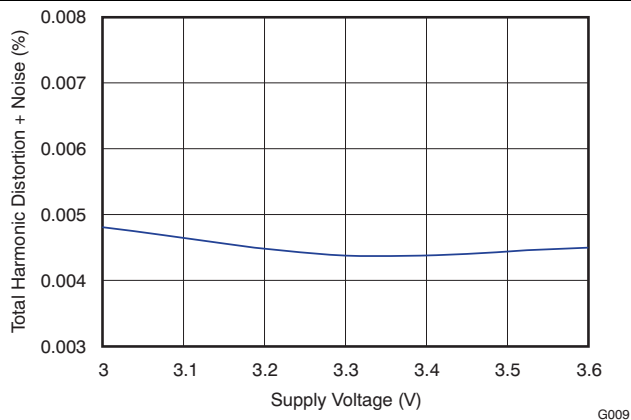


Figure 9. Total Harmonic Distortion + Noise at 0 dB vs Supply Voltage

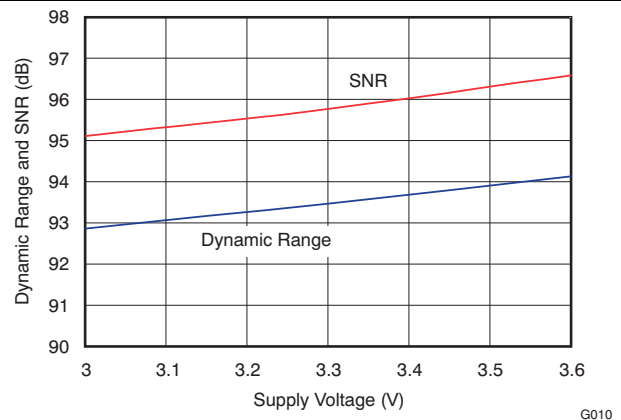


Figure 10. Dynamic Range and SNR vs Supply Voltage

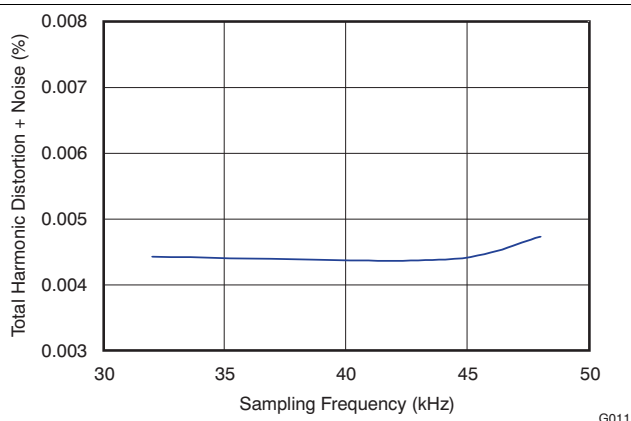


Figure 11. Total Harmonic Distortion + Noise at 0 dB vs Sampling Frequency

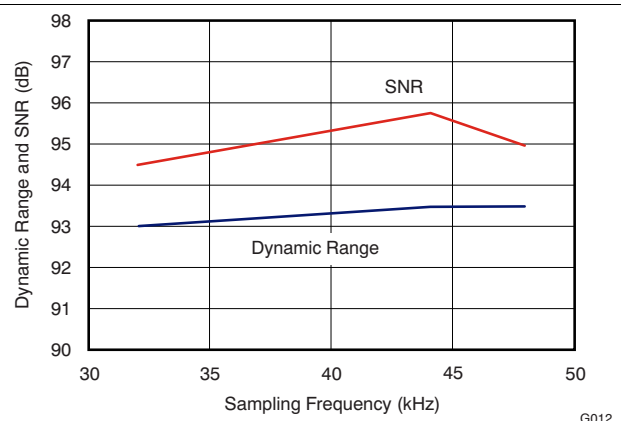
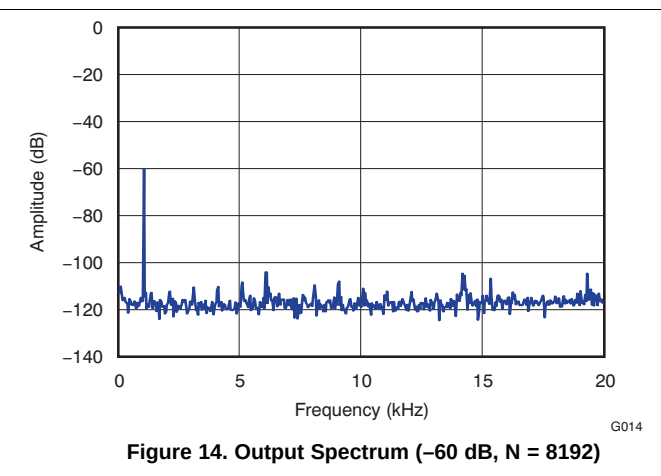
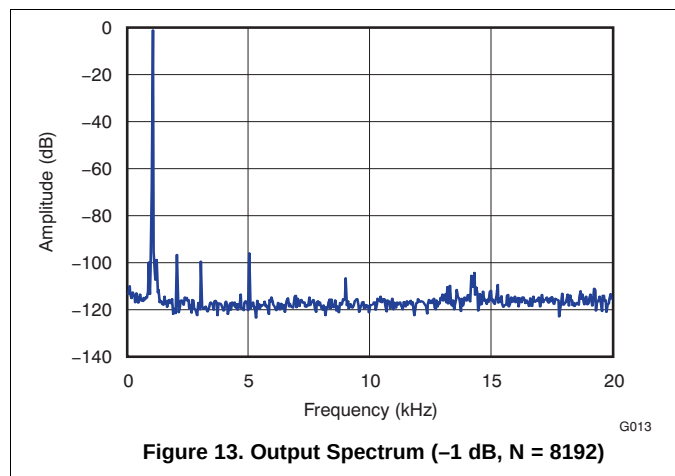


Figure 12. Dynamic Range and SNR vs Sampling Frequency

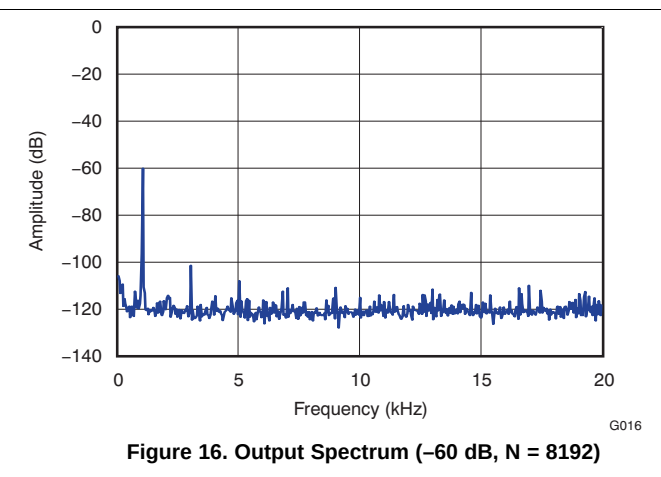
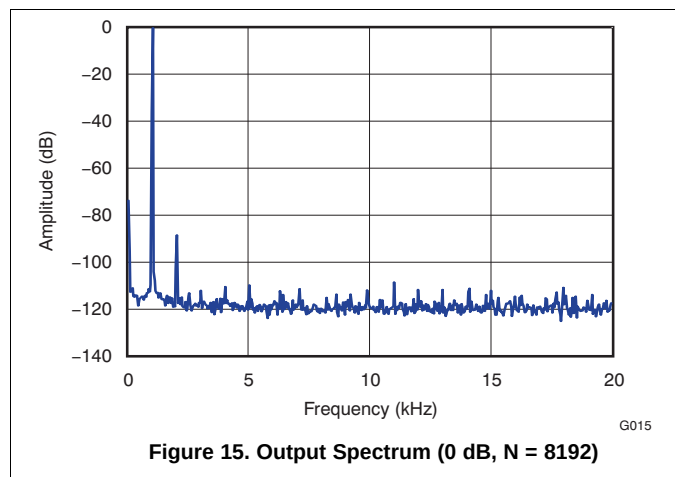
7.6.3 Typical Characteristics: ADC Output Spectrum

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCx} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.



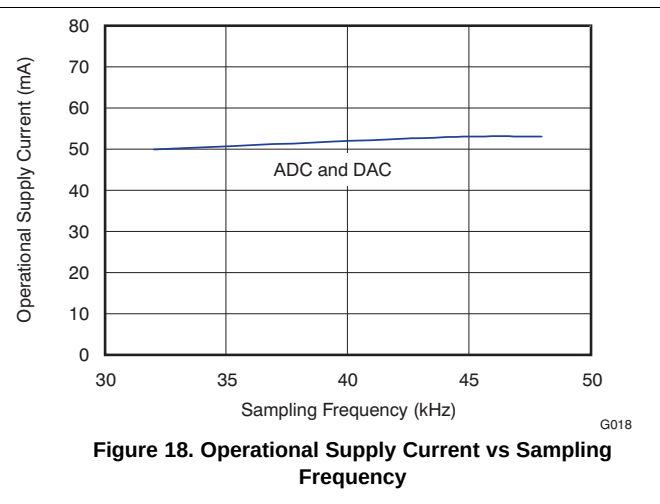
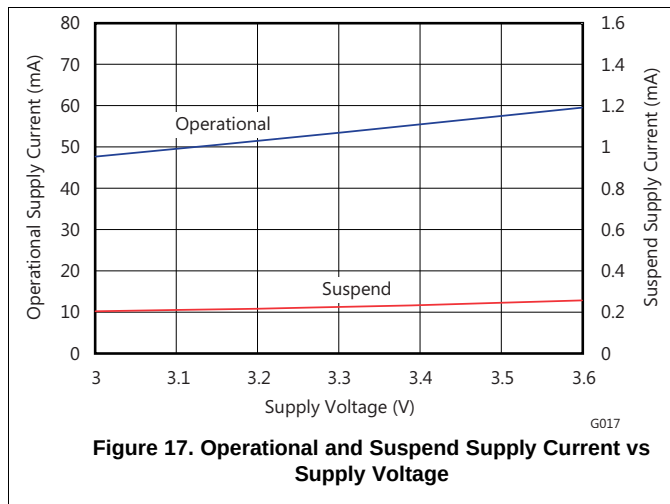
7.6.4 Typical Characteristics: DAC Output Spectrum

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCx} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.



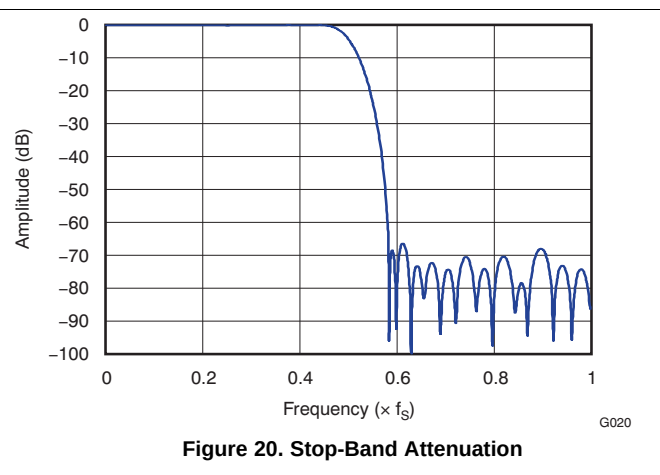
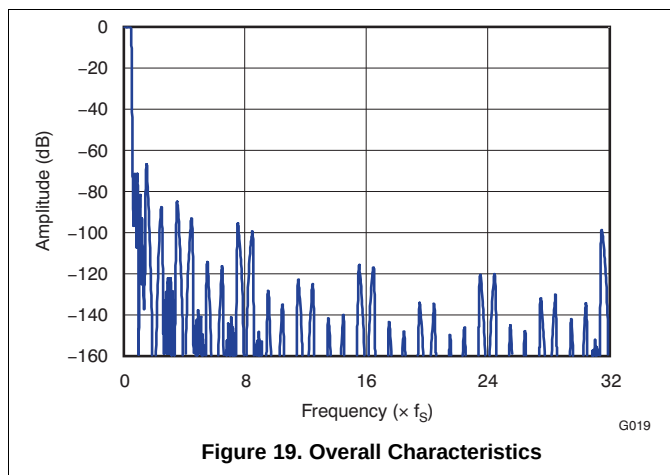
7.6.5 Typical Characteristics: Supply Current

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.



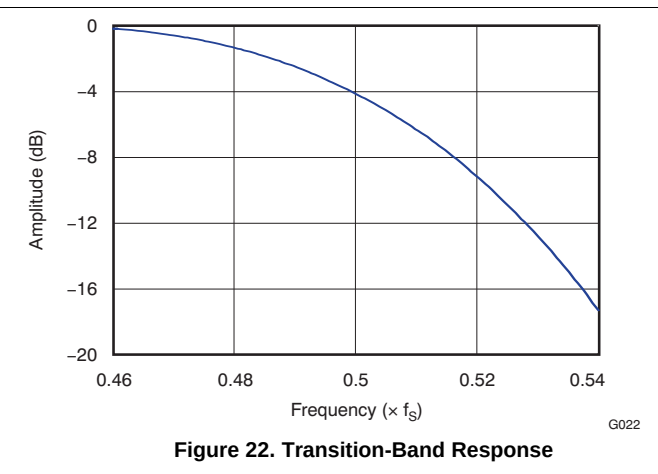
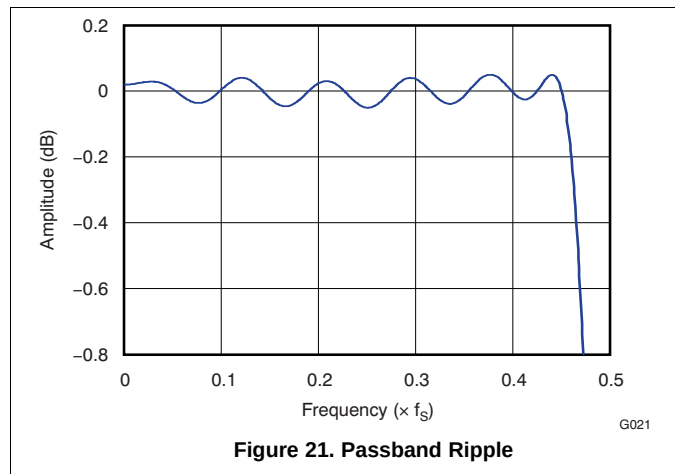
7.6.6 Typical Characteristics: ADC Digital Decimation Filter Frequency Response

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.



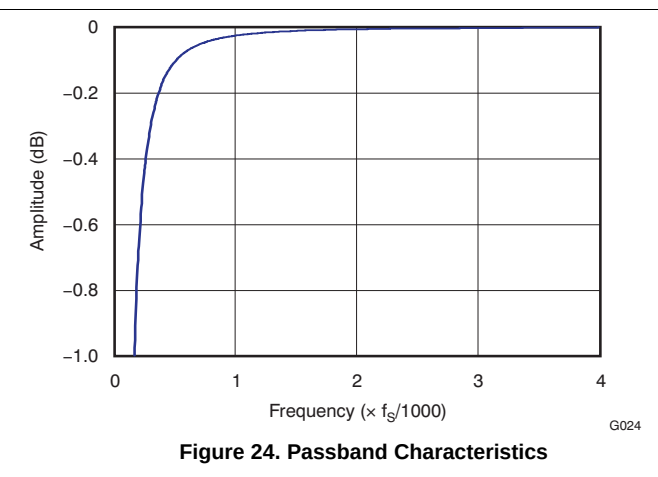
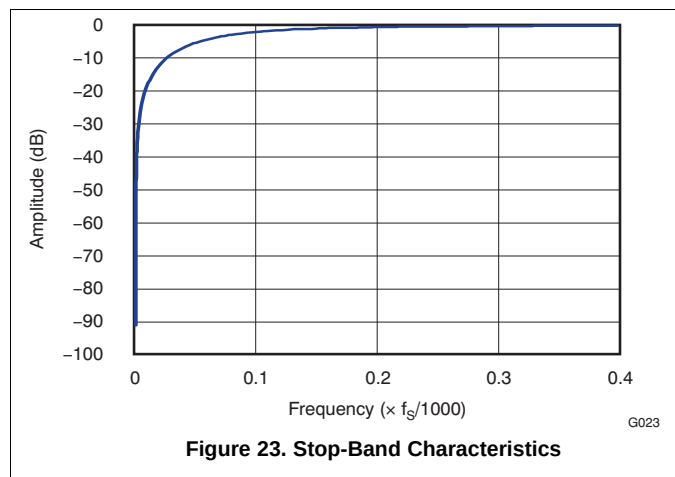
Typical Characteristics: ADC Digital Decimation Filter Frequency Response (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCx} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.



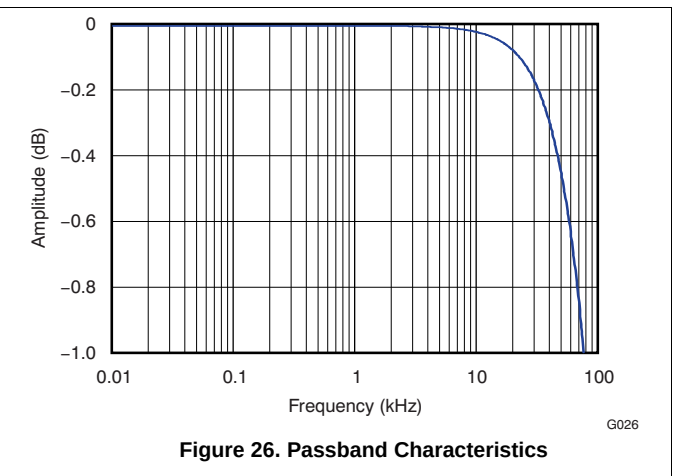
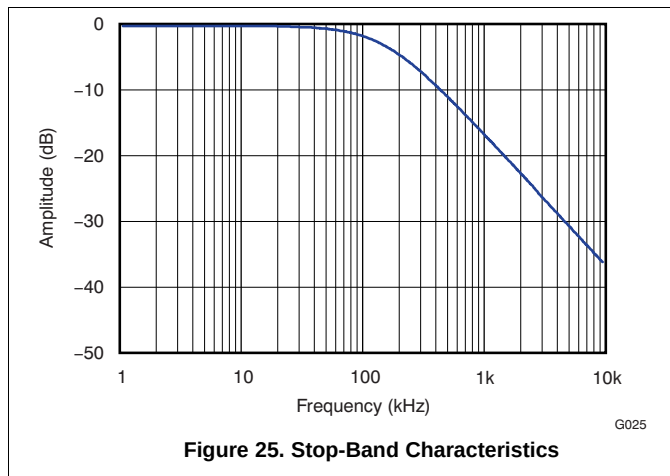
7.6.7 Typical Characteristics: ADC Digital High-Pass Filter Frequency Response

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCx} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.



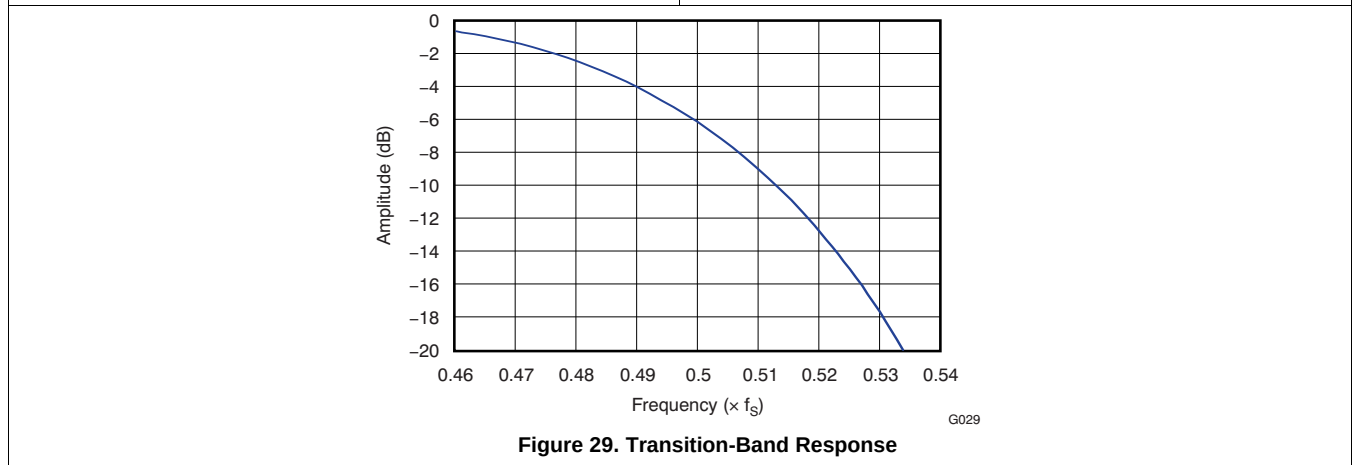
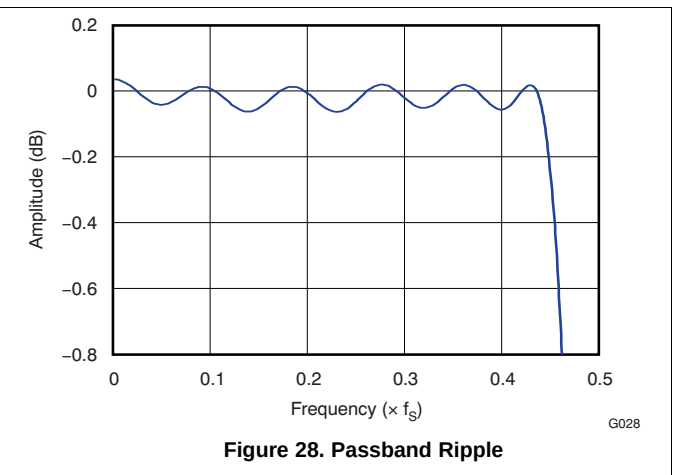
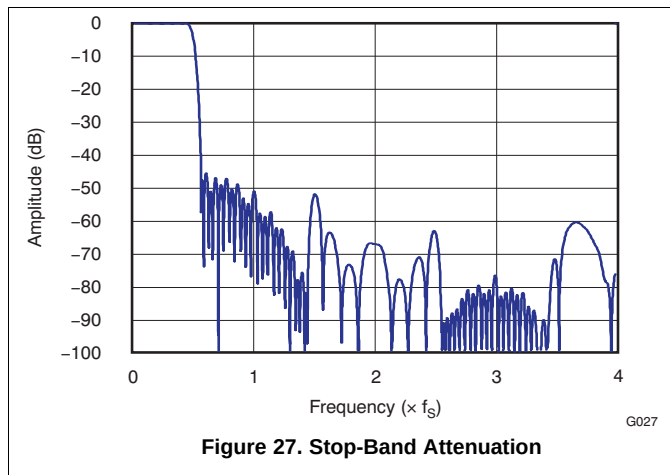
7.6.8 Typical Characteristics: ADC Analog Antialiasing Filter Frequency Response

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.



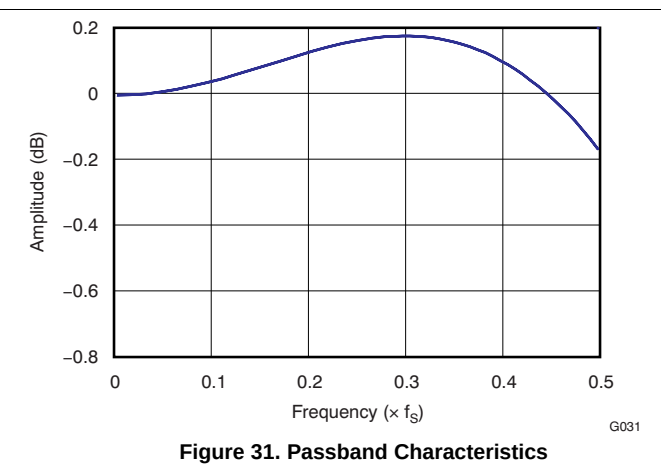
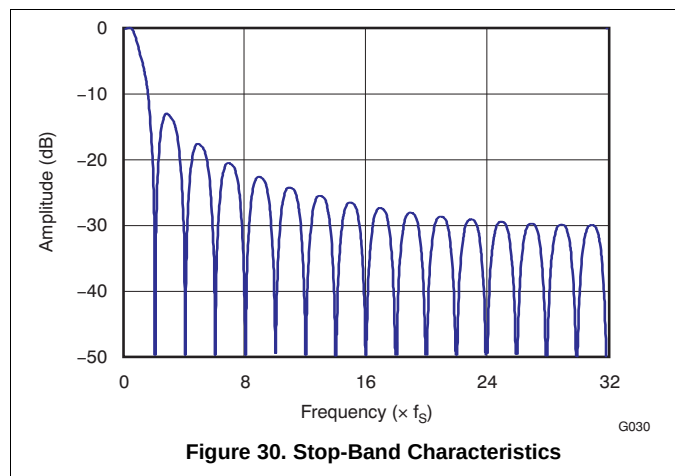
7.6.9 Typical Characteristics: DAC Digital Interpolation Filter Frequency Response

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCX} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.



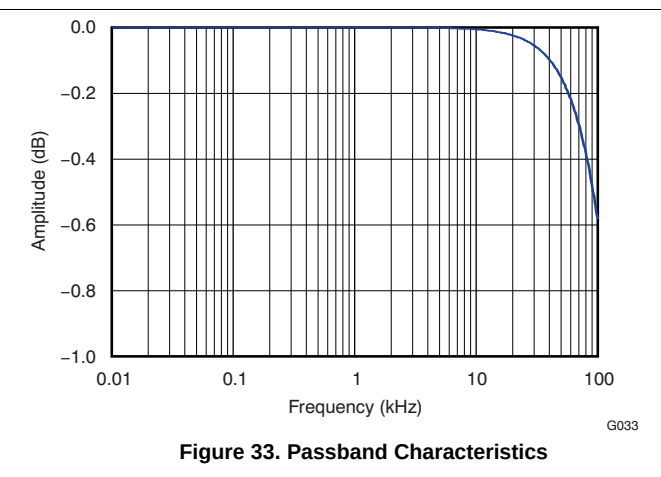
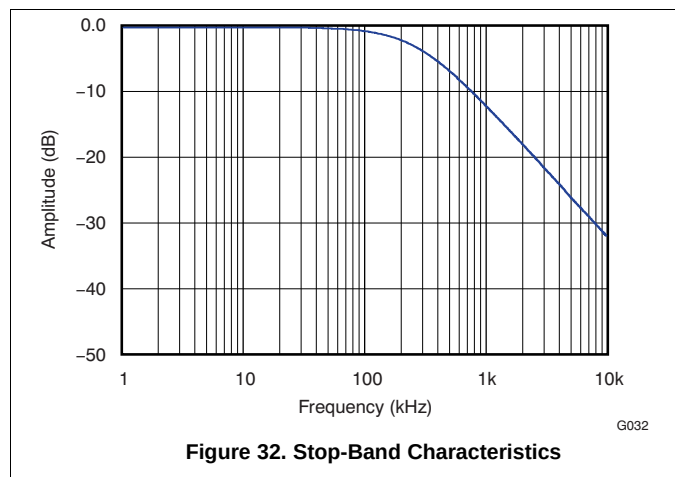
7.6.10 Typical Characteristics: DAC Analog Fir Filter Frequency Response

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCx} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.



7.6.11 Typical Characteristics: DAC Analog Low-Pass Filter Frequency Response

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CCC} = V_{CCP1} = V_{CCP2} = V_{CCx} = 3.3\text{ V}$, $f_s = 44.1\text{ kHz}$, $f_{IN} = 1\text{ kHz}$, 16-bit data, unless otherwise noted.



8 Parameter Measurement Information

All parameters are measured according to the conditions described in the [Specifications](#) section.

9 Detailed Description

9.1 Overview

The PCM2903C is an audio codec with USB connection capability and a digital S/PDIF digital interface. The PCM2903C is a self-powered device; it needs an external 3.3V voltage source. The PCM2903C meet the requirements of USB1.1 standard connection. This device has analog and digital inputs and outputs; it has a digital S/PDIF interface for input and output data. The PCM2903C has 3 external interrupts (HID) which control the Mute, Volume Up and Volume Down, these control inputs are active High. The PCM2903C requires a 12MHz clock; it can be provided by an external clock or generated by a built-in crystal resonator.

9.2 Functional Block Diagram

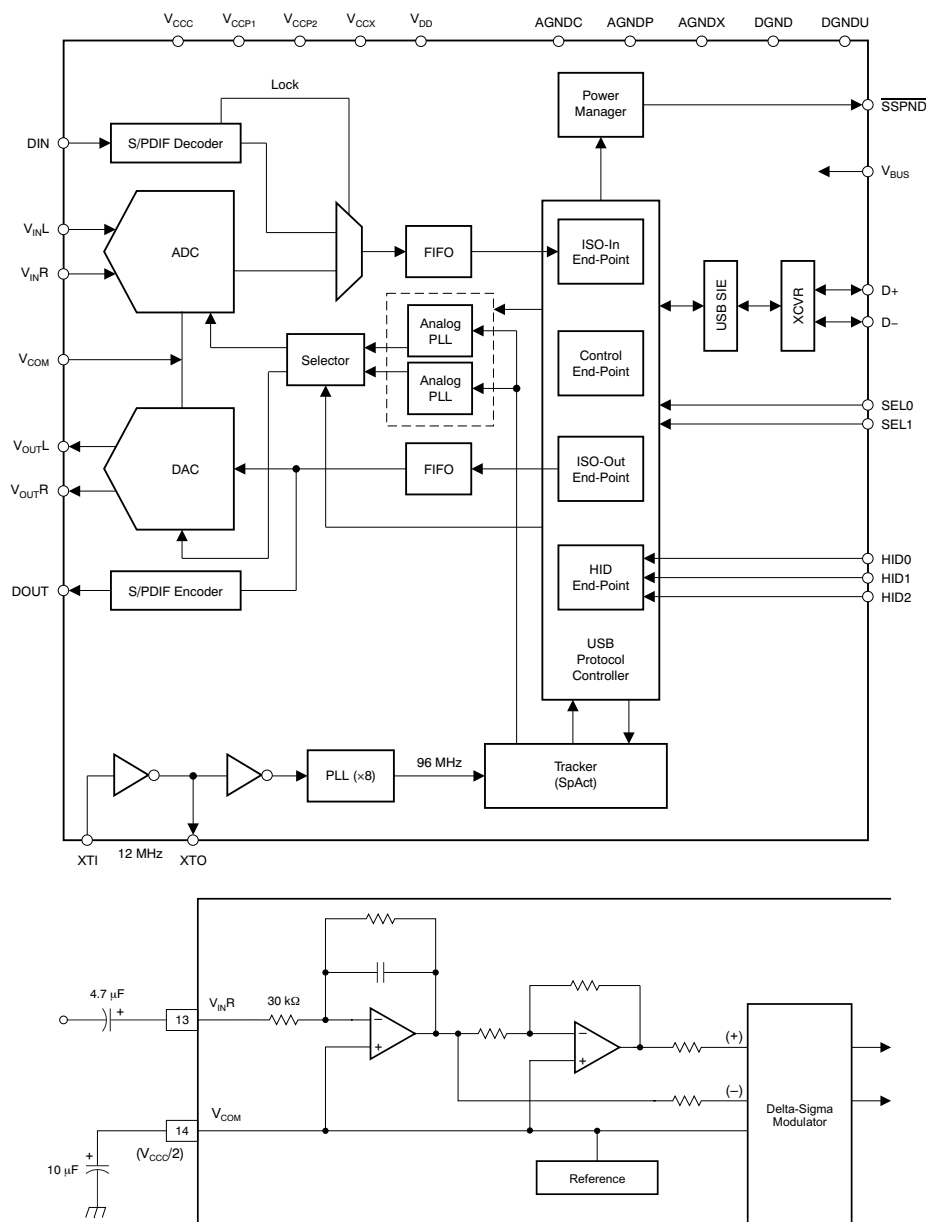


Figure 34. Block Diagram of Analog Front-End (Right Channel)

9.3 Feature Description

9.3.1 End-Points

The PCM2903C has the following four end-points:

- Control end-point (EP number 0)
- Isochronous-out audio data stream end-point (EP number 2)
- Isochronous-in audio data stream end-point (EP number 4)
- HID end-point (EP number 5)

The control end-point is a default end-point. The control end-point is used to control all functions of the PCM2903C by the standard USB request and an USB audio class specific request from the host. The isochronous-out audio data stream end-point is an audio sink end-point, which receives the PCM audio data. The isochronous-out audio data stream end-point accepts the adaptive transfer mode. The isochronous-in audio data stream end-point is an audio source end-point that transmits the PCM audio data. The isochronous-in audio data stream end-point uses asynchronous transfer mode. The HID end-point is an interrupt-in end-point. HID end-point reports HID0, HID1, and HID2 pin status every 32 ms.

The human interface device (HID) pins are defined as consumer control devices. The HID function is designed as an independent end-point from both isochronous-in and -out end-points. Therefore, the result obtained from the HID operation depends on the host software. Typically, the HID function is used as the primary audio-out device.

9.3.2 Clock and Reset

The PCM2903C requires a 12-MHz (± 500 ppm) clock for the USB and audio function, which can be generated by a built-in crystal oscillator with a 12-MHz crystal resonator or supplied by an external clock. The 12-MHz crystal resonator must be connected to XTI (pin 21) and XTO (pin 20) with one high (1-M Ω) resistor and two small capacitors, the capacitance of which depends on the load capacitance of the crystal resonator. If the external clock is used, the clock must be supplied to XTI, and XTO must be open.

The PCM2903C has an internal power-on reset circuit, which triggers automatically when V_{DD} (pin 27) exceeds 2.5 V typical (2.7 V to 2.2 V). Approximately 700 μ s is required until internal reset release.

9.3.3 Digital Audio Interface

The PCM2903C employs both S/PDIF input and output. Isochronous-out data from the host are encoded to the S/PDIF output and the DAC analog output. Input data are selected as either S/PDIF or ADC analog input. When the device detects an S/PDIF input and successfully locks on the received data, the isochronous-in transfer data source is automatically selected from S/PDIF itself; otherwise, the data source selected is the ADC analog input.

This feature is a customer option. It is the responsibility of the user to implement this feature.

9.3.4 Supported Input/Output Data

The following data formats are accepted by the S/PDIF input and output. All other data formats are unable to use S/PDIF.

- 48-kHz 16-bit stereo
- 44.1-kHz 16-bit stereo
- 32-kHz 16-bit stereo

Any mismatch of the sampling rate between the input S/PDIF signal and the host command is not acceptable. Any mismatch of the data format between the input S/PDIF signal and the host command may cause unexpected results, with the following exceptions:

- Recording in monaural format from stereo data input at the same data rate
- Recording in 8-bit format from 16-bit data input at the same data rate

A combination of these two conditions is not acceptable.

For playback, all possible data-rate sources are converted to 16-bit stereo format at the same source data rate.

Feature Description (continued)

9.3.5 Channel Status Information

The channel status information is fixed as consumer application, PCM mode, copyright, and digital/digital converter. All other bits are fixed as 0's except for the sample frequency, which is set automatically according to the data received through the USB.

9.3.6 Copyright Management

Isochronous-in data are affected by the serial copy management system (SCMS). When the control bit indicates that the received digital audio data are original, the input digital audio data are transferred to the host. If the data are indicated as first generation or higher, the transferred data are routed to the analog input.

Digital audio data output is always encoded as original with SCMS control.

9.4 Device Functional Modes

The PCM2903C is a USB controlled device. The PCM2903C is a codec, so it has analog input (that goes to an A/D converter) and analog output (that comes from a D/A converter), alongside of the digital path that goes to USB and S/PDIF. A wider explanation of these operational modes is in [Programming](#).

9.5 Programming

9.5.1 USB Interface

Control data and audio data are transferred to the PCM2903C via D+ (pin 1) and D– (pin 2). All data to and from the PCM2903C are transferred at full speed. The device descriptor contains the information described in [Table 1](#).

Table 1. Device Descriptor

USB revision	2.0 compliant
Device class	0x00 (device-defined interface level)
Device subclass	0x00 (not specified)
Device protocol	0x00 (not specified)
Max packet size for end-point 0	8 bytes
Vendor ID	0x08BB
Product ID	0x29C3
Device release number	1.0 (0x0100)
Number of configurations	1
Vendor strings	String number 1 (see Table 3)
Product strings	String number 2 (see Table 3)
Serial number	Not supported

The configuration descriptor contains the information described in [Table 2](#).

Table 2. Configuration Descriptor

Interface	Four interfaces
Power attribute	0xC0 (self-powered, no remote wakeup)
Maximum power	0x0A (20 mA)

The string descriptor contains the information described in [Table 3](#).

Table 3. String Descriptor

Number 0	0x0409
Number 1	BurrBrown from Texas Instruments
Number 2	USB Audio CODEC ⁽¹⁾

(1) Ensure that there are two blank spaces between "Audio" and "CODEC"; copying and pasting will not transfer the two blank spaces correctly.

9.5.2 Device Configuration

[Figure 35](#) illustrates the USB audio function topology. The PCM2903C has four interfaces. Each interface consists of alternative settings.

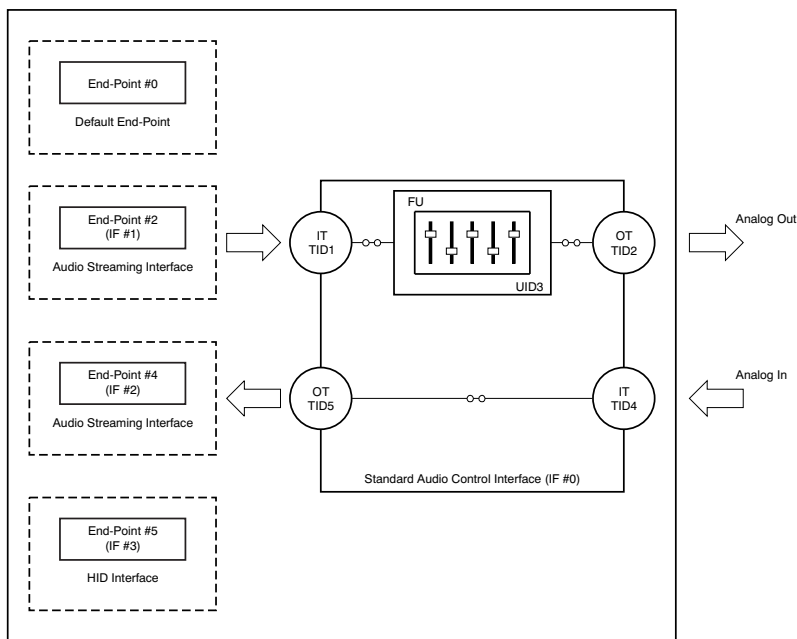


Figure 35. USB Audio Function Topology

9.5.2.1 Interface Number 0

Interface number 0 is the control interface. Alternative setting number 0 is the only possible setting for interface number 0. Alternative setting number 0 describes the standard audio control interface. The audio control interface consists of a single terminal. The PCM2903C has the following five terminals:

- Input terminal (IT number 1) for isochronous-out stream
- Output terminal (OT number 2) for audio analog output
- Feature unit (FU number 3) for DAC digital attenuator
- Input terminal (IT number 4) for audio analog input
- Output terminal (OT number 5) for isochronous-in stream

Input terminal number 1 is defined as *USB stream* (terminal type 0x0101). Input terminal number 1 can accept two-channel audio streams consisting of left and right channels. Output terminal number 2 is defined as a *speaker* (terminal type 0x0301). Input terminal number 4 is defined as a *line connector* (terminal type 0x0603). Output terminal number 5 is defined as a *USB stream* (terminal type 0x0101). Output terminal number 5 can generate two-channel audio streams composed of left and right channel data. Feature unit number 3 supports the following sound control features:

- Volume control
- Mute control

The built-in digital volume controller can be manipulated by an audio class specific request from 0 dB to –64 dB in 1-dB steps. Changes are made by incrementing or decrementing by one step (1 dB) for every $1/f_s$ time interval until the volume level has reached the requested value. Each channel can be set for different values. The master volume control is not supported. A request to the master volume is stalled and ignored. The built-in digital mute controller can be manipulated by audio class-specific request. A master mute control request is acceptable. A request to an individual channel is stalled and ignored.

9.5.2.2 Interface Number 1

Interface number 1 is the audio streaming data-out interface. Interface number 1 has the five alternative settings described in [Table 4](#). Alternative setting number 0 is the zero-bandwidth setting.

Table 4. Interface Number 1 Alternative Settings

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero bandwidth				
01	16-bit	Stereo	Twos complement (PCM)	Adaptive	32, 44.1, 48
02	16-bit	Mono	Twos complement (PCM)	Adaptive	32, 44.1, 48
03	8-bit	Stereo	Twos complement (PCM)	Adaptive	32, 44.1, 48
04	8-bit	Mono	Twos complement (PCM)	Adaptive	32, 44.1, 48

9.5.2.3 Interface Number 2

Interface number 2 is the audio streaming data-in interface. Interface number 2 has the 19 alternative settings described in [Table 5](#). Alternative setting number 0 is the zero-bandwidth setting. All other alternative settings are operational settings.

Table 5. Interface Number 2 Alternative Settings

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero bandwidth				
01	16-bit	Stereo	Twos complement (PCM)	Asynchronous	48
02	16-bit	Mono	Twos complement (PCM)	Asynchronous	48
03	16-bit	Stereo	Twos complement (PCM)	Asynchronous	44.1
04	16-bit	Mono	Twos complement (PCM)	Asynchronous	44.1
05	16-bit	Stereo	Twos complement (PCM)	Asynchronous	32
06	16-bit	Mono	Twos complement (PCM)	Asynchronous	32
07	16-bit	Stereo	Twos complement (PCM)	Asynchronous	22.05
08	16-bit	Mono	Twos complement (PCM)	Asynchronous	22.05
09	16-bit	Stereo	Twos complement (PCM)	Asynchronous	16
0A	16-bit	Mono	Twos complement (PCM)	Asynchronous	16
0B	8-bit	Stereo	Twos complement (PCM)	Asynchronous	16
0C	8-bit	Mono	Twos complement (PCM)	Asynchronous	16
0D	8-bit	Stereo	Twos complement (PCM)	Asynchronous	8
0E	8-bit	Mono	Twos complement (PCM)	Asynchronous	8
0F	16-bit	Stereo	Twos complement (PCM)	Synchronous	11.025
10	16-bit	Mono	Twos complement (PCM)	Synchronous	11.025
11	8-bit	Stereo	Twos complement (PCM)	Synchronous	11.025
12	8-bit	Mono	Twos complement (PCM)	Synchronous	11.025

9.5.2.4 Interface Number 3

Interface number 3 is the interrupt data-in interface. Alternative setting number 0 is the only possible setting for interface number 3. Interface number 3 consists of the HID consumer control device and reports the status of these three key parameters:

- Mute (0xE209)
- Volume up (0xE909)
- Volume down (0xEA09)

9.5.3 Interface Sequence

9.5.3.1 Power On, Attach, and Playback Sequence

The PCM2903C is ready for setup when the reset sequence has finished and the USB bus is attached. In order to perform certain reset sequences defined in the USB specification, V_{DD} , V_{CC} , V_{CCP1} , V_{CCP2} , and V_{CCX} must rise up within 10 ms / 3.3 V. After connection has been established by setup, the PCM2903C is ready to accept USB audio data. While waiting, the audio data (idle state) and analog output are set to bipolar zero (BPZ).

When receiving the audio data, the PCM2903C stores the first audio packet, which contained 1-ms audio data, into the internal storage buffer. The PCM2903C starts playing the audio data when detecting the next start of frame (SOF) packet, as illustrated in Figure 36 and Figure 37.

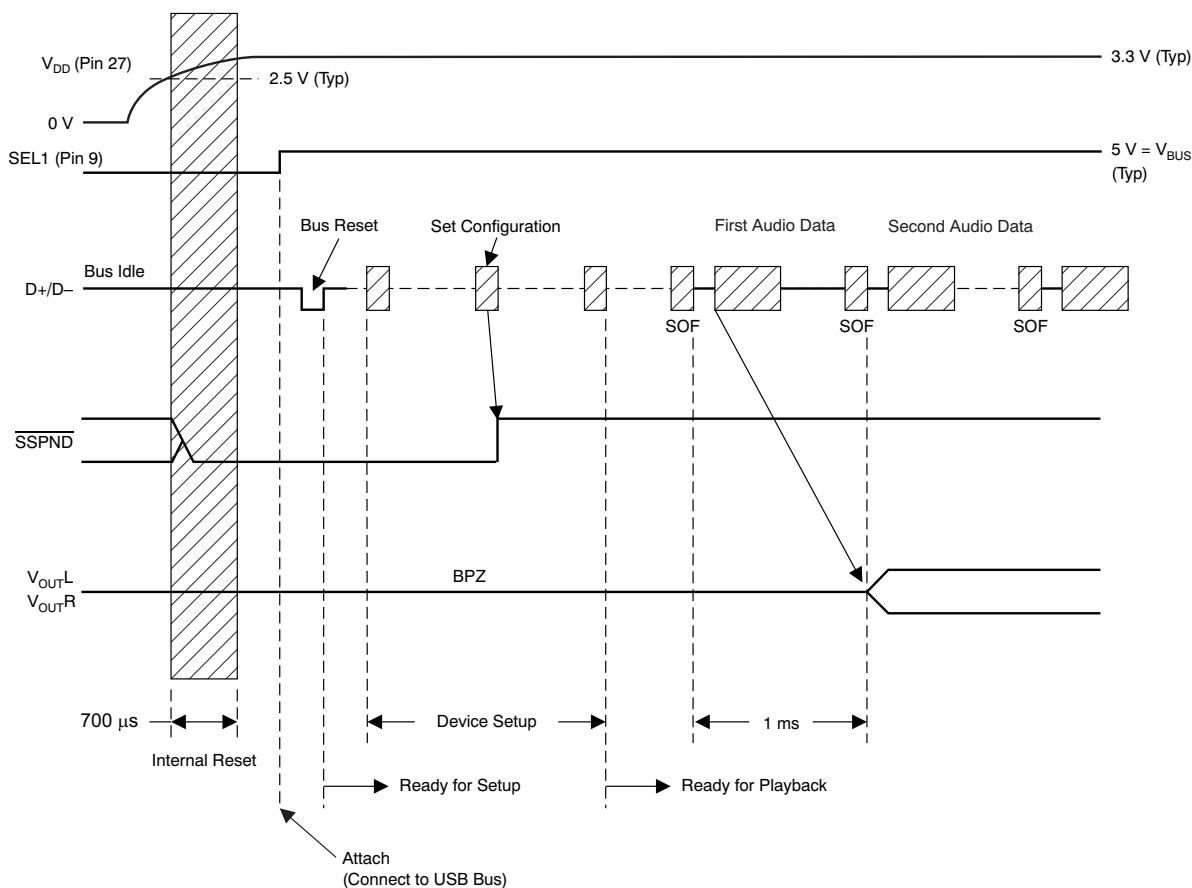
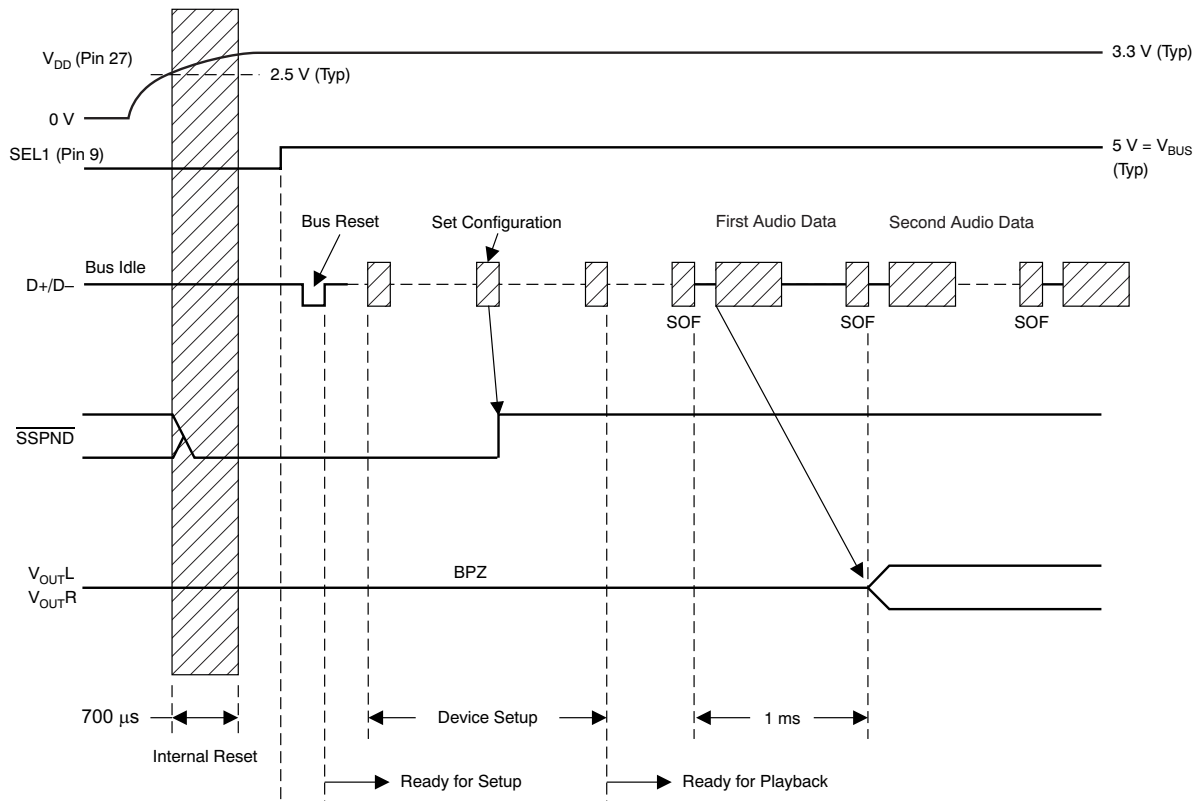
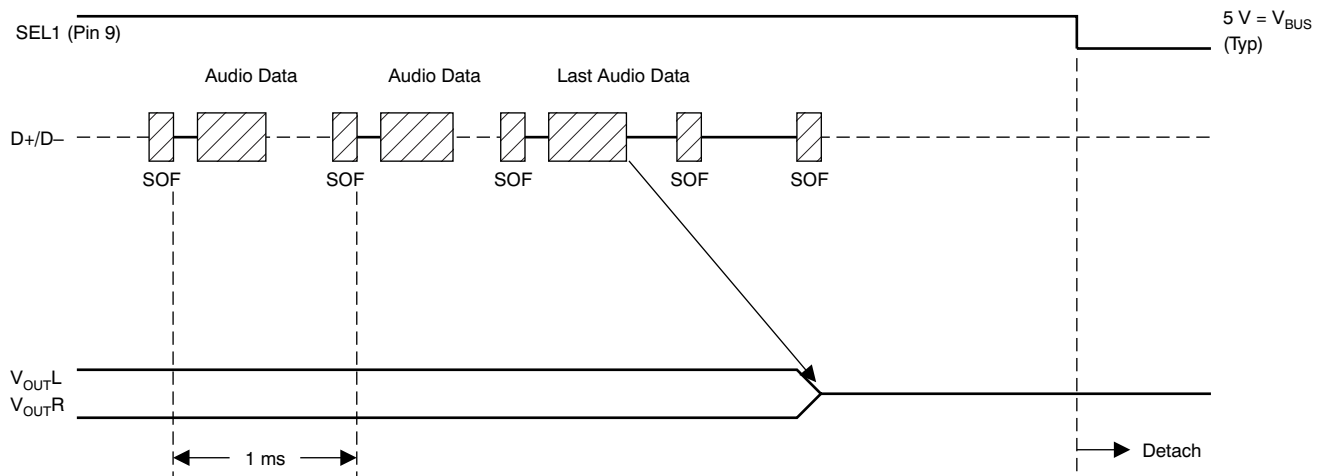


Figure 36. Attach After Poweron


Figure 37. Poweron Under Attach

9.5.3.2 Play, Stop, and Detach Sequence

When the host finishes or aborts the playback, the PCM2903C stops playing after the last audio data have played, as shown in Figure 38.


Figure 38. Play, Stop, and Detach Sequence

9.5.3.3 Record Sequence

The PCM2903C starts the audio capture into the internal memory after receiving the SET_INTERFACE command, as shown in Figure 39.

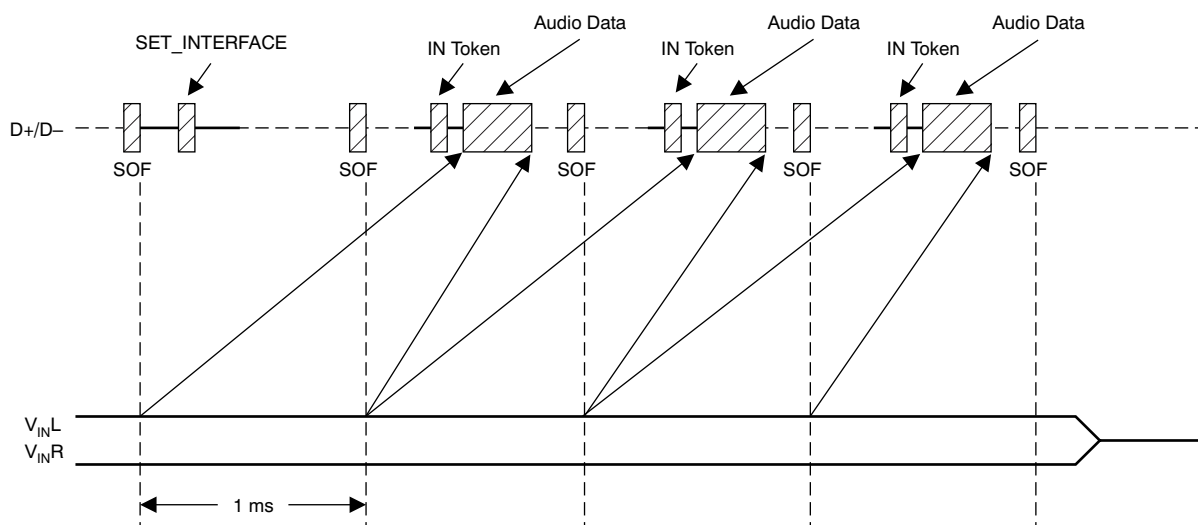


Figure 39. Record Sequence

9.5.3.4 Suspend and Resume Sequence

The PCM2903C enters the suspend state after it detects a constant idle state on the USB bus (approximately 5 ms), as shown in Figure 40. While the PCM2903C enters the suspend state, the SSPND flag (pin 28) is asserted. The PCM2903C wakes up immediately after detecting a non-idle state on the USB bus.

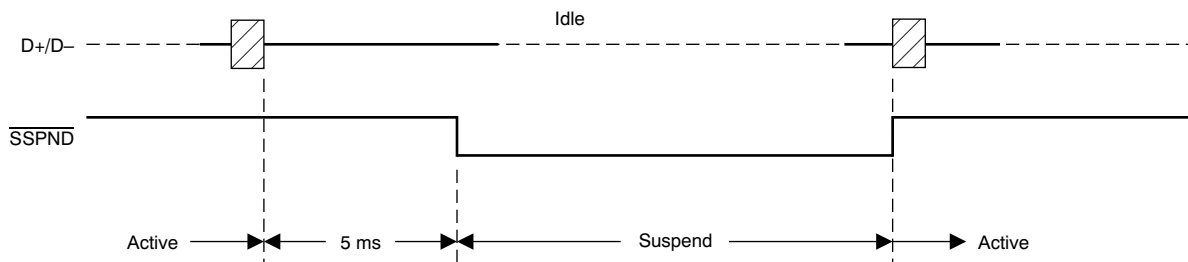


Figure 40. Suspend and Resume Sequence

10 Application and Implementation

NOTE

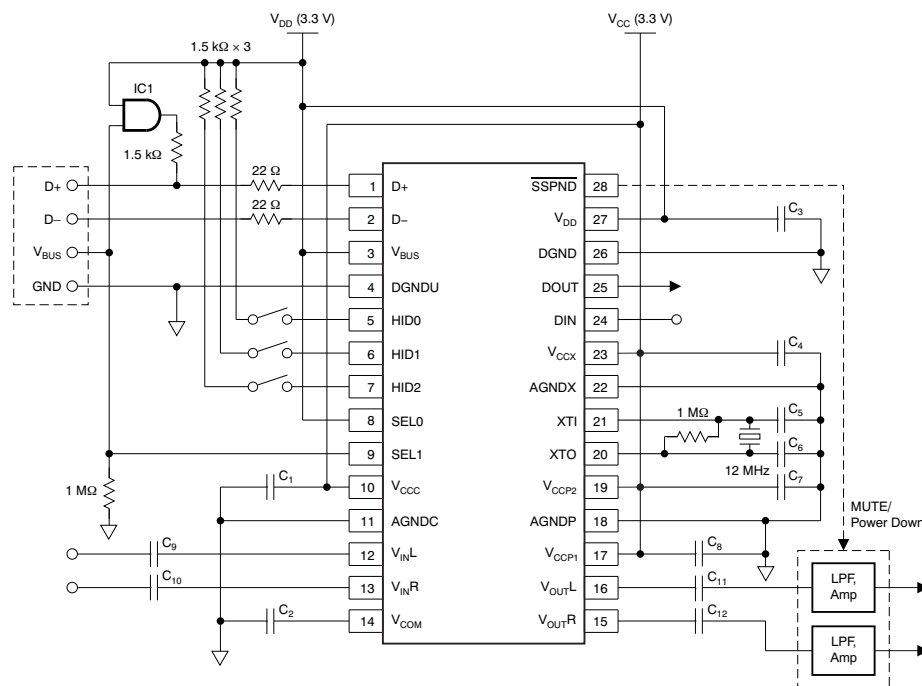
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The V_{BUS} allows the device to know when it has been plugged to a USB connection port. The SSPND' flag will notify when the USB input is idle for at least 5ms; this flag can be used to control or notify subsequent circuits. More functional details can be found on [Interface Sequence](#).

10.2 Typical Application

Figure 41 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.



NOTE: IC1 must be driven by V_{DD} with a 5-V tolerant input.

$C_1, C_2, C_3, C_4, C_7, C_8$: 10 μ F

C_5, C_6 : 10 pF to 33 pF (depending on crystal resonator)

$C_9, C_{10}, C_{11}, C_{12}$: The capacitance may vary depending on design.

Figure 41. Self-Powered Configuration

10.2.1 Design Requirements

For this example, [Table 6](#) lists the design parameters.

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3 V to 3.6 V
Current	50 mA to 70 mA
Input clock frequency	11.994 MHz to 12.006 MHz

10.2.2 Detailed Design Procedure

The PCM2903C is a simple design device since it is capable to connect directly to a USB port. Only two external ICs are needed, a 3.3-V regulator and an AND Gate. The switches connected to the HID ports must be normally open. Other than this, it only needs decoupling capacitors on the voltage source pins.

10.2.3 Application Curves

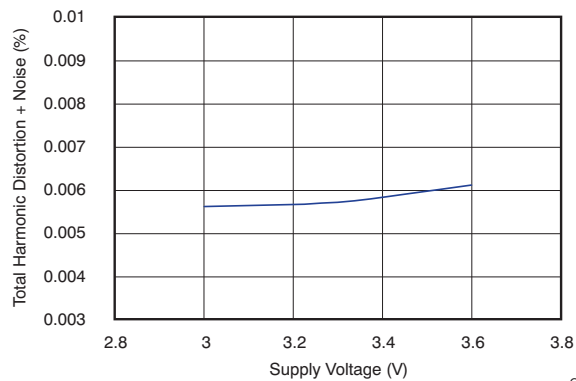


Figure 42. ADC Total Harmonic Distortion + Noise at -1 dB vs Supply Voltage

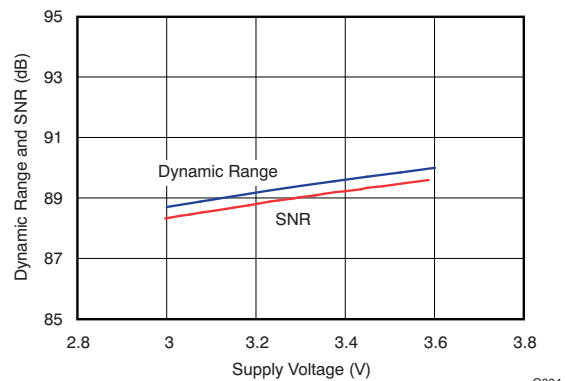


Figure 43. ADC Dynamic Range and SNR vs Supply Voltage

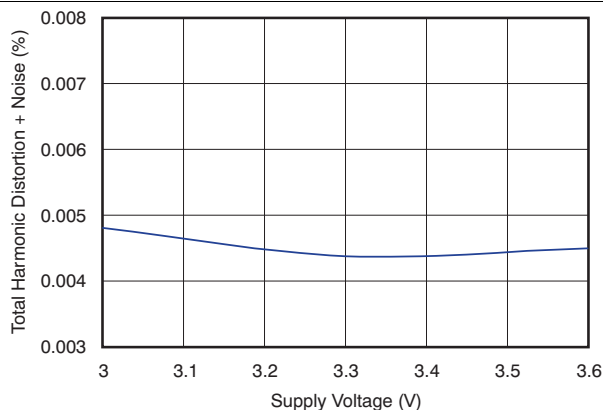


Figure 44. DAC Total Harmonic Distortion + Noise at 0 dB vs Supply Voltage

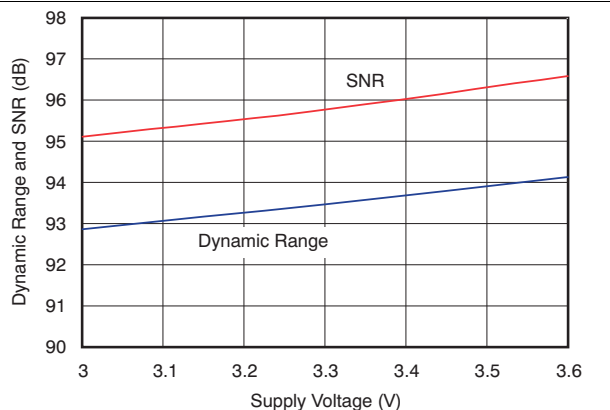


Figure 45. DAC Dynamic Range and SNR vs Supply Voltage

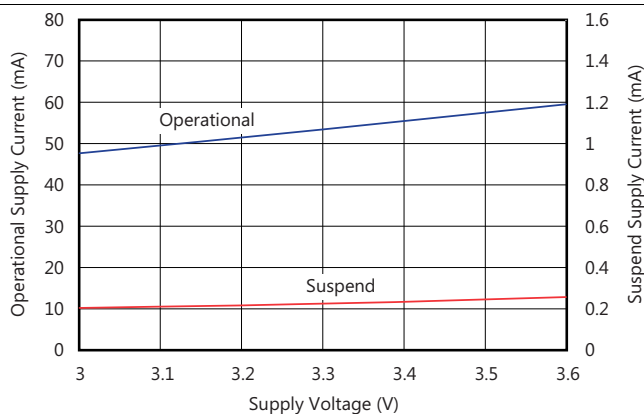


Figure 46. Operational and Suspend Supply Current vs Supply Voltage

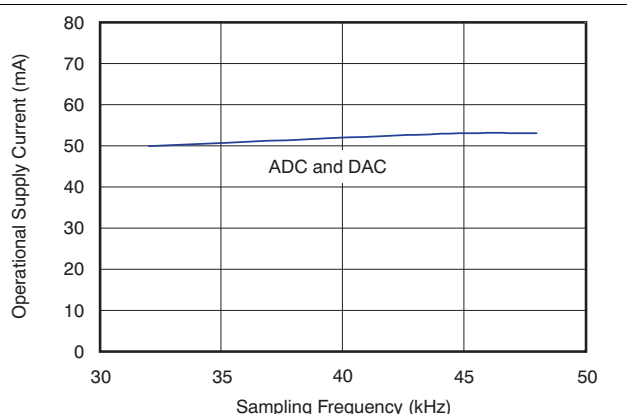


Figure 47. Operational Supply Current vs Sampling Frequency

11 Power Supply Recommendations

The voltage source needed to power the PCM2903C must be between 3 V and 3.6 V for a proper operation. It is recommended to place decoupling capacitor in every voltage source pin. This will help filter lower frequency power supply noise. Place these decoupling capacitors as close as possible to the PCM2903C.

12 Layout

12.1 Layout Guidelines

The decoupling capacitors must be as close as possible to the PCM2903C pins. It is recommended to place a lowpass Filter in the analog input and output. At least the analog input and analog output need a series capacitor to eliminate any possible offset level. The PCM2903C is a low power device so there is no need for a special heat sink PCB design.

12.2 Layout Example

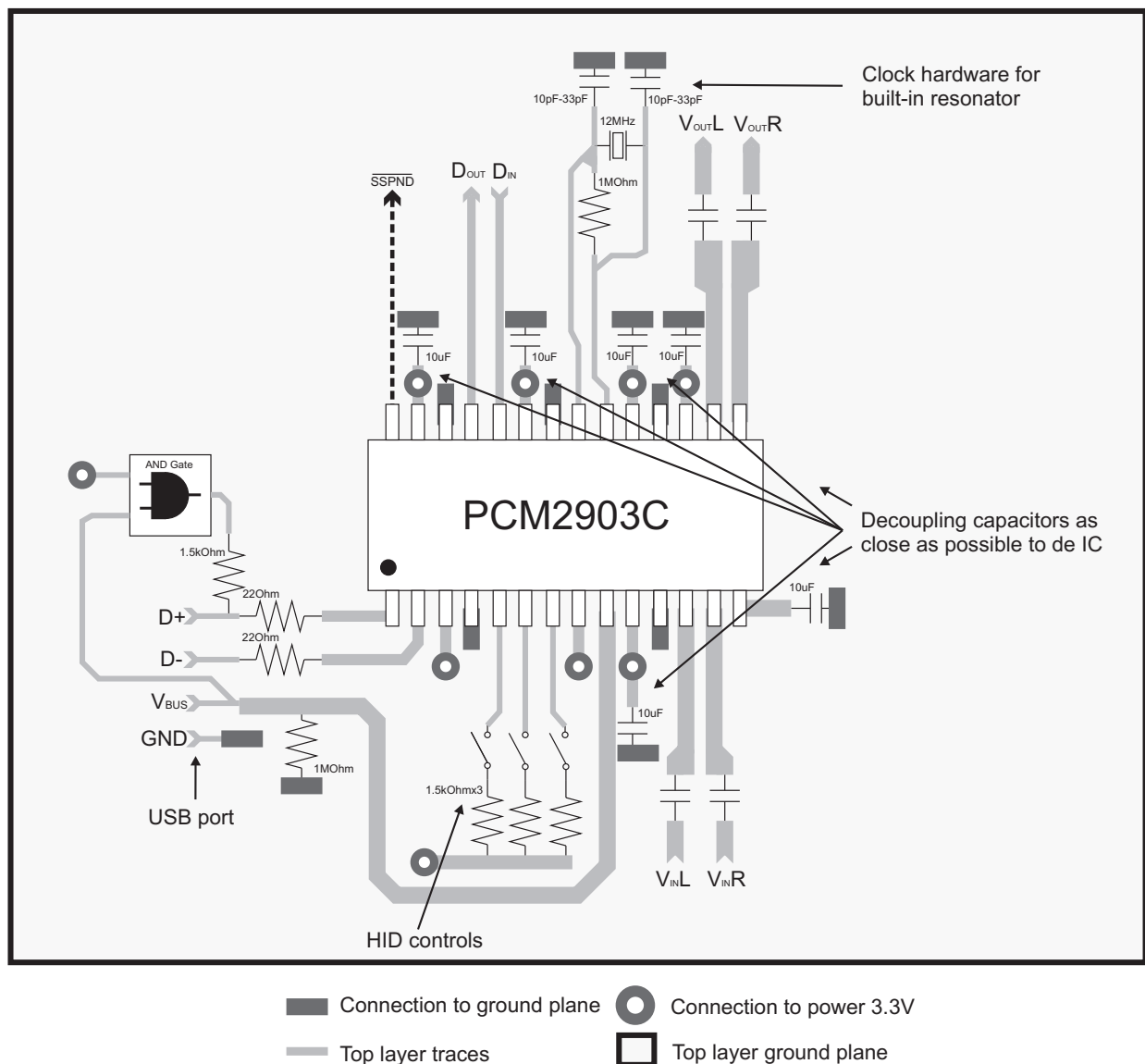


Figure 48. Layout Example Recommendation

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

- 已更新 PCM270X 和 PCM290X 的工作环境 应用, [SLAA374](#)

13.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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13.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本, 请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM2903CDB	Active	Production	SSOP (DB) 28	50 TUBE	Yes	Call TI Nipdau	Level-1-260C-UNLIM	-25 to 85	PCM2903C
PCM2903CDB.B	Active	Production	SSOP (DB) 28	50 TUBE	Yes	Call TI	Level-1-260C-UNLIM	-25 to 85	PCM2903C
PCM2903CDBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2903C
PCM2903CDBR.B	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2903C
PCM2903CDBRG4	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	PCM2903C
PCM2903CDBRG4.B	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	PCM2903C

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

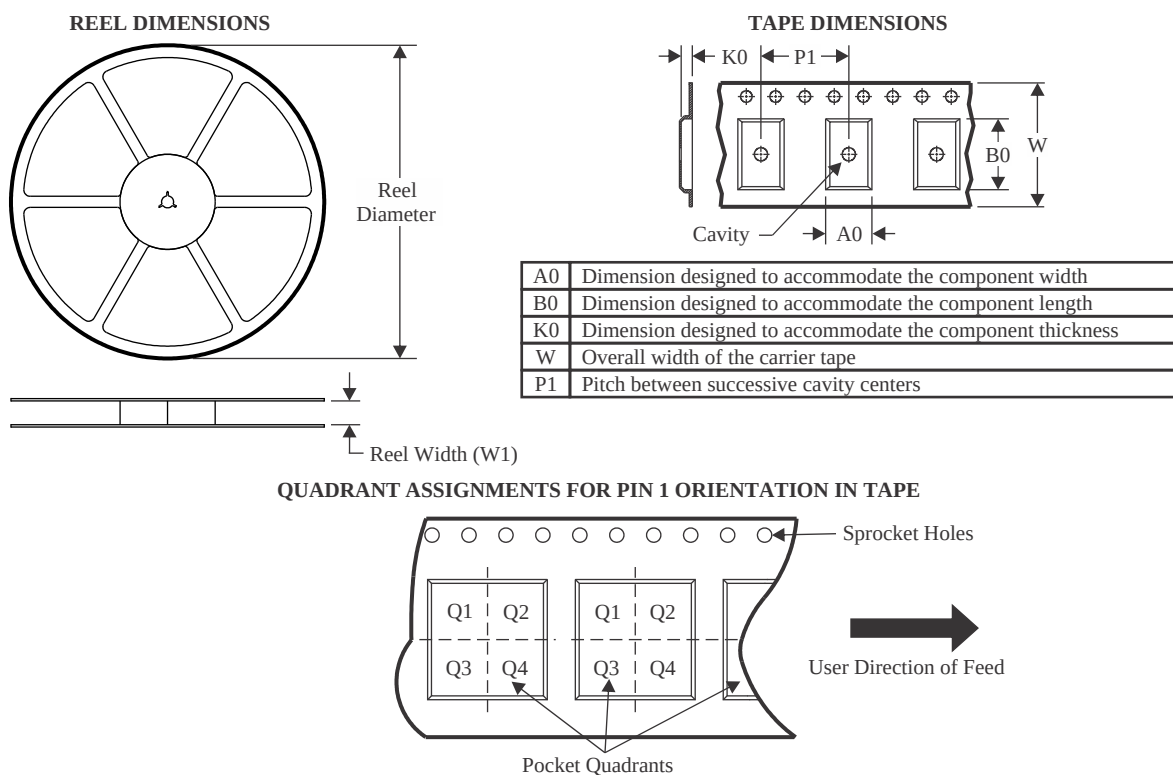
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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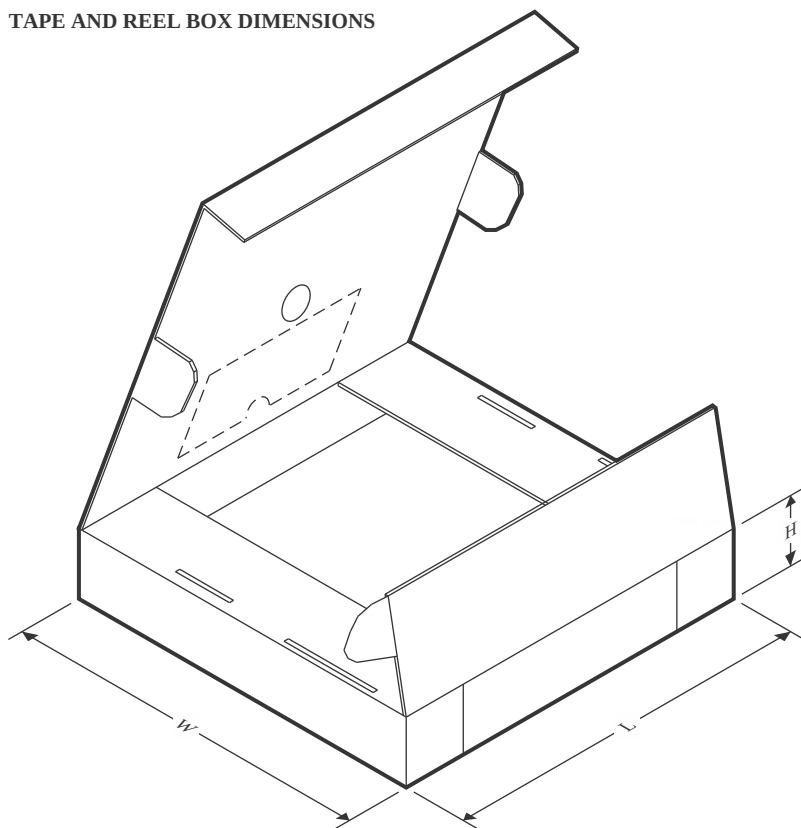
TAPE AND REEL INFORMATION



*All dimensions are nominal

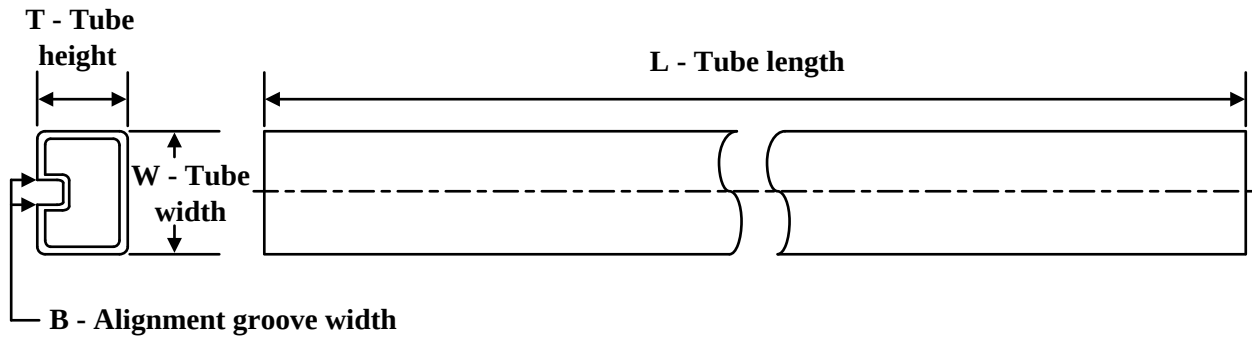
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM2903CDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
PCM2903CDBRG4	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

TAPE AND REEL BOX DIMENSIONS



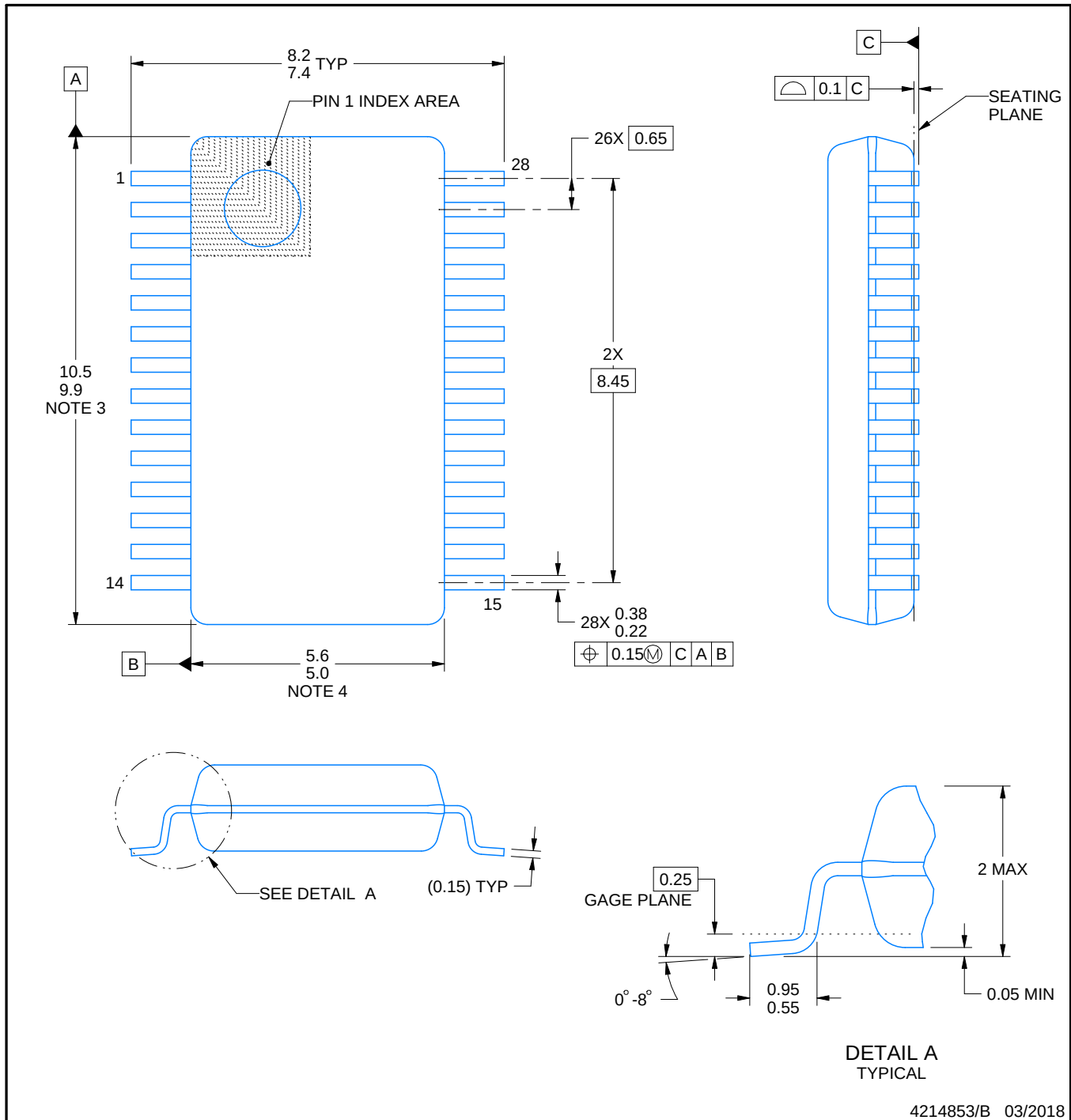
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM2903CDBR	SSOP	DB	28	2000	353.0	353.0	32.0
PCM2903CDBRG4	SSOP	DB	28	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
PCM2903CDB	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2903CDB	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2903CDB.B	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2903CDB.B	DB	SSOP	28	50	530	10.5	4000	4.1



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NOTES:

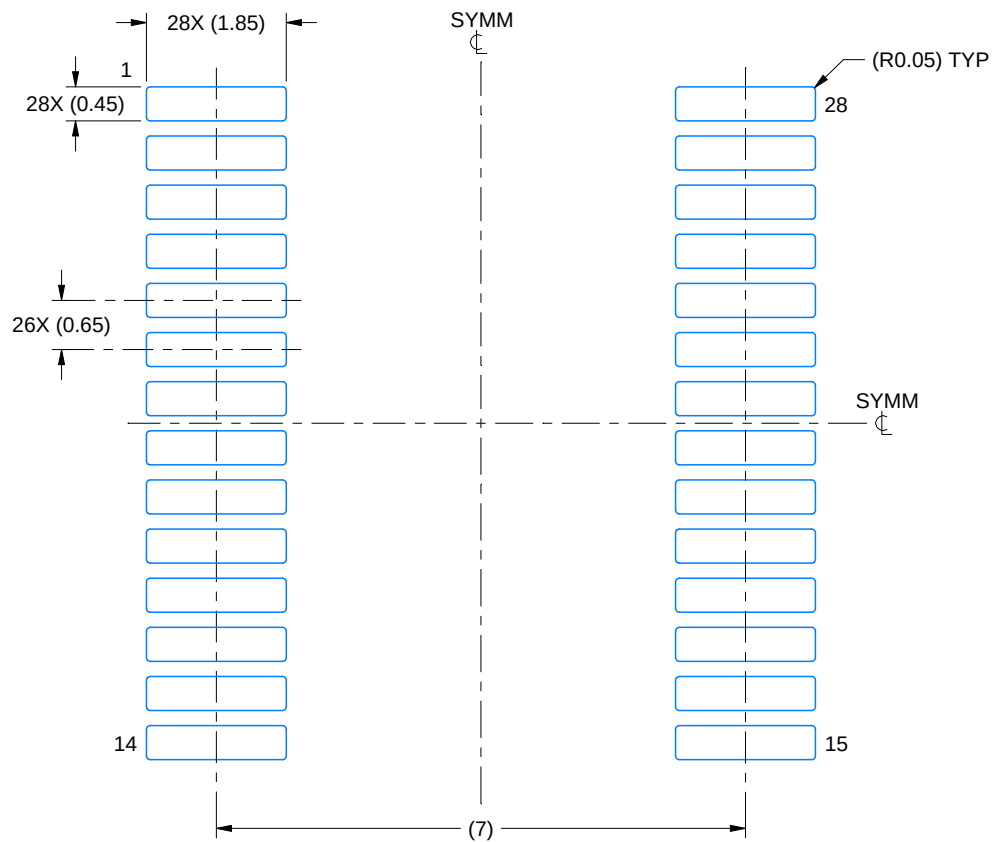
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

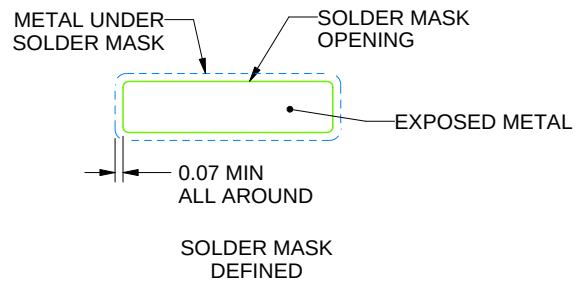
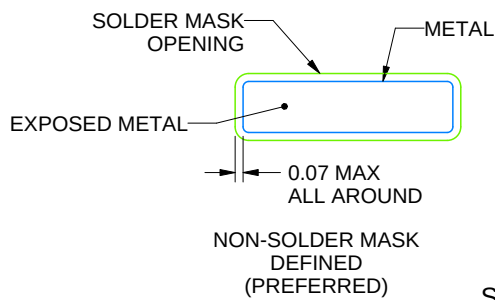
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

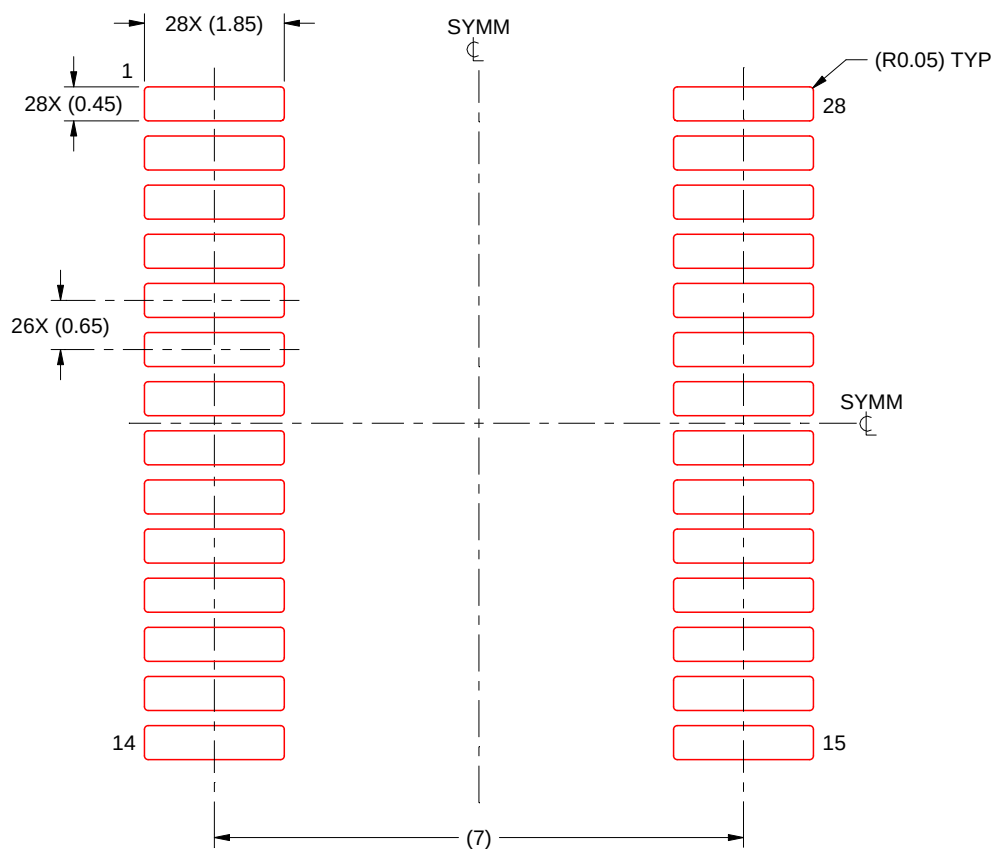
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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