# ONET2804TLP
# 低功耗 28 Gbps、4 通道限幅 TIA

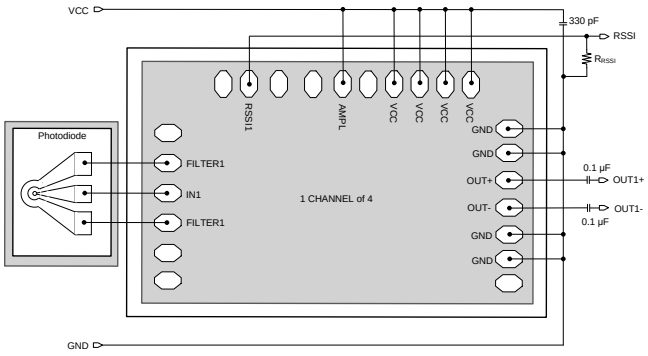
## 1 特性

- 4 通道多速率操作：高达 28Gbps
- 电源为 3V 时的功耗：每通道 90mW
- 差动互阻抗：7.5kΩ
- 带宽：17.5GHz
- 输入噪声：2μ$A_{rms}$
- 输入过载电流：3.2m$A_{PP}$
- 可编程输出电压
- 可调增益和带宽
- 每通道的接收信号强度指示器 (RSSI)
- 通道之间的隔离（仅限于裸片）：40 dB
- 单电源：2.8V 至 3.3V
- 增耗垫控制或 2 线控制
- 片上滤波电容器
- 运行温度范围：–40°C 至 +100°C
- 裸片尺寸：3250μm × 1450μm，通道间距为 750μm

## 2 应用

- 100G 以太网光发射器
- ITU OTL4.4
- 具有内部重定时功能的 CFP2、CFP4 和 QSFP28 模块

**LP38690** 的




## 3 说明

ONET2804TLP 器件是一款用于并行光互联的高增益、限幅互阻抗放大器 (TIA)，数据速率高达 28Gbps。此器件与 750μm 间距光电二极管阵列结合使用，可将光信号转换为差分输出电压。由内部电路提供光电二极管反向偏置电压并感测提供给各光电二极管的平均光电流。

该器件可配合引脚控制或两线制串口使用，从而实现对输出幅值、增益、带宽和输入阈值的控制。

ONET2804TLP 具有 17.5GHz 带宽、7.5kΩ 增益、2μ$A_{rms}$ 输入参考噪声和每通道的接收信号强度指示器 (RSSI)。通道间的 40dB 隔离可降低接收器中的串扰。

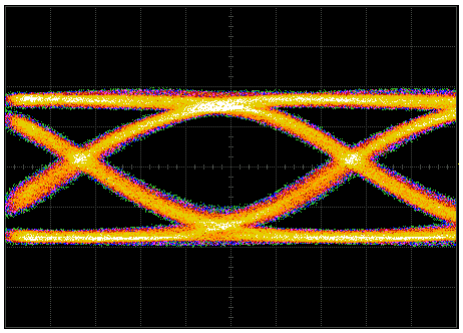
该器件需要单个 2.8V 至 3.3V 电源，每通道典型功耗为 90mW，差分输出幅度为 300 m$V_{PP}$。该器件工作温度范围为 –40°C 至 +100°C，采用裸片形式，通道间距为 750μm。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| ONET2804TLP | 采用叠片封装的裸片 | 3250μm × 1450μm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

眼图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# 目录

**1** 特性 ..... 1
**2** 应用 ..... 1
**3** 说明 ..... 1
**4** 修订历史记录 ..... 2
**5** **Pin Configuration and Functions** ..... 3
**6** **Specifications** ..... 5
6.1 Absolute Maximum Ratings ..... 5
6.2 ESD Ratings ..... 5
6.3 Recommended Operating Conditions ..... 5
6.4 DC Electrical Characteristics ..... 6
6.5 AC Electrical Characteristics ..... 6
6.6 Timing Requirements ..... 7
6.7 Typical Characteristics: General ..... 8
6.8 Typical Characteristics: Eye Diagrams ..... 10
**7** **Detailed Description** ..... 11
7.1 Overview ..... 11
7.2 Functional Block Diagram ..... 11
7.3 Feature Description ..... 12
7.4 Device Functional Modes ..... 13
7.5 Programming ..... 13
7.6 Register Maps ..... 15
**8** **Application and Implementation** ..... 21
8.1 Application Information ..... 21
8.2 Typical Applications ..... 21
**9** **Power Supply Recommendations** ..... 23
**10** **Layout** ..... 24
10.1 Layout Guidelines ..... 24
10.2 Layout Example ..... 24
**11** 器件和文档支持 ..... 27
11.1 接收文档更新通知 ..... 27
11.2 社区资源 ..... 27
11.3 商标 ..... 27
11.4 静电放电警告 ..... 27
11.5 Glossary ..... 27
**12** 机械、封装和可订购信息 ..... 27

## 4 修订历史记录

| 日期 | 修订版本 | 注意 |
|---|---|---|
| 2017 年 7 月 | * | 初始发行版。 |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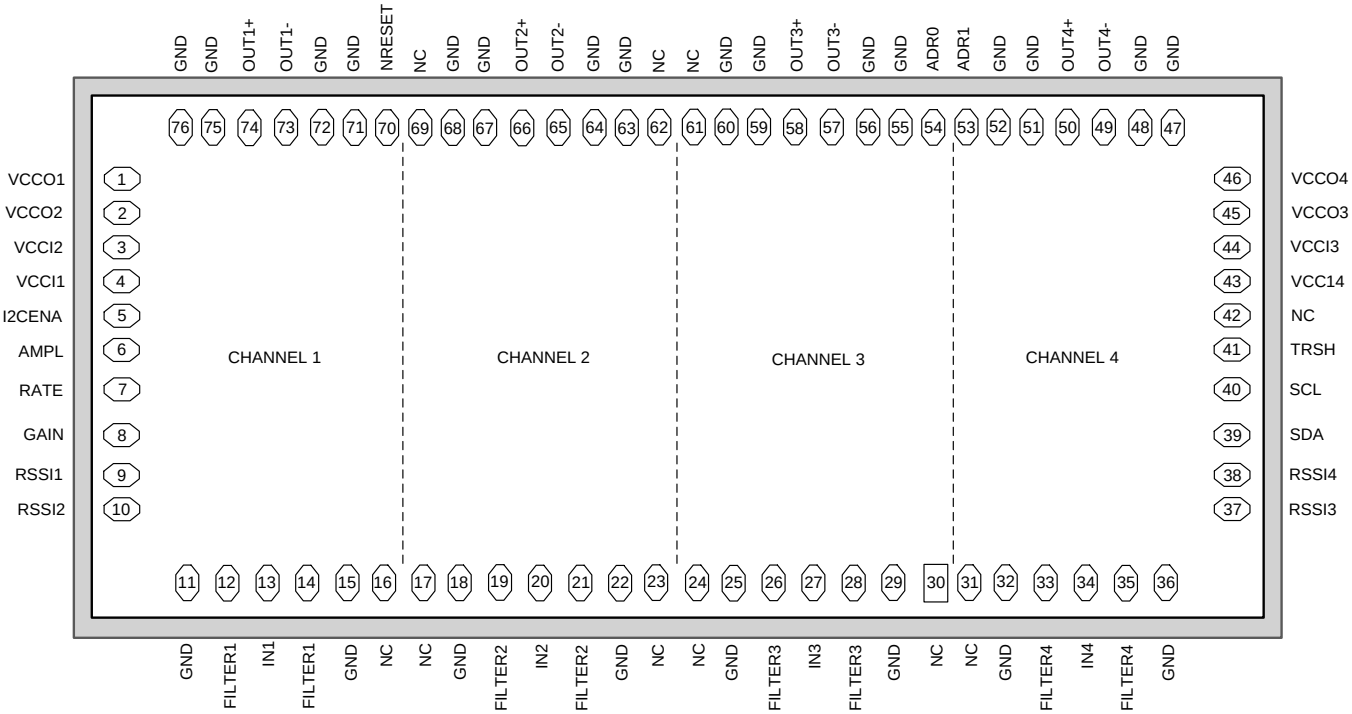
# 5 Pin Configuration and Functions

**ONET2804TLP Bond Pad Assignment: Y Package**
**76-Pad Die**
**Top View**




## Bond Pad Functions

| PAD | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ADR0 | 54 | Digital input | 2-wire interface address programming pin. Leave this pad open for a default address of 0001100. Grounding this pad changes the first address bit to a 1 (0001101). |
| ADR1 | 53 | Digital input | 2-wire interface address programming pin. Leave this pad open for a default address of 0001100. Grounding this pad changes the second address bit to a 1 (0001110). |
| AMPL | 6 | Digital input | 3-state input for amplitude control of all four channels.<br>$V_{CC}$: 500-$mV_{PP}$ differential output swing<br>Open: 300-$mV_{PP}$ differential output swing (default)<br>GND: 250-$mV_{PP}$ differential output swing |
| FILTER1 | 12, 14 | Analog output | FILTERx is the bias voltage for the photodiode cathode.<br>These pads are biased to $V_{CC}$ – 100 mV. |
| FILTER2 | 19, 21 | | |
| FILTER3 | 26, 28 | | |
| FILTER4 | 33, 35 | | |
| GAIN | 8 | Digital input | 3-state input for gain control of all four channels.<br>$V_{CC}$: Minimum transimpedance<br>Open: Default transimpedance<br>GND: Medium transimpedance |
| GND | 11, 15, 18, 22, 25, 29, 32, 36, 47, 48, 51, 52, 55, 56, 59, 60, 63, 64, 67, 68, 71, 72, 75, 76 | Supply | Circuit ground. All GND pads are connected on the die.<br>Bonding all pads is recommended, except for pads 11, 15, 18, 22, 25, 29, 32, and 36. |

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## Bond Pad Functions (continued)

| PAD | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| I2CENA | 5 | Digital input | 2-wire control option. Leave the pad unconnected for pad control of the device. Two-wire control can be enabled by applying a high signal to the pad. |
| IN1 | 13 | Analog input | INx is the data input to corresponding TIA channel (connect to photodiode anode) |
| IN2 | 20 | | |
| IN3 | 27 | | |
| IN4 | 34 | | |
| NC | 16, 17, 23, 24, 30, 31, 42, 61, 62, 69 | No connection | Do not connect |
| NRESET | 70 | Digital input | Used to reset the 2-wire state machine and registers. Leave open for normal operation and set low to reset the 2-wire interface. |
| OUT1– | 73 | Analog output | Inverted CML data output for channel x. On-chip, 50-Ω, back-terminated to $V_{CC}$. |
| OUT2– | 65 | | |
| OUT3– | 57 | | |
| OUT4– | 49 | | |
| OUT1+ | 74 | Analog output | Noninverted CML data output for channel x. On-chip, 50-Ω, back-terminated to $V_{CC}$. |
| OUT2+ | 66 | | |
| OUT3+ | 58 | | |
| OUT4+ | 50 | | |
| RATE | 7 | Digital input | 3-state input for bandwidth control of all four channels. $V_{CC}$: Increase the bandwidth Open: 21-GHz bandwidth (default) GND: Reduce the bandwidth |
| RSSI1 | 9 | Analog output | Indicates the strength of the received signal (RSSI) for channel x if the photodiode is biased from FILTERx. The analog output current is proportional to the input data amplitude. Connect to an external resistor to ground (GND). For proper operation, ensure that the voltage at the RSSIx pad does not exceed $V_{CC}$ – 0.65 V. If the RSSI feature is not used, leave these pads open. |
| RSSI2 | 10 | | |
| RSSI3 | 37 | | |
| RSSI4 | 38 | | |
| SCL | 40 | Digital input | 2-wire interface serial clock input. Includes a 10-kΩ pullup resistor to $V_{CC}$. |
| SDA | 39 | Digital input/output | 2-wire interface serial data input. Includes a 10-kΩ pullup resistor to $V_{CC}$. |
| TRSH | 41 | Digital input | 3-state input for the threshold control. $V_{CC}$: Crossing point shifted down Open: No threshold adjustment (default) GND: Crossing point shifted up |
| $V_{CC}I1$ | 4 | Supply | 2.8 V to 3.47 V supply voltage for the input TIAx stage. |
| $V_{CC}I2$ | 3 | | |
| $V_{CC}I3$ | 44 | | |
| $V_{CC}I4$ | 43 | | |
| $V_{CC}O1$ | 1 | Supply | 2.8 V to 3.47 V supply voltage for the AGCx and CMLx amplifiers. |
| $V_{CC}O2$ | 2 | | |
| $V_{CC}O3$ | 45 | | |
| $V_{CC}O4$ | 46 | | |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage(1) | $V_{CC}$Ix, $V_{CC}$Ox | –0.3 | 4 | V |
| Voltage(1) | FILTERx, OUTx+, OUTx–, RSSIx, SCL, SDA, I2CENA, ICC_ADJ, AMPL, RATE, GAIN, TRSH, ADR1, ADR0, and NRESET | –0.3 | 4 | V |
| Average input current | INx | –0.7 | 5 | mA |
| | FILTERx | –8 | 8 | mA |
| Continuous current at outputs | OUTx+, OUTx– | –8 | 8 | mA |
| Maximum junction temperature, $T_J$ | | | 125 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) All voltage values are with respect to network ground terminal.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | All pins except INx | ±1000 | V |
| | | | INx pins | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.8 | 3.3 | 3.47 | V |
| $I_{(INx)}$ | Average input current | | | | 2.7 | mA |
| $T_A$ | Operating backside die temperature | | –40 | | 100 | °C |
| $L_{(FILTER)}$, $L_{(IN)}$ | Wire-bond inductance at the FILTERx and INx pins | | | 0.3 | | nH |
| $C_{(PD)}$ | Photodiode capacitance | | | 0.1 | | pF |
| $V_{IH}$ | Digital input high voltage | SDA, SCL | 2 | | | V |
| $V_{IL}$ | Digital input low voltage | SDA, SCL | | | 0.8 | V |
| | 3-state input high voltage | | $V_{CC}$ – 0.4 | | | V |
| | 3-state input low voltage | | | | 0.4 | V |

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## 6.4 DC Electrical Characteristics

over recommended operating conditions with $V_{OD}$ = 300 $mV_{PP}$ (unless otherwise noted); typical values are at $V_{CC}$ = 3.3 V and $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | TEST LEVEL(1) |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.8 | 3.3 | 3.47 | V | A |
| $I_{CC}$ | Supply current | Per channel, 30-$\mu A_{PP}$ input, 27°C | 22 | | 42 | mA | A |
| | | Per channel, 30-$\mu A_{PP}$ input, maximum 85°C | | 30 | | | C |
| | | Per channel, 30-$\mu A_{PP}$ input, maximum 100°C | | 36 | | | C |
| $P_{(RX)}$ | Receiver power dissipation | Per channel, 30-$\mu A_{PP}$ input, 27°C | 73 | | 139 | mW | A |
| | | Per channel, 30-$\mu A_{PP}$ input, maximum 85°C | | 99 | | | C |
| | | Per channel, 30-$\mu A_{PP}$ input, maximum 100°C | | 118 | | | C |
| $V_{IN}$ | Input bias voltage | | 0.75 | 0.85 | 0.98 | V | A |
| $R_{OUT}$ | Output resistance | Single-ended to $V_{CC}$ | 40 | 50 | 60 | Ω | A |
| $V_{(FILTER)}$ | Photodiode bias voltage(2) | | 2.8 | 3.2 | | V | A |
| $A_{(RSSI_IB)}$ | RSSI gain | Resistive load to GND(3) | 0.49 | 0.5 | 0.54 | A/A | A |
| | RSSIx feature output offset current (no light) | | 0 | | 2.5 | µA | A |

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Regulated voltage is typically 100 mV lower than $V_{CC}$.
(3) The RSSIx output is a current output that requires a resistive load to ground (GND). The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation, ensure that the voltage at RSSIx does not exceed $V_{CC}$ – 0.65 V.

## 6.5 AC Electrical Characteristics

over recommended operating conditions with $V_{OD}$ = 300 $mV_{PP}$ (unless otherwise noted); typical values are at $V_{CC}$ = 3.3 V and $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | TEST LEVEL(1) |
|---|---|---|---|---|---|---|---|
| $Z_{21}$ | Small-signal transimpedance | 25-$\mu A_{PP}$ input signal | | 7.5 | | kΩ | C |
| $f_{(3dB-H)}$ | –3-dB bandwidth | 25-$\mu A_{PP}$ input signal(2) | | 17.5 | | GHz | C |
| $f_{(3dB-L)}$ | Low-frequency, –3-dB bandwidth | | | 30 | | kHz | C |
| $i_{N(IN)}$ | Input-referred RMS noise | CPD = 0.1 pF, 28-GHz BT4 filter(3) | | 2 | | µA | C |
| DJ | Deterministic jitter | 35 $\mu A_{PP} < i_{IN} < 250\ \mu A_{PP}$ (27.95 Gbps, PRBS9 pattern) | | 2 | | $ps_{PP}$ | C |
| | | 250 $\mu A_{PP} < i_{IN} < 500\ \mu A_{PP}$ (27.95 Gbps, PRBS9 pattern) | | 2 | | | C |
| | | 500 $\mu A_{PP} < i_{IN} < 2900\ \mu A_{PP}$ (27.95 Gbps, PRBS9 pattern) | | 4 | | | C |
| $V_{OD}$ | Differential output voltage | 500-$mV_{PP}$ setting | 250 | 500 | 700 | $mV_{PP}$ | C |
| | Crosstalk | Between adjacent channels, up to 20 GHz(4) | | –40 | | dB | C |
| | RSSIx response time | | | 1 | | µs | C |
| PSRR | Power-supply rejection ratio | f < 10 MHz(5) | | –15 | | dB | C |

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) The small-signal bandwidth is specified over process corners, temperature, and supply voltage variation. The assumed photodiode capacitance is 0.1 pF and the bond-wire inductance is 0.3 nH. The small-signal bandwidth strongly depends on environmental parasitics. Careful attention to layout parasitics and external components is necessary to achieve optimal performance.
(3) Input-referred RMS noise is (RMS output noise) / (gain at 100 MHz).
(4) Die only, no wire bonds.
(5) PSRR is the differential output amplitude divided by the voltage ripple on the supply. No input current at INx.


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## 6.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | | | 400 | kHz |
| $t_{BUF}$ | Bus free time between START and STOP conditions | 1.3 | | | µs |
| $t_{HDSTA}$ | Hold time after repeated START condition. After this period, the first clock pulse is generated. | 0.6 | | | µs |
| $t_{LOW}$ | Low period of the SCK clock | 1.3 | | | µs |
| $t_{HIGH}$ | High period of the SCK clock | 0.6 | | | µs |
| $t_{SUSTA}$ | Setup time for a repeated START condition | 0.6 | | | µs |
| $t_{HDDAT}$ | Data hold time | 0 | | | µs |
| $t_{SUDAT}$ | Data setup time | 100 | | | ns |
| $t_R$ | Rise time of both SDA and SCK signals | | | 300 | ns |
| $t_F$ | Fall time of both SDA and SCK signals | | | 300 | ns |
| $t_{SUSTO}$ | Setup time for STOP condition | 0.6 | | | µs |

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## 6.7 Typical Characteristics: General

typical operating condition is at $V_{CC}$ = 3.3 V, $T_A$ = 25°C, and $V_{OD}$ = 300 $mV_{PP}$ (unless otherwise noted)

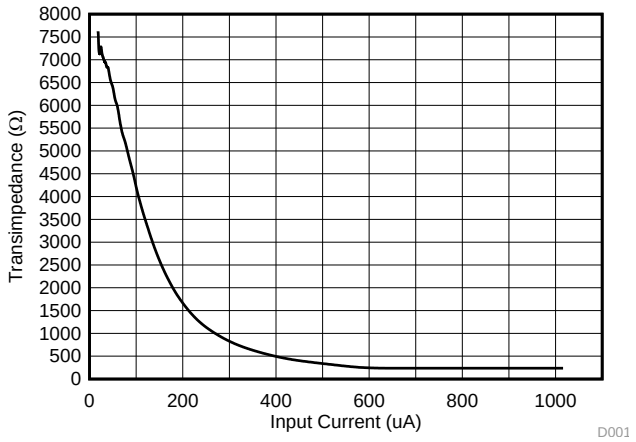


**Figure 1. Transimpedance vs Input Current**

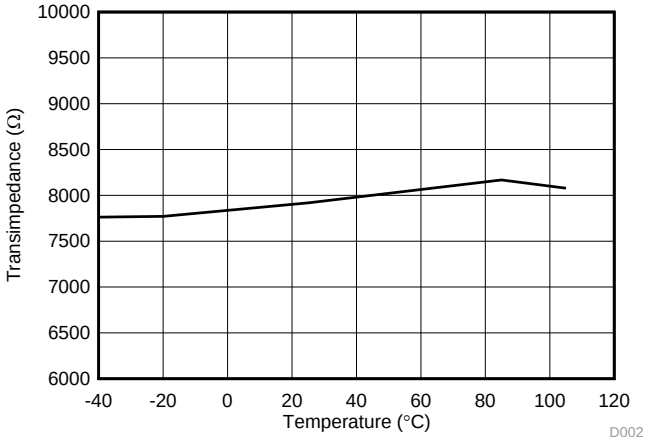


**Figure 2. Small-Signal Transimpedance vs Ambient Temperature**

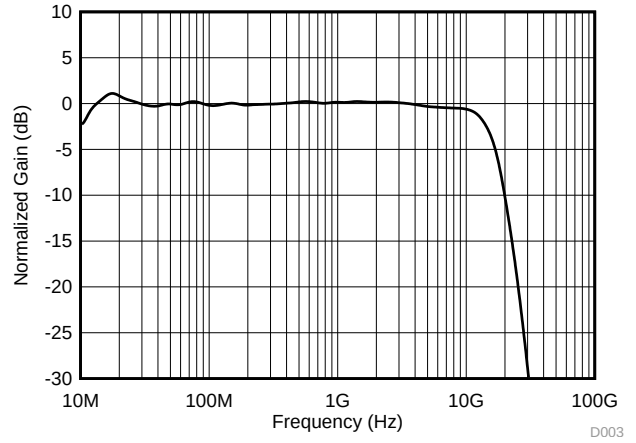


**Figure 3. Gain vs Frequency (Test Fixture Loss De-Embedded)**

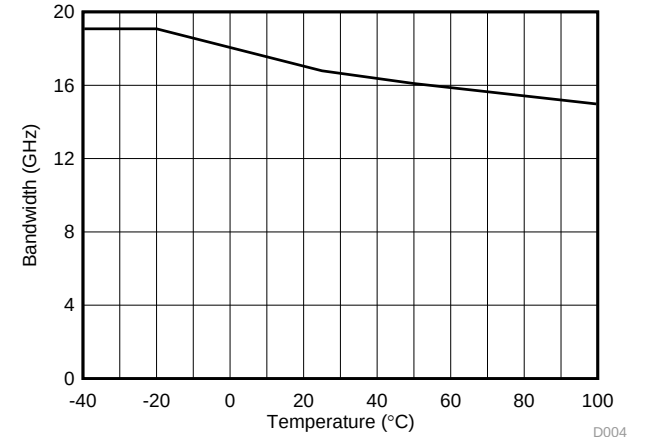


**Figure 4. Small-Signal Bandwidth vs Ambient Temperature (Test Fixture Loss De-Embedded)**

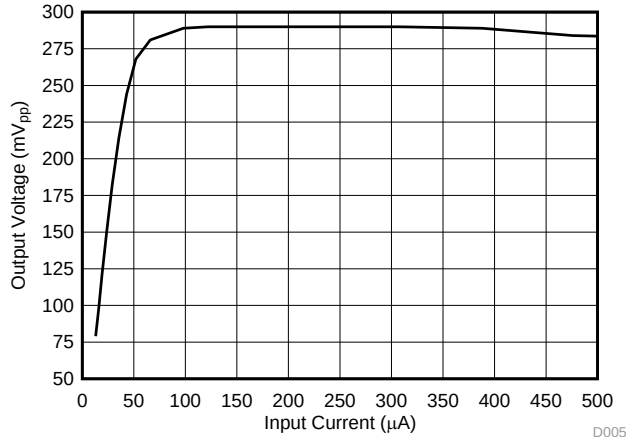


**Figure 5. Differential Output Voltage vs Input Current**

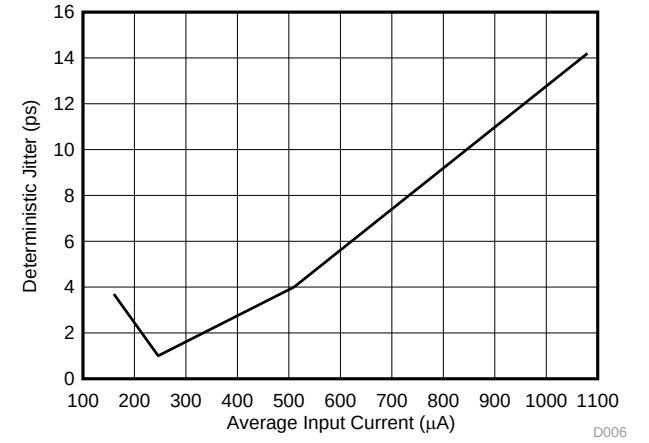


**Figure 6. Deterministic Jitter vs Input Current**


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## Typical Characteristics: General (continued)

typical operating condition is at $V_{CC}$ = 3.3 V, $T_A$ = 25°C, and $V_{OD}$ = 300 $mV_{PP}$ (unless otherwise noted)

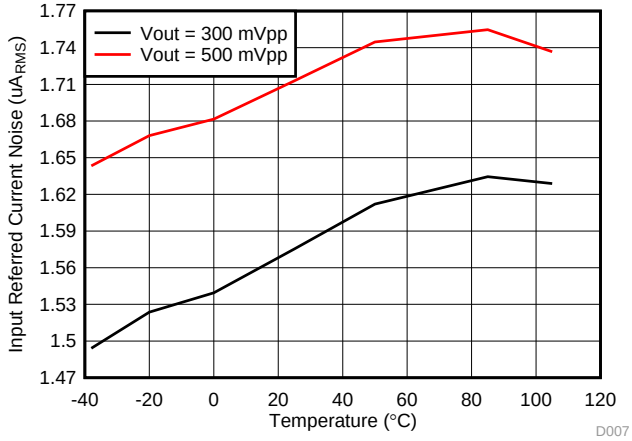


**Figure 7. Input-Referred Noise vs Ambient Temperature**

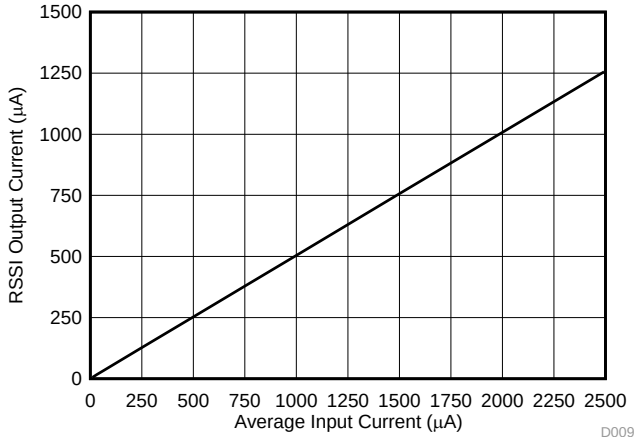


**Figure 8. RSSIx Output Current vs Average Input Current**

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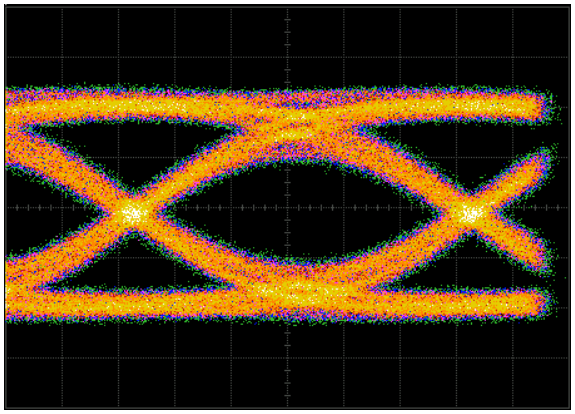
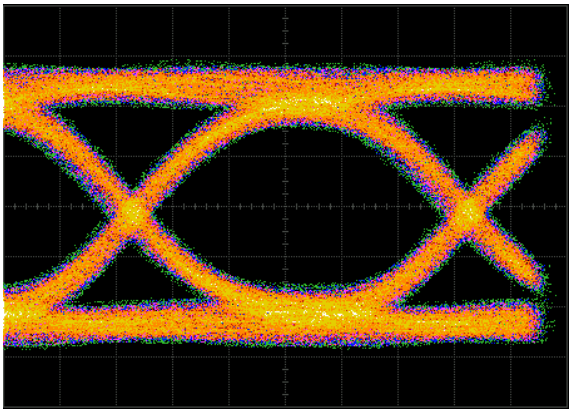
## 6.8 Typical Characteristics: Eye Diagrams

typical operating condition is at $V_{CC}$ = 3.3 V, $T_A$ = 25°C, and $V_{OD}$ = 500 $mV_{PP}$ (unless otherwise noted)



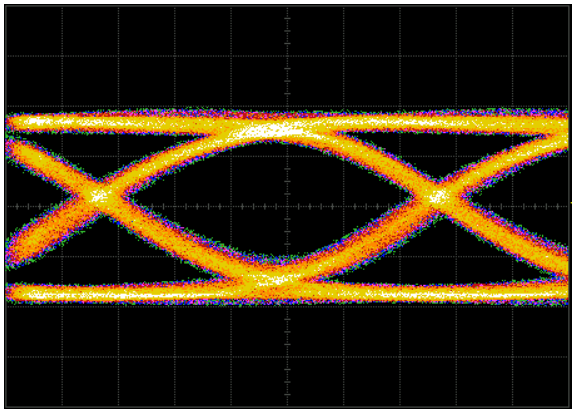
27.95 Gbps

**Figure 9. Output Eye-Diagram, 30-$\mu A_{PP}$ Input Current**



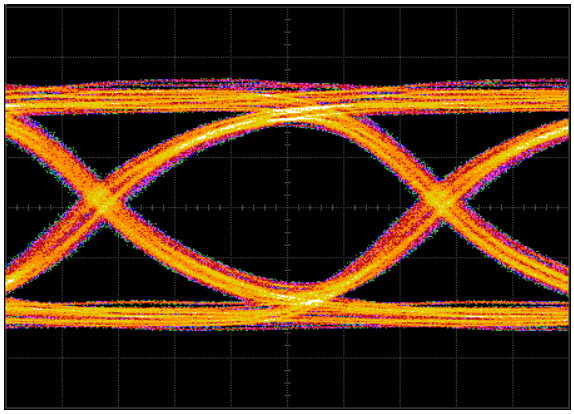
27.95 Gbps

**Figure 10. Output Eye-Diagram, 500-$\mu A_{PP}$ Input Current**



27.95 Gbps

**Figure 11. Output Eye-Diagram, 1.5-$mA_{PP}$ Input Current**



27.95 Gbps

**Figure 12. Output Eye-Diagram, 2.5-$mA_{PP}$ Input Current**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# 7 Detailed Description

## 7.1 Overview

The *Functional Block Diagram* section shows a simplified block diagram for one channel of the ONET2804TLP.

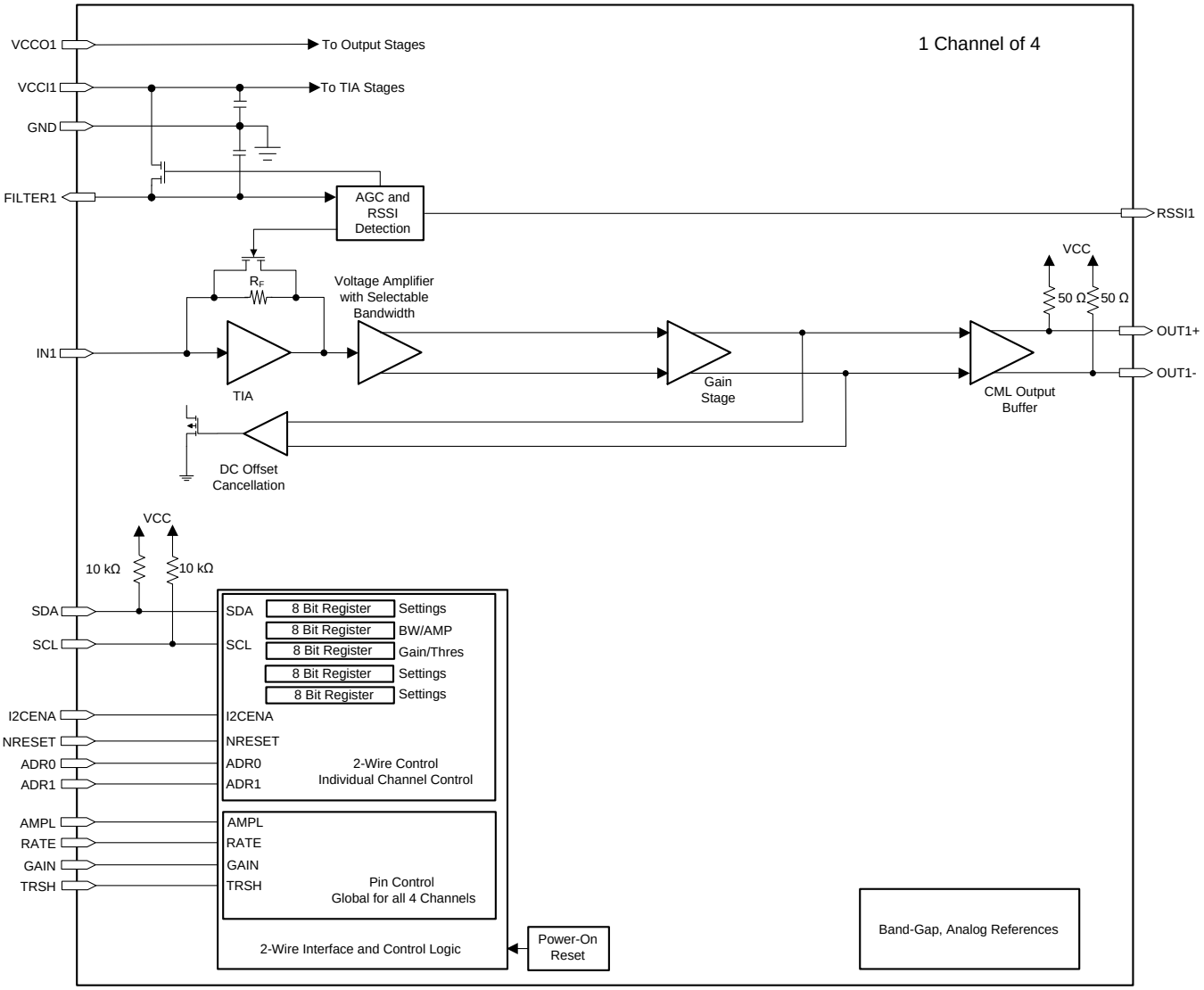
The ONET2804TLP consists of the signal path, supply filters, a control block for dc input bias, automatic gain control (AGC) and received signal strength indication (RSSI), an analog reference block and a two-wire serial interface and control logic block.

The signal path consists of a transimpedance amplifier (TIA) stage, a voltage amplifier, and a current-mode logic (CML) output buffer. The on-chip filter circuit provides a filtered $V_{CC}$ for the PIN photodiode and for the transimpedance amplifier. The RSSI provides the bias for the TIA stage and control for the AGC.

The DC input bias circuit and automatic gain control use internal low-pass filters to cancel the DC current on the input and to adjust the transimpedance amplifier gain. Furthermore, circuitry is provided to monitor the received signal strength.

The output amplitude, gain, bandwidth, and input threshold can be globally controlled through pin settings or each channel can be individually controlled through the two-wire interface.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Signal Path

The first stage of the signal path is a transimpedance amplifier that converts the photodiode current into a voltage. If the input signal current exceeds a certain value, the transimpedance gain is reduced by means of a nonlinear AGC circuit to limit the signal amplitude.

The second stage is a limiting voltage amplifier that provides additional limiting gain and converts the single-ended input voltage into a differential data signal. The output stage provides CML outputs with an on-chip, 50-Ω termination to $V_{CC}$.

The TIA has adjustable gain, amplitude, bandwidth, and input threshold that can be globally controlled through pad settings or each channel can be individually controlled through the two-wire interface. The default mode of operation is pad control where the state (open, high, or low) of the AMPL, BW, GAIN, and TRSH pads sets the respective parameter. To enable two-wire control, set the I2CENA pad high and the functionality of each channel can be controlled individually through the two-wire interface.

### 7.3.2 Gain Adjustment

The gain of all TIAs can be adjusted using the GAIN pad (pad 8) in pad control mode. Gain is set to default if the pad is left open. Gain is reduced by approximately 4 dB if the pad is tied to ground, and reduced by approximately 8 dB if the pad is tied to $V_{CC}$. In two-wire control mode, the gain of each channel can be adjusted from minimum to default. Gain is controlled with the GAIN[1:0] bits in registers 2, 8, 14, and 20 for channels 1, 2, 3, and 4, respectively.

### 7.3.3 Amplitude Adjustment

The output amplifier of all buffers can be adjusted using the AMPL pad (pad 6) in pad control mode. The amplitude is set to 300 $mV_{PP}$ differential if the pad is left open, 250 $mV_{PP}$ if the pad is tied to ground, and 450 $mV_{PP}$ if the pad is tied to $V_{CC}$ voltage (recommended mode of operation). In two-wire control mode, the amplitude of each channel can be adjusted from 0 $mV_{PP}$ to 600 $mV_{PP}$. The amplitude is controlled with the AMPL[3:0] bits in registers 1, 7, 13, and 19 for channels 1, 2, 3, and 4, respectively.

### 7.3.4 Rate Select

The small-signal bandwidth can be adjusted using the RATE pad (pad 7) in pad control mode. Bandwidth is typically 20 GHz if the pad is left open. Bandwidth is reduced by approximately 0.4 GHz if the pad is tied to ground, and increased by approximately 0.4 GHz if the pad is tied to $V_{CC}$. In two-wire control mode, the bandwidth of each channel can be adjusted up or down using the RATE[3:0] register settings in registers 1, 7, 13, and 19 for channels 1, 2, 3, and 4, respectively.

### 7.3.5 Threshold Adjustment

The TIAs have DC offset cancellation to maintain a 50% crossing point; however, the crossing point can be adjusted using the TRSH pad (pad 41) in pad control mode. No threshold adjustment is applied if the pad is left open. The crossing point is shifted up approximately 12% if the pad is tied to ground, and is shifted down by approximately 12% if the pad is tied to $V_{CC}$. In two-wire control mode, the crossing point can be adjusted up or down using the TH[3:0] register settings in registers 2, 8, 14, and 20 for channels 1, 2, 3, and 4, respectively.

### 7.3.6 Filter Circuitry

The FILTERx pins provide a regulated and filtered $V_{CC}$ for a PIN photodiode bias. The supply voltages for the transimpedance amplifier have on-chip capacitors but external filter capacitors are recommended to be used as well for best performance. The input stage has a separate $V_{CC}$ supply ($V_{CC}$Ix) that is not connected on-chip to the supply of the limiting and CML stages ($V_{CC}$Ox).

### 7.3.7 AGC and RSSI

The voltage drop across the regulated photodiode FET is monitored by the bias and RSSI control circuit block in the case where a PIN diode is biased using the FILTERx pins.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## Feature Description (continued)

If the DC input current exceeds a certain level then this current is partially cancelled by means of a controlled current source. This cancellation keeps the transimpedance amplifier stage within sufficient operating limits for optimum performance.

The automatic gain control circuitry adjusts the voltage gain of the AGC amplifier to ensure limiting behavior of the complete amplifier.

Finally, this circuit block senses the current through the FILTERx FET and generates a mirrored current that is proportional to the input signal strength. The mirrored currents are available at the RSSIx outputs and can be sunk to ground (GND) using an external resistor. For proper operation, ensure that the voltage at the RSSIx pad does not exceed $V_{CC}$ – 0.65 V.

## 7.4 Device Functional Modes

The device has two functional modes of operation: pad control mode and two-wire interface control mode.

### 7.4.1 Pad Control

The default mode of operation is pad control and the amplitude is recommended to be increased to the 450 $mV_{PP}$ setting by bonding AMPL (pad 6) to $V_{CC}$. If further adjustment is desired as described previously, then the RATE (pad 7), GAIN (pad 8), and TRSH (pad 41) control pads and can be bonded to either ground (GND) or $V_{CC}$.

### 7.4.2 Two-Wire Interface Control

To enable two-wire interface, the I2CENA (pad 5) control pad must be bonded to $V_{CC}$. In this mode of operation, pad control is not functional and all control is initiated through the two-wire interface as described in the *Programming* section.

## 7.5 Programming

The ONET2804TLP uses a two-wire serial interface for digital control. For example, the two circuit inputs (SDA and SCK) are driven by the serial data and serial clock from a microcontroller. Both inputs include 10-kΩ pullup resistors to $V_{CC}$. For driving these inputs, an open-drain output is recommended. The two-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The ONET2804TLP is a slave device only, which means that the device cannot initiate a transmission, but always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The device is recommended to be used on a bus with only one master. The protocol for a data transmission is as follows:

1. START command
2. 7-bit slave address (0001100) followed by an eighth bit that is the data direction bit (R/W). A zero indicates a write operation and a 1 indicates a read operation.
3. 8-bit register address
4. 8-bit register data word
5. STOP command

Regarding timing, the ONET2804TLP is $I^2C$ compatible. Figure 13 illustrates the typical timing and Figure 14 illustrates a complete data transfer. Parameters for Figure 13 are defined in the *Timing Requirements* table.

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## Programming (continued)

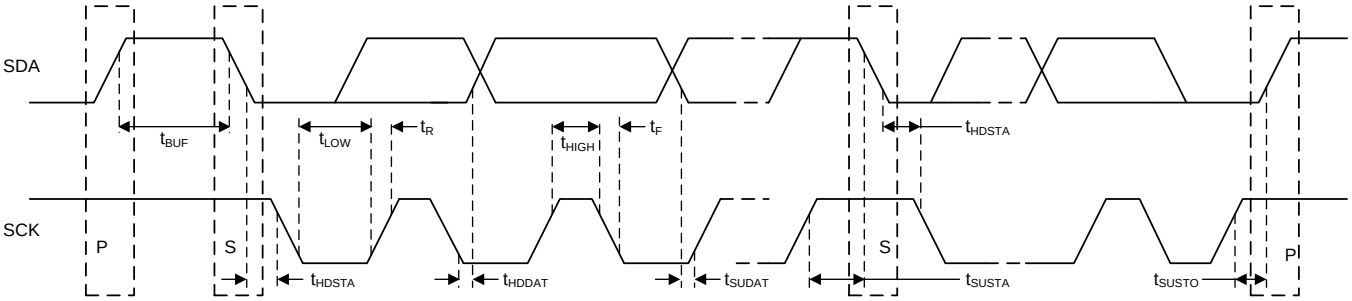


**Figure 13. I²C Timing Diagram**

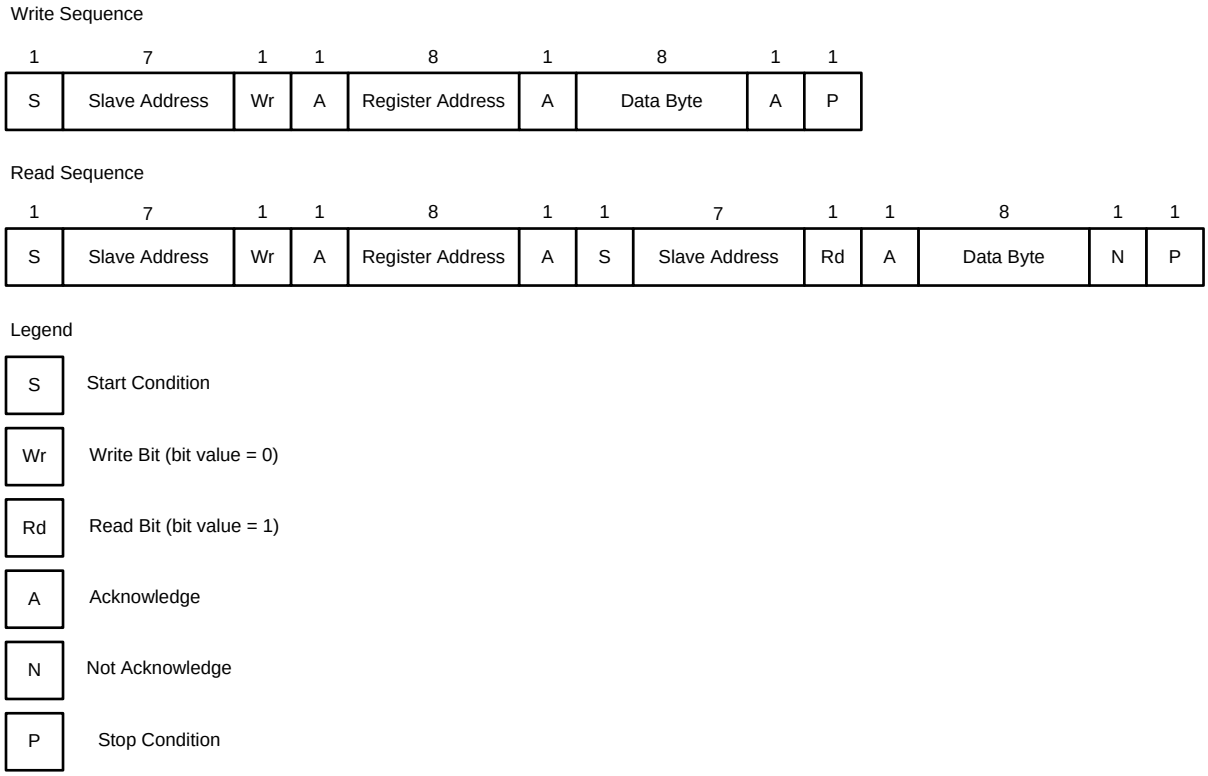


**Figure 14. Data Transfer**

### 7.5.1 Bus Idle

Both the SDA and SCK lines remain high.

### 7.5.2 Start Data Transfer

A change in the state of the SDA line from high to low when the SCK line is high defines a START condition (S). Each data transfer is initiated with a START condition.

### 7.5.3 Stop Data Transfer

A change in the state of the SDA line from low to high when the SCK line is high defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, to continue communication on the bus, the master can generate a repeated START condition and address another slave without first generating a STOP condition.


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## Programming (continued)

### 7.5.4 Data Transfer

Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

### 7.5.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver does not acknowledge the slave address, the data line must be left high by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This requirement is indicated by the slave generating a not acknowledge on the first subsequent byte. The slave leaves the data line high and the master generates the STOP condition.

## 7.6 Register Maps

Table 1 lists the registers for the ONET2804TLP.

**Table 1. Register Map**

| REGISTER | | REGISTER DATA | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| NAME | ADDRESS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Register 0 | 00h | RESET | PD | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | PWRITE |
| Register 1 | 01h | RATE3 | RATE2 | RATE1 | RATE0 | AMP3 | AMP2 | AMP1 | AMP0 |
| Register 2 | 02h | PD | DIS | GAIN1 | GAIN0 | TH3 | TH2 | TH1 | TH0 |
| Register 3 | 03h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 4 | 04h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 5 | 05h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 6 | 06h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 7 | 07h | RATE3 | RATE2 | RATE1 | RATE0 | AMP3 | AMP2 | AMP1 | AMP0 |
| Register 8 | 08h | PD | DIS | GAIN1 | GAIN0 | TH3 | TH2 | TH1 | TH0 |
| Register 9 | 09h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 10 | 0Ah | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 11 | 0Bh | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 12 | 0Ch | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 13 | 0Dh | RATE3 | RATE2 | RATE1 | RATE0 | AMP3 | AMP2 | AMP1 | AMP0 |
| Register 14 | 0Eh | PD | DIS | GAIN1 | GAIN0 | TH3 | TH2 | TH1 | TH0 |
| Register 15 | 0Fh | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 16 | 10h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 17 | 11h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 18 | 12h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 19 | 13h | RATE3 | RATE2 | RATE1 | RATE0 | AMP3 | AMP2 | AMP1 | AMP0 |
| Register 20 | 14h | PD | DIS | GAIN1 | GAIN0 | TH3 | TH2 | TH1 | TH0 |
| Register 21 | 15h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 22 | 16h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 23 | 17h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 24 | 18h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| Register 25 | 19h | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |

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### 7.6.1 Register Descriptions

This section describes the circuit functionality based on the register settings. Table 2 defines the various register bit field types used in this document.

**Table 2. Register Bit Field Types**

| SYMBOL | DESCRIPTION | ACCESS, READ ACTION, WRITE VALUE |
|---|---|---|
| R | Read | Read-only |
| R/W | Read, write, or both | Read-write |
| W | Write | Write-only |

### 7.6.2 Register 0: Control Settings (address = 00h) [reset = 0h]

**Figure 15. Register 0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESET | PD | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | PWRITE |
| W-0h | R/W-0h | R-Xh | R-Xh | R-Xh | R-Xh | R-Xh | R/W-0h |

**Table 3. Register 0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESET | W | 0h | **Reset registers bit.**<br>1 = Resets all registers to default values<br>0 = Normal operation |
| 6 | PD | R/W | 0h | **Power-down bit.**<br>1 = Power down all channels ($I_{CC}$ is approximately 4 mA)<br>0 = Normal operation |
| 5-1 | Reserved | R | Undefined | Reserved. Read-only. |
| 0 | PWRITE | R/W | 0h | **Parallel write mode bit.**<br>1 = Parallel write enabled (write register value to all channels)<br>0 = Serial write |

### 7.6.3 Register 1: Amplitude and Rate for Channel 1 (address = 01h) [reset = 0h]

**Figure 16. Register 1**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RATE3 | RATE2 | RATE1 | RATE0 | AMP3 | AMP2 | AMP1 | AMP0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 4. Register 1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RATE[3 :0] | R/W | 0h | **Rate adjustments bits for channel 1**.<br>0000 = 21 GHz (default)<br>0111 = BW decrease of approximately 0.4 GHz<br>1111 = BW increase of approximately 0.4 GHz<br>All others: Do not use |
| 3-0 | AMP[3:0] | R/W | 0h | **Amplitude adjustment bits for channel 1.**<br>Table 5 lists the bit settings for AMP[3:0]. |


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**Table 5. AMP[3:0] Bit Settings**

| BITS | AMPLITUDE ADJUSTMENT ($mV_{PP}$) | BITS | AMPLITUDE ADJUSTMENT ($mV_{PP}$) |
|---|---|---|---|
| 0000 | 0 (default) | 1000 | 250 |
| 0001 | 50 | 1001 | 300 |
| 0010 | 100 | 1010 | 350 |
| 0011 | 150 | 1011 | 400 |
| 0100 | 200 | 1100 | 450 |
| 0101 | 250 | 1101 | 500 |
| 0110 | 300 | 1110 | 550 |
| 0111 | 350 | 1111 | 600 |

### 7.6.4 Register 2: Threshold and Gain for Channel 1 (address = 02h) [reset = 0h]

**Figure 17. Register 2**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PD | DIS | GAIN1 | GAIN0 | TH3 | TH2 | TH1 | TH0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 6. Register 2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PD | R/W | 0h | **Power-down bit for channel 1**.<br>1 = Power down channel 1<br>0 = Normal operation |
| 6 | DIS | R/W | 0h | **Disable output buffer for channel 1.**<br>1 = Disable channel 1 output buffer<br>0 = Normal operation |
| 5-4 | GAIN[1:0] | R/W | 0h | **Gain adjustment bits for channel 1.**<br>00 = Default<br>01 = Do not use<br>10 = Medium (–4 dB)<br>11 = Minimum (–8 dB) |
| 3-0 | TH[3:0] | R/W | 0h | **Threshold adjustment bits for channel 1**.<br>0000 = Zero shift<br>0001 = Minimum positive shift<br>0111 = Maximum positive shift<br>1000 = Zero shift<br>1001 = Minimum negative shift<br>1111 = Maximum negative shift |

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### 7.6.5 Register 7: Amplitude and Rate for Channel 2 (address = 07h) [reset = 0h]

**Figure 18. Register 7**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RATE3 | RATE2 | RATE1 | RATE0 | AMP3 | AMP2 | AMP1 | AMP0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 7. Register 7 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RATE[3:0] | R/W | 0h | **Rate adjustments bits for channel 2**.<br>0000 = 21 GHz (default)<br>0111 = BW decreases by approximately 0.4 GHz<br>1111 = BW increases by approximately 0.4 GHz |
| 3-0 | AMP[3:0] | R/W | 0h | **Amplitude adjustment bits for channel 2.**<br>Table 5 lists the bit settings for AMP[3:0]. |

### 7.6.6 Register 8: Threshold and Gain for Channel 1 (address = 08h) [reset = 0h]

**Figure 19. Register 8**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PD | DIS | GAIN1 | GAIN0 | TH3 | TH2 | TH1 | TH0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 8. Register 8 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PD | R/W | 0h | **Power-down bit for channel 2**.<br>1 = Power down channel 2<br>0 = Normal operation |
| 6 | DIS | R/W | 0h | **Disable output buffer for channel 2.**<br>1 = Disable channel 2 output buffer<br>0 = Normal operation |
| 5-4 | GAIN[1:0] | R/W | 0h | **Gain adjustment bits for channel 2.**<br>00 = Default<br>01 = Do not use<br>10 = Medium (–4 dB)<br>11 = Minimum (–8 dB) |
| 3-0 | TH[3:0] | R/W | 0h | **Threshold adjustment bits for channel 2**.<br>0000 = Zero shift<br>0001 = Minimum positive shift<br>0111 = Maximum positive shift<br>1000 = Zero shift<br>1001 = Minimum negative shift<br>1111 = Maximum negative shift |


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### 7.6.7 Register 13: Amplitude and Rate for Channel 3 (address = 0Dh) [reset = 0h]

**Figure 20. Register 13**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RATE3 | RATE2 | RATE1 | RATE0 | AMP3 | AMP2 | AMP1 | AMP0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 9. Register 13 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RATE[3:0] | R/W | 0h | **Rate adjustments bits for channel 3**.<br>0000 = 21 GHz (default)<br>0111 = BW decreases by approximately 0.4 GHz<br>1111 = BW increases by approximately 0.4 GHz |
| 3-0 | AMP[3:0] | R/W | 0h | **Amplitude adjustment bits for channel 3.**<br>Table 5 lists the bit settings for AMP[3:0]. |

### 7.6.8 Register 14: Threshold and Gain for Channel 3 (address = 0Eh) [reset = 0h]

**Figure 21. Register 14**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PD | DIS | GAIN1 | GAIN0 | TH3 | TH2 | TH1 | TH0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 10. Register 14 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PD | R/W | 0h | **Power-down bit for channel 3**.<br>1 = Power down channel 3<br>0 = Normal operation |
| 6 | DIS | R/W | 0h | **Disable output buffer for channel 3.**<br>1 = Disable channel 3 output buffer<br>0 = Normal operation |
| 5-4 | GAIN[1:0] | R/W | 0h | **Gain adjustment bits for channel 3.**<br>00 = Default<br>01 = Do not use<br>10 = Medium (–4 dB)<br>11 = Minimum (–8 dB) |
| 3-0 | TH[3:0] | R/W | 0h | **Threshold adjustment bits for channel 3**.<br>0000 = Zero shift<br>0001 = Minimum positive shift<br>0111 = Maximum positive shift<br>1000 = Zero shift<br>1001 = Minimum negative shift<br>1111 = Maximum negative shift |

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### 7.6.9 Register 19: Amplitude and Rate for Channel 4 (address = 13h) [reset = 0h]

**Figure 22. Register 19**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RATE3 | RATE2 | RATE1 | RATE0 | AMP3 | AMP2 | AMP1 | AMP0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 11. Register 19 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RATE[3:0] | R/W | 0h | **Rate adjustments bits for channel 4**.<br>0000 = 21 GHz (default)<br>0111 = BW decreases by approximately 0.4 GHz<br>1111 = BW increases by approximately 0.4 GHz |
| 3-0 | AMP[3:0] | R/W | 0h | **Amplitude adjustment bits for channel 4.**<br>Table 5 lists the bit settings for AMP[3:0]. |

### 7.6.10 Register 20: Threshold and Gain for Channel 4 (address = 14h) [reset = 0h]

**Figure 23. Register 20**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PD | DIS | GAIN1 | GAIN0 | TH3 | TH2 | TH1 | TH0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**Table 12. Register 20 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PD | R/W | 0h | **Power-down bit for channel 4**.<br>1 = Power down channel 4<br>0 = Normal operation |
| 6 | DIS | R/W | 0h | **Disable output buffer for channel 4.**<br>1 = Disable channel 4 output buffer<br>0 = Normal operation |
| 5-4 | GAIN[1:0] | R/W | 0h | **Gain adjustment bits for channel 4.**<br>00 = Default<br>01 = Do not use<br>10 = Medium (–4 dB)<br>11 = Minimum (–8 dB) |
| 3-0 | TH[3:0] | R/W | 0h | **Threshold adjustment bits for channel 4**.<br>0000 = Zero shift<br>0001 = Minimum positive shift<br>0111 = Maximum positive shift<br>1000 = Zero shift<br>1001 = Minimum negative shift<br>1111 = Maximum negative shift |


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

Figure 24 shows the ONET2804TLP being used in a fiber optic receiver application with four channels running at 25 Gbps each and with pin control. Figure 27 illustrates the device being used with two-wire control. The ONET2804TLP converts the electrical current generated by the PIN photodiode into a differential output voltage. The FILTERx inputs provide a DC bias voltage for the PIN that is low-pass filtered. The photodiode must be connected to the FILTERx pads for the bias circuit to function correctly because the voltage drop across the photodiode FET is sensed and used by the bias circuit.

The RSSIx outputs are used to mirror the photodiode output current and can be connected via resistors to GND. The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation of the ONET2804TLP, ensure that the voltage at RSSIx never exceeds $V_{CC}$ – 0.65 V. If the RSSIx outputs are not used when using the internal PD bias, then leave these outputs open.

The OUTx+ and OUTx– pins are internally terminated by 50-Ω pullup resisters to $V_{CC}$. The outputs must be AC coupled (for example, by using 0.1-µF capacitors) to the succeeding device.

## 8.2 Typical Applications

### 8.2.1 Pad Control Application

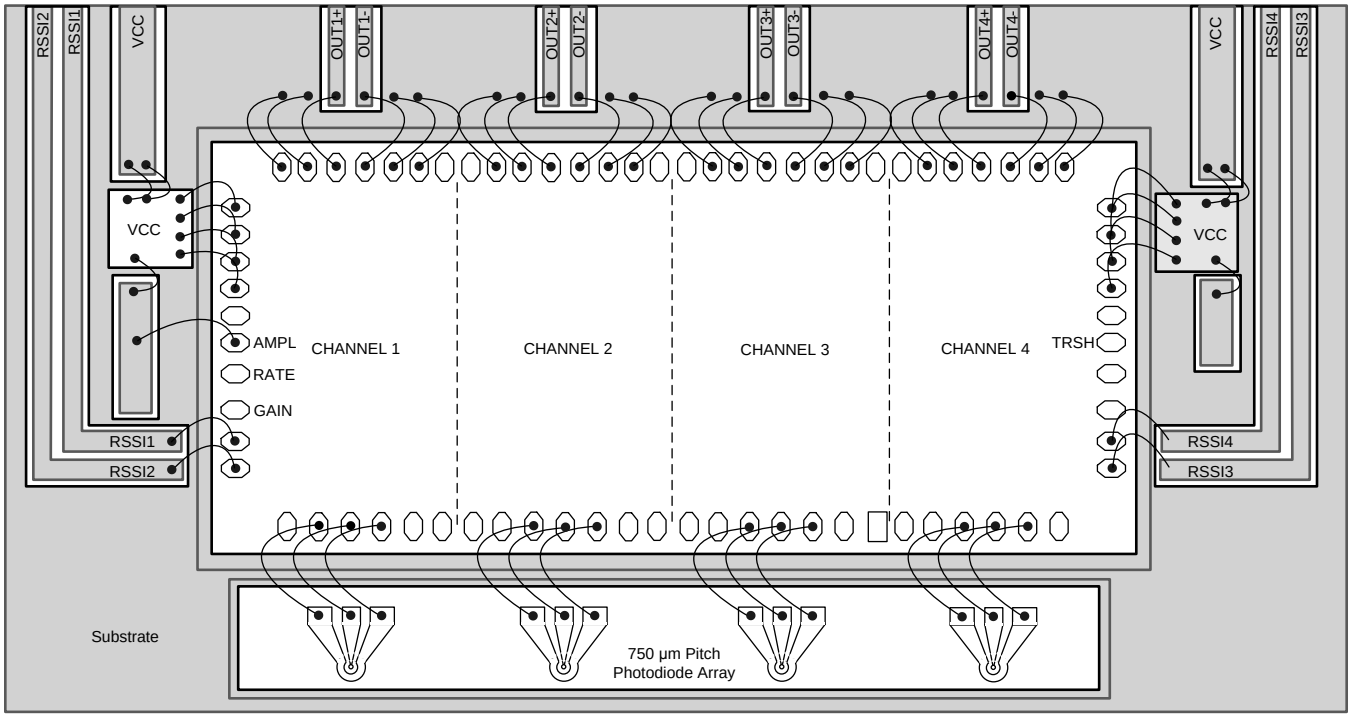


**Figure 24. Basic Application Circuit with Pad Control**

## Typical Applications (continued)

### 8.2.1.1 Design Requirements

**Table 13. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage | 3.3 V |
| Output voltage | 300 $mV_{PP}$ |

### 8.2.1.2 Detailed Design Procedure

The ONET2804TLP is designed to be used in conjunction with a 750-μm pitch photodiode array or individual photodiodes and assembled into a receiver optical subassembly (ROSA). The TIA is typically mounted on a ceramic substrate with etched connections for $V_{CC}$, RSSIx, and 100-Ω differential transmission lines for the output voltage. The photodiode converts the optical input signal into a current that is supplied to the TIA through wire bonds. The TIA then converts the input current into a voltage and further amplifies the signal. TI recommends setting the output amplitude to the 300-$mV_{PP}$ level by leaving AMPL (pad 6) floating.

The ROSA is typically mounted on a printed circuit board (PCB) with 100-Ω differential transmission lines and RF connectors [such as GPPO® or 2.4-mm subminiature version A (SMA) connectors]. When measuring the output from the ROSA mounted on the PCB, the frequency dependent loss of the transmission lines affects the frequency response. The loss can be de-embedded from the measurement to determine the actual frequency response at the output of the ROSA.

### 8.2.1.3 Application Curves

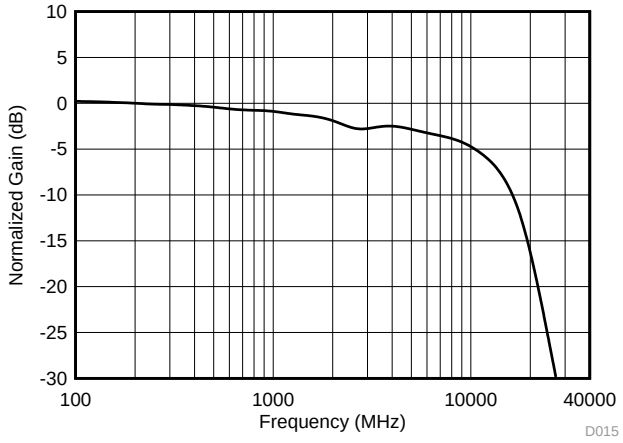


**Figure 25. Gain vs Frequency (Without De-Embedding)**

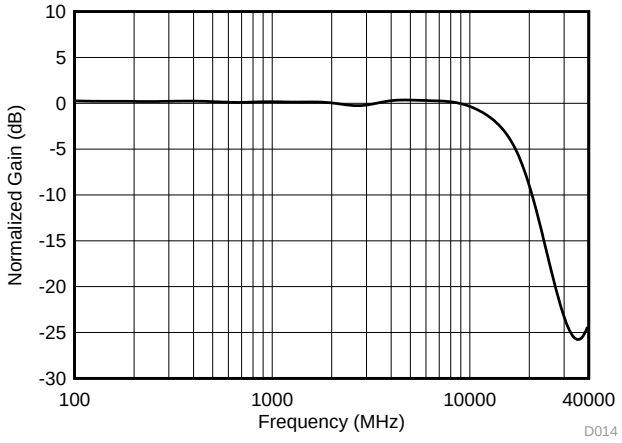


**Figure 26. Gain vs Frequency (With De-Embedding)**


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### 8.2.2 Two-Wire Control Application

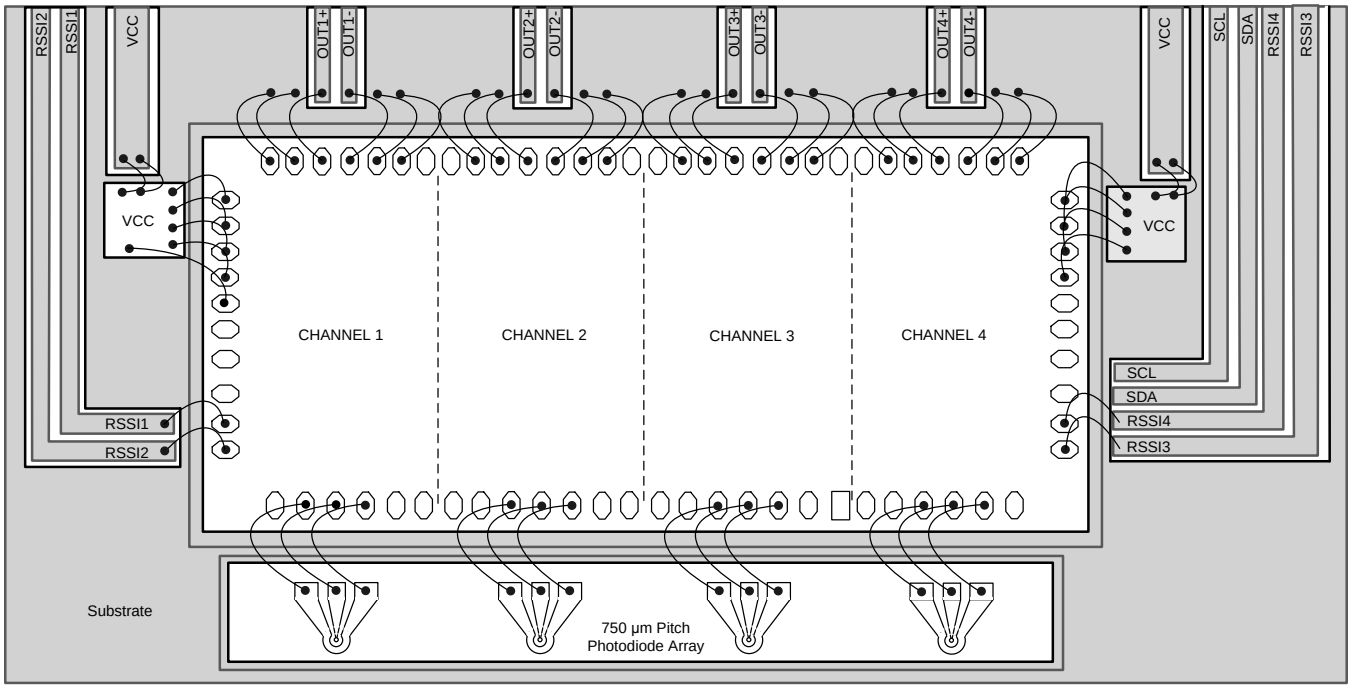


**Figure 27. Basic Application Circuit with Two-Wire Control**

#### *8.2.2.1 Design Requirements*

Table 14 lists the design requirements for this application.

**Table 14. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| I2CENA pin voltage | 3.3 V |
| Output voltage | 300 $mV_{PP}$ |

#### *8.2.2.2 Detailed Design Procedure*

As described in the *Detailed Design Procedure* section on the pad control application, TI generally recommends setting the output voltage of the device to the 300-$mV_{PP}$ setting. The output voltage setting can be controlled by bonding specific device pads as detailed in the *Pad Control Application* section, but can alternatively be controlled using the device $I^2C$ interface. To set the output amplitude via the $I^2C$ interface, the I2CENA pad must be connected to $V_{CC}$, which enables the $I^2C$ control and disables pad control. The output amplitude can then be set to the 300-$mV_{PP}$ mode by writing the value 0110 to bits[3:0] of the amplitude control registers for each channel as described in the *Register Maps* section. Requirements to operate the $I^2C$ interface are detailed in the *Programming* section.

## 9 Power Supply Recommendations

The ONET2804TLP is designed to operate from an input supply voltage range between 2.8 V and 3.47 V. There are a total of eight power-supply pads ($V_{CC}$I[4:1] and $V_{CC}$O[4:0]) that must be connected for proper operation. $V_{CC}$I[4:1] are used to supply power to the input transimpedance amplifier stages and $V_{CC}$O[4:1] are used to supply power to the voltage amplifiers and output buffers. Each amplifier is powered up separately but there are some common internal connections for support circuitry (such as the two-wire interface). Therefore, if only one channel is being evaluated, all eight supply pads must be connected. Use two single-layer ceramic (SLC) capacitors in the range of 270 pF to 680 pF for power-supply decoupling. $V_{CC}$I1, $V_{CC}$I2, $V_{CC}$O1, and $V_{CC}$O2 should be bonded to one capacitor and $V_{CC}$I3, $V_{CC}$I4, $V_{CC}$O3, and $V_{CC}$O4 should be bonded to the other capacitor; see Figure 24 and Figure 27 for reference.

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# 10 Layout

## 10.1 Layout Guidelines

Careful attention to assembly parasitics and external components is necessary to achieve optimal performance.

- Minimize the total capacitance on the INx pad by using a low capacitance photodiode (100 fF) and pay attention to stray capacitances. Place the photodiode close to the ONET2804TLP die and keep the wire bond inductance in the range of 300 pH to 400 pH.
- Use identical termination and symmetrical transmission lines at the AC-coupled differential output pins (OUTx+ and OUTx–).
- Use short bond wire connections for the supply pins $V_{CC}$Ix, $V_{CC}$Ox, and GND. Supply voltage filtering is provided on-chip but filtering can be improved by using an additional external capacitor.
- The die has backside metal and conductive epoxy must be used to attach the die to ground.

## 10.2 Layout Example

The device dimensions are shown in Figure 28 and Table 15 provides the pad locations. The device is designed for wire bonding not flip chip layouts.

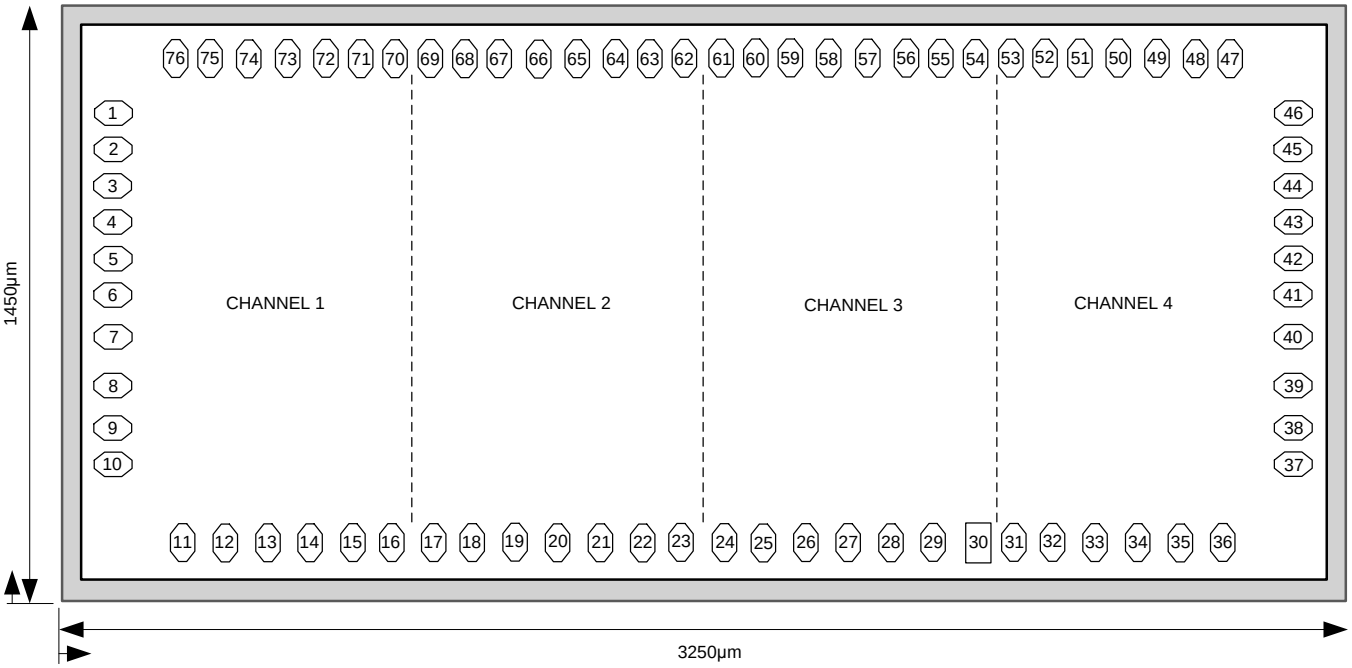


**Figure 28. Device Dimensions and Pad Locations**

Die thickness: 203 µm ± 13 µm
Pad dimensions: 105 µm × 65 µm
Die size: 3250 µm ± 40 µm × 1450 µm ± 40 µm


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## Layout Example (continued)

**Table 15. Bond Pad Coordinates**

| PAD | COORDINATES (Referenced to Pad 1) | | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| | X (µm) | Y (µm) | | | |
| 1 | 0 | 0 | $V_{CC}O1$ | Supply | 3.3-V supply voltage |
| 2 | 0 | –94 | $V_{CC}O2$ | Supply | 3.3-V supply voltage |
| 3 | 0 | –188 | $V_{CC}I2$ | Supply | 3.3-V supply voltage |
| 4 | 0 | –282 | $V_{CC}I1$ | Supply | 3.3-V supply voltage |
| 5 | 0 | –376 | I2CENA | Digital input | $I^2C$ enable |
| 6 | 0 | –470 | AMPL | Digital input | Amplitude control |
| 7 | 0 | –580 | RATE | Digital input | Rate selection |
| 8 | 0 | –704 | GAIN | Digital input | Gain control |
| 9 | 0 | –814 | RSSI1 | Analog output | Receiver signal strength indicator for channel 1 |
| 10 | 0 | –908 | RSSI2 | Analog output | Receiver signal strength indicator for channel 2 |
| 11 | 180 | –1110 | GND | Supply | Circuit ground |
| 12 | 290 | –1110 | FILTER1 | Analog output | Bias voltage for photodiode 1 |
| 13 | 400 | –1110 | IN1 | Analog input | TIA input for channel 1 |
| 14 | 510 | –1110 | FILTER1 | Analog output | Bias voltage for photodiode 1 |
| 15 | 620 | –1110 | GND | Supply | Circuit ground |
| 16 | 720 | –1110 | NC | No connection | Do not connect |
| 17 | 829 | –1110 | NC | No connection | Do not connect |
| 18 | 929 | –1110 | GND | Supply | Circuit ground |
| 19 | 1039 | –1110 | FILTER2 | Analog output | Bias voltage for photodiode 2 |
| 20 | 1149 | –1110 | IN2 | Analog input | TIA input for channel 2 |
| 21 | 1259 | –1110 | FILTER2 | Analog output | Bias voltage for photodiode 2 |
| 22 | 1369 | –1110 | GND | Supply | Circuit ground |
| 23 | 1469 | –1110 | NC | No connect | Do not connect |
| 24 | 1580 | –1110 | NC | No connect | Do not connect |
| 25 | 1680 | –1110 | GND | Supply | Circuit ground |
| 26 | 1790 | –1110 | FILTER3 | Analog output | Bias voltage for photodiode 3 |
| 27 | 1900 | –1110 | IN3 | Analog input | TIA input for channel 3 |
| 28 | 2010 | –1110 | FILTER3 | Analog output | Bias voltage for photodiode 3 |
| 29 | 2120 | –1110 | GND | Supply | Circuit ground |
| 30 | 2239 | –1110 | NC | No connect | Do not connect |
| 31 | 2329 | –1110 | NC | No connect | Do not connect |
| 32 | 2429 | –1110 | GND | Supply | Circuit ground |
| 33 | 2539 | –1110 | FILTER4 | Analog output | Bias voltage for photodiode 4 |
| 34 | 2649 | –1110 | IN4 | Analog input | TIA input for channel 4 |
| 35 | 2759 | –1110 | FILTER4 | Analog output | Bias voltage for photodiode 4 |
| 36 | 2869 | –1110 | GND | Supply | Circuit ground |
| 37 | 3051 | –908 | RSSI3 | Analog output | Receiver signal strength indicator for channel 3 |
| 38 | 3051 | –814 | RSSI4 | Analog output | Receiver signal strength indicator for channel 4 |
| 39 | 3051 | –704 | SDA | Digital input/output | 2-wire data |
| 40 | 3051 | –579 | SCL | Digital input | 2-wire clock |
| 41 | 3051 | –470 | TRSH | Digital input | Input threshold control (cross-point) |
| 42 | 3051 | –376 | NC | No connect | Do not connect |
| 43 | 3051 | –282 | $V_{CC}I4$ | Supply | 3.3-V supply voltage |
| 44 | 3051 | –188 | $V_{CC}I3$ | Supply | 3.3-V supply voltage |

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## Layout Example (continued)

**Table 15. Bond Pad Coordinates (continued)**

| PAD | COORDINATES (Referenced to Pad 1) | | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| | X (µm) | Y (µm) | | | |
| 45 | 3051 | –94 | $V_{CC}O3$ | Supply | 3.3-V supply voltage |
| 46 | 3051 | 0 | $V_{CC}O4$ | Supply | 3.3-V supply voltage |
| 47 | 2888 | 140 | GND | Supply | Circuit ground |
| 48 | 2799 | 140 | GND | Supply | Circuit ground |
| 49 | 2699 | 140 | OUT4– | Analog output | Inverted data output for channel 4 |
| 50 | 2599 | 140 | OUT4+ | Analog output | Noninverted data output for channel 4 |
| 51 | 2499 | 140 | GND | Supply | Circuit ground |
| 52 | 2410 | 140 | GND | Supply | Circuit ground |
| 53 | 2322 | 140 | ADR1 | Digital input | 2-wire address bit 1 control |
| 54 | 2228 | 140 | ADR0 | Digital input | 2-wire address bit 0 control |
| 55 | 2139 | 140 | GND | Supply | Circuit ground |
| 56 | 2050 | 140 | GND | Supply | Circuit ground |
| 57 | 1950 | 140 | OUT3– | Analog output | Inverted data output for channel 3 |
| 58 | 1850 | 140 | OUT3+ | Analog output | Noninverted data output for channel 3 |
| 59 | 1750 | 140 | GND | Supply | Circuit ground |
| 60 | 1661 | 140 | GND | Supply | Circuit ground |
| 61 | 1572 | 140 | NC | No connection | Do not connect |
| 62 | 1477 | 140 | NC | No connection | Do not connect |
| 63 | 1388 | 140 | GND | Supply | Circuit ground |
| 64 | 1299 | 140 | GND | Supply | Circuit ground |
| 65 | 1199 | 140 | OUT2– | Analog output | Inverted data output for channel 2 |
| 66 | 1099 | 140 | OUT2+ | Analog output | Noninverted data output for channel 2 |
| 67 | 999 | 140 | GND | Supply | Circuit ground |
| 68 | 910 | 140 | GND | Supply | Circuit ground |
| 69 | 821 | 140 | NC | No connect | Do not connect |
| 70 | 728 | 140 | NRESET | Digital input | 2-wire negative reset |
| 71 | 639 | 140 | GND | Supply | Circuit ground |
| 72 | 550 | 140 | GND | Supply | Circuit ground |
| 73 | 450 | 140 | OUT1– | Analog output | Inverted data output for channel 1 |
| 74 | 350 | 140 | OUT1+ | Analog output | Noninverted data output for channel 1 |
| 75 | 250 | 140 | GND | Supply | Circuit ground |
| 76 | 161 | 140 | GND | Supply | Circuit ground |


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| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ONET2804TLPY | Obsolete | Production | DIESALE (Y) \| 0 | - | - | Call TI | Call TI | -40 to 100 | |
| ONET2804TLPY.A | Obsolete | Production | DIESALE (Y) \| 0 | - | - | Call TI | Call TI | -40 to 100 | |

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